Isolated Double Step-Down DC–DC Converter With Improved ZVS Range and No Transformer Saturation Problem

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***Abstract*—In this paper, an isolated double step-down dc–dc converter with high efficiency and high step-down function is proposed. The proposed converter employs an additional capacitor in the primary side. Compared to the conventional full-bridge converters, the proposed converter has a double step-down feature with reduced voltage stress at the primary side of the transformer. Moreover, voltage stress of three primary-side switches reduces to half of the input voltage and zero voltage switching (ZVS) is naturally achieved for all switches with lower output capacitor energy of the switches. Therefore, the proposed converter requires smaller leakage inductance than the conventional full-bridge converter. Without adding complexity to the hardware and control, the proposed converter inherently prevents transformer saturation problem caused by the dc component of the transformer. A 3-kW experimental prototype is constructed to verify the performance of the proposed converter.**

***Index Terms*—Double step down, full-bridge converter, phase-shift, transformer saturation, zero voltage switching.**

I. Introduction

NOWADAYS, distributed power system (DPS) is extensively employed in industries, such as telecommunications, computer technology, and information technology, which require high quality and reliability. The DPS generally consists of a power factor correction (PFC) circuit and an isolated dc–dc converter. The dc–dc converter requires both isolation and high step-down conversion ratio from 400 to 48 V [1]–[4], [35]–[37].

The forward, half-bridge (HB), full-bridge (FB), and three-level (TL) converters are generally considered for the DPS because they provide the step-down function and isolation. Fig. 1 shows typical transformer isolated dc–dc converters. The forward converter [see Fig. 1(a)] has been widely used in low to medium power applications due to its high reliability and simple structure. However, it has some drawbacks, such as the transformer reset problem and a limitation in the maximum duty ratio. Many studies have been undertaken to solve these problems [5]–[10]. The conventional HB converter [see Fig. 1(b)] has been widely employed in industrial applications due to its lack of the transformer saturation problem, while providing a simple

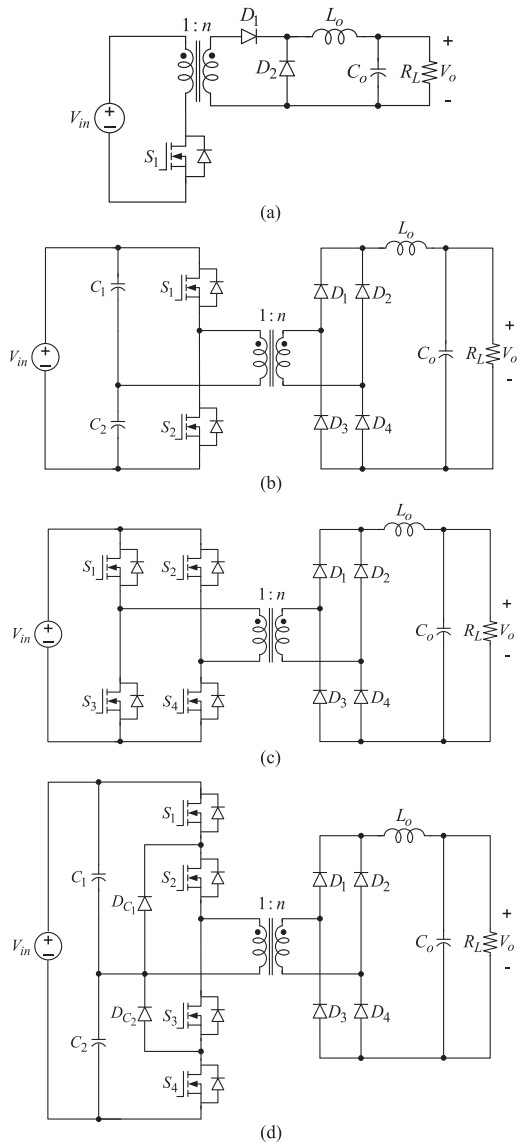

Fig. 1. Conventional transformer isolated dc–dc converters.

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control strategy and structure. Nevertheless, soft-switching is not possible and the voltage stress of switches is equal to the input voltage [28]. Although the asymmetrical HB converter can achieve soft switching, the diodes at the secondary side of the transformer have asymmetrical voltage stress [4], [11]–[14]. The phase-shifted pulsewidth modulation (PS-PWM) FB converter [see Fig. 1(c)] has been widely employed because all the switches at the primary side achieve soft-switching operation. Although the PS-PWM converter achieves soft switching with the phase-shift control scheme, it requires relatively large transformer leakage inductance (or separate inductor in series with transformer) to achieve zero voltage switching (ZVS) under a light-load condition. The large leakage inductance results in limitations, such as a high circulating current, duty ratio loss, excessive voltage spikes across the secondary rectifier diodes, and the oscillation-generating electromagnetic interference (EMI) problem.

Many studies have been performed to overcome the above mentioned problems [15]–[24], [29]. One more drawback of the conventional FB and PS-PWM converters is that they are vulnerable to transformer saturation caused by the dc offset current of the transformer. In order to prevent the transformer saturation, a dc blocking capacitor is generally connected in series with the transformer. To reduce voltage stress of switching devices, the HB three-level converters [see Fig. 1(d)] have been introduced [31]. Similar to the HB converter in Fig. 1(b), it is free from transformer saturation problem, and the voltage stress of four switches reduces to half of input voltage. However, two extra clamping diodes (D_{C_1}, D_{C_2}) are required and this topology also cannot achieve soft switching without auxiliary circuit [32]–[34].

Fig. 2(a) shows the double step-down dc–dc converter introduced in [25]–[27], and its key waveforms are depicted in Fig. 2(b). With the addition of one extra capacitor, C_i, the converter has following advantages over the conventional two-phase interleaved dc–dc converter. First, there is no current unbalance problem between L_1 and L_2 due to the charge (amp-sec) balance condition of the C_i. Therefore, no additional current sensing circuit and control scheme is required. Secondly, voltage stress of the three switches (S_1,S_3, and S_4) becomes half of input voltage.

However, the double step-down converters in [25]–[27] were only applied to non-isolated dc–dc converter and has not been explored in the transformer isolated dc–dc converter [30]. In this paper, an isolated double step-down dc–dc converter is proposed. The proposed converter features wider ZVS range and does not have transformer saturation problem. To verify the performances of the proposed converter, a 3 kW prototype has been built and tested.

II. Circuit Topology and Operation of the Proposed Converter

Fig. 3 shows the proposed converter. The structure of the transformer primary side is the same as that of Fig. 2(a) and the secondary side of the transformer remains the same as the conventional FB or PS-PWM converter. The $C_{S_1} - C_{S_4}$ and

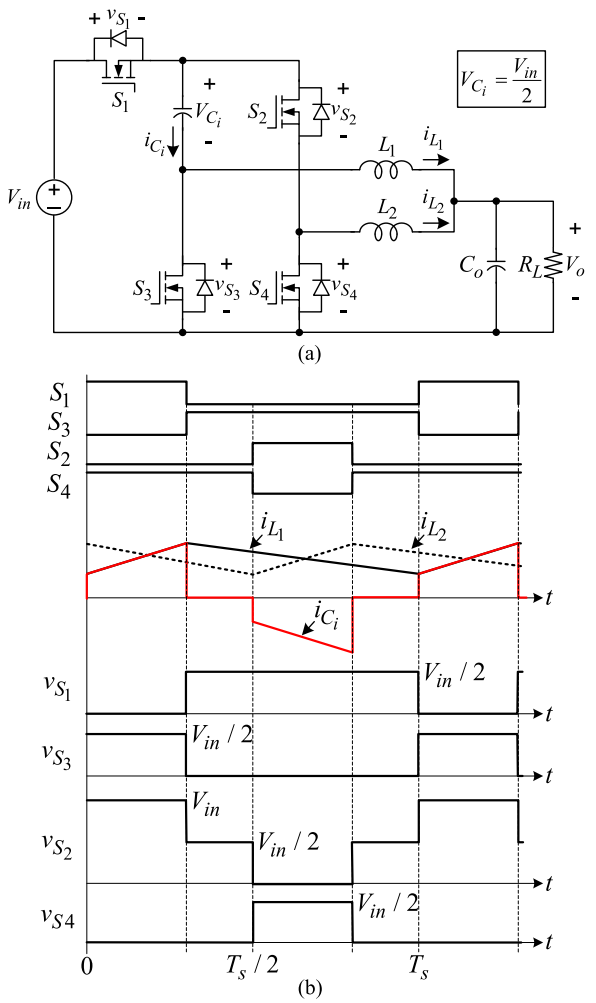


Fig. 2. Double step-down dc–dc converter [25]–[27].

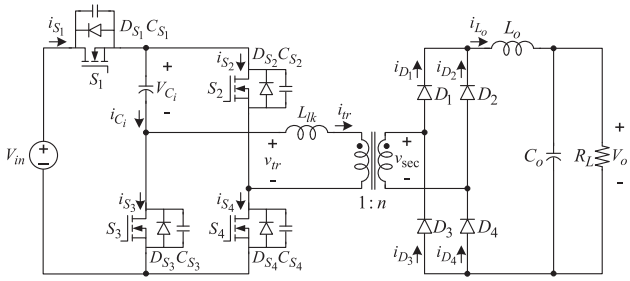


Fig. 3. Proposed isolated double step-down dc–dc converter.

$D_{S_1} - D_{S_4}$ in Fig. 3 represent the output capacitances and body diodes of the switches $S_1 - S_4$, respectively.

Fig. 4 shows key waveforms of the proposed converter. The two gate signals of switches S_1 and S_3 (or S_2 and S_4) are complementary with finite dead time, and S_1 and S_2 are phase shifted by 180°. Same as the double step-down converter in Fig. 2(a), the capacitor C_i voltage (V_{C_i}) is half of the input voltage. The converter has eight operational modes and the detailed operational modes are depicted in Fig. 5.

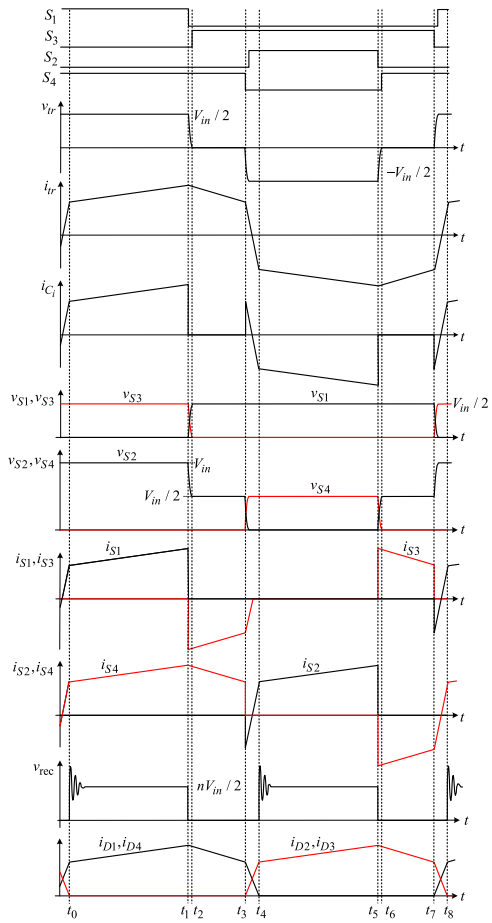


Fig. 4. Key waveforms of the proposed converter.

A. Mode 1 $[t_0 - t_1]$

At $t = t_0$, switches S_1 and S_4 are turned on while rectifier diodes D_1 and D_4 conduct. The input power is delivered to the output. Capacitor C_i is charged and the leakage inductance (L_{lk}) stores energy. Since the capacitor voltage (V_{C_i}) is equal to $V_{in}/2$, transformer primary voltage (v_{tr}) also becomes $V_{in}/2$, and the switchS_2 voltage is equal to input voltage. The transformer primary current (t_{tr}) is expressed as

$$i_{tr}(t_1) = i_{tr}(t_o) + \frac{(v_{tr} - v_{\text{sec}}/n)}{L_{lk}}(t_1 - t_o). \tag{1}$$

B. Mode 2 $[t_1 - t_2]$

At $t = t_1$, switch S_1 is turned off and S_4 remains on. The capacitors C_{S_2} and C_{S_3} are discharged and C_{S_1} is charged by the energy stored in the L_{lk}, respectively [see Fig. 5(b)]. When C_{S_3} is fully discharged, then D_{S_3} is turned on [see Fig. 5(c)]. As shown in Fig. 5(b), the energy stored in L_{lk} has to charge C_{S_1} and discharge C_{S_2} and C_{S_3}. Therefore, 1/3 of energy in the L_{lk} is used for ZVS operation for switch S_3 and the ZVS condition is expressed as follows:

$$E_{C_3} = \frac{1}{2}C_{S_3}\left(\frac{V_{in}}{2}\right)^2 = \frac{1}{3}\left[\frac{1}{2}L_{lk}(i_{tr}(t_1))^2\right] \tag{2}$$

where E_{C_3} is the energy stored in capacitor C_{S_3} for achieving ZVS.

C. Mode 3 $[t_2 - t_3]$

At $t = t_2$, switch S_3 is turned on and S_4 remains on. The stored energy of the leakage inductance freewheels through switch S_4 and D_{S_3}; thus, v_{tr} becomes zero and the switch S_2 voltage is equal to the capacitor C_i voltage. Switch $S_3$is turned on, while diode D_{S_3} conducts. Thus, switch S_3 achieves the ZVS operation. The i_{tr} in this mode is expressed as

$$i_{tr}(t_3) = i_{tr}(t_2) - \frac{(v_{\text{sec}}/n)}{L_{lk}}(t_3 - t_2). \tag{3}$$

D. Mode 4 $[t_3 - t_4]$

At $t = t_3$, switch S_4 is turned off and S_3 remains on. The current in the output filter inductor (L_o) freewheels through the all rectifier diodes. C_{S_2} is discharged again and C_{S_4} is charged [see Fig. 5(e)]. After C_{S_2} is fully discharged by the stored energy of the leakage inductance, diode D_{S_2} is turned on [see Fig. 5(f)]. The stored energy in L_{lk} freewheels through D_{S_2} and C_i, and no current passes through switch S_2 until the transformer current polarity changes from positive to negative. The energy required to achieve ZVS is as follows:

$$E_{C_2} = \frac{1}{2}C_{S_2}\left(\frac{V_{in}}{2}\right)^2 = \frac{1}{2}\left[\frac{1}{2}L_{lk}(i_{tr}(t_3))^2\right] \tag{4}$$

where E_{C_2} is the energy in capacitor C_{S_2} for achieving ZVS.

E. Mode 5 $[t_4 - t_5]$

At $t = t_4$, rectifier diodes D_2 and D_3 conduct while switches S_2 and S_3 are turned on. The stored energy in C_i is mostly delivered to the output through the transformer and partly stored in the L_{lk} [see Fig. 5(g)]. In this mode, v_{tr} is equal to $-V_{in}/2$ and i_{tr} is expressed as

$$i_{tr}(t_5) = i_{tr}(t_4) + \frac{(v_{tr} - v_{\text{sec}}/n)}{L_{lk}}(t_5 - t_4). \tag{5}$$

F. Mode 6 $[t_5 - t_6]$

At $t = t_5$, switch S_2 is turned off and S_3 remains on. C_{S_2} is charged and C_{S_4} is discharged [see Fig. 5(h)]. After C_{S_4} is fully discharged by the energy in L_{lk}, diode D_{S_4}starts conducting [see Fig. 5(i)]. The stored energy in L_{lk} freewheels through switch S_3 and diode D_{S_4}. The energy required to achieve ZVS for switch S_4 is expressed as

$$E_{C_4} = \frac{1}{2}C_{S_4}\left(\frac{V_{in}}{2}\right)^2 = \frac{1}{2}\left[\frac{1}{2}L_{lk}(i_{tr}(t_5))^2\right] \tag{6}$$

where E_{C_4} is the energy stored in capacitor C_{S_4} for achieving ZVS.

G. Mode 7 $[t_6 - t_7]$

At $t = t_6$, switches S_4 is turned on while D_{S_4} conducts; thus, switch S_4 achieves the ZVS operation. The stored energy in

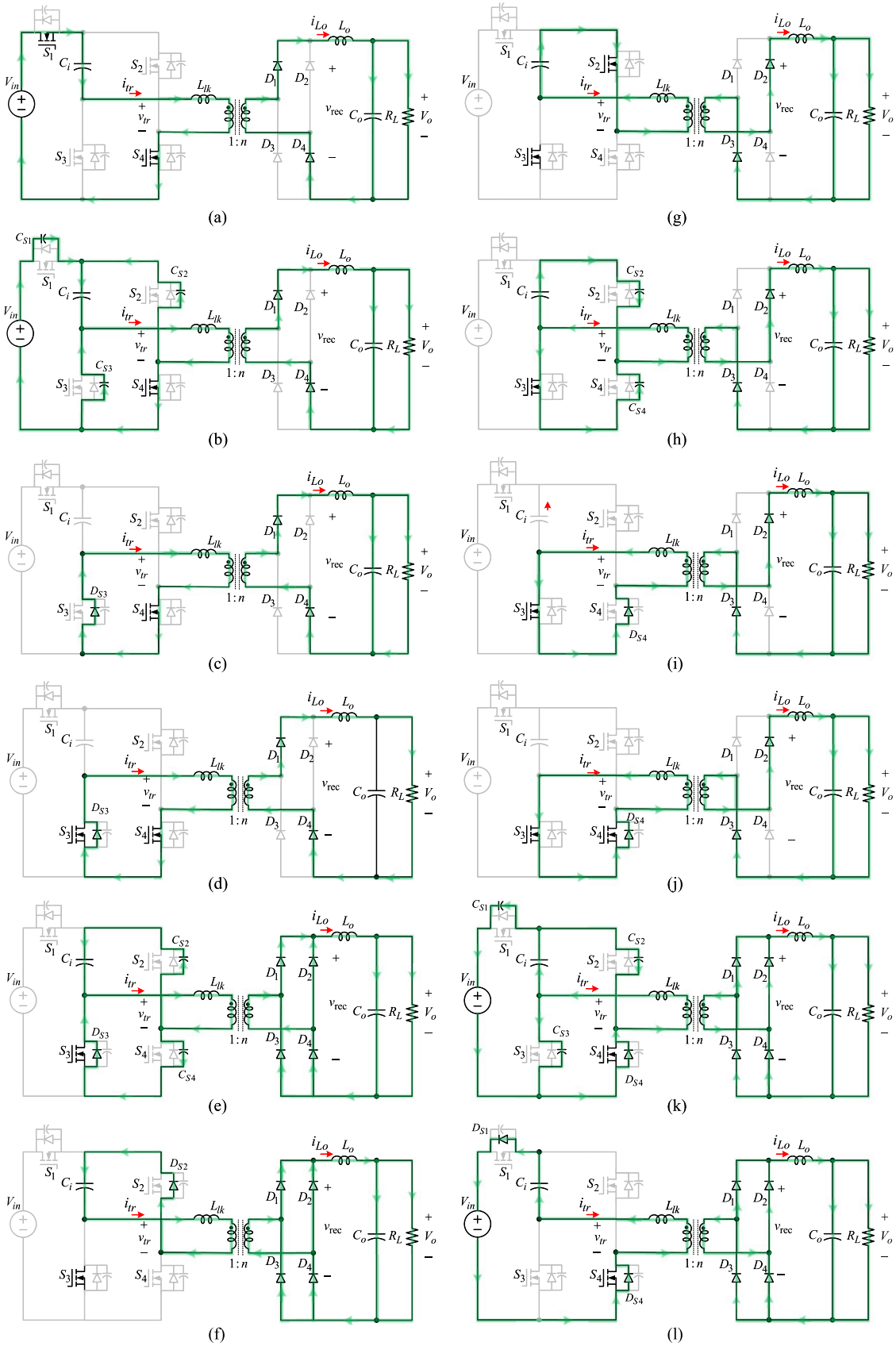


Fig. 5. Operating modes of the proposed converter.

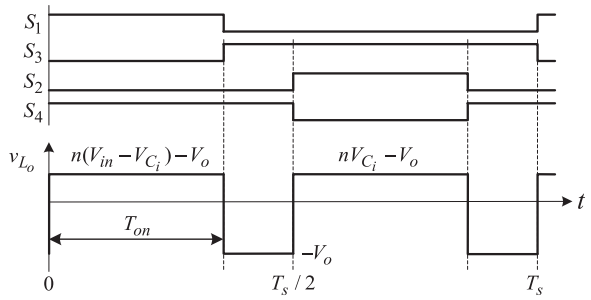


Fig. 6. Output inductor voltage waveform.

L_{lk} freewheels through the switch S_3 and diode D_{S_4}, and v_{tr} becomes zero [see Fig. 5(j)]

$$i_{tr}(t_7) = i_{tr}(t_6) - \frac{v_{\text{sec}}/n}{L_{lk}}(t_7 - t_6). \tag{7}$$

H. Mode 8 $[t_7 - t_8]$

At $t = t_7$, switch S_3 is turned off and the energy in L_o freewheels through the rectifier diodes. C_{S_2} and C_{S_3} are charged and C_{S_1} is discharged [see Fig. 5(k)]. After C_{S_1} is fully discharged, diode D_{S_1} is turned on. The stored energy in L_{lk} freewheels through diodes D_{S_1} and D_{S_4} [see Fig. 5(l)]. Switch S_1 is turned on, while D_{S_1} conducts and no current passes through switch S_1 until the transformer current polarity changes from negative to positive. Thus, similar to Mode 2, the energy required to achieve ZVS for switch S_1 is shown as follows:

$$E_{C_1} = \frac{1}{2}C_{S_1}\left(\frac{V_{in}}{2}\right)^2 = \frac{1}{3}\left[\frac{1}{2}L_{lk}(i_{tr}(t_7))^2\right] \tag{8}$$

where E_{C_1} is the energy in capacitor C_{S_1} for achieving ZVS.

III. Characteristics of the Proposed Converter

A. Capacitor (C_i) Voltage and Voltage Gain of the Proposed Converter

Fig. 6 shows the voltage waveform across L_o. For the sake of simplicity, the effect of L_{lk} is not considered in this figure.

The relationships between the capacitor C_i voltage and input voltage, and voltage gain of the proposed converter can be derived from the flux (volt–sec) balance condition on the output filter inductor (L_o). From Fig. 6, the two relationships are derived as follows:

$$V_{C_i} = \frac{V_{in}}{2} \tag{9}$$

$$\frac{V_o}{V_{in}} = \frac{nD}{2} \tag{10}$$

where V_{C_i} is the voltage across capacitor (C_i), n is the turns ratio of the transformer, and D is the effective duty ratio defined at the secondary side ($D = T_{on}/(T_s/2)$).

From (9) and (10), it is found that the C_i voltage becomes half of input voltage and the voltage gain of the proposed converter reduces to half of the conventional FB converters with the same turns ratio. Therefore, it is concluded that the proposed converter has double step-down function and the voltage stresses of switches S_1,S_3, and S_4 are reduced to half of input voltage due to the addition of C_i.

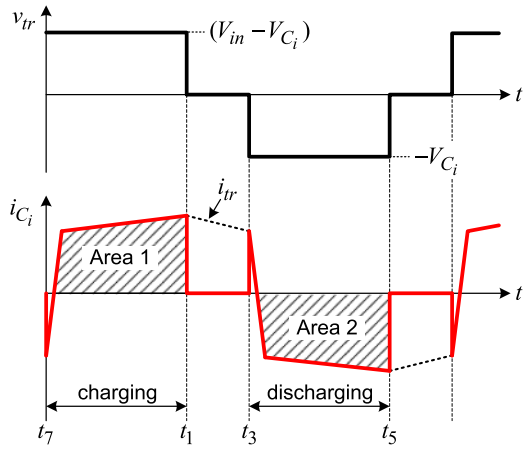


Fig. 7. Removal of transformer saturation problem.

B. Automatic Removal of Transformer Saturation Problem

It is well known that conventional bridge-type converters have transformer saturation problem due to the slightly different time delays in gate drive circuitry or in switching devices. However, the proposed converter can solve this problem automatically for the following reason. The capacitor C_i current waveform is depicted again in Fig. 7 for detailed illustration. As shown in Figs. 7 and 4, the capacitor C_i is charged in Mode 1 ($t_7 - t_1$) and discharged in Mode 5 ($t_3 - t_5$), respectively. In addition, the C_i current constitutes part of the transformer current (i_{tr}). To avoid transformer saturation, the two areas (area 1 and area 2) in Fig. 7 must be the same. In the proposed converter, with the addition of C_i, the two areas become the same due to the charge (amp–sec) balance condition on the C_i. For example, if area 1 is larger than area 2, the C_i voltage is increased because more current is flowing through capacitor C_i, thus the positive transformer voltage ($V_{in} - V_{C_i}$) is reduced and the negative transformer voltage (V_{C_i}) is increased. As a result, the saturation of transformer is removed automatically and completely.

C. ZVS Characteristics

Fig. 8 shows the comparison of switching waveforms in the proposed and conventional PS-PWM converters. In the conventional PS-PWM converter, all the switch voltages are changing from V_{in} to zero. However, in the proposed converter, switch voltages in S_1, S_3, and S_4 are changing from $V_{in}/2$ to zero. Although the voltage stress of S_2 is equal to V_{in}, its voltage transition at the instant of switching is also from $V_{in}/2$ to zero or from V_{in} to $V_{in}/2$. Therefore, all the switch voltage transition in the proposed converter is reduced to half of the conventional PS-PWM converter and this unique feature contributes to the extension of ZVS range in the proposed converter.

It is well known that most of the soft-switching PWM converters use L_{lk} for soft switching and extra inductor is sometimes used if L_{lk} is not sufficient. The stored energy in L_{lk} is $(1/2)L_{lk}I^2$. From (10), the turns ratio of the proposed converter

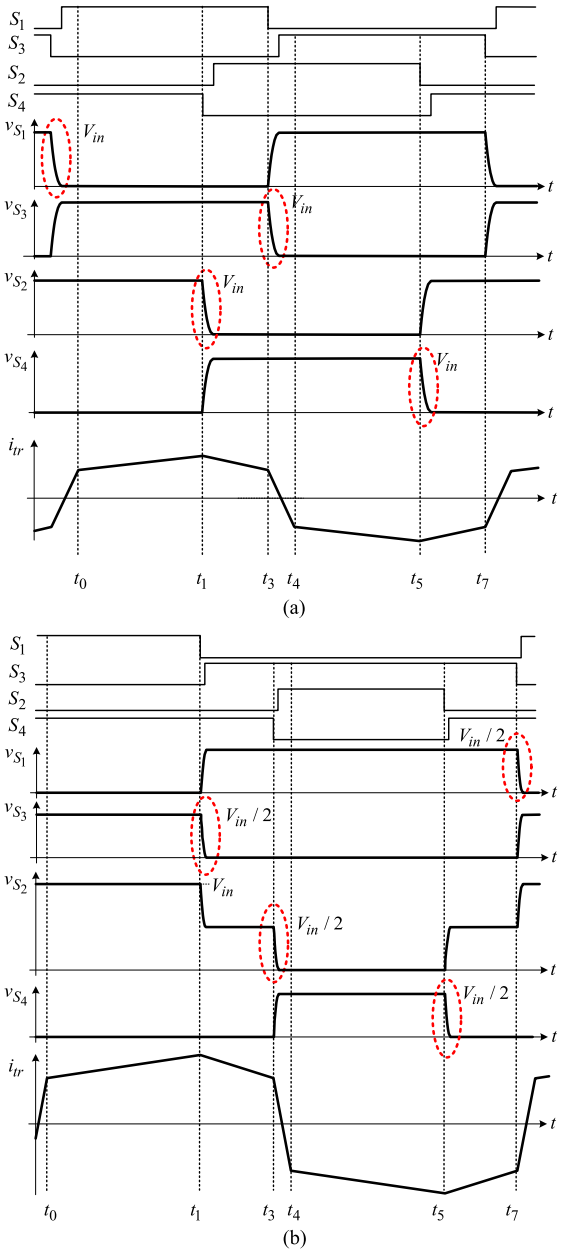


Fig. 8. Comparison of switching waveforms.

is half of the conventional PS-PWM converter, thus transformer primary current is doubled. From this, one quarter of inductor is required in the proposed converter to store the same energy as the PS-PWM converter. The governing equation for the analysis of ZVS range is given by

$$\frac{1}{2}CV^2 = \frac{1}{2}L_{lk}I^2. \tag{11}$$

As shown in Fig. 8(b), the switch voltage transition in the proposed converter is reduced by half. Thus, from (11), the transformer (or load) current required for ZVS is also reduced by half if we assume the same C in both cases.

As depicted in Fig. 8(a), in the conventional PS-PWM converter, the two phase arms have different ZVS condition. The phase leg comprising S_1 and S_3 has lower transformer current at the instant of switching than the phase leg comprising S_2 and S_4. Therefore, the ZVS range of converter is determined by the phase leg comprising S_1 and S_3. However, in the proposed converter, as depicted in Fig. 8(b), the switches S_3 and S_4 have higher transformer current than S_1 and S_2 at the instant of switching. In addition, as mentioned in the mode analysis shown in Fig. 5, three capacitors are charged/discharged at $t = t_1$ [see Fig. 5(b)] and $t = t_7$ [see Fig. 5(k)]. The transformer current at $t = t_7$ is smaller than that of at $t = t_1$; thus, the ZVS range of the proposed converter is determined at $t = t_7$, which is the worst-case condition for achieving ZVS.

In order to compare the ZVS range, (11) can be used in both converters. As mentioned earlier, although the proposed converter has to charge/discharge three rather than two capacitors at the same time with the same energy stored in L_{lk}, switch voltage transition is reduced by half.

Table I compares the ZVS condition in both converters. From the results of Table I, it is concluded that the load current or output power required for achieving ZVS is reduced to $\sqrt{3/8} = 0.612$ times of the PS-PWM converter with the proposed converter. In other words, the proposed converter can achieve ZVS at a much lower output power level; thus, the ZVS range is extended. Table II compares the key features of the proposed converter with the conventional PS-PWM and HB converters.

TABLE I
COMPARISON OF ZVS CONDITION

	Conventional PS-PWM Converter	Proposed Converter
No. of capacitors charged/discharged	2	3
Switch voltage transition	V_{in} to zero	$V_{in}/2$ to zero
$\frac{1}{2}CV^2$	$\frac{1}{2}(2C){V_{in}}^2 = C{V_{in}}^2$	$\frac{1}{2}(3C)(\frac{V_{in}}{2})^2 = \frac{3}{8}C{V_{in}}^2$
Energy stored in L_{lk}	same	

TABLE II
COMPARISON OF KEY FEATURES

	PS-PWM Converter	Conventional HB Converter	Proposed Converter
Transformer voltage (v_{tr})	V_{in}	$V_{in}/2$	$V_{in}/2$
Switch voltage stress	V_{in} for all switches	V_{in} for all switches	• $V_{in}/2$ for S_1, S_3, S_4 • V_{in} for S_2
ZVS	ZVS (limited)	no ZVS	ZVS (extended)
Transformer saturation problem	O	X	X

D. Selection of C_i Value

In (9), it was found that the voltage across C_i is $V_{in}/2$. Since the C_i value cannot be infinite practically, it will have

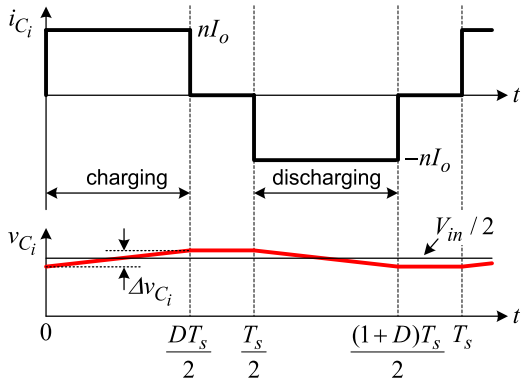


Fig. 9. Calculation of voltage ripple of C_i.

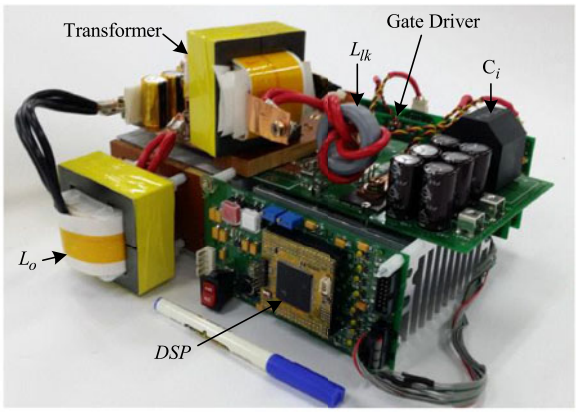


Fig. 10. Photograph of the proposed converter.

voltage ripple. The C_i value and ripple voltage can be found from Fig. 9. For the sake of simplicity, the output inductor current ripple is ignored and the ripple factor (k) is defined as

$$k = \frac{\Delta v_{C_i}}{V_{C_i}} = \frac{\Delta v_{C_i}}{V_{in}/2}. \tag{12}$$

From the capacitor voltage and current relationship, the equation for C_i is expressed as

$$C_i = \frac{i\Delta t}{\Delta v_{C_i}} = \frac{nI_o(DT_s/2)}{kV_{in}/2}. \tag{13}$$

From (10), (13) can be rewritten as

$$C_i = \frac{n^2 D^2 T_s}{2kR_L} \tag{14}$$

where R_L is the load resistance defined as V_o/I_o. In this paper, 50 μF capacitor is used for C_i; thus, k is 0.015 (1.5%) and Δv_{C_i} is 3 V.

In the proposed topology, the input power is transferred to output through S_1 only. Therefore, higher current should flow through S_1, and this will result in increased root-mean-square (rms) current in S_1. However, the S_1 in the dc rail is useful because by inserting S_1 and additional capacitor C_i, the proposed converter is able to perform double step-down operation of the input voltage. Although, the rms current of S_1 is higher,

TABLE III
CIRCUIT PARAMETERS

	Conventional PS-PWM Converter	Proposed Converter
V_{in}, V_o	400 V, 48 V	
P_o, f_s	3 kW, 50 kHz	
L_o	70 μH	
MOSFET ($S_1 - S_4$)	SPW47N60CFD	
Diode ($D_1 - D_4$)	APT100S20BG	
$N_1 : N_2$	26:4	13:4
L_{lk}, C_i	11 μH, none	2.5 μH, 50 μF

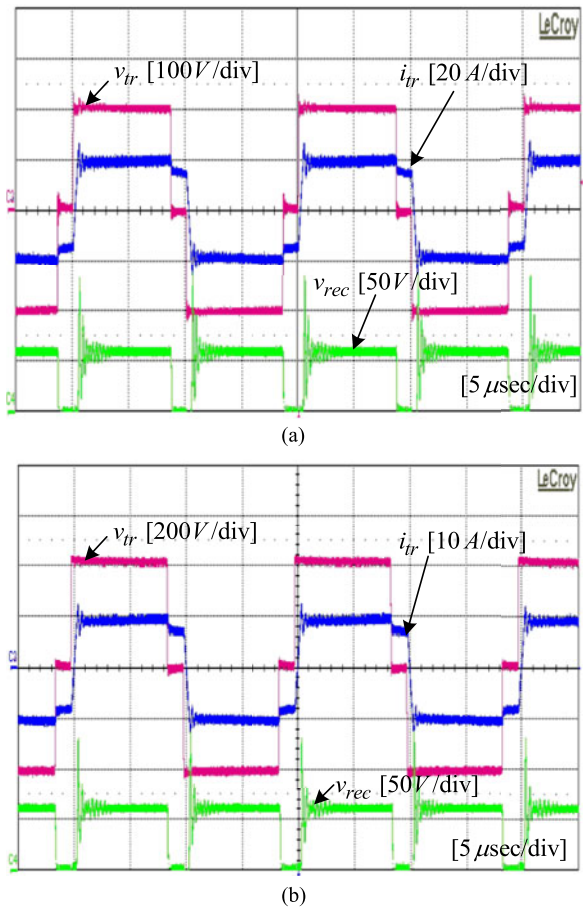


Fig. 11. Transformer voltage, current, and rectifier voltage (P_o = 3kW).

it can utilize lower voltage rating MOSFET with lower $R_{\mathrm{ds(on)}}$ and conduction loss still can be reduced. Therefore, with lower switch voltage stresses and improved ZVS range, the proposed converter is very suitable for high voltage and low current applications.

Moreover, it should be noted that the switch S_1 is in series with input dc voltage source same as in the case of the conventional buck converter, which makes the proposed converter capable of naturally limiting the inrush current and protecting against short circuit (and open circuit as well) [38]–[40]. This is because if overload or short-circuit condition occurs, then the proposed converter is disconnected from input dc voltage source by simply turning off switch S_1 similar to that in the buck

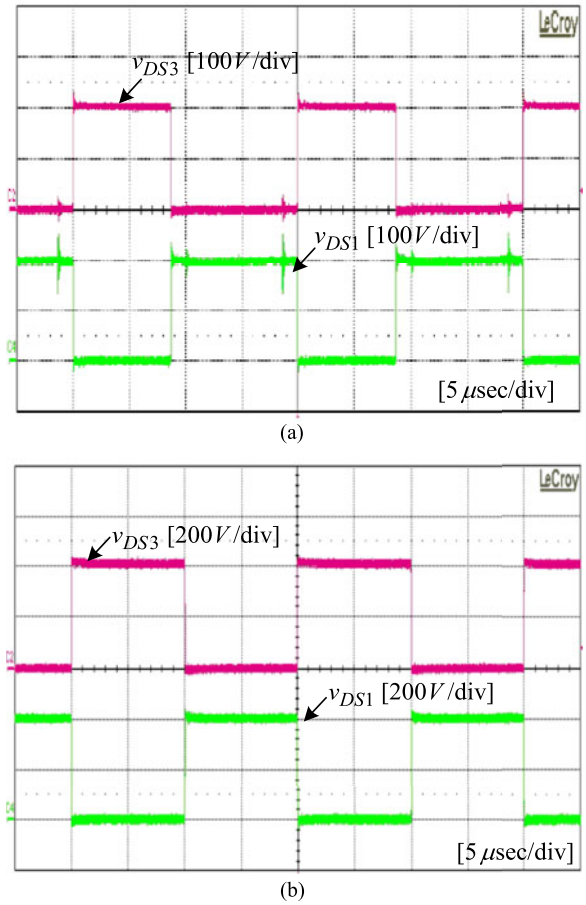


Fig. 12. Switch (S_1, S_3) voltage waveforms. (a) Proposed converter (b) Conventional PS-PWM converter.

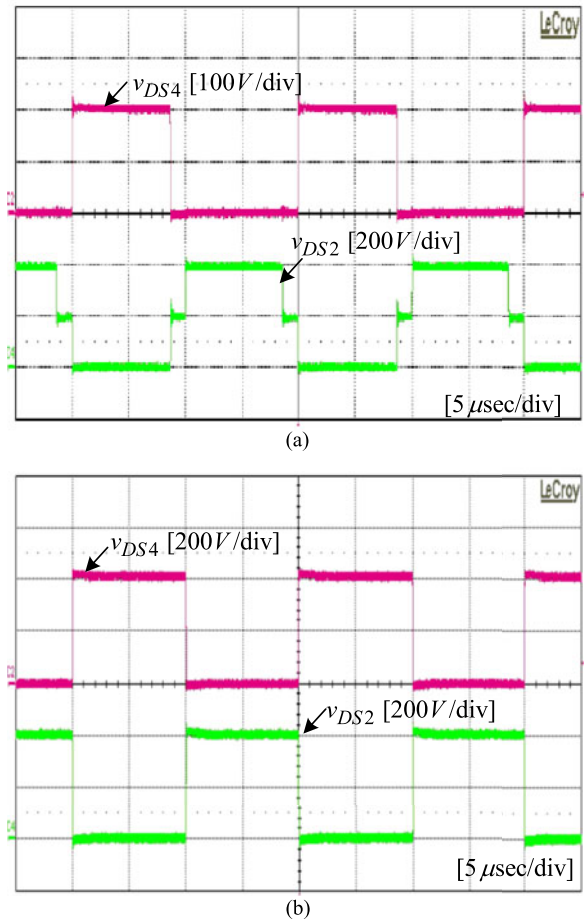


Fig. 13. Switch (S_2, S_4) voltage waveforms. (a) Proposed converter (b) Conventional PS-PWM converter.

converter, which protects the proposed circuit from damaging due to over current.

IV. Experimental Results and Comparison

A 3-kW prototype of the proposed and conventional PS-PWM converters with a bridge rectifier was fabricated, as shown Fig. 10, and compared to verify the performance of the proposed converter. The design parameters and electrical specifications of both converters are given in Table III.

When compared with the PS-PWM converter, due to the double step-down function of the proposed converter, the transformer turns ratio is reduced by half and the L_{lk} is reduced by one-quarter, respectively. Therefore, the circuit behaviors at the transformer's secondary side are exactly the same in both converters. In this paper, L_{lk} is selected for the proposed converter to start ZVS operation at about 25% of the maximum output power, i.e., 750 W. Thus, the theoretical minimum output power required for the ZVS operation for the conventional PS-PWM converter is increased to $750\ \mathrm{W}/0.612 = 1.22\ \mathrm{kW}$.

Fig. 11 shows the transformer voltage (v_{tr}) and current (i_{tr}) waveforms of the conventional PS-PWM and the proposed converter. The secondary rectifier diode voltage (v_{rec}) waveforms are also shown in Fig. 11, and they are exactly the same. Figs. 12 and 13 compare switch voltage stresses in both converters. As expected, all the switch voltage stresses in the conventional PS-PWM converter are equal to V_{in}. However, in the proposed converter, only switch S_2 voltage stress is equal to V_{in}, and the switches S_1, S_3, and S_4 voltages reduce to half of input voltage. Figs. 14–17 show the switching waveforms measured at 1.3 kW output power. As shown, for the conventional PS-PWM converter, the switches S_1 and S_3 cannot achieve ZVS at this power level. However, all the switches in the proposed converter are switched at ZVS condition due to the extended ZVS range of the proposed converter. Figs. 18–21 show the turn-off waveforms of switches measured at 1.3 kW output power.

Fig. 22 shows the transformer current waveforms for both types of converters when the gate signals are slightly mismatched. Unlike the conventional PS-PWM converter, the proposed converter is immune to the transformer saturation problem.

Fig. 23 shows efficiency comparison between the proposed and conventional PS-PWM converters. For the conventional converter, the efficiency was measured with and without dc-blocking capacitor, respectively. In the efficiency comparison of both converters, the same voltage rating devices are used for all switches although the voltage stresses of switches S_1, S_3, and S_4 are reduced by half in the proposed converter. Due to the extended ZVS range of the proposed converter, there is a

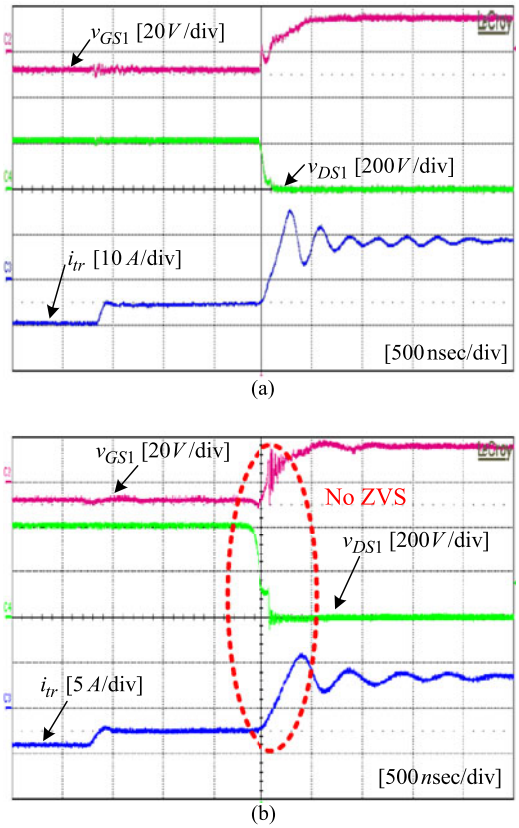


Fig. 14. ZVS waveforms of switch S_1 ($P_o = 1.3$ kW). (a) Proposed converter (b) Conventional PS-PWM converter.

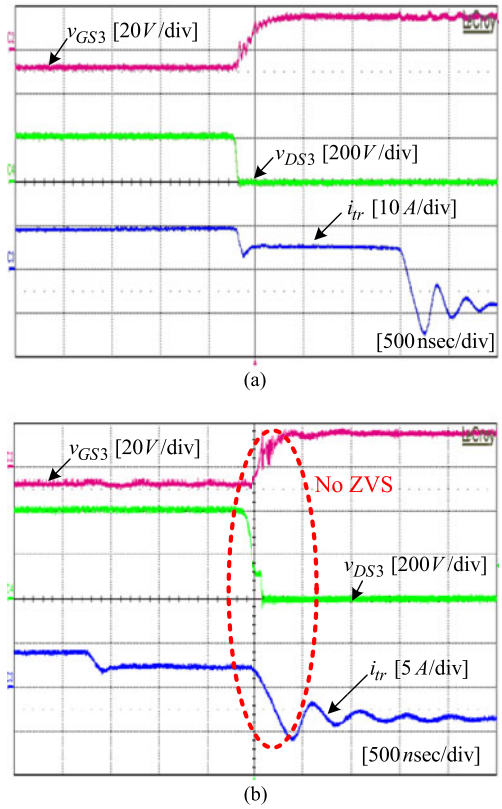


Fig. 16. ZVS waveforms of switch S_3 ($P_o = 1.3$ kW). (a) Proposed converter (b) Conventional PS-PWM converter.

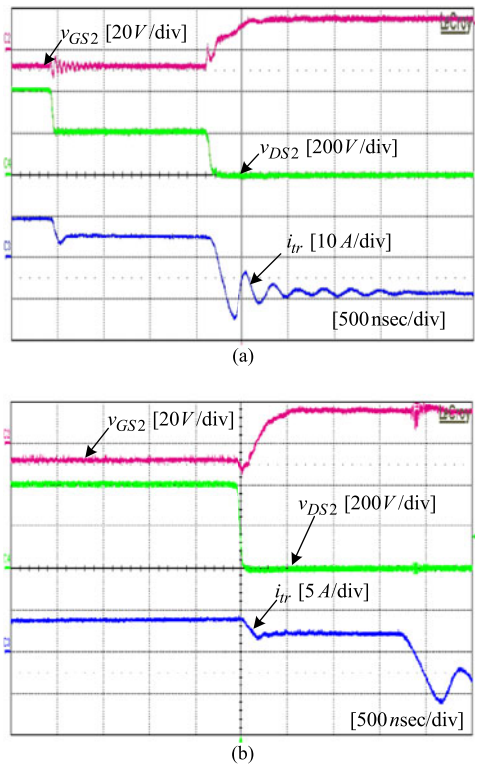


Fig. 15. ZVS waveforms of switch S_2 ($P_o = 1.3$ kW). (a) Proposed converter (b) Conventional PS-PWM converter.

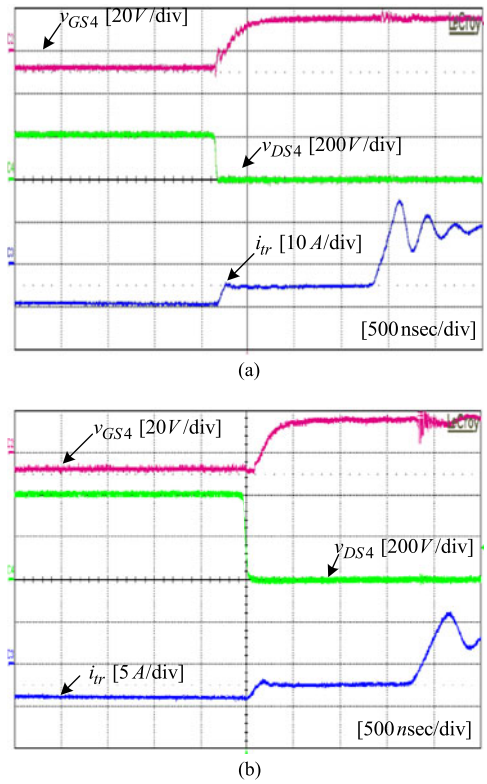


Fig. 17. ZVS waveforms of switch S_4 ($P_o = 1.3$ kW). (a) Proposed converter (b) Conventional PS-PWM converter.

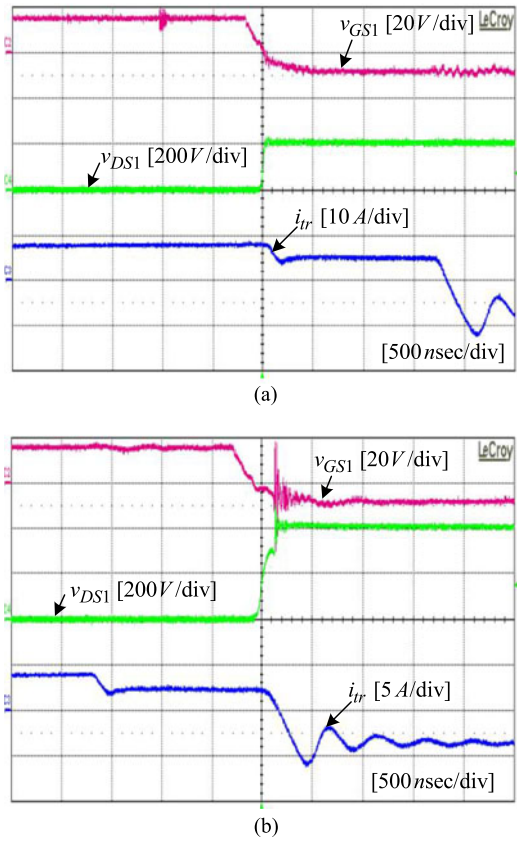


Fig. 18. Turn-off waveforms of switch S_1 ($P_o = 1.3$ kW).

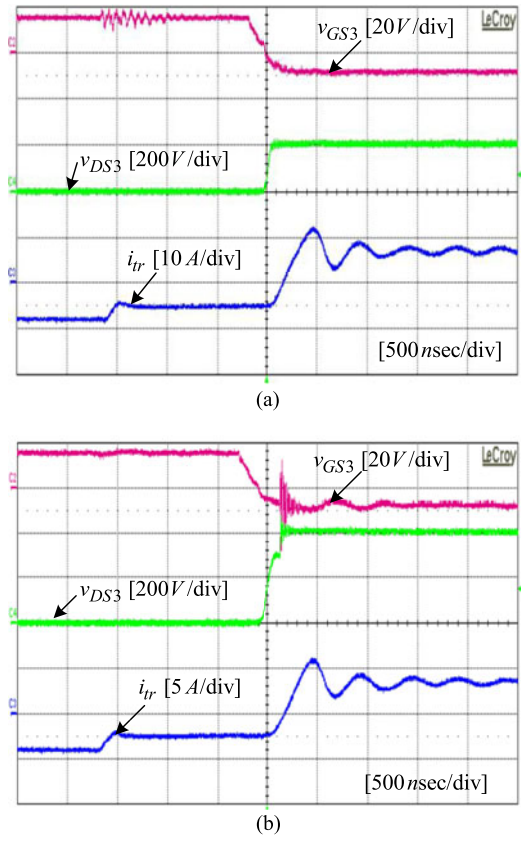


Fig. 20. Turn-off waveforms of switch S_3 ($P_o = 1.3$ kW).

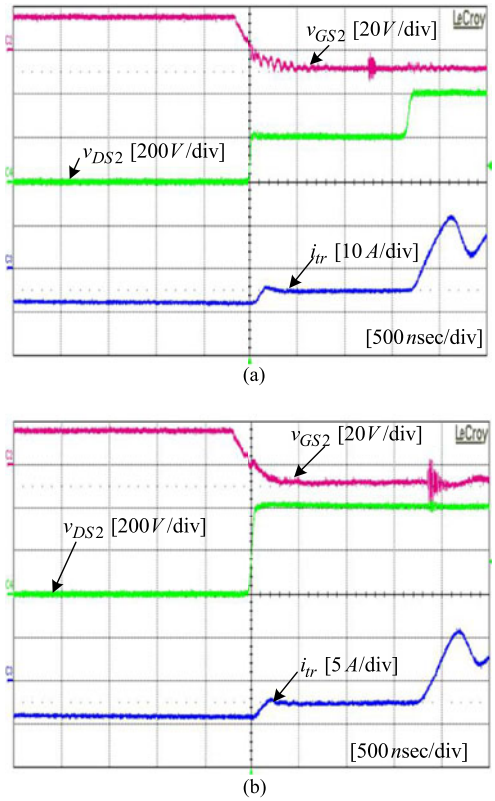


Fig. 19. Turn-off waveforms of switch S_2 ($P_o = 1.3$ kW).

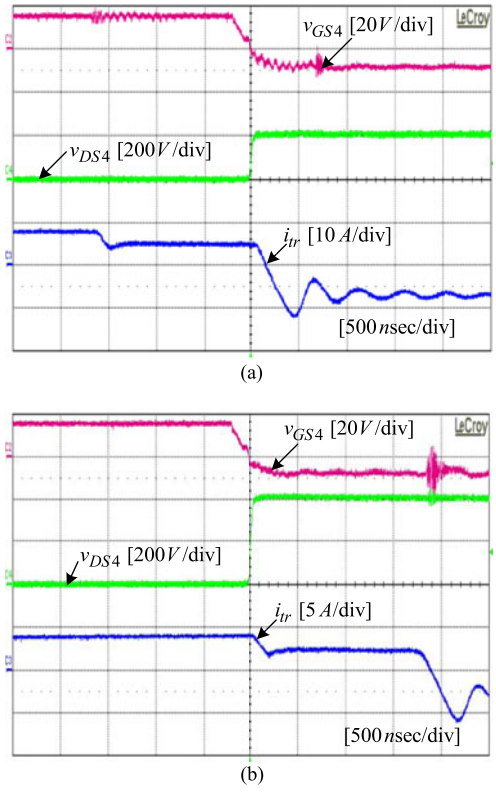
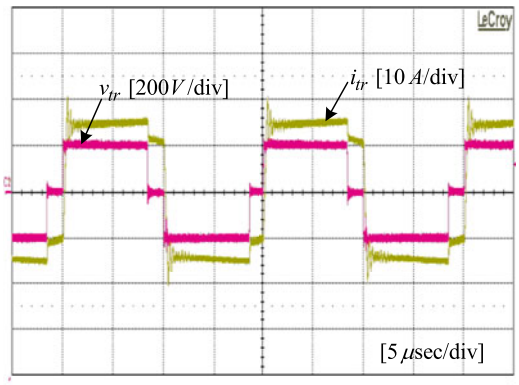
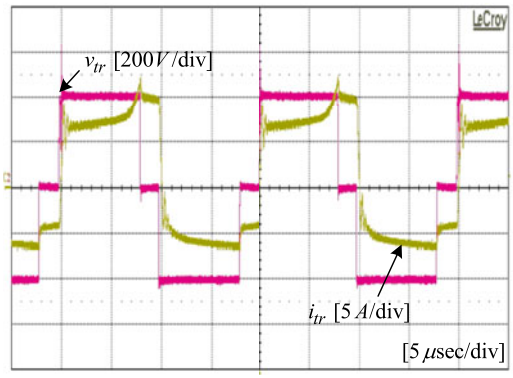


Fig. 21. Turn-off waveforms of switch S_4 ($P_o = 1.3$ kW).



(a)



(b)

Fig. 22. Transformer current with slightly different duty ratios ($P_o = 2$ kW). (a) Proposed converter (b) Conventional PS-PWM converter.

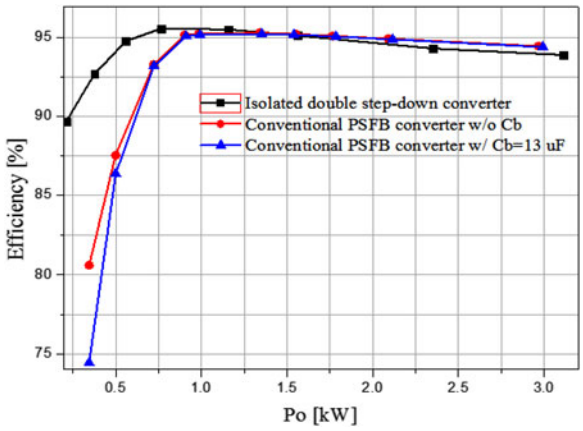


Fig. 23. Comparison of efficiencies.

noticeable difference in efficiency at light load. Since the conventional converter loses ZVS operation around 1.3 kW, there is relatively sharp efficiency drop at this power level. However, the ZVS range of the proposed converter is extended to about 750 W. The proposed converter has slightly lower efficiency at heavy load. This is caused by the higher transformer current and hence higher switch currents and conduction loss. As shown in Fig. 23, with the addition of dc-blocking capacitor ($C_b = 13\,\mu$F), light-load efficiency of the conventional PS-PWM converter becomes slightly lower than that of without dc-blocking capacitor. This is because the addition of dc-blocking capacitor causes lower transformer current, which results in lower available energy for ZVS.

In this paper, the proposed and conventional PS-PWM converters are tested with the full-bridge rectifier circuits at the secondary sides. However, for this low output voltage of 48 V, the center-tapped rectifier can replace the full-bridge rectifier to further improve the efficiency of both the converters.

IV. Conclusion

In this paper, an isolated double step-down dc–dc converter was proposed. Similar to the nonisolated double step-down converter, the proposed converter has double step-down function and reduced switch voltage stress. The proposed converter can obtain higher efficiency than the conventional PS-PWM converter because the reduced voltage stress enables the proposed converter to operate at a wider ZVS range with reduced switching losses. Furthermore, the proposed converter has no transformer saturation problem even when a mismatch exists in the switch duty ratio. Hence, the proposed converter has a higher efficiency and is well suited to applications that require isolation with high step down in voltages.

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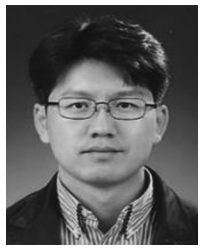

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