Experimental Comparisons Between Modular Multilevel DSCC Inverters and TSBC Converters for Medium-Voltage Motor Drives

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***Abstract*—This paper makes an intensive comparison in operating performance between a modular multilevel double-star chopper-cells (DSCC) inverter and a modular multilevel triple-star bridge-cells (TSBC) converter. Both inverter and converter are intended to drive medium-voltage motors in industrial applications. First, it makes numerical comparisons, thus, resulting in revealing that the torque and frequency of a driven motor produce a significant effect on capacitor-voltage fluctuation and arm or cluster current in the individual DSCC inverter and TSBC converter. Next, a three-phase DSCC inverter and a three-phase TSBC converter with the same rating as 400 V and 15 kW are designed and compared to drive the following two general purposes and specially-designed induction motors; one is rated at the 380-V, 15-kW, 50-Hz four-pole motor, and the other is at the 320-V, 15-kW, 38-Hz six-pole motor. This experimental comparison based on the two downscaled drive systems confirms the validity of the numerical comparison. Finally, this paper concludes that the DSCC inverter is more suitable for driving medium-voltage high-speed motors loaded with quadratic-torque-to-speed profiles like fans, blowers, pumps, and centrifugal compressors. On the other hand, the TSBC converter is more suitable for driving medium-voltage low-speed high-torque motors like mills, kilns, conveyors, and extruders.**

***Index Terms*—Capacitor-voltage fluctuation, medium-voltage motor drives, modular multilevel converter family.**

I. Introduction

MEDIUM-VOLTAGE high-power adjustable-speed motor drives using multilevel converters have been receiving considerable attention for energy savings [1]. Among several multilevel converter candidates, the modular multilevel cascade converter (MMCC) family has been considered as one of emerging high-power converters suitable for medium-voltage motor drives [2].

The basic circuit unit of the MMCC family is either bidirectional dc-to-dc chopper or single-phase H-bridge (full bridge) converter equipped with a dc floating capacitor. This paper refers it to as a "chopper cell" or a "bridge cell," respectively. For the sake of simplicity, a modular multilevel cascade inverter based on double-star chopper cells (MMCC-DSCC) is referred to as a DSCC inverter, and that based on triple-star bridge cells (MMCC-TSBC) as a TSBC converter. A three-phase DSCC inverter is also called as the "modular multilevel converter (MMC)" in [3]. It consists of six arms. Each of the six arms is based on a cascaded connection of multiple chopper cells, leading to dc-to-ac (three phase) bidirectional power conversion. A three-phase TSBC converter is also called as the "modular matrix converter" in [4]. It consists of nine clusters. Each of the nine clusters is based on a cascaded connection of multiple bridge cells, enabling ac (three phase)-to-ac (three phase) bidirectional power conversion with three-phase sinusoidal input (supply or line side) and output (motor side) currents.

Historically, the following two main streams exist in basic research on both DSCC inverter and TSBC converter: one has come from three-phase two-level voltage-source inverters and matrix converters [3]–[7]. The other has come from the so-called "single-star bridge-cells (SSBC)" converter [2], [8]–[25]. The former has no inductor connected in series with each arm or cluster, whereas the latter has it. The existence of the inductor allows a circulating current to flow through the arm or cluster, thus, making it possible to adjust the circulating current actively and appropriately for providing voltage-balancing control of all the chopper-cell or bridge-cell capacitors [8], [9].

Capacitor-voltage control based on the three-phase circulating currents makes both DSCC inverter and TSBC converter applicable to motor drives loaded with any torque-to-speed profile from a theoretical point of view. However, the capacitor-voltage fluctuation, appearing across the dc capacitor of each chopper or bridge cell, imposes a practical limitation on their applications to motor drives. Considerable efforts have been made at applying both DSCC inverter and TSBC converter to motor drives [10]–[25]. The efforts have resulted in putting full-scale DSCC-based motor drives on the market [26], [27]. On the other hand, TSBC-based motor drives are on research stage because only

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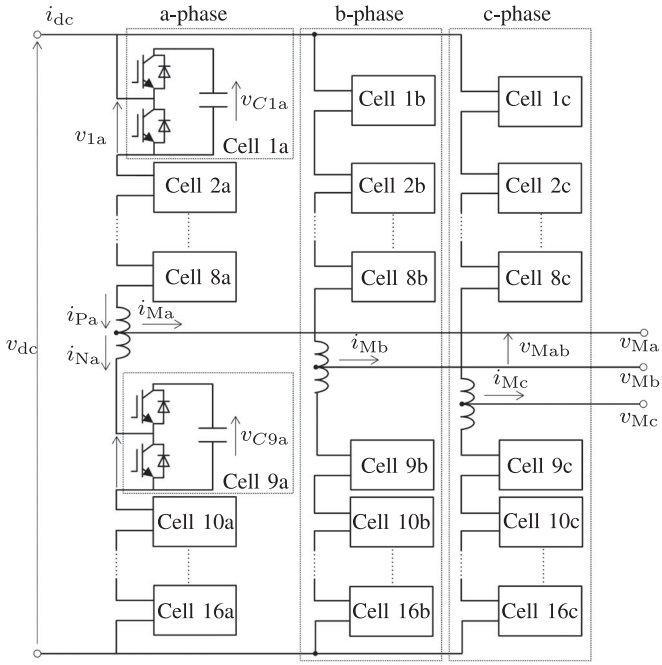

Fig. 1. Circuit configuration of the DSCC inverter with 16 chopper cells per leg, used for the experiments.

three research groups have succeeded in experimental verification of a TSBC-based motor drive [20], [24], [25], and three other research groups have done experiments with three-phase R-L loads [5], [7], [22].

Ilves, Bessegato, and Norrga [28] presented a comprehensive theoretical comparison among a DSCC inverter, a TSBC converter, and a "hexverter" [29], intended for motor drives. They did put emphasis on discussing both current stress accounting for the number of power devices and energy fluctuations appearing on a single capacitor. However, the comparison was made with the following assumption: the driven motor was running at the rated power, voltage, and frequency. Moreover, no experimental verification was included in [28].

The aim of this paper is to make an intensive comparison in capacitor-voltage fluctuation and arm or cluster current between a DSCC inverter and a TSBC converter [30]. Both numerical and experimental comparisons are made under the common use of a three-phase 380-V, 15-kW, 50-Hz, four-pole induction motor. The results obtained from the two downscaled systems are applicable easily to actual medium-voltage motor drives. Finally, two different sets of downscaled motor drives are tested under different load torque-to-speed profiles. The following conclusions are obtained from numerical and experimental results: the DSCC inverter is more suitable for a quadratic-torque load such as fans, blowers, pumps, and centrifugal compressors, whereas the TSBC converter is more suitable for a constant-torque load such as mills, kilns, conveyors, and extruders.

II. Circuit Configuration

A. DSCC Inverter

Fig. 1 illustrates the circuit configuration of a three-phase DSCC inverter with eight chopper cells per arm, which is used for the following experiments. Two arms in each phase are connected in series via a center-tapped inductor, that is smaller in size and lighter in weight than two noncoupled inductors [9]. The center tap of each inductor is directly connected to one of the three motor terminals.

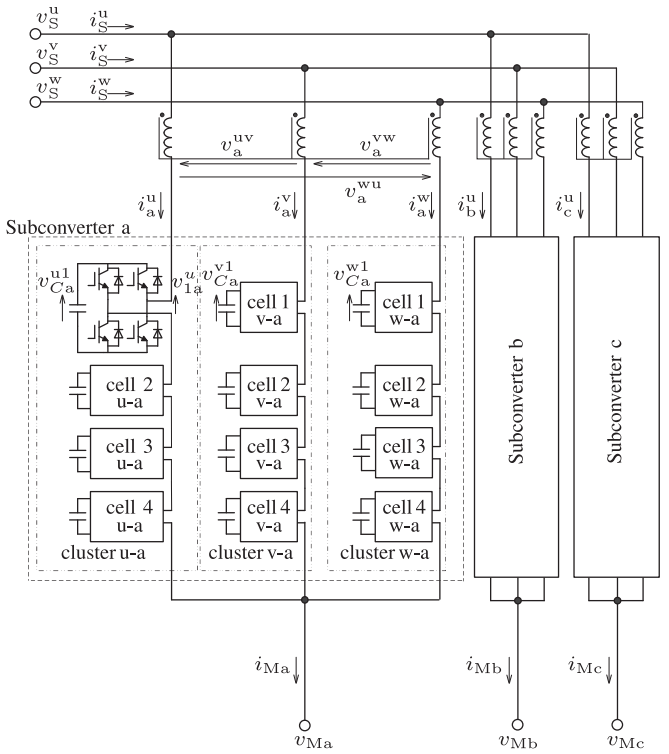

Fig. 2. Circuit configuration of the TSBC converter with four bridge cells per cluster, used for the experiments.

B. TSBC Converter

Fig. 2 illustrates the circuit configuration of a three-phase TSBC converter with four bridge cells per cluster, which is used in the following experiments. The TSBC converter consists of three star-connected subconverters or SSBC converters [2], each of which consists of three clusters. Each cluster is connected directly to one of three terminals in a three-phase three-legged inductor. Using three three-phase three-legged inductors for the TSBC converter results in reducing their size and weight dramatically, compared with using nine noncoupled inductors [20]. The neutral point of each subconverter is connected to one of the three motor terminals.

C. Power Circuit Configurations for Motor Drives

Fig. 3 shows four possible power circuit configurations of DSCC-based motor drives. Each of front-end diode rectifiers has to meet harmonic guidelines or regulations [31]. Fig. 3(a) uses a three-phase six-pulse diode rectifier at the front end. This configuration is characterized by eliminating a line-frequency transformer from the DSCC-based motor drive. The installation of a hybrid active filter combining a neutral-point-clamped (NPC) pulse width modulation (PWM) converter with a single tuned passive filter [32] results in meeting the harmonic guidelines in

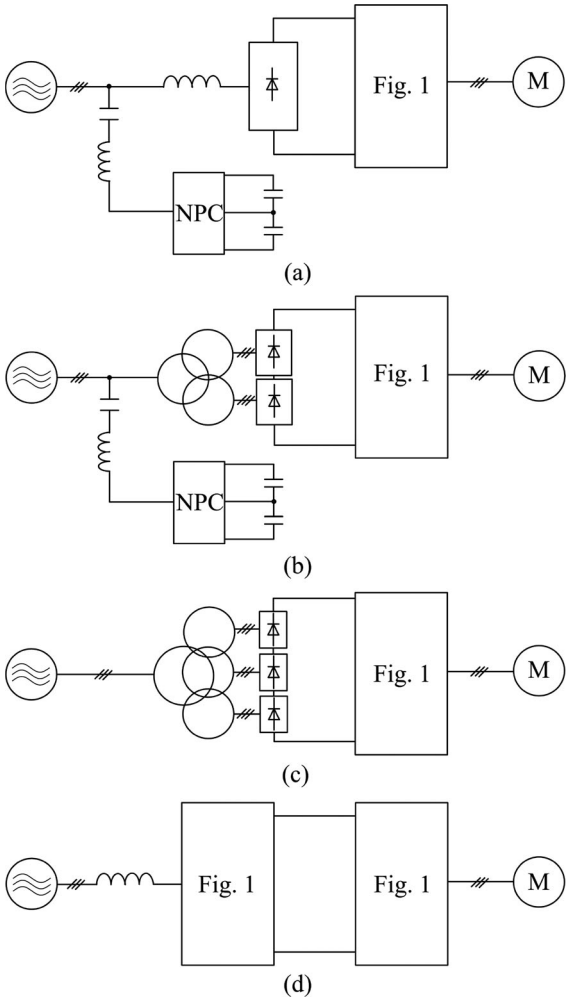

Fig. 3. Power circuit configurations for a DSCC-based motor drive. (a) Six-pulse diode rectifier at the front end. (b) 12-pulse diode rectifier at the front end. (c) 18-pulse diode rectifier at the front end. (d) DSCC converter at the front end (BTB system).

IEEE-519 [31]. Required power ratings of the passive filter and the active filter are 25% and 6% of that of the diode rectifier, respectively [11].

Fig. 3(b) is the case when a three-phase 12-pulse diode rectifier sits at the front end. A widely used three-phase 12-pulse transformer can be employed for voltage matching and galvanic isolation between the ac mains and the motor. Another hybrid filter is connected to mitigate the most dominant 11th- and 13th-harmonic currents, where the passive filter and the active filter have power ratings of 8% and 0.8%, respectively, with respect to the power rating of the 12-pulse diode rectifier [33].

Fig. 3(c) uses a 18-pulse diode rectifier at the front end. This rectifier would meet harmonic regulations without any harmonic filter, but at the expense of using a complicated phase-shifted multiwinding transformer. Full-scale DSCC-based motor drives are available on the market, offering three-phase 12-, 18-, 24-, and 36-pulse diode rectifiers [27]. The three power circuit configurations using the diode rectifiers are suitable for large-capacity fans, blowers, and compressors in terms of reliability, and availability because neither fast-speed control nor regenerative braking is required for these applications.

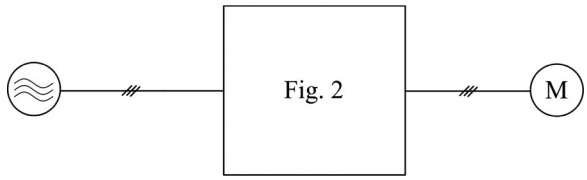

Fig. 4. Power circuit configuration for a TSBC-based motor drive.

As for motor drives without regenerative braking, the power circuit configuration shown in Fig. 3(b) can be considered as the most prospective one among the three configurations shown in Fig. 3(a)–(c). This is coming from the fact that the configuration can meet the grid guidelines, using a simple three-winding transformer with the small-rated hybrid filter.

Fig. 3(d) shows a back-to-back (BTB) system using two DSCC converters, which provides the function of regenerative braking. Three-phase sinusoidal currents can be properly drawn from the ac mains due to three-phase multilevel voltage waveforms produced by the front-end DSCC converter. This results in eliminating both harmonic filter and transformer from the system. Additionally, this system can produce a higher motor voltage than the ac mains voltage by adjusting the common dc-link voltage without dc-link capacitor.

Fig. 4 shows the power circuit configuration for a TSBC-based motor drive. It can achieve ac-to-ac bidirectional power conversion with multilevel input and output voltages. As a result, no harmonic filter is installed at the ac mains side. Appropriately adjusting the capacitor voltage of each bridge cell allows the TSBC converter to produce a higher motor voltage than the ac mains voltage. It is interesting from a practical point of view that neither transformer nor active filter is required on the ac mains in Fig. 3(d) and Fig. 4 as long as the voltage rating of the driven motor is nearly equal to the ac mains voltage. However, the simplest transformer with six terminals can be installed just for voltage matching and/or galvanic isolation between the ac mains and the motor. Both Figs. 3(d) and 4 are applicable to motor drives with regenerative braking.

This paper selects Fig. 3(b) as a DSCC-based motor drive among the three DSCC-based motor drives without regenerative braking, and Fig. 4 out of Fig. 3(d) and Fig. 4, both of which have the function of regenerative braking.

D. Control Method

Control methods of both DSCC inverter and TSBC converter consist of the following three subcontrols:

1) hierarchal capacitor-voltage subcontrol [16], [18], [34];
2) AC-voltage-mitigating subcontrol [13], [19];
3) decoupled current subcontrol among supply, motor, and circulating currents [8], [16], [18], [34].

Subcontrol 1) consists of several feedback controllers for dc-voltage balancing of the floating capacitors, whereas the subcontrol 2) consists of a feedforward controller for ac-voltage mitigation, or capacitor-voltage fluctuation mitigation. It should

TABLE I
PARAMETER OF THE 50-HZ INDUCTION MOTOR

Rated output power		15 kW
Rated frequency		50 Hz
Rated line-to-line rms voltage	$V_{\rm M}$	380 V
Motor power factor	$\cos\phi_{\rm M}$	0.71
Rated rotating speed		1460 r/min
Rated stator rms current	$I_{\rm Mrat}$	32 A
Mutual inductance	M	60 mH
Pole number	$2p$	4
Moment inertia	$J_{\rm M}$	0.2 kg·m^2

TABLE II
COMPARISON CRITERIA USED IN FIGS. 5–8

Supply line-to-line voltage (TSBC converter)	$V_{\rm S}$	396 V
DC-Link voltage (DSCC inverter)	$V_{\rm dc}$	560 V
Supply frequency (TSBC converter)	$f_{\rm S}$	50 Hz
Common-mode frequency (DSCC inverter)	$f_{\rm com}$	100 Hz
Common-mode voltage (TSBC converter)		100 V
Unit capacitance constant [37]	H	50 ms
Supply power factor (TSBC converter)	$\cos\phi_{\rm S}$	1 (or $\cos\phi_{\rm M}$ *)

*Supply power-factor is adjusted to $\cos\phi_{\rm M}$ when the ac-voltage-mitigating control is applied, where $\cos\phi_{\rm M}$ is the motor power-factor.

be noted that control gains for subcontrol 1) determine the regulating performance of the dc-voltage balancing. As long as the control gains are designed in a broad range of tolerance, the amount of capacitor-voltage fluctuation would be independent of the control gains. The circulating-current commands coming from subcontrols 1) and 2) are sent to a circulating-current feedback controller in subcontrol 3). The so-called "field-oriented control" or "vector control" is employed for motor-speed control, which yields and sends three-phase motor-current commands to subcontrol 3). All the three subcontrols are integrated into phase-shifted-carrier PWM. As a result, switching frequencies of all the power devices are always equal to the carrier frequency in any operating condition.

III. COMPARISON BY NUMERICAL ANALYSIS

The following numerical analysis is performed by combining mathematical expressions and the software package "Mathematica," which is completely different in calculating principle from circuit simulation using software packages such as "PSCAD/EMTDC" and "MATLAB/Simulink."

A. Assumptions and Conditions for Numerical Comparisons

Table I summarizes the specifications of the 50-Hz induction motor used for numerical analysis. The following assumptions are made to achieve numerical analysis:

1) the dc mean capacitor voltage of either chopper or bridge cell is kept equal to its command;
2) PWM operation is replaced with the so-called "averaged model switch" [35], this means that the arm or cluster voltage and current are equal to its command;
3) the motor mechanical speed is kept equal to its command;
4) the motor current is controlled to be the minimum by adjusting a magnetizing-current component. How to implement it can be found in [36].

Assumptions 1) and 2) mean that a relationship between the instantaneous power flowing into each arm or cluster $p_{\rm x}$ and the instantaneous voltage fluctuation $\tilde{v}_{C\rm x}$ is approximately given as follows [11], [13], [18], [19]:

$$\tilde{v}_{C\rm x} \simeq \frac{1}{nCV_C}\int p_{\rm x}dt \tag{1}$$

where n is the number of chopper or bridge cells per arm or cluster, C is the capacitance value, and V_C is the dc mean capacitor voltage. The subscript "x" is either d or t, indicating either DSCC inverter or TSBC converter, respectively. Assumption 3) implies that the numerical analysis assumes steady-state operation. Assumption 4) determines the minimum motor rms current under a given motor torque.

Moreover, the following conditions are introduced to the numerical analysis:

1) evaluation indices are the peak-to-peak capacitor-voltage fluctuation normalized by its dc mean value $\Delta\tilde{v}_{C\rm x}/V_C$, and the arm or cluster current normalized by the rated motor current $I_{\rm Pa}/I_{\rm Mrat}$ and $I_{\rm a}^{\rm u}/I_{\rm Mrat}$, respectively;
2) the ac-voltage-mitigating controls proposed in [13] and [19] are used for the numerical comparison;
3) the amplitude of the supply line-to-line voltage in the TSBC converter is set to the same as the dc-link voltage in the DSCC inverter;
4) Table II summarizes the circuit parameters of the DSCC inverter and the TSBC converter.

Condition 1) approximates the normalized peak-to-peak capacitor-voltage fluctuation as follows:

$$\frac{\Delta\tilde{v}_{C\rm x}}{V_C} \simeq \frac{2|\tilde{v}_{C\rm x}|_{\max}}{V_C} \tag{2}$$

where, $|\tilde{v}_{C\rm x}|_{\max}$ is the amplitude of $\tilde{v}_{C\rm x}$ in (1). Note that both voltage fluctuation and arm or cluster current are expressed in terms of motor and circuit parameters, motor torque, and motor frequency with the help of assumptions 3) and 4). Condition 4) makes it possible to compare the DSCC inverter with the TSBC converter under the same unit capacitance constant [37] and motor parameters.

The normalized peak-to-peak capacitor-voltage fluctuation is calculated by using (1) and (2), whereas the arm or cluster rms current is calculated by using the already derived equations described in [11] and [18]. Hagiwara, Nishimura, and Akagi [11] and Hagiwara, Hasegawa, and Akagi [13] provided the mathematical expression given by (1) to a DSCC inverter, while Kawamura, Hagiwara, and Akagi [18], [19] to a TSBC converter with and without the ac-voltage-mitigating control, respectively.

B. Numerical Comparisons Without AC-Voltage-Mitigating Control

Fig. 5 shows three-dimensional (3-D) contour plots with color graduation for the DSCC inverter. Here, (a) shows the normalized peak-to-peak voltage fluctuation, and (b) shows the normalized arm rms current. Both are calculated without ac-voltage-mitigating control. This means that neither common-mode voltage nor circulating current is superimposed

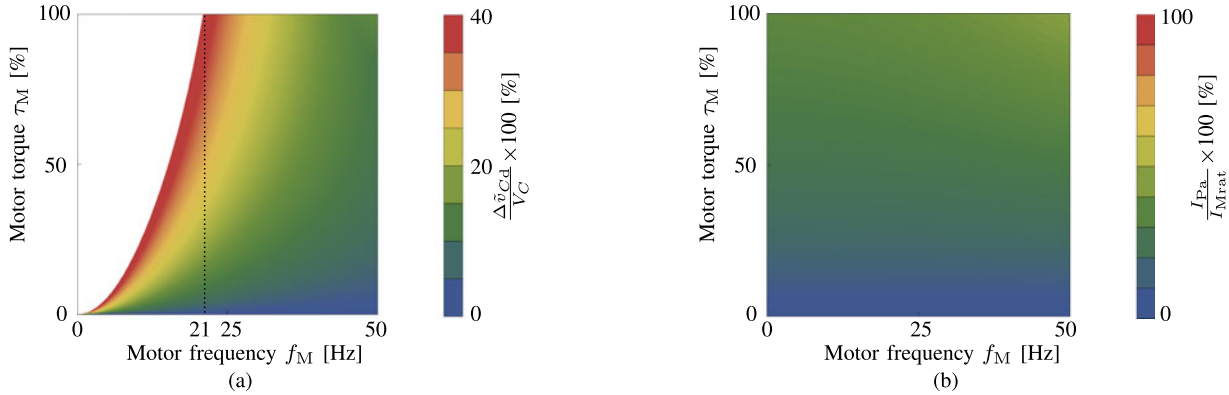

Fig. 5. Numerical calculations of both normalized peak-to-peak capacitor-voltage fluctuation $\Delta\tilde{v}_{\rm Cd}/V_C$ and normalized arm rms current $I_{\rm Pa}/I_{\rm Mrat}$ in the DSCC inverter. No ac-voltage-mitigating control is applied. (a) Normalized capacitor-voltage fluctuation. (b) Normalized arm rms current.

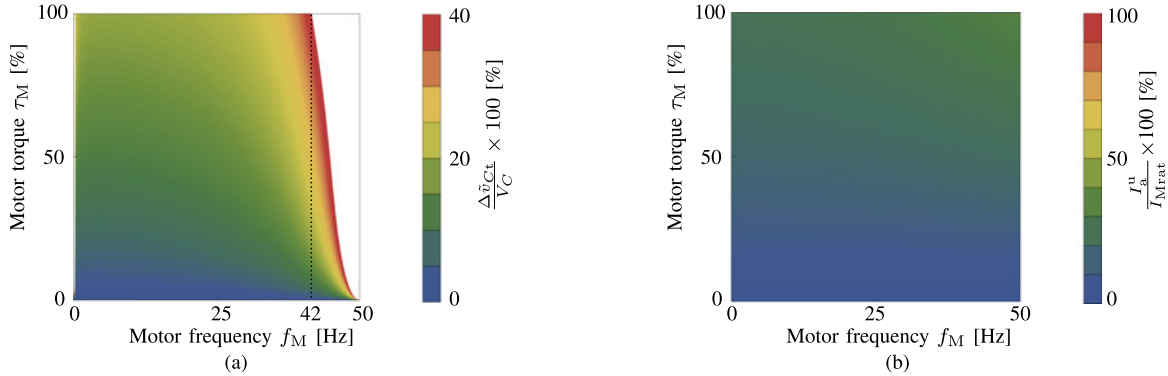

Fig. 6. Numerical calculations of both normalized peak-to-peak capacitor-voltage fluctuation $\Delta\tilde{v}_{\rm Ct}/V_C$ and normalized cluster rms current $I_{\rm a}^{\rm u}/I_{\rm Mrat}$ in the TSBC converter. No ac-voltage-mitigating control is applied. (a) Normalized capacitor-voltage fluctuation. (b) Normalized cluster rms current.

on arm or cluster voltage and arm or cluster current. Fig. 6(a) and (b) describe those for the TSBC converter. The white area means that the capacitor-voltage fluctuation is over 40% of its dc mean value, and the arm or cluster rms current is larger than the rated motor rms current.

Fig. 5(a) indicates that the value of $\Delta\tilde{v}_{\rm Cd}/V_C$ is more than 40% for a major part of the motor torque in a low-frequency range. However, as the motor frequency $f_{\rm M}$ increases, the value of $\Delta\tilde{v}_{\rm Cd}/V_C$ is reduced quadratically.[1] In a frequency range of $f_{\rm M}\geq 21$ Hz, the DSCC inverter can produce any motor torque with a peak-to-peak voltage fluctuation of less than 40%. In Fig. 5(b), the value of $I_{\rm Pa}/I_{\rm Mrat}$ increases as a motor torque gets higher. However, it is less than 60% in all the frequency range.

In Fig. 6(a), the value of $\Delta\tilde{v}_{\rm Ct}/V_C$ is smaller than 40% in a frequency range of $f_{\rm M}\leq 42$ Hz, regardless of the motor torque $\tau_{\rm M}$. However, it increases drastically as the motor frequency is getting close to the supply frequency of 50 Hz. In Fig. 6(b), the value of $I_{\rm a}^{\rm u}/I_{\rm Mrat}$ is less than 35% in all the operating frequencies, which is smaller by 33% than that of the DSCC inverter. The above difference between arm and cluster rms currents comes from the following difference between the DSCC inverter and the TSBC converter: one of the three motor currents flows through two arms to one motor terminal in the DSCC inverter, whereas it flows through three clusters to one motor terminal in the TSBC converter.

C. Numerical Comparisons With AC-Voltage-Mitigating Control

Fig. 7(a) and (b) shows 3-D contour plots of the normalized peak-to-peak voltage fluctuation and the normalized arm rms current, respectively, for the DSCC inverter. Fig. 8(a) and (b) shows those for the TSBC converter. The ac-voltage-mitigating controls described in [13] and [19] are used in all the frequency range for both DSCC inverter and TSBC converter. The common-mode voltage applied to the DSCC inverter is maximized in all the frequency range to obtain the minimum circulating current [13]. On the other hand, a dc common-mode voltage is superimposed on all the nine clusters in the TSBC converter. The common-mode voltage superimposition is indispensable for achieving stable capacitor-voltage control when the ac-voltage-mitigating control described in [19] is used. The dc common-mode voltage is set to a constant value of 100 V in all the frequency range. Design considerations on the common-mode voltage have been described in [13] and [19].

[1]The motor frequency $f_{\rm M}$ [Hz] is defined as $pN_{\rm rm}/60$, where $p=2$ in Sections III and IV, and $N_{\rm rm}$ has a unit of [r/min].

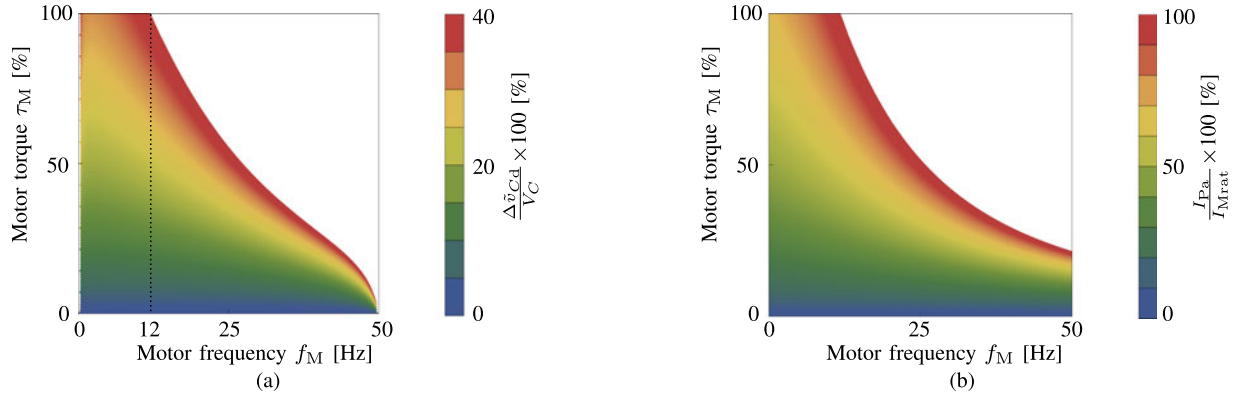

Fig. 7. Numerical calculations of both normalized peak-to-peak capacitor-voltage fluctuation $\Delta\tilde{v}_{C\rm d}/V_C$ and normalized arm rms current $I_{\rm Pa}/I_{\rm Mrat}$ in the DSCC inverter. The ac-voltage-mitigating control in [13] is applied in all the frequency range. (a) Normalized capacitor-voltage fluctuation. (b) Normalized arm rms current.

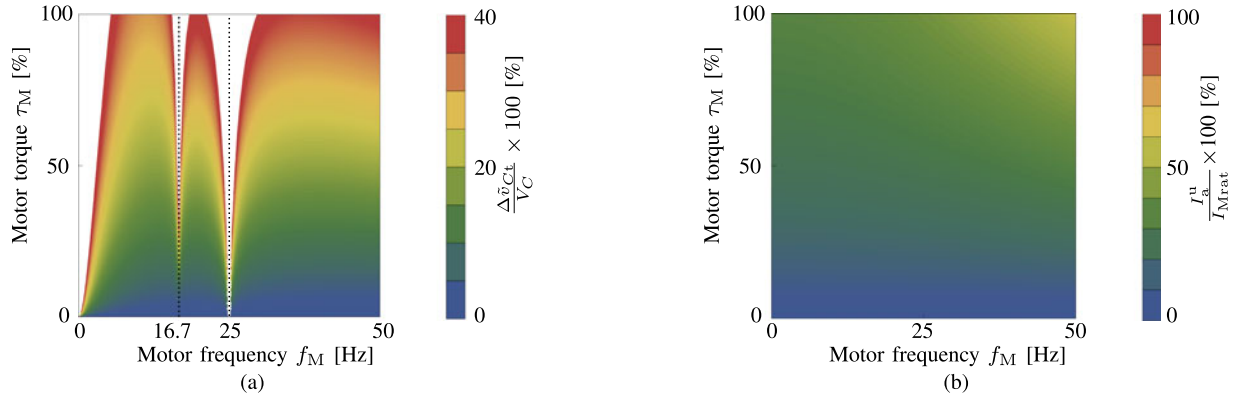

Fig. 8. Numerical calculations of both normalized peak-to-peak capacitor-voltage fluctuation $\Delta\tilde{v}_{C\rm t}/V_C$ and normalized cluster rms current $I_{\rm a}^{\rm u}/I_{\rm Mrat}$ in the TSBC converter. The ac-voltage-mitigating control in [19] is applied in all the frequency range. (a) Normalized capacitor-voltage fluctuation. (b) Normalized cluster rms current.

Fig. 7(a) finds that the value of $\Delta\tilde{v}_{C\rm d}/V_C$ gets smaller than that in Fig. 5(a) in a low-frequency range. On the other hand, it gets larger than that in Fig. 5(a) in a high-frequency range because of the following reasons:

1) as a motor voltage increases, the common-mode rms voltage superimposed should be reduced to avoid overmodulation;
2) the circulating rms current is inversely proportional to the common-mode rms voltage [12].

An increased circulating rms current is accompanied by an increased voltage fluctuation in a high-frequency range. Therefore, the mitigating control is useful only in a low-frequency range. The mitigating control allows the DSCC inverter to produce any motor torque with a capacitor-voltage fluctuation of less than 40% in a frequency range of $f_{\rm M} \leq 12$ Hz. However, the voltage fluctuation at 1 Hz with the rated torque is 1.5 times as high as that of the TSBC converter shown in Fig. 6(a). In Fig. 7(b), the arm rms current gets more than twice as high as that in Fig. 5(b) in all the frequency range. Figs. 5 and 7 reveal that the use of the DSCC inverter is more suitable for applications to high-speed motor drives, even when the mitigating control is fully active.

Fig. 8(a) provides the effectiveness of the mitigating control for the TSBC converter, where the rated torque can be produced even when the motor frequency is close, and equal to, the supply frequency, with a voltage fluctuation of less than 40%. However, it gets larger than that in Fig. 6(a) in a low- to middle-frequency range, and it diverges at the following two frequencies:

1) around $f_{\rm M} = 16.7$ Hz, the circulating current superimposed to achieve the mitigating control interacts with motor voltages;
2) around $f_{\rm M} = 25$ Hz, a frequency component present in the circulating currents becomes a low frequency or dc. As a result, the circulating currents interact with the dc common-mode voltage superimposed to achieve capacitor-voltage control.

The above two cases result in forming low frequency or dc power sent to, or back from, each capacitor. Thus, the low frequency and dc powers bring voltage divergence to each capacitor. This imposes a limitation on the use of the mitigating control to the case that the motor frequency is close, and equal to, the supply frequency or ac mains. Although the mitigating control is effective around the frequency, the value of the peak-to-peak voltage fluctuation at $f_{\rm M} = 50$ Hz and $\tau_{\rm M} = 100\%$ (the rated

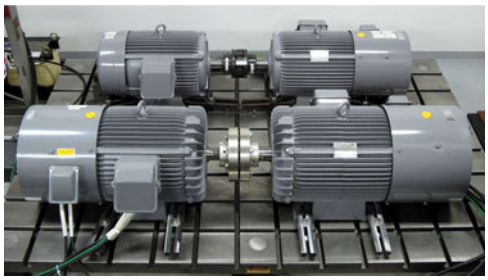

Fig. 9. Photograph of the 380-V, 50-Hz, 4-pole, 15-kW induction motor (back-left side), the 320-V, 38-Hz, 6-pole, 15-kW induction motor (front-left side), and mechanically-coupled induction generators (right-side). Note that mechanical-coupling covers for safety are removed to take this photo.

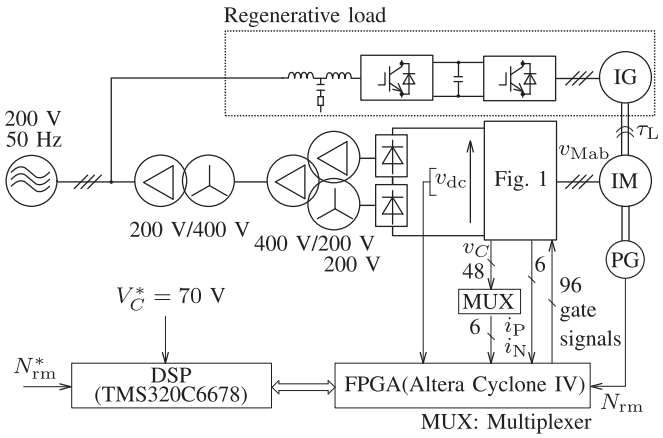

Fig. 10. The 400-V, 15-kW downscaled DSCC-inverter system used in experiments.

torque) is 2.6 times as large as that of the DSCC inverter shown in Fig. 5(a). In Fig 8, the cluster rms current is smaller than the rated motor rms current in all the frequency range. However, it increases by 1.5 times larger than that in Fig. 6(b) at 50 Hz and the rated torque. Figs. 6 and 8 lead to the following conclusion: the TSBC converter is more suitable for low-speed motor drives.

IV. Experimental Comparisons by Downscaled Systems

A. Experimental System

Fig. 9 shows the photograph of two sets of induction motors and generators. The one at the back side was commonly used in this section, whereas the other at the front side was used in the next section. As described in the previous section, Table I summarized the specifications of the 380-V, 15-kW, 4-pole, 50-Hz induction motor sitting at the back side of Fig. 9.

Fig. 10 depicts the 400-V, 15-kW downscaled DSCC-inverter system. Table III summarizes the circuit parameters of the inverter. The dc mean capacitor-voltage command of each chopper cell, V_C^* was set to 70 V.

Fig. 11 depicts the 400-V, 15-kW downscaled TSBC-converter system. Table IV summarizes circuit parameters of the converter. The dc mean capacitor-voltage command of each bridge cell, V_C^* was set to 200 V. The control methods described in Section II-D were employed for both DSCC inverter and TSBC converter.

TABLE III
Circuit Parameters of Fig. 1 (DSCC Inverter)

Rated active power	P	15 kW
Rated dc-link voltage	V_{dc}	560 V
Center-tapped inductor	L_Z	2.0 mH (5.9%)
DC capacitor of chopper cells	C	6.6 mF
DC-capacitor voltage	V_C	70 V
Unit capacitance constant	H	52 ms
Cell count per leg	n	16
Triangle-carrier frequency	f_C	1.5 kHz
Equivalent carrier frequency	nf_C	24 kHz

Note: The value in () is on a 400-V, 15-kW, and 50-Hz base.

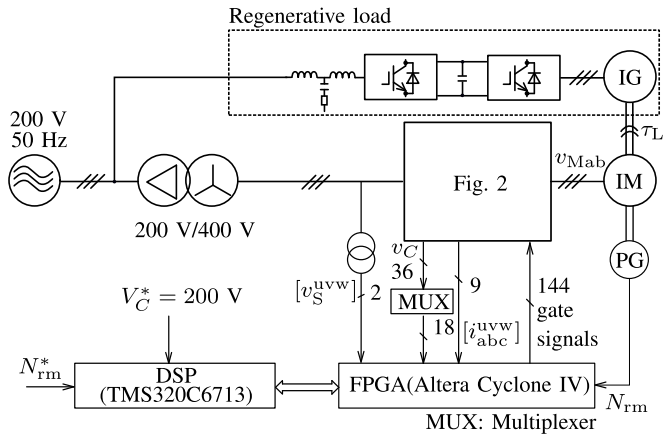

Fig. 11. 400-V, 15-kW downscaled TSBC-converter system used in experiments.

TABLE IV
Circuit Parameters of Fig. 2 (TSBC Converter)

Rated active power	P	15 kW
Supply line-to-line rms voltage	V_S	400 V
Supply line frequency	f_S	50 Hz
Three-legged inductor	L	5 mH (15%)
DC capacitor of bridge cells	C	1.7 mF
DC-capacitor voltage	V_C	200 V
Unit capacitance constant	H	81 ms
Cell count per cluster	n	4
Triangular-carrier frequency	f_C	1 kHz
Equivalent-carrier frequency	$2nf_C$	8 kHz

Note: The value in () is on a 400-V, 15-kW, and 50-Hz base.

B. Comparisons in Start-Up Performance of the 50-Hz Induction Motor

Figs. 12 and 13 show the experimental start-up performance of the 50-Hz induction motor loaded at 40% torque, which were driven by the DSCC inverter and the TSBC converter, respectively. The mechanical speed command N_{rm}^* was increased up from 0 to 1500 r/min with a ramp rate of 90 r/min/s for both experiments.

In Fig. 12, the ac-voltage-mitigating control discussed in [13] was switched over, according to the motor frequency as follows:

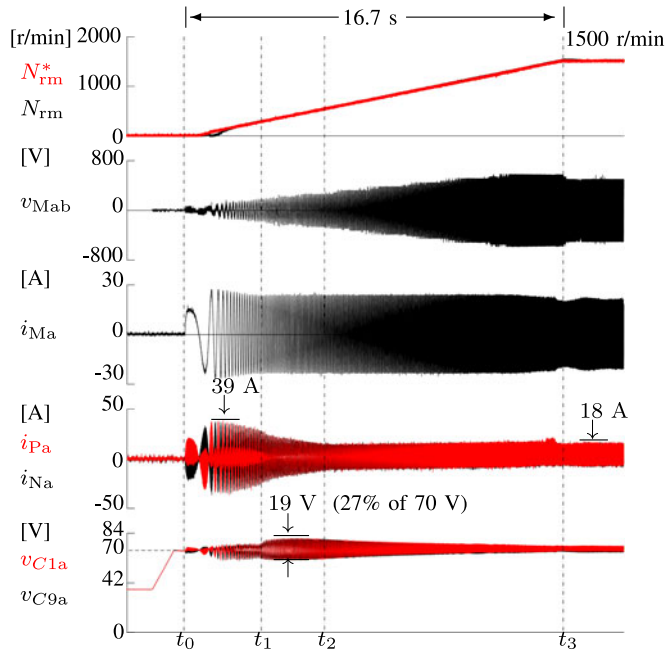

Fig. 12. Experimental start-up performance of the DSCC-driven 50- Hz induction motor loaded at 40% torque.

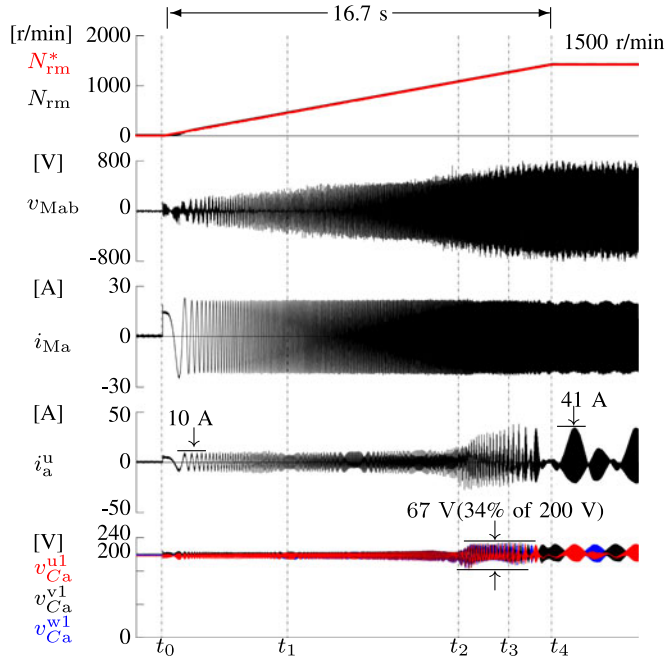

Fig. 13. Experimental start-up performance of the TSBC-driven 50- Hz induction motor loaded at 40% torque.

1) $t = t_0$ to t_1 (0–20 Hz): It was active where a square-wave circulating current and a square-wave common-mode voltage of 200 V and 100 Hz were superimposed.
2) $t \geq t_1$ (20 Hz): It was inactive completely.

Note that the mitigating control was getting gradually inactivate from 10 to 20 Hz, where both circulating current and common-mode voltage were reduced linearly.

The peak value of the arm current $i_{\rm Pa}$ takes the maximum of 39 A at 1 Hz and 18 A at 50 Hz. The maximum peak-to-peak voltage fluctuation of v_{C1a} is 19 V at 15 Hz.

In Fig. 13, two kinds of ac-voltage-mitigating controls were switched over as follows:

1) $t = t_0$ to $t = t_1$ (0– 14 Hz): the control proposed in [18] was active;
2) $t = t_1$ to $t = t_2$ (14–35 Hz): neither controls were active;
3) $t = t_2$ to $t = t_3$ (35– 40 Hz): the other in [19] was being gradually activated where both circulating current and dc common-mode voltage were being increased linearly;
4) $t \geq t_3$ (40 Hz): the mitigating control in [19] was activated completely.

The peak value of the cluster current, $i^{\rm u}_{\rm a}$ is 10 A in a low-frequency range, and the maximum of 41 A around 50 Hz. The voltage fluctuation of $v^{\rm u1}_{Ca}$ is 67 V at 50 Hz. These experimental results find out clear differences in peak-to-peak voltage fluctuation and arm or cluster current between the DSCC inverter and the TSBC converter.

C. Comparisons in Steady-State Performance of the 50-Hz Induction Motor

Fig. 14 shows the voltage and current waveforms of the DSCC inverter where the motor was loaded at 40% torque, and running at 30 r/min. Each of the positive and negative arm currents in a phase, $i_{\rm Pa}$ and $i_{\rm Na}$, includes the following three-frequency components; 100-Hz square-wave circulating current, 1-Hz motor current, and small switching-ripple components. The rms value of the positive arm current $i_{\rm Pa}$ was 15 A in rms (47% on a 32-A base). The capacitor-voltage fluctuation v_{C1a} was 11 V in peak-to-peak (16% on a 70-V base).

Fig. 15 shows the voltage and current waveforms of the TSBC converter where the 50-Hz motor was loaded at 40% torque and running at 1500 r/min. Note that the output frequency of the TSBC converter was 50.4 Hz due to the existence of a slip frequency of 0.4 Hz. The three cluster currents, $i^{\rm u}_{\rm a}$, $i^{\rm v}_{\rm a}$, and $i^{\rm w}_{\rm a}$, include the following two frequency components; a 0.4-Hz component related to the frequency difference between the motor and the ac mains, and the other is the line frequency of 50 Hz because switching ripple components were negligibly small. The cluster rms current was 11 A in rms (33% on a 32-A base). The capacitor-voltage fluctuation was 42 V in peak-to-peak (21% on a 200-V base).

Figs. 16 and 17 show the voltage and current waveforms of the DSCC inverter and the TSBC converter, respectively, where the 50-Hz motor was loaded at 40% torque, and running at 750 r/min. The arm current waveform of the DSCC inverter consists of dc, motor frequency (= 25 Hz), and switching-ripple-frequency components. It was measured to be 8 A in rms (25%). On the other hand, the cluster current waveform of the TSBC converter consists of the motor frequency (= 25 Hz), line frequency (=50 Hz), and switching-ripple-frequency components. Note that the switching-ripple components of both arm and cluster currents look negligibly small. The cluster rms current was 5 A in rms (16%), which is smaller by 38% than the arm current of the DSCC inverter as it is expected in Section

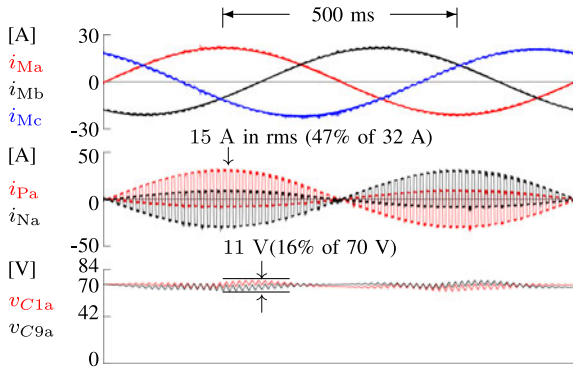

Fig. 14. Experimental steady-state performance of the DSCC-driven 50- Hz induction motor loaded at 40% torque and f_{M} =1 Hz.

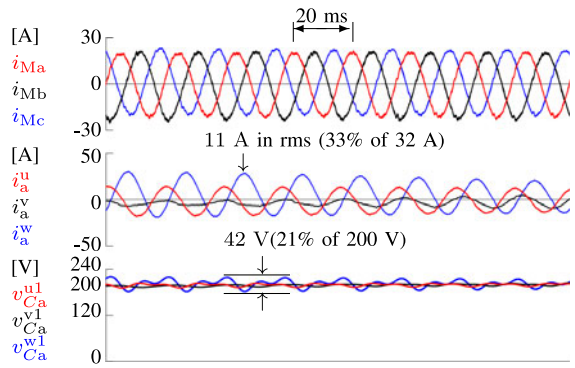

Fig. 15. Experimental steady-state performance of the TSBC-driven 50- Hz induction motor loaded at 40% torque and f_{M} =50 Hz.

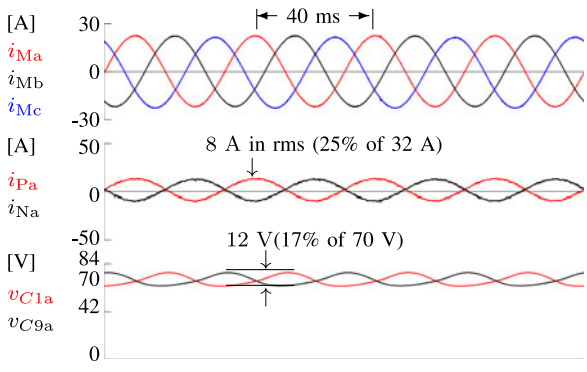

Fig. 16. Experimental steady-state performance of the DSCC-driven 50- Hz induction motor loaded at 40% torque and f_{M} =25 Hz.

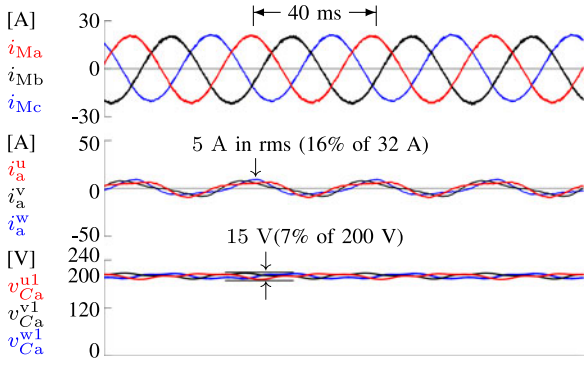

Fig. 17. Experimental steady-state performance of the TSBC-driven 50- Hz induction motor loaded at 40% torque and f_{M} =25 Hz.

III-B. The DSCC inverter had a peak-to-peak capacitor-voltage fluctuation of 12 V (7%), while the TSBC converter had that of 15 V (7%).

Fig. 18 shows comparisons under the same motor and control parameters and the same motor-operating conditions between the numerical analysis and the experiment. Here, (a) is related to normalized capacitor-voltage fluctuation in peak-to-peak, and (b) to normalized arm or cluster current in rms. The red lines are for the DSCC inverter, while the black lines are for the TSBC converter. The white circles in Fig. 18 are plotted from the experimental waveforms shown in Figs. 14–17.

It should be emphasized that all the white circles in red and black are plotted around the red and black lines, respectively, which are obtained from the numerical analysis in Fig. 18(a) and (b). The traces of the red and black lines in Fig. 18(a) are somewhat similar to the profiles of the peak capacitor voltages shown in Figs. 12 and 13, respectively.

V. Operating Performance of Two Motor Drives

A. Startup Performance of the DSCC-Driven 50-Hz Motor Loaded at a Quadratic-Torque-to-Speed Profile

Fig. 19 shows a quadratic-torque-to-speed profile, considering the large-capacity fans or blowers. From 0 to 15 r/min, the inverter-driven motor was loaded with a torque of 40%, considering the static friction of the fans or blowers. After 15 r/min, the load torque is proportional to a square of motor speed.

Fig. 20 shows the start-up waveforms of the DSCC-driven 50-Hz induction motor. From $t = t_0$ to $t = t_1$, the motor was loaded at a constant torque of 40%. The motor started up from a standstill to 1500 r/min ($t = t_0$ to $t = t_3$) with a ramp rate of 30 r/min/s without any instability. The line-to-line motor voltage v_{Mab} was controlled to a constant value of 340 V from $t = t_2$ to avoid overmodulation. It can be realized by reducing a magnetizing-current component in the motor current. Although a small change occurs in the motor-current waveform of i_{Ma} at $t = t_2$, it produced no effect on the motor-drive performance. The amplitudes of the positive and negative arm currents i_{Pa} and i_{Na} at 1 Hz and at the rated frequency of 50 Hz are 28 and 32 A, respectively. The maximum peak-to-peak capacitor-voltage fluctuation of $v_{C1\mathrm{a}}$ is 9.6 V at 20 Hz, which is 13.7% on a 70-V base.

B. Startup Performance of the TSBC-Driven 38-Hz Motor Loaded at the Rated Torque

Table V summarizes the parameters of the 320-V, 15-kW, 38-Hz, 6-pole induction motor driven by the TSBC converter.

Fig. 21 shows the startup waveforms of the 38-Hz induction motor loaded at the rated torque in the whole speed range. The motor started up from a standstill to the rated speed of 750 r/min

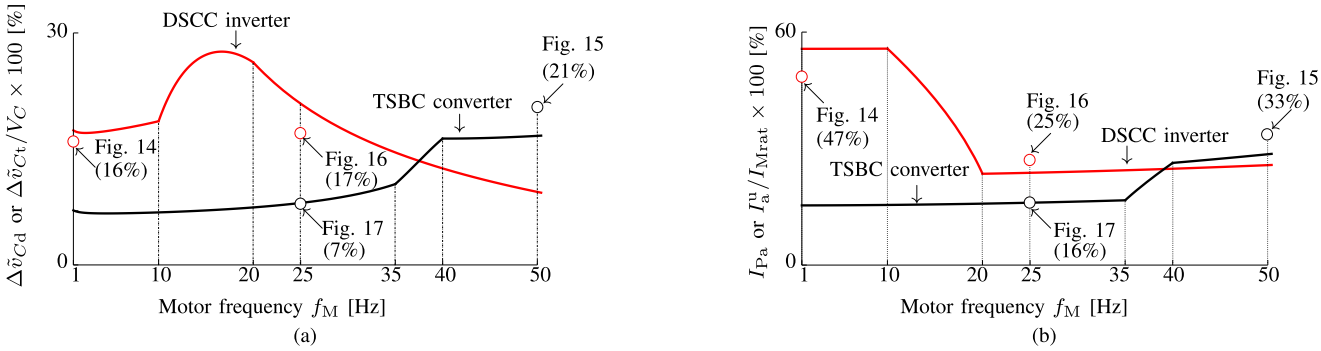

Fig. 18. Numerical and experimental comparisons between the DSCC inverter and the TSBC converter. (a) Normalized capacitor-voltage fluctuation in peak-to-peak. (b) Normalized arm or cluster current in rms.

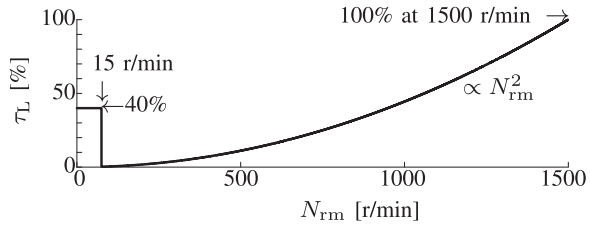

Fig. 19. Hypothetical load torque-to-speed profile used for the experiment shown in Fig. 20.

TABLE V
PARAMETERS OF THE 38-HZ INDUCTION MOTOR

Rated output power		15 kW
Rated frequency		38 Hz
Rated line-to-line rms voltage	V_M	320 V
Rated rotating speed		750 r/min
Rated stator rms current	I_{Mrat}	41 A
Pole number	$2p$	6
Moment of inertia	J_M	0.3 kg·m^2

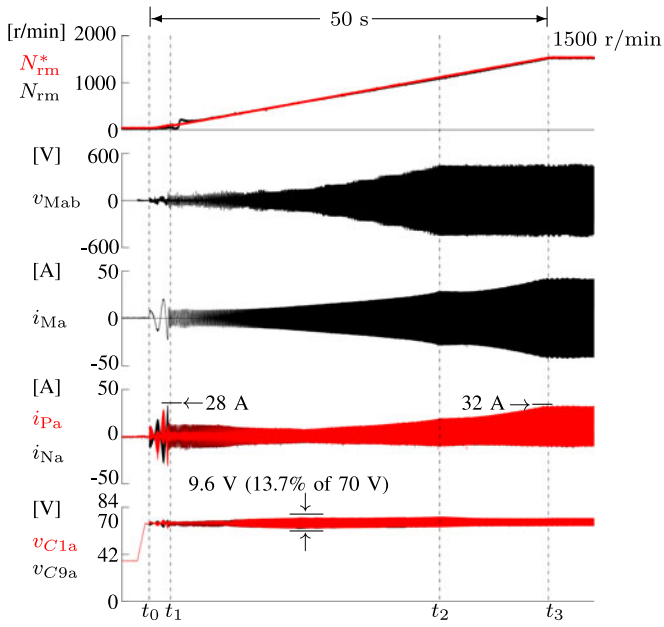

Fig. 20. Experimental start-up waveform of the DSCC-driven 50-Hz, 4-pole induction motor loaded with the quadratic torque-to-speed profile sh- own in Fig. 19.

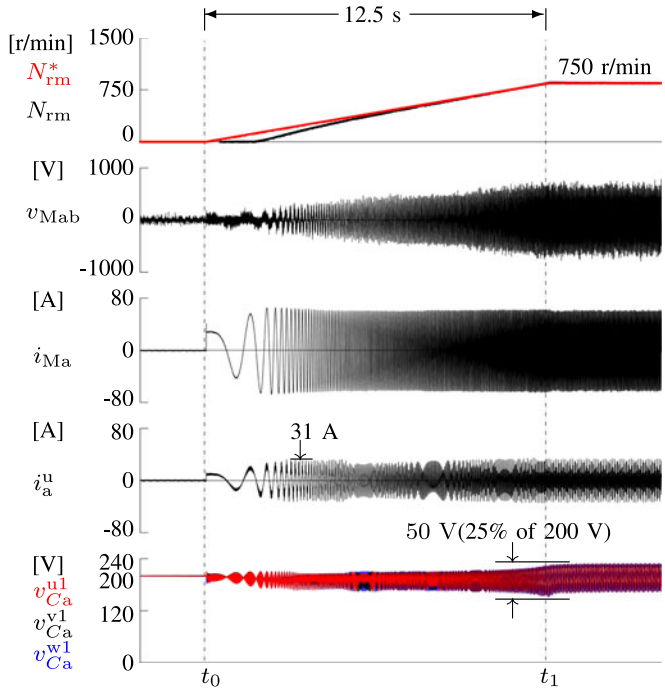

Fig. 21. Experimental start-up performance of the TSBC-driven 38-Hz, 6-poles induction motor loaded at the rated torque.

with a ramp rate of 60 r/min/s. Although the rated motor torque is twice as high as that of the 50-Hz motor in Fig. 20, both cluster current and voltage fluctuation are acceptable values. The cluster peak current is 31 A, whereas the peak-to-peak capacitor-voltage fluctuation is 68 V, which is 34 % on a 200-V base.

C. Steady-State Performance of the DSCC-Driven 50-Hz Motor Operated at 50 Hz and 100% Torque

Fig. 22 shows the steady-state waveforms of the DSCC-driven 50-Hz induction motor at the rated motor frequency of 50 Hz and $\tau_M = 100\%$. Two kinds of voltage ripples are included in the dc-link voltage v_{dc}:

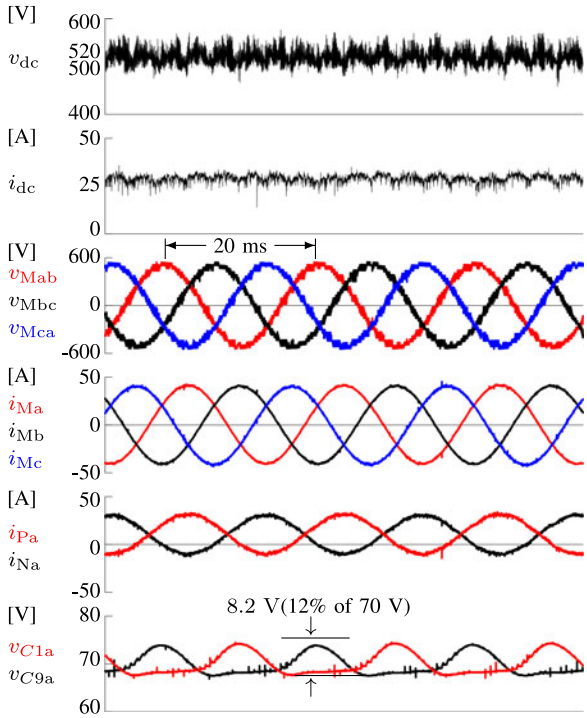

Fig. 22. Experimental steady-state performance of the DSCC-driven 50- Hz, 4-pole induction motor loaded at the rated torque at $N^*_{\rm rm} = 1500$ r/min.

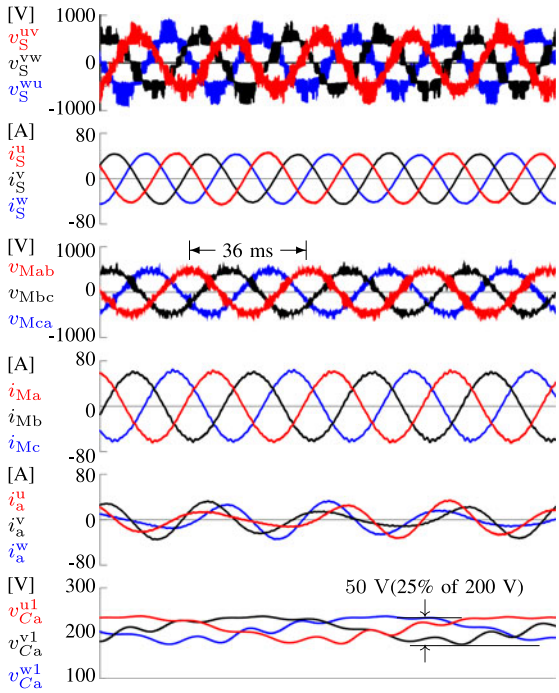

Fig. 23. Experimental steady-state performance of the TSBC-driven 38-Hz, 6-pole induction motor loaded at the rated torque at $N^*_{\rm rm} = 750$ r/min.

1) One came from the 12-pulse diode rectifier: It was absorbed by the capacitor of each chopper cells.
2) The other came from the DSCC inverter: It had no effect on the motor-drive performance because its voltage step are as small as a single capacitor voltage.

Installing a simple filter on the dc link would eliminate the voltage ripples from the DSCC inverter [38]. Each of three-phase line-to-line voltages, $v_{\rm Mab}$, $v_{\rm Mbc}$, and $v_{\rm Mca}$, has a 27-level voltage waveform. The multilevel line-to-line voltages result in producing three-phase sinusoidal motor currents $i_{\rm Ma}$, $i_{\rm Mb}$, and $i_{\rm Mc}$. The arm current waveforms $i_{\rm Pa}$ and $i_{\rm Na}$ include dc, 50-Hz, and switching-ripple components, where the switching-ripple component is negligibly small. Capacitor voltages $v_{C1\rm a}$ and $v_{C9\rm a}$ are balanced perfectly with its peak-to-peak value of 6.3 V (9.6%). The experimental results shown in Figs. 20 and 22 suggest that it would be possible to reduce the unit capacitance constant [37] of the DSCC inverter from 52 to 24 ms if a peak-to-peak capacitor voltage fluctuation of 25% were acceptable.

D. Steady-State Performance of the TSBC-Driven 38-Hz Motor Operated at 38 Hz and 100% Torque

Fig. 23 shows those of the TSBC-driven 38-Hz induction motor at the rated motor frequency of 38 Hz and $\tau_{\rm M} = 100\%$. Each of three-phase line-to-line voltages at the supply side, $v_{\rm a}^{\rm uv}$, $v_{\rm a}^{\rm vw}$, and $v_{\rm a}^{\rm wu}$, has a nine-level voltage waveform. This made $i_{\rm S}^{\rm u}$, $i_{\rm S}^{\rm v}$, and $i_{\rm S}^{\rm w}$ sinusoidal at unity power factor. Moreover, three-phase line-to-line voltages at the motor side $v_{\rm Mab}$, $v_{\rm Mbc}$, and $v_{\rm Mca}$ and currents $i_{\rm Ma}$, $i_{\rm Mb}$, and $i_{\rm Mc}$ were controlled to produce the rated torque with a negligible amount of torque ripple. Cluster currents $i_{\rm a}^{\rm u}$, $i_{\rm b}^{\rm u}$, and $i_{\rm c}^{\rm u}$ were controlled to sinusoidal waveforms with small current ripples. A peak-to-peak capacitor voltage fluctuation in $v_{C\rm a}^{\rm u1}$, $v_{C\rm a}^{\rm v1}$, and $v_{C\rm a}^{\rm w1}$ is only 50 V (25%).

VI. Conclusion

This paper has made numerical and experimental comparisons in induction-motor drive between a DSCC inverter and a TSBC converter. Emphasis has been laid on a capacitor-voltage fluctuation in peak-to-peak and an arm or cluster current in rms. The numerical and experimental comparisons using the common 380-V, 15-kW, 50-Hz induction motor have revealed that the DSCC inverter suffers from capacitor-voltage fluctuations in a low-frequency range including the startup, whereas the TSBC converter suffers from it as the motor frequency is close, and equal to, the supply frequency, even when any appropriate mitigating control is used. Experimental results obtained from two different motors and torque-to-speed profiles have prescribed motor-drive applications suitable to the DSCC inverter and the TSBC converter. Finally, this paper has led to the following conclusions:

1) the DSCC inverter is more suitable for high-speed motor drive loaded with a quadratic-torque-to-speed profile such as fans, blowers, pumps, and centrifugal compressors;
2) the TSBC converter is more suitable for low-speed motor drive at the rated torque such as mills, kilns, conveyors, and extruders.

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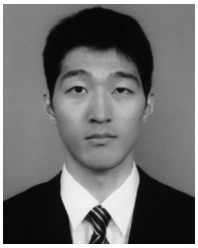

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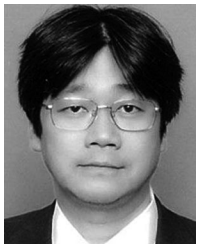

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