A Bidirectional Battery Charger With Modular Integrated Charge Equalization Circuit

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***Abstract*—High-voltage battery pack and charger structure are the main concerns of the electric vehicle (EV) developments. To achieve required voltage and power in propulsion systems, cascading battery stacks is essential. However, due to small discrepancies between different cells, charge imbalance occurs. Charge imbalance reduces battery cells life cycle, accessible energy, and system performance. Hence, charge equalization among battery stacks is necessary. Furthermore, EVs should have some essential requirements to provide desired contributions in future networks. Therefore, bidirectional power flow and reactive power control are other important capabilities of the battery charger system. In this paper, a bidirectional structure with two operation modes for a modular battery stack is developed. The developed structure has active and reactive control capabilities during grid to vehicle and vehicle to grid operations. To improve the battery system performance, a modular charge equalizer circuit (CEC) for both operation modes is developed. The modular configuration of the battery stack improves the system reliability and flexibility. Moreover, the overall system performance for the CEC and converter is improved by utilizing the integrated control strategy. Performance of the proposed structure is evaluated using simulations and laboratory experiments. The results confirm the capability of the proposed structure.**

***Index Terms*—Battery charger, bidirectional, charge equalization (CE), electric vehicle (EV), reactive power control.**

NOMENCLATURE

V_s, i_s	AC-side voltage and current signals.
Δi_s	AC-side current ripple.
L_1, C_1	AC-side low-pass filter components.
L_2	Inductor of the H-Bridge ac–dc converter.
C_2	DC-link capacitor.
L_3, C_3	Battery-side low-pass filter components.
B_i	*i*th Battery cell.
$\mathrm{S_{ij}}$	IGBT switches of the ac–dc or dc–dc converter.
hip, hin	Battery cell's high-side and low-side switches.
n	Number of battery cells in a battery system.
V_{dc} *or* V_c	DC-link voltage.
ΔV_{dc}	DC-link voltage ripple.
V_{cref}	DC-link reference voltage.
V_{batt}	Battery pack voltage.
I_{batt}	Battery current.
ΔI_{batt}	Battery current ripple.
r_d, V_{fd}	Diode internal resistance and voltage drop.
r_s, V_{sw}	Switch conduction resistance and voltage drop.
r_L	Inductors internal resistance.
r_{ESR}	Batteries equivalent series resistance.
i_α, i_β	Sine and cosine components of the PLL.
i_p, i_q, i_{ref}	Active and reactive components of reference current.
D	Switches duty cycle.
P_{ref}, Q_{ref}	Reference active and reactive power components.
f_s, f_{source}	Switching frequency and ac source frequency.

Manuscript received December 18, 2015; revised March 28, 2016; accepted May 2, 2016. Date of publication May 18, 2016; date of current version December 9, 2016. Recommended for publication by Associate Editor M. Ferdowsi.

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Digital Object Identifier 10.1109/TPEL.2016.2569541

I. INTRODUCTION

ALTHOUGH there has been a growing interest in electric vehicles (EVs) in the last decade, there are some reasons which prevent the wide acceptance of the EVs [1], [2]. Without a doubt, the main obstacles in EV advancement are high-voltage battery system and charger structure [3], [4]. There are other concerns regarding EVs' development such as their impact on network power quality as well as increased and unplanned power consumption [5]–[7].

Due to increasing penetration of EVs and their aptness for smart grid integration, a high-power and high-efficiency charger with low total harmonic distortion (THD) is essential. Furthermore, to accommodate adequate EV-grid interaction, especially for EVs integration in smart grids, reactive power control and vehicle to grid (V2G) capabilities are required [4]. In this content, the first step is to develop a suitable charging structure with control strategy that fulfills all the mentioned capabilities in addition to other requirements for the adequate management of the battery system. The second step is to focus on battery system itself [3]. A suitable charge/discharge method can lengthen battery pack life cycle, but a charger cannot be as effective without considering the EV battery pack peculiarities. The required voltage and power level in an EV is relatively high, whereas the rating of a battery cell is insufficient [8]. In order to achieve the necessary current and voltage ratings, a number of battery cells are connected in parallel and in series, respectively. Due to the inherent charge balancing feature in a parallel connection, no charge imbalance occurs between paralleled battery cells or modules [9]. While because of some small differences such as manufacturing tolerances, environment condition, aging, etc., even among identical battery cells, there are small variations in capacity and/or discharge profile. Furthermore, these discrepancies increase with battery aging. The battery cells mismatch would result in different charge/discharge speed and after

TABLE I
SUMMARIZED COMPARISON OF CHARGER AND CEC

Type	reference	V2G capability	Reactive control	Isolation	T2A mode	CE capability	CEC reliability	CEC flexibility	Switch number in CEC	Overall cost	Control complexity	Efficiency	Battery current ripple
CECs only	[10]	–	–	–	–	√	Medium	Medium	$2n+2$	Medium	Medium	Good	High
	[22]	–	–	–	–	√	Medium	Good	$2n+4$	High	High	Medium	Low
	[24]	–	–	-	–	√	Good	Good	$2n$	High	High	Good	Low
	[26]	–	–	–	–	√	Medium	Medium	$n+4$	High	Simple	Good	High
	[35]	–	–	–	–	√	Very good	Good	$3n$ or $4n$	Very high	Medium	Medium	Medium
	[36]	–	–	–	–	√	Medium	Low	$2n$	Very high	Medium	Good	High
	[37]	–	–	–	–	√	Medium	Low	n	High	Simple	Medium	Medium
Charger only	[19]	**X**	√	√	**X**	–	–	–	–	Medium	Medium	Medium	Low
	[29]	√	√	**X**	√	–	–	–	–	Medium	High	Medium	Very low
	[30]	**X**	√	**X**	**X**	–	–	–	–	Medium	High	Medium	Low
	[31]	√	√	√	√	–	–	–	–	High	High	High	Medium
	[21]	**X**	**X**	√	**X**	–	–	–	–	Medium	High	High	High
	[28]	**X**	√	**X**	**X**	–	–	–	–	Medium	High	Medium	Medium
	[38]	**X**	√	√	**X**	–	–	–	–	Medium	Medium	Medium	Low
Charger /CEC	[33]	√	**X**	**X**	**X**	√	Very good	Good	$2n+4$	Medium	Medium	Medium	High
	Proposed structure	√	√	**X**	**X**	√	Good	Very high	$2n$	Medium	High	Medium	Very low

"–" denotes irrelevant features in each type; "**X**" denotes relevant shortcomings; "√" denotes relevant capabilities; n is number of required switches in each topology.

number of successive cycles, charge imbalance occurs. This would limit the battery stack efficiency and increases battery degradation. Therefore, for longer life time and proficiency, charge equalization (CE) is necessary [10].

The CE is a procedure by which energy imbalance between different cell/modules in a battery pack is balanced via dissipation or redistribution [9], [11]. The CE methods can be classified in two major categories: 1) passive CE methods; and 2) active CE methods. In the passive methods, the excessive charge is lost in a passive element such as resistor [12]. Although these methods usually have simple structure and control strategy, the efficiency and CE speed are much lower than the active equalization methods. Therefore, they are rarely used in new battery management systems. In the active CE methods, energy is transferred from the cell/module with higher energy to another cell/module with lower energy. In these methods, efficiency and speed as well as control system complexity are increased. Almost all the recently proposed methods for the CE rely on active techniques [12], [13].

Generally, there are two types of energy transfer for any battery charger: 1) conductive method and 2) inductive method. Conductive charging is a well-established method in high-power battery chargers, while inductive chargers are yet to be fully developed for such applications. Therefore, inductive chargers are not considered in this paper. The main obstacle is lower efficiency of the inductive chargers. Nevertheless, since inductive charging is more convenient for the driver and also considering the simpler hardware in the charging stations, a rapid growth in inductive charging market is expected in the future [14].

There are many converter topologies with different capabilities, which can be used for the EV battery charger structures [15]–[21], but they usually consider battery pack as one large battery stack. There are also a number of CE topologies in the literature [10], [22]–[27], in which independent circuit and control strategy have been proposed to realize CE in a battery pack. However, interaction between charger and charge equalizer circuit (CEC) is usually neglected. In this section, to develop a suitable charger topology, some state-of-the-art chargers and CEC topologies are extensively studied. Several main criteria such as active and reactive controls, ability for V2G operation, flexibility and reliability, integrated CEC, cost, and semiconductor device count are taken into account to assess the topologies in this paper. Table I summarizes the comparison results. In general, the EVs are charged at home during the night, so only the single-phase on-board chargers (level 1 charger according to SAE EV ac charging power levels) are considered [4].

In [19], design procedure for an isolated charger with interleaved power factor (PF) correction has been proposed. Interleaved topology improves dc-link voltage fluctuation and input current ripple, while zero voltage switching (ZVS) ability increases overall efficiency [20]. In this topology, there is not any CE and effective control on the battery pack charging current. Another important shortcoming is that this topology is unidirectional.

In [28], a single-phase unidirectional battery charger based on an H-bridge boost rectifier is proposed. In order to achieve unity PF, a novel phase shift control is implemented. Moreover, the phase shift control algorithm is combined with an active damping control to reduce ac current distortions. However, lack of CE capability and the unidirectional structure are some of its shortcomings.

In [29], an on-board single-phase EV charger with integrated traction to auxiliary (T2A) mode is proposed. The high-voltage battery pack is charged with constant current and controlled PF. The control strategy is rather simple and reliable. The integrated T2A mode is another advantage of this structure. But high switching losses, nonisolated charger, and more importantly the requirement of an independent CEC are some of its

shortcomings. A similar structure is used in [30], in which a unified control strategy for grid to vehicle (G2V) operation is developed. The unified control improves the charger performance in the smart grids, but in the control strategy, V2G mode is not considered. Also, in the control strategy, constant voltage charging or charge imbalance problems are not taken into account in the battery packs. The structure proposed in [31] is a developed version of the last two structures, where ZVS is utilized for enhancing charger efficiency. Galvanic isolation and T2A operation are other advantages in [31]. In this structure, CE is not considered and battery current ripple is considerable. Also, in comparison with two last mentioned structures, the number of the utilized semiconductors is rather high.

In [21], a diode-clamped series resonant converter with resonant valley compensator is proposed. Due to the zero current switching control, switching loss is decreased. However, increased elements and converter complex control are the main issues for this topology. In [32], a resonant converter with ZVS capability and simpler structure with rather complex control has been presented. Meanwhile, CE is not considered in these structures.

A hybrid multilevel converter topology for EV applications is proposed in [33]. The proposed converter achieves multilevel voltage via bypassing and/or connecting battery cells in series. Because of the modular design of the converter, the reliability is increased and also CE capability during V2G and G2V modes is another advantage of this structure. Although this converter could be utilized as battery charger, due to the high ripple of charging current, battery cells life time is decreased. Furthermore, efficiency reduces due to increased switching frequency. Another problem for this application is considerable number of switches in a three-phase structure. In this topology, there are $2n + 4$ switches for single-phase topology and $6n + 12$ switches in three-phase topology.

A dc/dc converter for CE is proposed in [10]. The CE is realized using buck–boost operation. In this topology, $2n + 2$ unidirectional switches are needed. This topology has the capability of CE in charging, discharging, and idle modes, but it does not have ability for bypassing the possible damaged battery. Furthermore, the required independent inductance increases the volume, weight, and overall cost of the complete charger structure.

In [26], an active charge equalizer for cascaded lithium battery cells using a supercapacitor (SC) as an intermediate device is proposed. The system initially stores charge drawn from a cell in the SC and then the charge is transferred to another cell with lower state of charge (SOC). The proposed topology requires at least $2n + 2$ switches. Utilization of SC has improved conduction and switching losses. Since battery module voltage is relatively larger than the rated voltage of SC cells, the overall cost is increased.

In [34], a procedure is proposed to select batteries with similar electrochemical characteristics. This procedure has two screening process: 1) capacity screening that matches the open-circuit voltage (OCV) to achieve balance SOCs; and 2) resistance screening that facilitate selection of batteries with similar parameters in the battery equivalent circuit model. However, as the batteries age and degrade, their chemical characteristics can vary significantly.

A battery system with a modular design is reported in [35], where each battery cell and a small bidirectional converter are integrated to form a module. These modules can be easily connected in series to form a battery pack. This technique can realize CE and reduces the voltage stresses of the power electronic devices. The modular design improves system reliability and controllability, while the overall costs are increased. Furthermore, in this structure, the ac–dc interface between the grid and battery pack is not considered.

Another challenge of the battery systems is the time-consuming process of CE. To increase equalization speed, a multilayer CE control is proposed in [23]. In [23], the need to balance the charge one by one between the battery cells is satisfied using parallel architectures. The main problem is that an independent CEC is necessary for each layer. Also, in [27], a similar approach to improve CE flexibility has been proposed.

In this paper, a three-stage bidirectional charger/CEC is developed. In the proposed topology, the number of battery modules is connected in series to realize CE procedure. The proposed control algorithm for charge balancing with constant current mode is discussed. The main contributions of this paper are: 1) development of a bidirectional charger structure with CE capability; and 2) introducing an integrated control strategy to improve overall system performance and flexibility. The charger structure is developed to enhance battery life cycle and the control strategy is designed to provide desirable charger-CEC interaction during V2G, G2V.

Some of the main features of the proposed structure are described as follows:

1) it has active and reactive control in G2V and V2G operation;
2) it offers CE capability during V2G and G2V operation;
3) it increases battery life time with low ripple charge and discharge battery current;
4) control strategy of the CEC is fully integrated into charger control algorithm;
5) due to modular structure reliability and flexibility is increased.

The proposed structure and control are simulated in MATLAB/Simulink software and a low-scale prototype is implemented at the lab. The performance of the system is evaluated in different conditions by some simulations and experiments. The results verify the performance of the developed topology and control algorithm.

II. Charger-CEC Topology and Operation

Fig. 1 represents the developed bidirectional converter with the integrated CEC topology for a three module battery system. However, the proposed modular CEC could be developed for any number of battery modules to accommodate desired ratings, straightforwardly. The bidirectional converter consists of two power conversion stages. The first stage is an ac–dc H-bridge converter followed by a large dc link. The second stage of power conversion is a dc–dc bidirectional buck/boost converter.

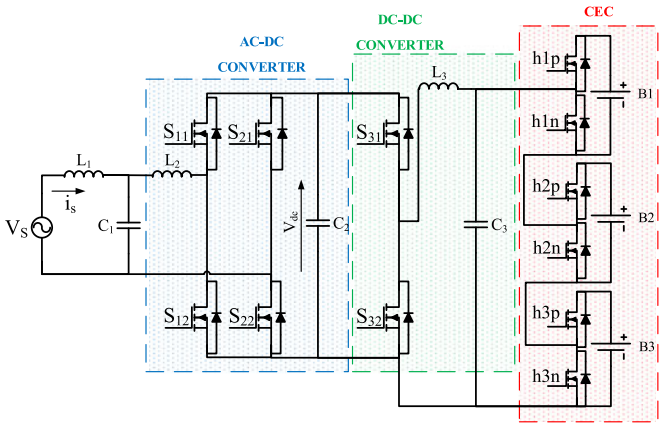

Fig. 1. Bidirectional charger/CEC topology.

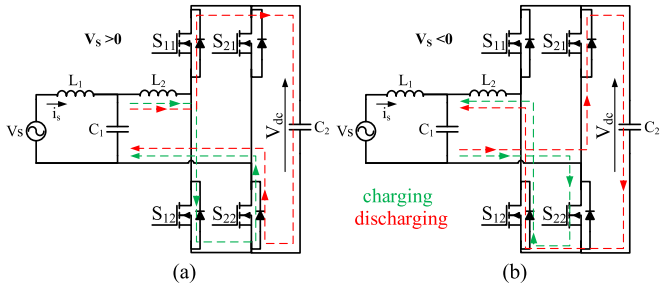

Fig. 2. Current path during G2V operation: (a) $V_s > 0$; (b) $V_s < 0$.

Since most on-board chargers have power levels of one or two [4], they need to be compatible with residential or private installations, hence a single-phase structure is considered. The structure shown in Fig. 1 has two modes: 1) V2G and 2) G2V. Operation of the structure during each mode is explained in the following section.

A. G2V Mode

In this mode, ac–dc converter operates as a boost rectifier to provide the needed dc voltage and the dc–dc converter is a current-controlled step-down converter to control the battery charging current.

1) H-Bridge Converter Operation and Analysis: In the G2V mode, H-bridge works as a boost rectifier with sinusoidal input current and controlled reactive power. Compared to a full-bridge diode rectifier, it has lower harmonic distortion and improved PF. To reduce switching losses, the switching pattern used in [39] is utilized. It has the advantage of only one switching in each cycle. Depending on the input voltage sign, there are two conditions.

1) $V_s > 0$: First, S_{12} is switched ON and L_2 is charged via S_{12} switch and S_{22} diode. Then, the S_{12} is switched OFF and L_2 is discharged via S_{11} diode, C_2, and S_{22} diode path. In Fig. 2, current path during L_2 charging and discharging is shown. There is another scenario where S_{11} is used to control charging and discharging of L_2. In [39], more detailed analysis of this mode has been presented.
2) $V_s < 0$: For negative input voltages, the procedure is similar. First the S_{22} switch is turned ON and L_2 is charged via S_{22} switch and S_{12} diode path. When the S_{22} is turned OFF, the L_2 discharges via S_{21} diode and S_{12} diode. Fig. 2(b) shows the current path of L_2 when $V_s < 0$.

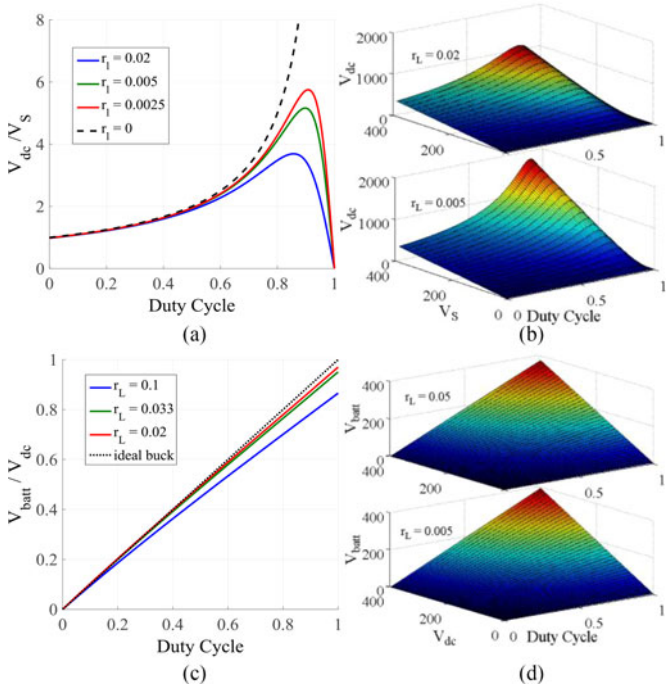

Fig. 3. H-bridge converter: (a) $V_{\rm dc}/V_{\rm S}$ ratio; (b) variation of $V_{\rm dc}$ versus $V_{\rm S}$ and D; dc–dc converter: (c) $V_{\rm batt}/V_{\rm dc}$ ratio; (d) variation of $V_{\rm batt}$ versus $V_{\rm dc}$ and D.

If D is the duty cycle of the conducting switch, then considering ideal components, output voltage can be calculated using (1). According to (1), for $D = 1$, the dc-link voltage should be $V_{\rm dc} = \infty$, but due to nonideal elements, this is not realized. Equation (2) represents $V_{\rm dc}$ as a function of D, considering inductor, switch, and diode resistances. For driving (2), each diode or switch is modeled by a voltage source in series with an internal resistance

$$\frac{V_{\rm dc}}{V_S} = \frac{1}{1-D} \tag{1}$$

$$V_{\rm dc} = \frac{V_S - 2(1-D)V_{\rm fd} + D(V_{\rm sw} + V_{\rm fd})}{1 - D + \dfrac{r_L}{1-D} + (1-D)2r_d + \dfrac{D^2(r_s + r_d)}{1-D}} \tag{2}$$

where r_L, r_d, and r_s are per unit values of inductor, diode, and switch resistances, respectively, which are based on $R_{\rm base} = \frac{V_{\rm dc,rated}}{I_{\rm dc,rated}}$. Here, $R_{\rm base}$ is considered to be 100 Ω. Moreover, V_S is the instantaneous magnitude of the ac voltage. Due to high switching frequency, the input and output voltages of the converter can be considered to be constant during a switching cycle.

In Fig. 3(a) and (b), $V_{\rm dc}/V_{\rm S}$ ratio versus r_L and D using (1) and (2) are illustrated. Here, the value of r_s and r_d are considered equal to 0.2 r_L.

2) DC–DC Converter: During G2V mode, S_{32} switch is always OFF and the dc–dc converter operates as a buck converter with pulse width modulation (PWM) of S_{31} to control battery

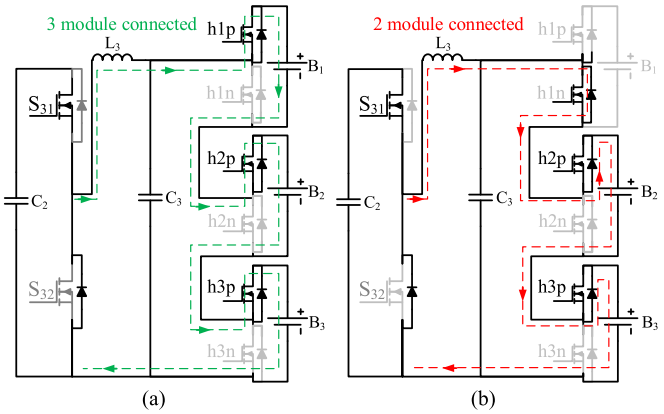

Fig. 4. Current path during the G2V mode: (a) three modules connected; (b) two modules connected.

charging current. Again, considering nonideal components, V_{batt} as a function of *D,* considering inductor, switch, and diode resistances is as follows:

$$V_{\text{batt}} = \frac{DV_{\text{dc}} - DV_{\text{sw}} + (1-D)\,V_{\text{fd}}}{1 + D^2 r_s + (1-D)^2 r_d + r_l}. \tag{3}$$

Fig. 3(c) and (d) shows the ideal and nonideal output curves of the buck converter. Similarly, the input and output voltages of the dc–dc converter are considered to be constant during a switching cycle. It can be observed that here the problem of voltage drop is not as acute as the boost converter.

3) CEC Operation and Analysis: This circuit provides CE during battery charging. Charging starts with one module and other modules are switch in, one by one. To connect a module to the stack, *hip* is switched ON and *hin* is switched OFF, where *i* is the module number. For example, in a three-module system, current path during charging is illustrated in Fig. 4, where all three modules are connected at first and then one module is bypassed.

The modular structure of the battery pack provides possibility of bypassing a damaged module without interruption of any main function. This ability improves the reliability of the overall system. In case of a damaged module, its low-side switch (*hin*) is permanently turned ON, while the high-side switch is OFF. Therefore, the faulty module can be easily replaced at a suitable time.

B. V2G Mode

In this mode, the charger-battery system returns the stored energy back to the grid. The amounts of the needed active and reactive power are determined by the smart grid controller. The CEC determines the battery stack configuration considering CE, the dc–dc converter boosts the voltage to obtain required voltage level at the dc link, and the H-bridge converter inverts the voltage to ac.

1) CEC Operation and Analysis: Here, based on the needed active and reactive power, the CEC determines the minimum number of the required battery packs to obtain the minimum voltage limit. Then discharging starts with the minimum number of batteries with the highest SOC. Each time the lowest SOC

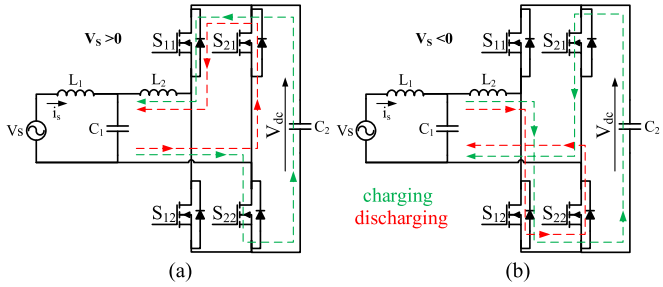

Fig. 5. Current path of H-bridge in V2G mode: (a) $V_s > 0$; (b) $V_S < 0$.

in the connected batteries reaches a battery SOC that is currently bypassed, the bypassed battery is switched into the stack and this procedure continues until all the batteries are switched in. If there is no limit to the number of connected batteries, discharging starts with one battery that has the highest SOC. Therefore, complete CE is possible. If current directions in Fig. 4 are reversed, the current paths in V2G mode with three and two connected modules can be determined straightforwardly.

2) DC–DC Converter Operation and Analysis: In V2G mode, the dc–dc converter operates as a single-switch boost converter. Here, the S_{31} is always OFF and the S_{32} with the antiparallel diode of the S_{31} forms a boost converter. Battery discharge current and dc-link voltage are regulated with PWM switching of the S_{32}. Again, considering nonideal switches, the V_{dc} as a function of *D,* considering inductor, switch, and diode resistances is calculated using (4). Its output curve is similar to Fig. 3

$$V_{\text{dc}} = \frac{V_{\text{batt}} - (1-D)V_{\text{fd}} - DV_{\text{sw}}}{1 - D + \dfrac{r_l}{1-D} + (1-D)r_d + \dfrac{D^2}{1-D}r_s}. \tag{4}$$

3) AC–DC Converter Operation and Analysis: Here, the ac–dc converter operates as a single-phase full-bridge inverter. The switching is controlled in a way that the output current is sinusoidal and output PF is regulated. Similar to *G2V* mode, the single switching pattern proposed in [39] is utilized. In Fig. 5, current paths for $V_s > 0$ and $V_s < 0$ are illustrated. The V_S as a function of *D,* considering nonideal full-bridge buck is

$$V_S = \frac{DV_{\text{dc}} - 2DV_{\text{sw}} - (1-D)\,(V_{\text{fd}} + V_{\text{sw}})}{1 + r_l + 2D^2 r_s + (1-D)^2 (r_s + r_d)}. \tag{5}$$

III. System Control Algorithm

In this section, system control algorithms are presented. For better understanding, control system is divided into *G2V* and *V2G* modes.

A. G2V Mode

There are some requirements in G2V mode that need to be satisfied. Sinusoidal input current with low harmonic distortion (less than 5% [30]) is the first requirement. In order to have suitable control over the charging current of the battery stack, a low ripple dc-link voltage is essential. In [40], an optimized

charge strategy based on the battery's temperature is proposed, that has lower energy losses. Since optimization of energy loss is not a goal in this paper, in order to improve battery life cycle, constant-current constant-voltage (CC-CV) charging strategy is chosen and temperature variations are not considered. For safety issues, a temperature sensor should be used in order to ensure battery operation within acceptable range. If temperature exceeds the permissible limit, the charger is disabled [41]. In the following, control algorithms for each stage of the charger are presented.

1) AC–DC H-Bridge Converter Control: To obtain a low ripple dc output and low harmonic input current, dual-loop PI controller is considered. The first loop calculates the required input active power and a reference sinusoidal current signal to achieve the desired output voltage. In the second loop, the difference between measured and reference currents are calculated and the switching signals are generated.

A phased-locked loop (PLL) drives the in-phase and quadrature signals of the input voltage. In Fig. 6(a), block diagram of a single-phase PLL is illustrated. When the PLL is synchronized, i_α and i_β are the direct and quadrature components of the input ac voltage with unity amplitude. They are used to synthesize the active and reactive components of the reference current.

As shown in Fig. 6(b), first the difference between the measured and desired dc voltage is passed through a PI controller to calculate the needed reference power. Next, reference power is divided by the rms voltage to calculate rms value of the active component of the current signal. To obtain the active component of current signal, it is multiplied to the in-phase component of the PLL with amplitude equal to $\sqrt{2}$. Reactive power reference is considered an input value set by the grid, but the same procedure should be followed to obtain the reactive component of the reference current. If a specific value is not provided by the smart grid controller, $Q_{\rm ref}$ is considered to be zero. Since the converter has power limits, a limiter is used after the PI controller.

Using the reference current and the measured current, the error signal is calculated. The error is fed to a second *PI* controller. The output of the controller is compared to a triangle waveform to obtain the PWM control signals. The control diagram of the reduced switching controller for V2G and G2V operation is shown in Fig. 6(c), in which i_p and i_q are active and reactive components of reference current signal. In G2V, $P_{\rm ref}$ is positive, hence the *mode* value is 1 and the upper *AND* gates for each switch may have nonzero outputs. In V2G, $P_{\rm ref}$ is negative and *mode* value is zero, hence the lower *AND* gates are generating the switching pulses.

2) DC–DC Converter Control: The dc-link voltage is higher than the battery pack voltage; hence the dc–dc converter is in buck operation. To improve battery life time, CC-CV charging strategy is chosen. It means that battery is charged with constant current until its voltage reaches its rated value (depending on the battery type), then battery is charged in CV mode. The desired output voltage of the dc-dc converter during CV charging is selected based on the nominal voltage of the battery modules. Usually it is a little above the open-circuit terminal voltage of the battery pack, when it is fully charged. As shown in Fig. 6(d), the dc-dc converter uses the voltage/current feedback to adjust

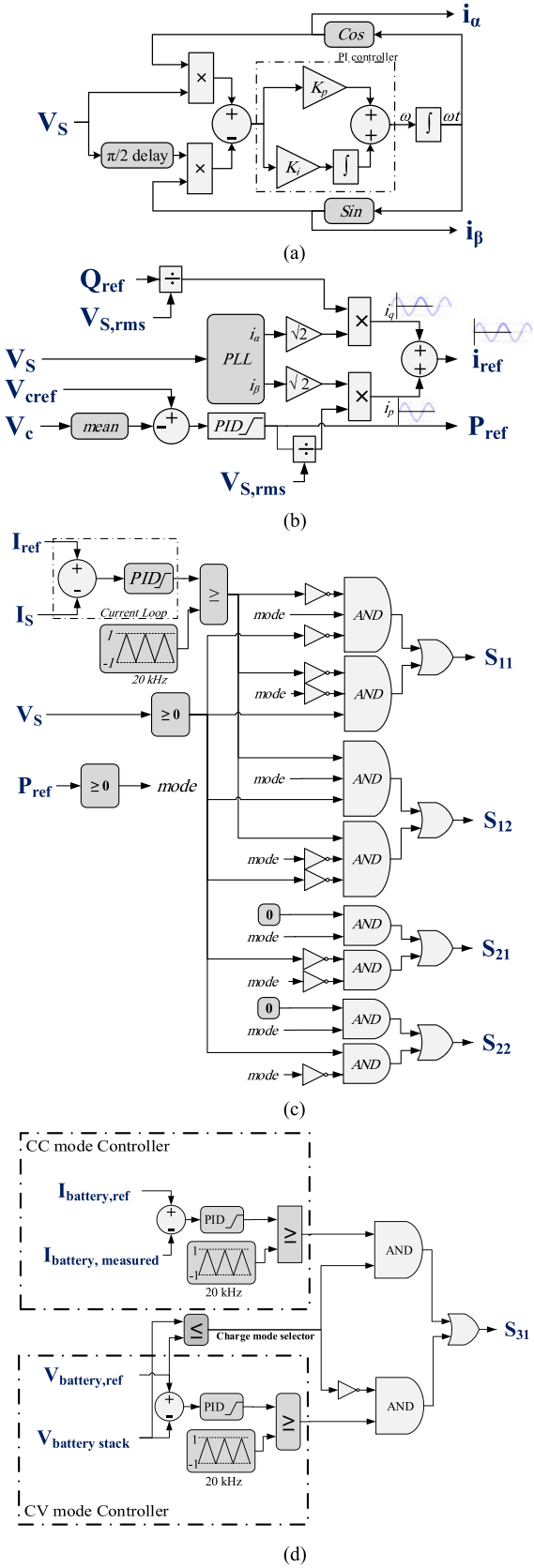

Fig. 6. AC–DC converter controller: (a) single-phase PLL; (b) reference current control diagram in G2V mode; (c) current loop and switching control diagram; (d) control block diagram of the buck converter.

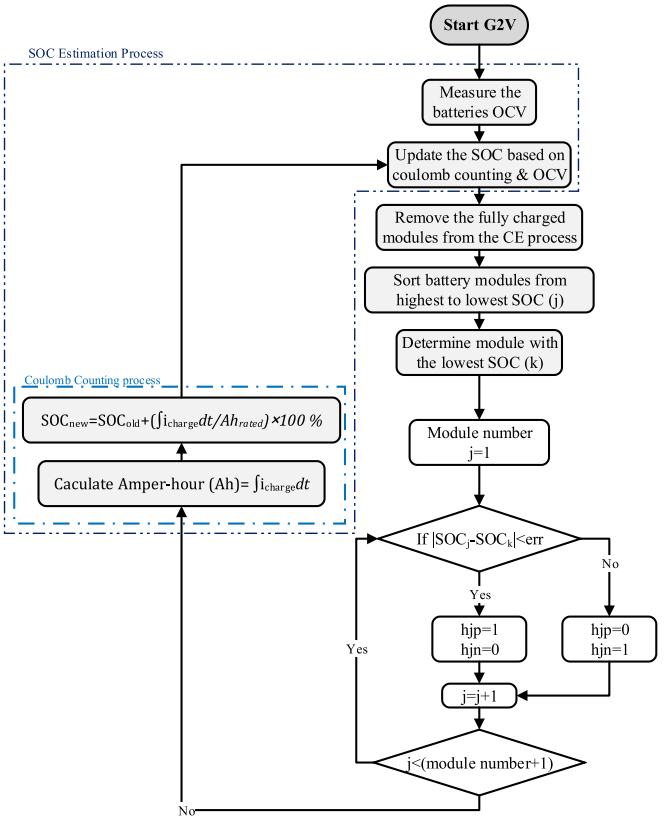

Fig. 7. CEC control algorithm to obtain the battery pack configuration.

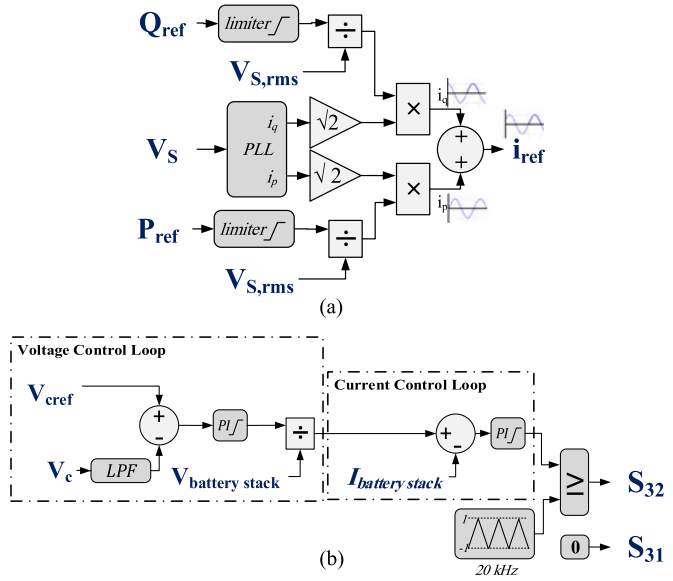

Fig. 8. V2G mode: (a) schematic of the reference current control in the V2G mode; (b) schematic of the step-up converter control during V2G mode.

the duty cycle of the S_{31} switch. The PWM frequency is 20 kHz. The saturation block is used to limit the maximum and minimum duty cycle of the PWM controller.

3) CEC Control: The main function of the CEC controller is to reconfigure the battery stack based on the modules' SOC in order to realize CE. In Fig. 7, flow chart of the CEC controller is shown.

The SOC estimation method is a combined method of OCV and Coulomb Counting (CC) method. Hence, first the OCV of the batteries are measured to update the SOC estimation based on CC method. Then the battery module with the lowest SOC is determined (SOC_k). To obtain the gate signals of the *hip* and *hin* switches, the SOC of each battery is compared to SOC_k, as shown in Fig. 7. If the two SOCs are close to each other, the battery module is switched in. Next, the increased Ampere-hour in the last cycle is calculated to update the SOC estimation. This procedure continues until all the battery modules are charged. When a module is completely charged, it is bypassed and CE continues for the rest of battery modules. CE is finalized via bypassing the fully charged modules.

B. V2G Mode

In this mode, ac-dc converter acts as a full-bridge inverter with controlled output current and the dc-dc converter is a step-up converter to increase battery voltage levels to the dc-link reference voltage. Also, CEC reconfigures the battery pack structure to obtain the required voltage levels and realize CE.

1) AC–DC H-Bridge Converter Controller: Control diagram of this mode is shown in Fig. 8(a). The ac-dc converter is in inverter-buck operation with controlled output current. In this mode, the required active and reactive powers are considered as input variables, which are determined by the smart grid controller. Because of charger power limitations, the input powers are limited using the relevant limiters. Since power is injected back to the grid, power sign is negative in the block diagram and hence the calculated reference current has 180-degree phase difference with the grid voltage. The current loop and switching control diagram is the same as Fig. 6(c), but since the $P_{\rm ref}$ is negative, the converter is in inverter mode. Again switching frequency in this mode is 20 kHz. Control diagram of the PLL and switching pattern is similar to Fig. 6(a) and (b), respectively.

2) DC–DC Converter Controller: The output voltage of the boost converter is controlled using PI controlled PWM switching. To improve the battery life time, batteries are discharged using constant current. As seen in Fig. 3(a), a nonideal step-up topology has limited capability in boosting battery pack voltage. Based on (4), considering typical values for internal resistance of the inductor, switches, and diodes, maximum voltage ratio 3 is considered. Therefore, to limit the maximum required voltage ratio, the minimum number of required battery modules can be calculated. Dual-loop control diagram of the boost converter is shown in Fig. 8(b). A low-pass filter (LPF) for the measured voltage is used to reduce system fluctuations.

3) CEC Controller: Main function of this controller is to reconfigure the battery stack in order to obtain the minimum input voltage needed for the boost converter and at the same time realize CE during the discharging procedure. First, the controller identifies the battery modules SOC and the minimum number of battery modules with the highest SOC is switched in the pack and the others are bypassed. After every prespecified time interval, the SOC estimations for all modules are updated

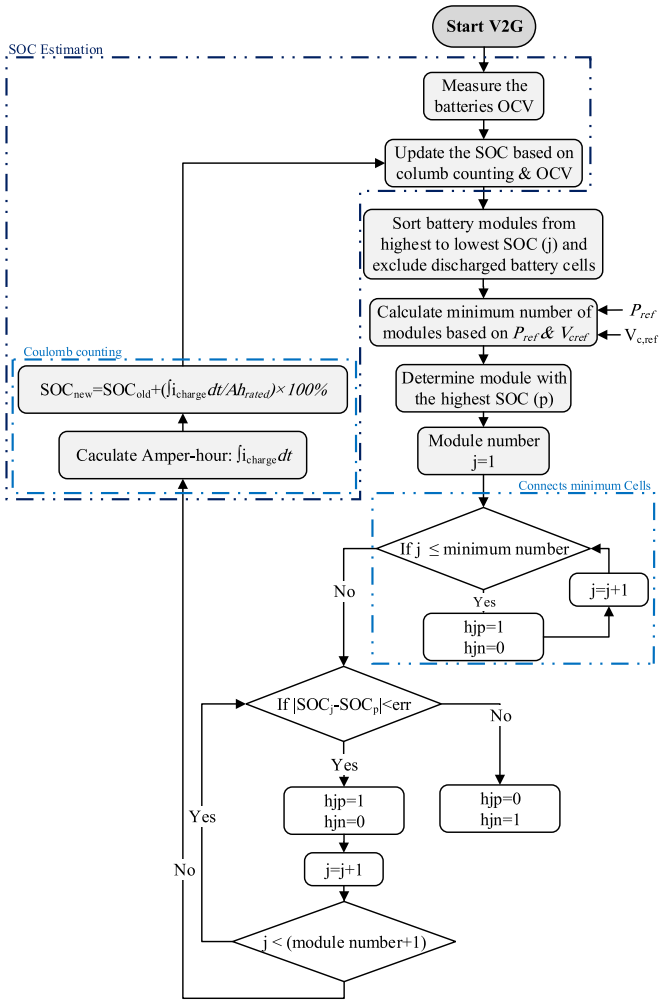

Fig. 9. CEC control algorithm during V2G mode.

and SOC of the selected modules are compared with the highest SOC of the bypassed ones. When SOC of the selected modules become lower than the highest SOC of the bypassed modules, the module with the highest SOC is switched in. The procedure is similar for other bypassed modules, until all of them are switched into the battery pack.

If there is no limit to the minimum number of connected modules, total CE is possible. Similar to the CEC control algorithm in G2V mode, control algorithm of the CEC in V2G mode is shown in Fig. 9. To prevent overdischarging, the modules are bypassed and removed from the CE procedure when their SOC reaches the lower permissible limit. It should be noted that if number of the connected modules becomes lower than the minimum required modules, the charger performance can be effected and complete CE may not be possible.

IV. System Design Considerations

Table II shows specifications of the simulated and implemented battery charger system. The built prototype charger has one-fifth of the simulated ratings. Since this topology is proposed as an on-board single-phase charger, power level is in range of 3 to 5 kW. Maximum current and voltage ripple is considered to be about 2%. The *LC* filters and other components are designed accordingly.

TABLE II
Battery Charger Specifications

Parameters	Simulations Value	Simulations Unit	Experiments Value	Experiments Unit
Input ac voltage (RMS)	220	V	36	V
AC input frequency	50	Hz	50	Hz
Maximum input ac current (RMS)	23	A	8	A
Maximum input current ripple	0.65	A	0.1	A
Desired dc-link voltage	400	V	80	V
Output dc voltage ripple	8	V	3	V
Maximum battery current in CC mode	10	A	3	A
Maximum output dc current ripple	0.2	A	0.05	A
Desired output voltage in CV mode	281	V	40	V
Maximum Output Power	5	kW	500	W
Maximum/minimum battery stack voltage	290–85	V	40–10	V
PWM switching frequency	20–30	kHz	30	kHz
Power factor at full load	0.99	–	0.97	–
THD full load	3	%	5	%

With the maximum power of 5 kW and input voltage of 220 V, the maximum peak current is 32 A. Considering maximum 2% current ripple, the $\Delta i_{s,\max}$ is 650 mA. With the dc voltage of 400 V and switching frequency of $f_s = 30$ kHz, the inductance voltage L_2 can be calculated. During inductor charging, using KVL we have

$$V_{L_2} = V_S - R_l I_S. \tag{6}$$

By substituting the V_S from (2), we have

$$V_S = V_{\rm dc}\left[1 - D + \frac{r_L}{1-D} + (1-D)2r_d + \frac{D^2(r_s+r_d)}{1-D}\right] \tag{7}$$

where $-2(1-D)V_{\rm fd} + D(V_{\rm sw} + V_{\rm fd})$ compared to $V_{\rm dc}$ is negligible.

Furthermore, considering $I_S = \frac{I_{\rm dc}}{\frac{V_S}{V_{\rm dc}}}$, I_S can be calculated using

$$I_S = \frac{V_{\rm dc}}{R_{\rm load}\left[1 - D + \frac{r_L}{1-D} + (1-D)2r_d + \frac{D^2(r_s+r_d)}{1-D}\right]}. \tag{8}$$

Using (7) and (8), (6) can be written as

$$V_{L_2} = V_{\rm dc}\left[A - \frac{r_L}{A}\right] \tag{9}$$

where $A = 1 - D + \frac{r_L}{1-D} + (1-D)2r_d + \frac{D^2(r_s+r_d)}{1-D}$ and $r_l = R_l/R_{\rm load}$.

AC current ripple can be calculated using

$$\Delta i_S = \frac{V_{L_2} D T_s}{L_2}. \tag{10}$$

Hence, Δi_S can be calculated using

$$\Delta i_S = \frac{V_{\rm dc}}{L_2 f_s} D\left[A - \frac{r_l}{A}\right]. \tag{11}$$

TABLE III
BATTERY MODULE SPECIFICATIONS

		Simulations			Experiments		
Battery cell	Battery type	Nominal voltage	Rated capacity	Internal resistance ($r_{\rm ESR}$)	Nominal voltage	Module capacity	Battery cells
Cell 1	Li-Ion	80 V	25 Ah	0.02 Ω	12 V	5.2 Ah	3 × 3.7 V - 5.2 Ah (in series)
Cell 2	Li-Ion	80 V	22.5 Ah	0.03 Ω	12 V	5.2 Ah	3 × 3.7 V - 5.2 Ah (in series)
Cell 3	Li-Ion	80 V	27.5 Ah	0.02 Ω	12 V	5.2 Ah	3 × 3.7 V - 5.2 Ah (in series)

Considering typical values for the switch and diode resistances, maximum value for $D\left(A-\frac{r_L}{A}\right)$ can be calculated to be around 0.33 for $D=0.85$, hence maximum Δi_s can be calculated. From (11), L_2 can be calculated to be 12.7 mH. With neglecting the switch and diode resistances, L_2 can be calculated using (12), which results in $L_2=5.1$ mH. In this paper, a 12.7 mH inductor is selected

$$L_2=\frac{V_{\rm dc}}{4\times\Delta i_S\times f_s}. \tag{12}$$

In order to charge and discharge batteries, with low ripple current, a constant dc-link voltage is essential. The dc-link capacitor acts as a filter and damps any sudden voltage fluctuation due to inductor charge and/or discharge. DC-link capacitor can be calculated using [29]

$$C_2=\frac{2\times V_{S,\rm rms}\times I_{S,\rm rms}}{\omega_s\times\Delta v_{\rm dc}\times V_{\rm dc}} \tag{13}$$

where $\Delta V_{\rm dc}$ is dc voltage ripple $\omega_s=2\times\pi\times f_{\rm source}$. Using (13), dc-link capacitor (C_2) is 10 mF, where a 12 mF value is selected.

To design the dc–dc output filter, low ripple charging current is essential. The *LC* filter can be calculated using

$$L_3C_3=\frac{(1-D)\times D\times V_{\rm dc}}{8\times f_s^2\times r_{\rm ESR}\times\Delta i_{\rm batt}}. \tag{14}$$

The worst case in calculating L_3 and C_3 is related to the condition, in which only one battery module is charging. To obtain maximum value of C_3, considering $D=0.5$, maximum $r_{\rm ESR}$ value of 0.1 Ω and ripple current of 0.2 A, L_3 and C_3 can be calculated. If L_3 is 500 μH, then C_3 would be 1.38 mF. Also, to design L_1 and C_1 LPF parameters, (15) can be used

$$C_1=\frac{1}{8\times\pi^2\times f_s^2\times L_1}. \tag{15}$$

Selecting L_1 to be 100 μH, C_1 would be about 140 nF and two 330 nF polyester capacitors in series were utilized.

V. SIMULATION AND EXPERIMENTAL RESULTS

To verify the system analysis, the proposed charger and CEC are simulated in MATLAB software. The design specifications for the simulated and implemented systems are tabulated in Table II. The battery pack consists of three different modules. Battery pack characteristics are presented in Table III. Table IV presents utilized components for the simulation and low-scaled prototype.

TABLE IV
CHARGER/CEC UTILIZED PARAMETERS IN SIMULATION AND EXPERIMENTS

	Simulations		Experiments	
Component	Value/type	Unit	Value/type	Unit
L_1	100	μH	100	μH
r_{L1}	0.1	Ω	0.1	Ω
C_1	150	nF	150	nF
L_2	12.7	mH	11.5	mH
r_{L2} (L_2 resistance)	0.1	Ω	0.1	Ω
C_2	10.1	mF	11.9	mF
L_3	500	μH	600	μH
r_{L3} (L_3 resistance)	0.1	Ω	0.1	Ω
C_3	1.4	mF	1	mF
IGBT	–	–	BUP314D	–
IGBT resistance	0.03	Ω	0.05	Ω
Current sensor	–	–	ACS712	–
dsPIC controller	–	–	30F4011	–

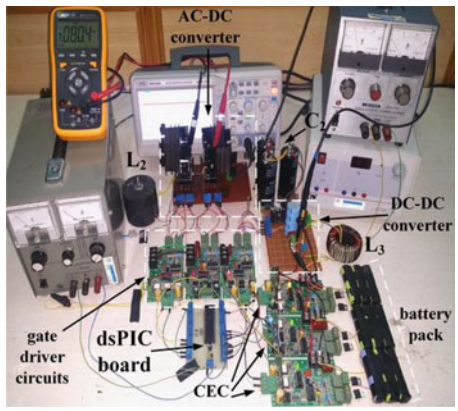

Fig. 10. Implemented system in the laboratory.

As seen in Table III, in simulations, each battery module has slightly different capacity and state of charge. The charger should estimate the SOC of each module and reconfigure the battery stack according to operation mode. The proposed controller is implemented using dsPIC30F4011. To obtain the required dc-link capacitor, three electrolyte 3300 μF/100 V capacitors are utilized in parallel combined with two 1-mF ceramic capacitor. In Fig. 10, the implemented system is shown and the main components are depicted.

A. G2V Mode

In Fig. 11, simulation result for SOC of the modules during CE is shown. Since module 2 has the lowest SOC, the charging

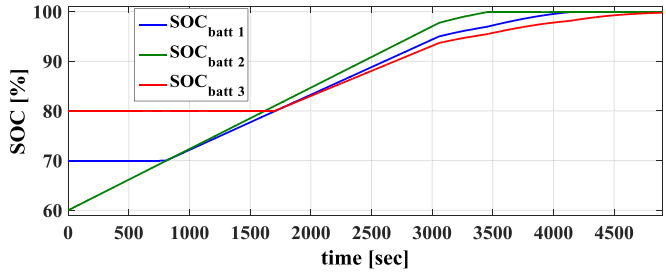

Fig. 11. SOC of the battery modules during the G2V mode.

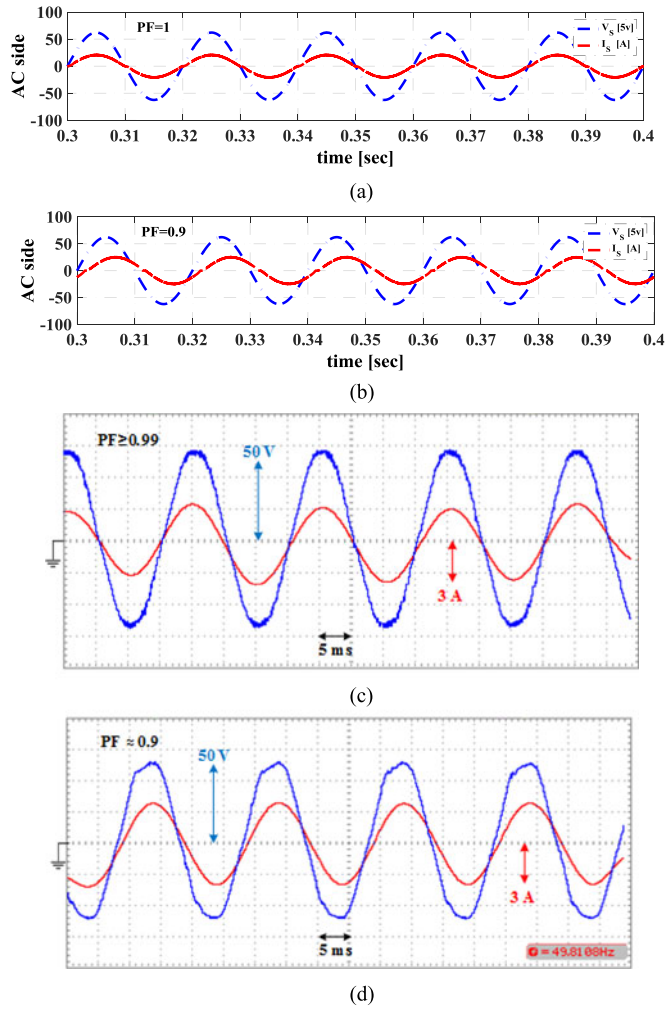

Fig. 12. Simulation and experimental results for ac–dc converter in G2V mode: (a) simulation result for V_S and I_S with PF = 1; (b) simulation result for V_S and I_S with PF = 0.9; (c) experimental results for with PF = 1; (d) experimental results for PF = 0.9.

procedure starts from this module. When SOC of module 2 reaches module 1, module 1 is switched in. This procedure is repeated for module 3, too. When all the modules have the same SOC, CE is complete. After the CE is complete, if the batteries are not charged, completely, the charging continues. As shown in Fig. 11, each battery that is charged completely would be bypassed. When the batteries voltage reaches a certain level, CV charging starts. Here, CV charging starts at 3000th s, where the charging slope changes.

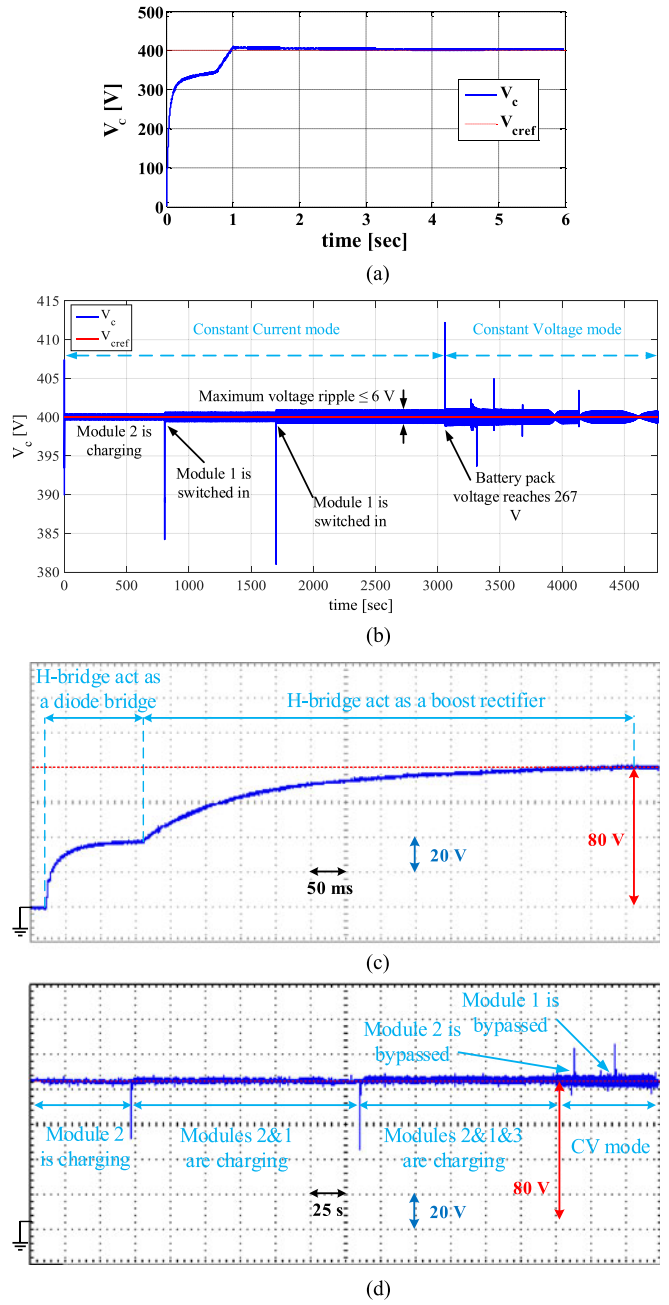

Fig. 13. Simulation and experimental results for dc-link voltage during G2Vmode: simulation results during (a) the start-up, (b) the CE procedure; experimental results during, (c) the start-up, (d) the CE procedure.

In Fig. 12(a), simulation results for input ac voltage and current during the G2V mode with unity PF are shown. Fig. 12(b) shows simulation results for ac side with PF = 0.9. Fig. 12(a) and (b) shows ac input current. It is obvious that I_S is sinusoidal. Experimental results for the G2V mode is shown in Fig. 12(c) and (d). It can be observed that maximum current ripple is 5% and PF is about 0.99.

The dc-link voltage is kept constant with 2% ripple. In Fig. 13(a), dc-link voltage at startup and in Fig. 13(b) dc-link voltage during CE are shown. As depicted, the dc link has good response time and low ripple. When a module is connected,

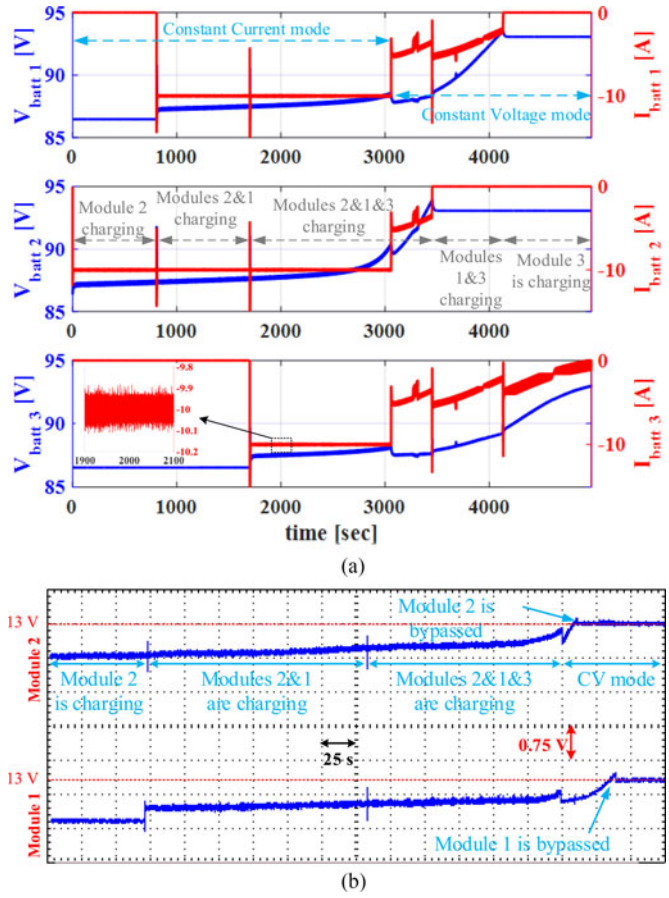

Fig. 14. G2V operation: (a) simulation results for battery modules voltage and current; (b) experimental battery voltage for modules 1 and 2.

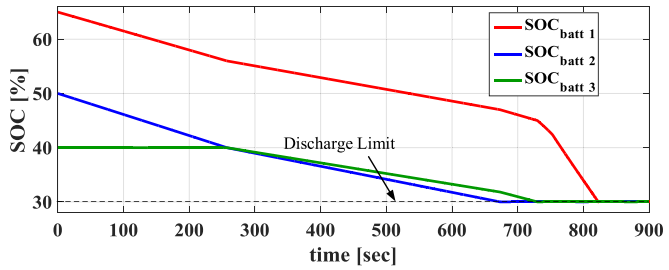

Fig. 15. SOC of the battery modules during the V2G mode.

since the output power is increased, there is a momentary voltage drop at the dc link, but the controller would compensate the voltage drop by increasing the input power. Similarly, when a module is bypassed, there is a temporary increase in the voltage. In case of the module insertion, maximum voltage drop is less than 5%, while it is less than 2% at steady-state operation.

The battery charging current and input voltage is shown in Fig. 14. Here, positive current is considered to be the battery discharging current. Since $SOC_2 < SOCS_1 < SOC_3$, order of charging is module 2, module 1, and module 3. Batteries are charged with constant current equal to 10 A during the CC mode with maximum current ripple of 2%. When the batteries are charged to a certain level, charge strategy changes to constant voltage.

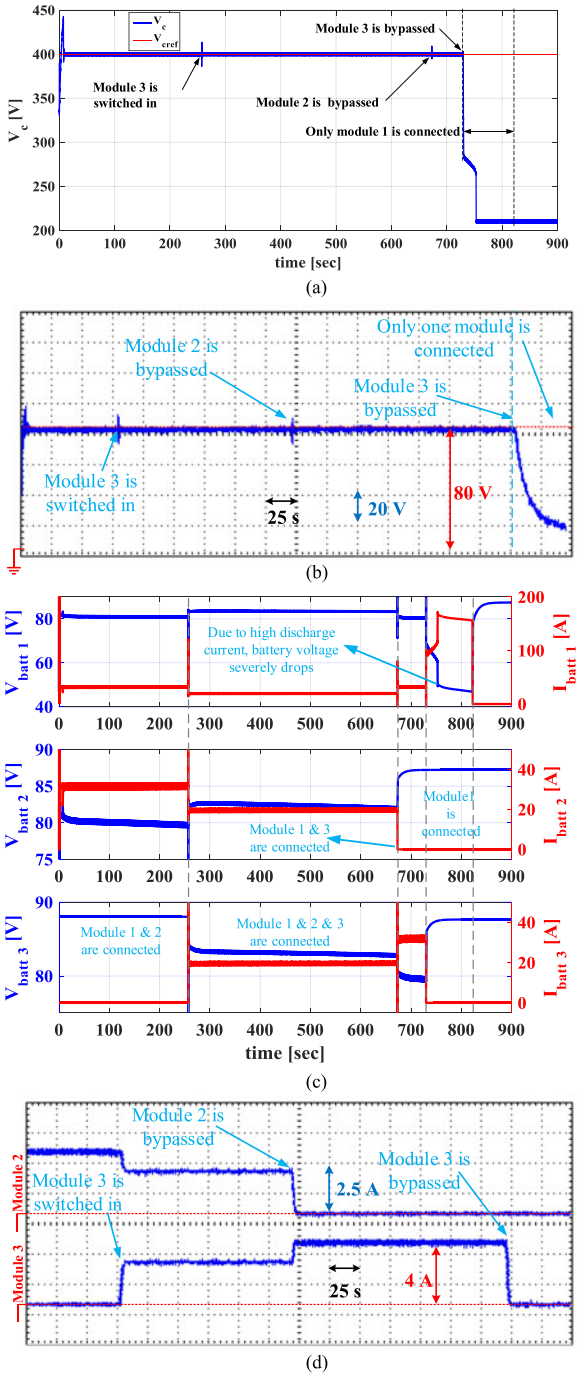

Fig. 16. DC side during V2G: (a) simulation result of dc-link voltage during CE; (b) experimental result of dc-link voltage during CE; (c) simulation result for battery pack voltage and current; (d) experimental results for the battery pack currents.

B. V2G Mode

Considering the maximum boosting ratio equal to 3, the minimum number of required modules is 2. Modules 1 and 2 are selected and module 3 is bypassed. When the SOC of the module 2 reaches the SOC of the module 3, it is added to the battery pack. In Fig. 15, SOC of the modules during CE in V2G mode is shown.

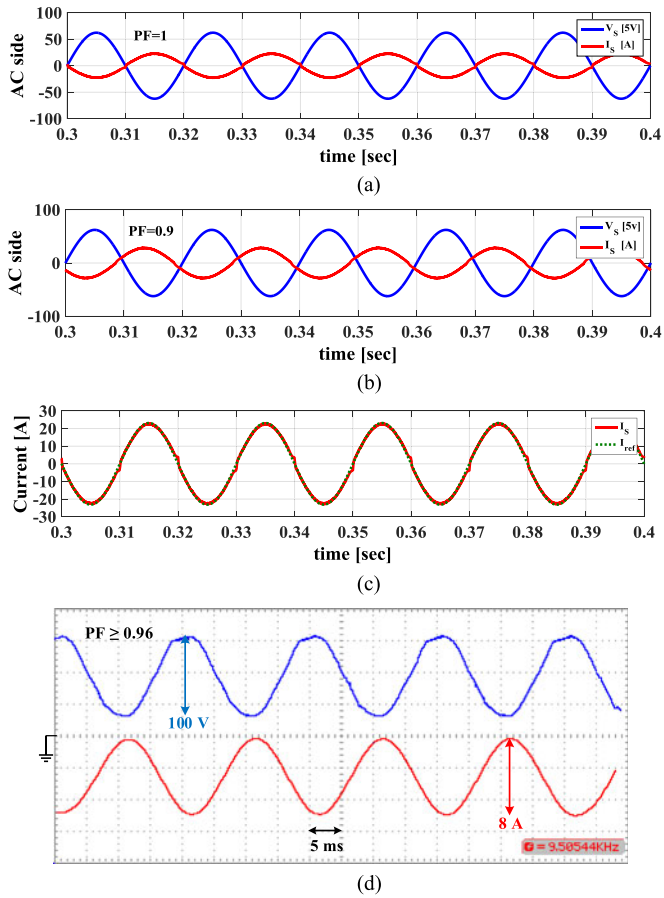

Fig. 17. Simulation and experimental results for ac–dc converter in the V2G mode: (a) simulation result for V_S and I_S with PF $= 1$; (b) simulation result for V_S and I_S with PF $= 0.9$; (c) simulation result for I_S and I_{ref}; (d) experimental results for V_S and I_S with unity PF.

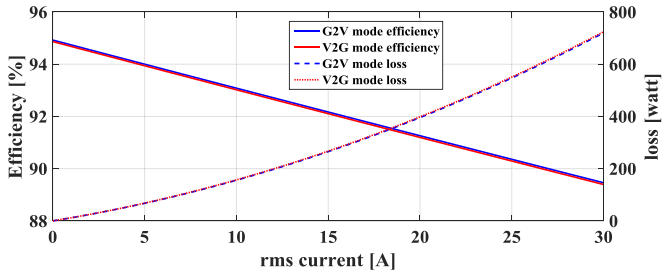

Fig. 18. Total efficiency and power loss during G2V and V2G operation.

In order to enhance battery pack life cycle and prevent overdischarging the battery cells, a discharge limit is selected during V2G operation. When SOC of a module reduces to the lower limit, it should be bypassed by the CEC. Here, 30% is selected as the minimum permissible SOC. At about 670 and 730, modules 2 and 3 are discharged to their limit and are bypassed by the CEC. At 730 s, since only one module is connected, the boost converter cannot maintain the desired output voltage during the full load, as shown in Fig. 16(a) and (b), and voltage drops.

The dc–dc converter boosts the battery pack voltage to achieve the required dc voltage. The dual-loop control of the dc–dc converter discharges the battery pack with constant current, while holding the dc-link voltage constant. In Fig. 16(c) and (d), discharge current of the battery modules are shown. During normal operation, with 4.7 kW output power, maximum current ripple is about 8%. In comparison with the single-loop boost control addressed in [29], the ripple has decreased more than 50%. Since the injected power to the grid is constant, any time a module is switched in or out, the discharge current changes to accommodate the power variation. As the modules are discharged, their terminal voltage decreases. Therefore, their current is increased to maintain the power constant. Also, in this mode, dc-link voltage ripple is less than 2%.

The controller of the ac–dc converter calculates the $I_{\rm ref}$ required providing the specified active and reactive powers. In Fig. 17(a), ac-side voltage and current with $Q_{\rm ref} = 0$ are shown, while the result in PF $= 0.9$ is shown in Fig. 17(b). From Fig. 17(c), it can be observed that I_S follows the $I_{\rm ref}$ accurately and the output current has acceptable ripple about 3%. Also, in Fig. 17(d), an experimental result for the V2G operation mode is shown. Here, PF is more than 0.96 and THD is lower than 5%.

Converter efficiency can be analyzed for both modes of operation. In order to analyze system efficiency, there are some assumptions: 1) converters are assumed to operate in CCM; 2) PF is assumed to be unity; 3) dc-side voltage is assumed to be a dc voltage with negligible ripples; and 4) efficiency of 100% is assumed. Battery charger efficiency is analyzed using the presented method in [42], [43]. Considering the simulated system parameters, battery charger efficiency curve based on the ac current is shown in Fig. 18.

Furthermore, input and output power of the battery charger was measured and the combined efficiency of the ac–dc and dc–dc converters with unity PF was about 95% and 94% for G2V and V2G operation, respectively. Although measuring the efficiency of the CEC is not possible, based on the presented efficiency analysis, the CEC efficiency was calculated to be about 98% and 99% during G2V and V2G operation. Therefore, total efficiency of the charger is about 92% for both operations.

VI. Conclusion

In this paper, an on-board single-phase battery charger with integrated modular CEC is developed. The operation principle and control algorithms are explained in detail. In addition to integrated CE capability, the developed charger has advantage of low THD input current with active and reactive power control. The ability of charging/discharging the battery with constant current improves battery pack life cycle. Because of the implemented switching pattern, the switching loss is reduced. Furthermore, due to the modular structure, the CEC can bypass damaged modules without interrupting the charge/discharge procedure. It should be noted that the CEC efficiency reduces as the module number increases, however the CE capability improves. Therefore, usually there is a tradeoff between maximum number of battery modules, overall efficiency, and costs should be made. To evaluate the performance of the proposed charger, some simulations and experiments are carried out. The results confirm the capabilities of the proposed method. The batteries are charged with maximum ripple 2% and discharged with maximum ripple 8%. Also, ripple of the input ac current is less than 3%. THD of the

input current is less than 3%, in which harmonics third and fifth have the highest amplitude about 2% and 1.5%, respectively.

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Authors' photographs and biographies not available at the time of publication.