A 10-MHz eGaN Isolated Class-Φ_2 DCX

Zhiliang Zhang, Xue-Wen Zou, Zhou Dong, Yuan Zhou, and Xiaoyong Ren

***Abstract*—Derived from the class-E resonant converters, the isolated class-Φ_2 resonant converters have much reduced voltage stress of the control FET owing to a shunt branch paralleled with the switch to provide low pass path for the second harmonic voltage. With the increase of the input voltage, the reverse conduction time of the power FETs varies seriously and the gate drive voltage can hardly match efficiently with the drain voltage of the synchronous rectifier (SR) FET. This causes the earlier turn-on of the SR FET before zero voltage switching (ZVS) is achieved, which results in high turn-on loss at multi-MHz. Moreover, with the enhancement mode gallium nitride (eGaN) HEMTs, the mismatch between the drive voltage and drain voltage results in high reverse conduction mechanism loss after the SR FET turns off in the switching period of hundreds of nanoseconds. The reverse conduction mechanism of the control eGaN HEMT can be triggered before ZVS turn-on, which causes high reverse conduction loss. It is interesting to find that when the output voltage is controlled to follow the input voltage proportionally, the drive voltage can match well with the drain voltage of the power FETs over a wide input voltage range, which is proved mathematically by the state-space analysis. Then, a voltage following control is proposed to control the isolated resonant converters as dc transformers (DCXs). The turn-on loss of the SR FET and reverse conduction loss of the SR and control FETs can be minimized. An 18–24 V input, 18 W/2 A output, 10-MHz eGaN DCX was implemented to verify the advantages. With the proposed control, the efficiency is improved from 79.9% to 85.5% at 18 W output and 24 V input.**

***Index Terms*—DC transformer (DCX), enhancement mode gallium nitride (eGaN) HEMT, isolated resonant converter, multi-MHz, voltage following control.**

I. Introduction

NORMALLY, increasing the switching frequency of the converters to megahertz is an effective way to reduce the volume of the passive components and increase the power density [1]–[3]. Recently, a lot of researches have been done on multi-MHz class-Φ_2 resonant converters owing to zero voltage switching (ZVS) capability and lower voltage stress of the switches compared to the class-E resonant converters [4]–[6].

In the multi-MHz resonant converters, the realization of the synchronous rectifier (SR) is of great importance because the rectifier diodes have serious impact on the efficiency of the converters [7]–[9]. Typically, the conduction loss dissipated in the rectifier diodes accounts for 30–35% of the total loss [9], [10]. This is because that the forward recovery loss of the diodes becomes extremely high at multi-MHz. Comparing the enhancement mode gallium nitride (eGaN) HEMTs to the silicon MOSFETs with the same voltage and current rating, it is noted that the eGaN HEMTs have much reduced conduction resistance and parasitic capacitance [11]–[14]. Owing to fast switching speed and low gate charge, the eGaN HEMTs are suitable to the multi-MHz resonant converters, which leads to significant improvement of the conversion efficiency [15]–[18]. The power loss is reduced by 25% in the 1.2-MHz resonant bus converter when the Si MOSFETs are replaced by the eGaN HEMTs in [18]. However, the eGaN HEMTs have no body diodes, and when using as the SR FETs, the reverse current has to flow via the channel by the reverse conduction mechanism, which causes high reverse conduction loss. Therefore, it is important to minimize the reverse conduction time when the eGaN HEMTs are used in the multi-MHz resonant converters.

To drive eGaN HEMTs efficiently over a wide input voltage range is another challenge when they are used in the multi-MHz isolated resonant converters. Normally, the hysteresis control is applied to the multi-MHz resonant converters to regulate the output voltage for fast dynamic response. With the hysteresis control, the reverse conduction time before the turn-on of the control FETs and after the turn-off of the SR varies with the input voltage seriously. With the increase of the input voltage, the gate drive voltage can hardly match with the drain-to-source voltage of the SR FET efficiently. This results in the earlier turn-on of the SR FET before ZVS condition is realized, which causes high turn-on loss at multi-MHz. Moreover, with the eGaN HEMTs, the reverse conduction mechanism is triggered after the gate drive voltage of the SR FET turns off. So, the high reverse conduction loss of the SR FET happens [19]. On the other hand, with the increase of the input voltage, the reverse conduction mechanism of the control eGaN HEMT can also be triggered before ZVS turn-on, which results in the high reverse conduction loss similarly.

In this paper, a state-space method is applied to prove that the drive voltage can match well with the drain voltage of the power FETs over a wide input voltage range when the output voltage is controlled according to the input voltage proportionally. A voltage following control is proposed for the isolated resonant GaN HEMT converter. The output voltage is controlled to follow the input voltage proportionally as a DCX. The drive voltage can match well with the drain voltage of the power FETs over a wide input voltage range. The hard-switching of the SR FET and reverse conduction problem of the SR and control FETs mentioned above are solved.

The proposed DCX can be used as the first stage of the distributed two-stage power architecture to achieve isolation, and the low dropout regulators can be cascaded after the DCX. The

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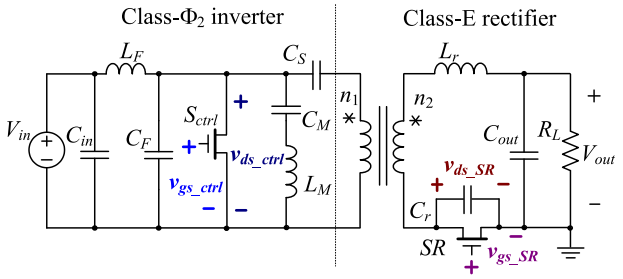


Fig. 1. Isolated class-Φ_2 resonant converter.

TABLE I
SPECIFICATIONS OF THE CONVERTER

Input voltage $V_{\rm in}$	18–24 V
Output voltage V_o	9 V
Output current I_o	2 A
Switching frequency f_s	10 MHz

distributed two-stage power architecture with a wide input voltage range is often used to power the IC devices in the communication system and industrial electronics system, etc., where the isolation is normally required. In addition, the main idea of the proposed voltage following control can be extended to other high frequency isolated resonant converters, and the output power of the DCX can be designed from tens of watts to hundreds of watts according to different applications.

Section II introduces the hard-switching and reverse conduction problem. The mathematical modeling is presented in Section III. The realization and characteristics of the proposed voltage following control are given in Section IV. Section V contains the experimental validation. Finally, Section VI concludes this paper.

II. Hard-Switching and Reverse Conduction Problem of eGaN HEMTs

Fig. 1 shows the isolated class-Φ_2 resonant converter. Table I gives the specifications.

The simulation model of the isolated class-Φ_2 resonant converter was built in the LTspice. The spice models of the EPC2001 are used. Fig. 2 shows the simulated waveforms of the drain-to-source voltage of the SR FET when the input voltage is 18 and 24 V, respectively. In Fig. 2(a), the reverse conduction mechanism of the SR FET is not triggered, the zero reverse conduction of the SR FET is obtained, and ZVS of the SR FET is achieved at the same time. However, the resonant status of the converter varies seriously with the wide input voltage. In Fig. 2(b), when the input voltage increases to 24 V, the SR FET turns on early before ZVS condition is realized. Without ZVS, the hard-switching of the SR FET occurs, which results in high turn-on loss at multi-MHz. Moreover, the reverse conduction mechanism is triggered after the SR FET turns off. The reverse conduction time is 9 ns at 24 V input, which is more than 15% of the total conduction time in one switching cycle. This results

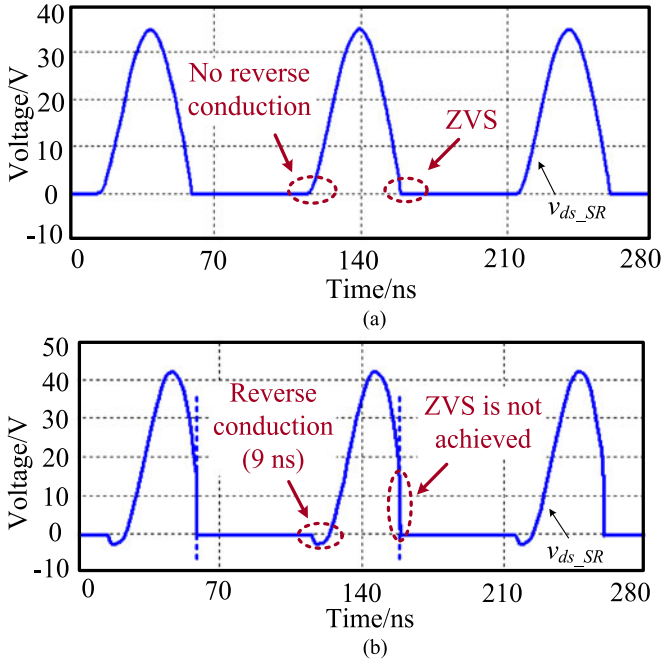


Fig. 2. Simulated drain-to-source voltage of SR FET with different input voltage: (a) $V_{\rm in} = 18$ V and (b) $V_{\rm in} = 24$ V.

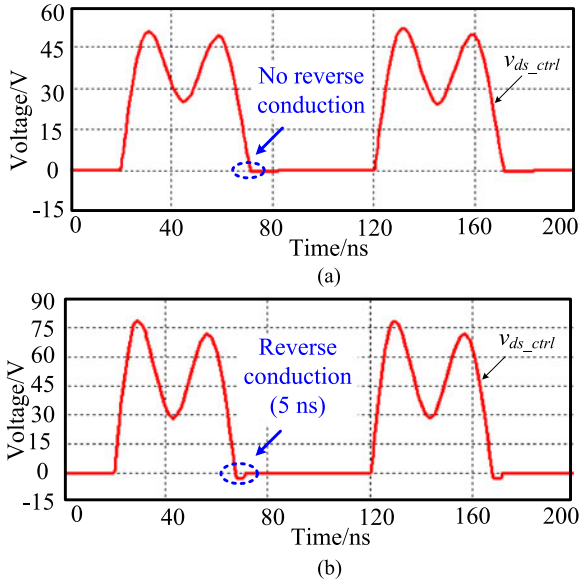


Fig. 3. Simulated drain-to-source voltage of the control FET with different input voltage: (a) $V_{\rm in} = 18$ V and (b) $V_{\rm in} = 24$ V.

in the reverse conduction loss of 0.08 W when the Si MOSFET Si7454DDP from Vishay company is used as the SR FET. The reverse conduction loss of the eGaN HEMT is even higher. When the eGaN HEMT EPC2001 from efficient power conversion (EPC) is used, the reverse conduction voltage is 1.8 V and the reverse conduction loss is as much as 0.18 W, which is 1% of the output power.

Fig. 3 shows the simulated waveforms of the drain-to-source voltage of the control FET when the input voltage is 18 and 24 V,

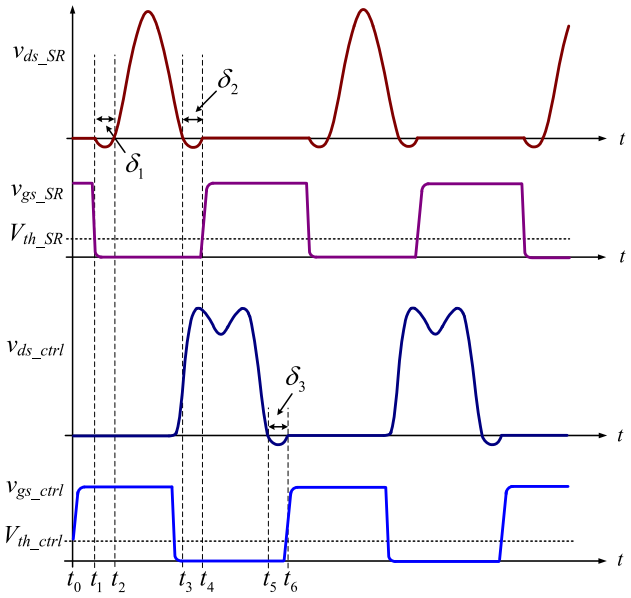


Fig. 4. Reverse conduction time of the control FET and SR FET.

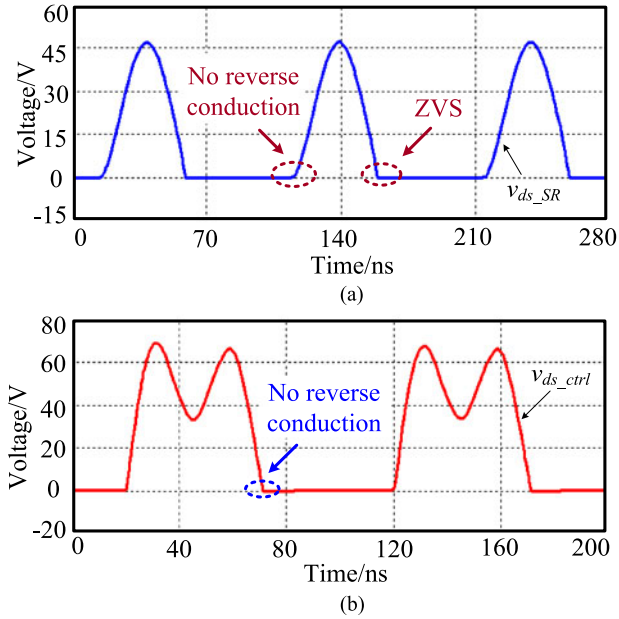


Fig. 5. Simulated open-loop drain-to-source voltage waveforms at 24 V input. (a) Drain-to-source voltage of the SR FET. (b) Drain-to-source voltage of the control FET.

respectively. In Fig. 3(a), the zero reverse conduction of the control FET is achieved at 18 V input. However, when the input voltage increases to 24 V, the reverse conduction mechanism is triggered before the control eGaN HEMT turns on. The reverse conduction time of the control eGaN HEMT is 5 ns at 24 V input which causes high reverse conduction loss. It is noted from Fig. 3 that with the increase of the input voltage, the reverse conduction loss of the control eGaN HEMT increases too.

In summary, it should be noted that when the output voltage of the isolated class-Φ_2 resonant converter is regulated to the fixed value, ZVS of the SR FET may lose with the change of the input voltage and the hard-switching of the SR FET occurs. In addition, with the increase of the input voltage, the reverse conduction time of the power FETs increases and the reverse conduction problem happens.

III. Reverse Conduction Time and Mathematical Modeling

A. Reverse Conduction Time Under Open-Loop Status

Fig. 4 shows the reverse conduction time of the power FETs. δ_1 is defined as the reverse conduction time after the turn-off of the gate drive voltage of the SR FET. δ_2 and δ_3 are defined as the reverse conduction time before the turn-on of the SR FET and control FET, respectively. In Fig. 4, the drive voltage of the control FET reaches its threshold and it turns on at $t = t_0$. The drive signal of the SR FET turns off at $t = t_1$. The drain-to-source voltage of the SR FET starts to increase at $t = t_2$. During $[t_1, t_2]$, the reverse conduction mechanism of the SR eGaN HEMT is triggered. At $t = t_3$, the drain voltage of the SR FET decreases to zero and it turns on at $t = t_4$. The drain-to-source voltage of the control FET resonates to zero at $t = t_5$ and control FET turns on again at $t = t_6$. During $[t_5, t_6]$, the reverse conduction mechanism of the control eGaN HEMT is triggered.

Fig. 5 shows the simulated waveforms of the SR FET and control FET when the converter operates at the open-loop status with the rated load at 24 V input. From Fig. 5(a), it is noted that ZVS of the SR FET is achieved and the reverse conduction mechanism is not triggered when the input voltage of the converter reaches 24 V. In Fig. 5(b), the zero reverse conduction of the control FET is observed.

It is noticed that when the converter is in the open-loop status with the rated load, the hard-switching of the SR FET and the reverse conduction problem mentioned earlier are minimized. This is because the output voltage follows the input voltage proportionally under this condition. The proportional variation of the output voltage according to the input voltage leads the gate drive voltage to match well with the drain voltage of the power FETs. The reverse conduction time δ_1, δ_2, and δ_3 defined in Fig. 4 remains constant and is minimized to zero over a wide input voltage range. Then, ZVS of the SR FET and zero reverse conduction of the power FETs can be achieved over a wide input voltage range.

B. Mathematical Modeling

As shown in Fig. 6, the equivalent circuit of the isolated class-Φ_2 resonant converter is established. The load of the converter is modeled by a dc voltage source $V_{\rm out}$. The control FET and the SR FET are replaced by their equivalent resistances r_{Q1} and r_{Q2}, respectively. r_F and r_M represent the equivalent resistance of the inductance L_F and L_M, respectively. r_p represents the equivalent resistance of the primary winding of the transformer and r_s is the total equivalent resistance of the secondary winding and the inductance L_r. The inductance L_S represents the

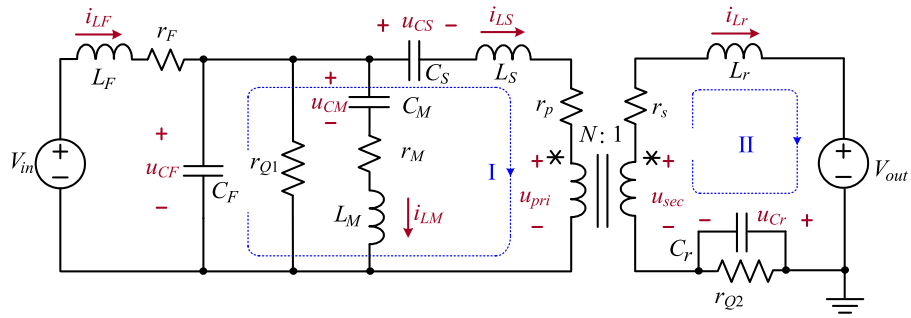


Fig. 6. Unified equivalent circuit.

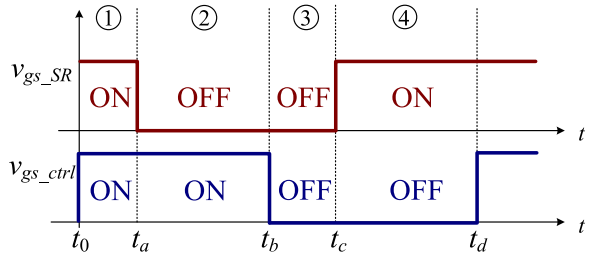


Fig. 7. Operation modes related to control FET and SR FET in one switching cycle.

primary-side leakage inductance of the transformer. The analysis will be based on the following three assumptions:

1) the control FET and SR FET have zero switching time, infinite OFF resistances and ON resistances r_{ON1} and r_{ON2}, respectively;
2) the capacitance C_F and C_r absorbs the output capacitance of the control FET and SR FET, respectively;
3) the transformer is used as an ideal transformer and its secondary-side leakage inductance is absorbed by the inductor L_r.

Fig. 7 shows four operation modes related to drive voltage of the power FETs in one switching cycle. The equivalent circuits of each operation mode are given in Fig. 8. The converter has four operation modes depending on the status of the switches, which are defined in Table II and $t_d - t_0 = T_s, T_s$ is the time of a switching cycle. Fig. 9 shows the drain-to-source voltage waveforms of the control FET and SR FET with the designed input voltage V_{in} and output voltage V_{out}.

C. Mathematical Analysis

1) Establishment of State-Space Equations: The equivalent circuit is shown in Fig. 6, where N is the turns ratio of the primary winding and secondary winding, respectively. u_{pri} and u_{sec} are the primary and secondary voltage, respectively, where $u_{pri} = N \cdot u_{\mathrm{sec}}, i_{Ls} = i_{Lr}/N$. KVL is applied for the loop I and loop II, respectively, to obtain

$$L_S \frac{di_{LS}(t)}{dt} = u_{CF}(t) - u_{CS}(t) - u_{\mathrm{pri}} - rp \cdot i_{LS}(t) \quad (1)$$

$$L_r \frac{di_{Lr}(t)}{dt} = u_{\mathrm{sec}} - V_{\mathrm{out}} - u_{Cr}(t) - r_s \cdot i_{Lr}(t). \quad (2)$$

Substituting (1) into (2), combined with $u_{pri} = N \cdot u_{\mathrm{sec}}$, (3) is derived

$$L_r \frac{di_{Lr}(t)}{dt} + \frac{L_S}{N} \cdot \frac{di_{LS}(t)}{dt} = \frac{u_{CF}(t)}{N} - \frac{u_{CS}(t)}{N} - V_{\mathrm{out}} - u_{Cr}(t) - \frac{r_p \cdot i_{LS}(t)}{N} - r_s \cdot i_{Lr}(t). \quad (3)$$

Substituting $i_{Ls} = i_{Lr}/N$ into (3), (4) is obtained

$$\left(L_r + \frac{L_S}{N^2}\right) \cdot \frac{di_{Lr}(t)}{dt} = \frac{u_{CF}(t)}{N} - \frac{u_{CS}(t)}{N} - V_{\mathrm{out}} - u_{Cr}(t) - \left(\frac{r_p}{N^2} + r_s\right) \cdot i_{Lr}(t). \quad (4)$$

It is noted from (4) that the leakage inductance L_S of the primary side can be equivalent to the secondary side and be absorbed by the inductor L_r. Fig. 6 can be simplified to Fig. 10, where equivalent inductance $L_{re} = L_r + L_s/N^2$. Substituting $L_{re} = L_r + L_s/N^2$ into (4), (5) is derived

$$\frac{di_{Lr}(t)}{dt} = \frac{u_{CF}(t)}{L_{re} \cdot N} - \frac{u_{CS}(t)}{L_{re} \cdot N} - \frac{V_{\mathrm{out}}}{L_{re}} - \frac{u_{Cr}(t)}{L_{re}} - \frac{1}{L_{re}} \cdot \left(\frac{r_p}{N^2} \cdot + r_s\right) \cdot i_{Lr}(t). \quad (5)$$

In Fig. 10, KCL is applied on the node A and (6) is obtained

$$\frac{du_{CF}(t)}{dt} = \frac{i_{LF}(t)}{C_F} - \frac{u_{CF}(t)}{C_F \cdot r_{Q1}} - \frac{i_{LM}(t)}{C_F} - \frac{i_{Lr}(t)}{C_F \cdot N}. \quad (6)$$

Calculating the current i_{LM} of the capacitance C_M and i_{Cs} of the capacitance C_S, respectively, (7) and (8) are derived

$$\frac{du_{CM}(t)}{dt} = \frac{i_{LM}(t)}{C_M} \quad (7)$$

$$\frac{du_{CS}(t)}{dt} = \frac{i_{Lr}(t)}{C_S \cdot N}. \quad (8)$$

Applying KCL on the node B, (9) can be obtained

$$\frac{du_{Cr}(t)}{dt} = \frac{i_{Lr}(t)}{C_r} - \frac{u_{Cr}(t)}{C_r \cdot r_{Q2}}. \quad (9)$$

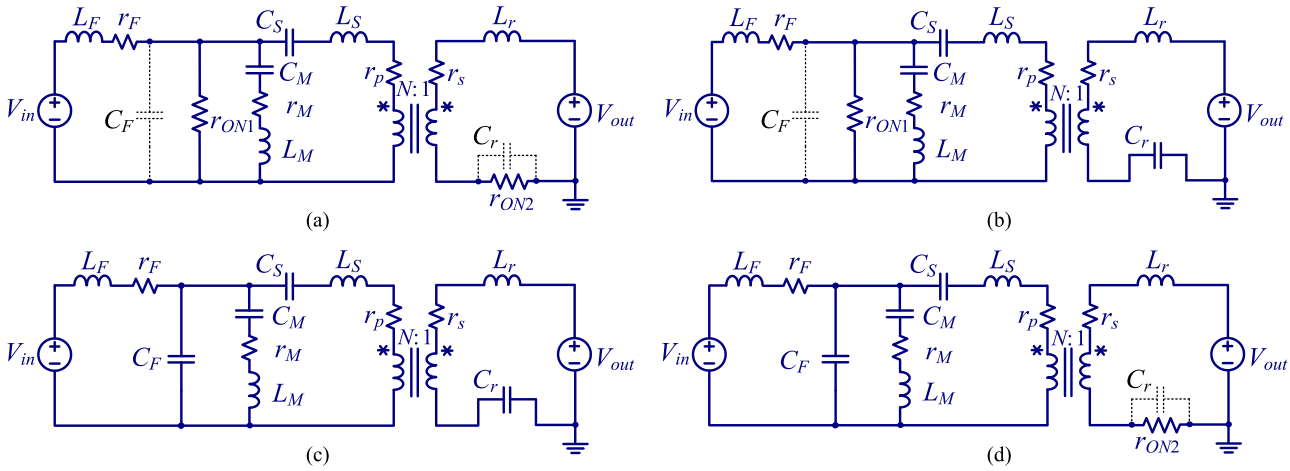


Fig. 8. Equivalent circuits of operation modes: (a) $[t_0, t_a]$, (b) $[t_a, t_b]$, (c) $[t_b, t_c]$, and (d) $[t_c, t_d]$.

TABLE II
DEFINITION OF THE FOUR OPERATING MODES

Mode	Time	r_{Q1}	r_{Q2}
①	$t_0 < t \le t_a$	r_{ON1}	r_{ON2}
②	$t_a < t \le t_b$	r_{ON1}	∞
③	$t_b < t \le t_c$	∞	∞
④	$t_c < t \le t_d$	∞	r_{ON2}

Applying KVL in the loops III and IV, (10) and (11) can be derived

$$\frac{di_{LF}(t)}{dt} = \frac{V_{\text{in}}}{L_F} - \frac{i_{LF}(t)\cdot r_F}{L_F} - \frac{u_{CF}(t)}{L_F} \tag{10}$$

$$\frac{di_{LM}(t)}{dt} = \frac{u_{CF}(t)}{L_M} - \frac{u_{CM}(t)}{L_M} - \frac{r_M \cdot i_{LM}(t)}{L_M}. \tag{11}$$

The state (5)–(11) can be represented by the following state-space equation:

$$\dot{X}(t) = AX(t) + BU(t) \tag{12}$$

where $X(t)$ is the state vector and contains the following voltage and current state variables:

$$X(t) = \begin{bmatrix} u_{CF}(t) & u_{CM}(t) & u_{CS}(t) & u_{Cr}(t) \\ i_{LF}(t) & i_{LM}(t) & i_{Lr}(t) & \end{bmatrix}^T. \tag{13}$$

From Fig. 1, it isnoted that the state variables $u_{CF}(t) = v_{ds\_ctrl}$ and $u_{Cr}(t) = -v_{ds\_SR}$, where v_{ds_ctrl} and v_{ds_SR} are the drain-to-source voltage of the control FET and SR FET, respectively. $\dot{X}(t)$ is the state vector consisting of the differential form of the above voltage and current state variables. The state vector of $\dot{X}(t)$ is

$$\dot{X}(t) = \begin{bmatrix} \frac{du_{CF}(t)}{dt} & \frac{du_{CM}(t)}{dt} & \frac{du_{CS}(t)}{dt} & \\ \frac{du_{Cr}(t)}{dt} & \frac{di_{LF}(t)}{dt} & \frac{di_{LM}(t)}{dt} & \frac{di_{Lr}(t)}{dt} \end{bmatrix}^T. \tag{14}$$

In (12), the matrices A, B and state vector $U(t)$ are given in (15), shown at the bottom of the page, (16), and (17), respectively

$$B = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{1}{L_F} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_{re}} \end{bmatrix}^T \tag{16}$$

$$U(t) = \begin{bmatrix} V_{\text{in}} & V_{\text{out}} \end{bmatrix}^T \tag{17}$$

where matrix A varies according to the operation modes.

From (17), for the fixed input voltage V_{in} and output voltage V_{out}, the state vector $U(t)$ is independent of time. So, the state vector $U(t)$ can be replaced by the matrix U, which is

$$U = U(t) = \begin{bmatrix} V_{\text{in}} & V_{\text{out}} \end{bmatrix}^T. \tag{18}$$

Substituting (18) into (12), the state-space equation of the equivalent circuit is

$$\dot{X}(t) = AX(t) + BU. \tag{19}$$

$$A = \begin{bmatrix} -\frac{1}{C_F \cdot r_{Q1}} & 0 & 0 & 0 & \frac{1}{C_F} & -\frac{1}{C_F} & -\frac{1}{C_F \cdot N} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_M} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_S \cdot N} \\ 0 & 0 & 0 & -\frac{1}{C_r \cdot r_{Q2}} & 0 & 0 & \frac{1}{C_r} \\ -\frac{1}{L_F} & 0 & 0 & 0 & -\frac{r_F}{L_F} & 0 & 0 \\ \frac{1}{L_M} & -\frac{1}{L_M} & 0 & 0 & 0 & -\frac{r_M}{L_M} & 0 \\ \frac{1}{L_{re} \cdot N} & 0 & -\frac{1}{L_{re} \cdot N} & -\frac{1}{L_{re}} & 0 & 0 & -\frac{1}{L_{re}} \cdot \left(\frac{r_p}{N^2} + r_s\right) \end{bmatrix} \tag{15}$$

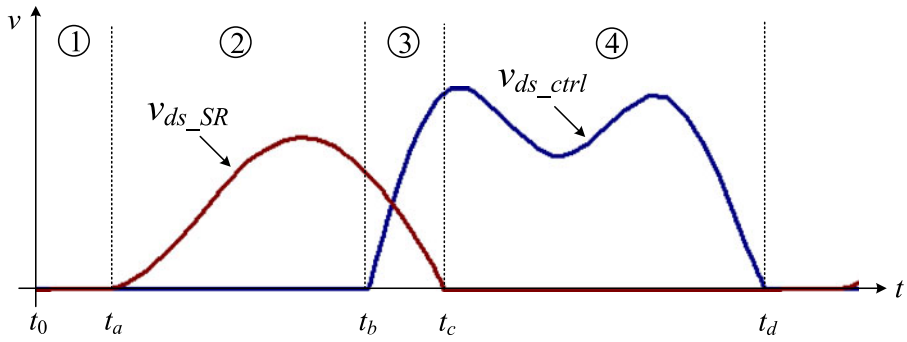


Fig. 9. Drain-to-source voltage waveforms of the control FET and SR FET.

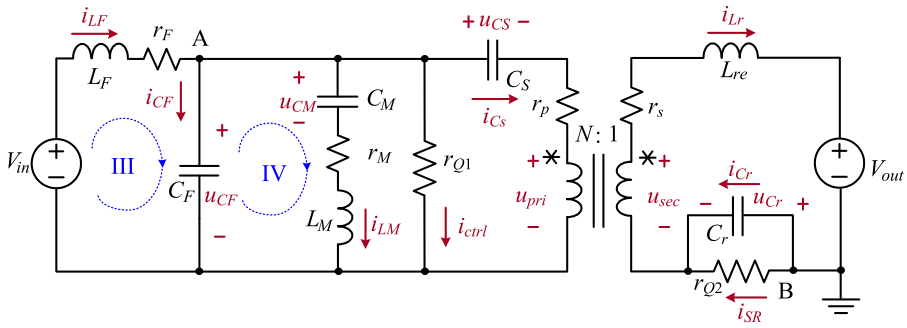


Fig. 10. Simplified equivalent circuit.

2) Interval Calculation of Operation Modes: The general solution to the state-space equation of (19) is

$$X(t) = X_n(t) + X_f(t). \tag{20}$$

Function $X_n(t)$ is the natural response matrix, or the zero-input response matrix, and is equal to

$$X_n(t) = e^{At} \cdot X(0) \tag{21}$$

where e is the matrix exponential function. $X(0)$ is the initial condition matrix.

Function $X_f(t)$ is the forced response matrix, or the zero-state response matrix, and is equal to

$$X_f(t) = \int_0^{\tau} e^{A(t-\tau)} \cdot B \cdot U d\tau = A^{-1} \cdot \left(e^{At} - \mathrm{I}\right) \cdot B \cdot U \tag{22}$$

where I is the 7×7 unit matrix.

Substituting (22) and (21) into (20), (23) is derived

$$X(t) = e^{At} \cdot X(0) + A^{-1} \cdot \left(e^{At} - \mathrm{I}\right) \cdot B \cdot U. \tag{23}$$

The converter has four operation modes. The initial conditions are determined by applying the continuity conditions of the voltage across C_F, C_M, C_S, and C_r and the current of L_F, L_M, and L_r when the converter switched from one mode to the next. So, the initial conditions of all variables in the four operation modes are obtained as follows:

$$X_{①}(0) = X_{④}(t_d - t_c) \tag{24}$$

$$X_{②}(0) = X_{①}(t_a - t_0) \tag{25}$$

$$X_{③}(0) = X_{②}(t_b - t_a) \tag{26}$$

$$X_{④}(0) = X_{③}(t_c - t_b). \tag{27}$$

By substituting $t = t_d - t_c$ into (23), the final condition of all variables in Mode ④ can be calculated, which is given in (28). Similarly, the final condition in other three modes can be calculated when the final instant of each mode is substituted into (23), which are given in (29), (30), and (31), respectively

$$X_{④}(t_d - t_c) = e^{A_{④} \cdot (t_d - t_c)} \cdot X_{④}(0) + A_{④}^{-1} \cdot \left(e_{④}^{A} \cdot (t_d - t_c) - \mathrm{I}\right) \cdot B \cdot U \tag{28}$$

$$X_{①}(t_a - t_0) = e^{A_{①} \cdot (t_a - t_0)} \cdot X_{①}(0) + A_{①}^{-1} \cdot \left(e_{①}^{A} \cdot (t_a - t_0) - \mathrm{I}\right) \cdot B \cdot U \tag{29}$$

$$X_{②}(t_b - t_a) = e^{A_{②} \cdot (t_b - t_a)} \cdot X_{②}(0) + A_{②}^{-1} \cdot \left(e_{②}^{A} \cdot (t_b - t_a) - \mathrm{I}\right) \cdot B \cdot U \tag{30}$$

$$X_{③}(t_c - t_b) = e^{A_{③} \cdot (t_c - t_b)} \cdot X_{③}(0) + A_{③}^{-1} \cdot \left(e_{③}^{A} \cdot (t_c - t_b) - \mathrm{I}\right) \cdot B \cdot U \tag{31}$$

where $A_{①}$, $A_{②}$, $A_{③}$, and $A_{④}$ represent the matrix *A* in different operation modes.

By substituting (28) into (24), (29) into (25), (30) into (26), and (31) into (27), respectively, the initial conditions *X*(0) of all variables in the four modes are calculated as (32), shown at the bottom of the page.

As shown in Fig. 9, for the converter with the designed input voltage $V_{\rm in}$ and output voltage $V_{\rm out}$, the optimal ZVS turn-on of the control FET without the body diode conduction happens at $t = t_0$ in Mode ①. Moreover, the optimal ZVS condition of the SR occurs at $t = t_c$ in Mode ④ and the ZCS condition of the SR occurs at $t = t_a$ in Mode ②. These constrains are

$$v_{ds\_ctrl}\left(t_0\right) = 0 \rightarrow X_{①1}\left(0\right) = u_{CF}(t_0) = 0 \quad (33)$$

$$v_{ds\_SR}\left(t_c\right) = 0 \rightarrow X_{④4}\left(0\right) = u_{Cr}(t_c) = 0 \quad (34)$$

$$i_{Lr}\left(t_a\right) = 0 \rightarrow X_{②7}\left(0\right) = 0 \quad (35)$$

where $X_{①1}(0)$ represents the initial value of the first variable of *X*(*t*) in Mode ①, $X_{④4}(0)$ is the initial value of the fourth variable of *X*(*t*) in Mode ④, and $X_{②7}(0)$ is the initial value of the seventh variable of *X*(*t*) in Mode ②. From (33)–(35), combined with t_d–$t_0 = T_s$, the time interval of each mode can be calculated based on the parameters of the converter.

3) Proving Drive Voltage Matches With Drain Voltage Over a Wide Voltage Range: As shown in Fig. 7, the operation modes are determined by the drive voltage of the power FETs. With the fixed drive signals, the four modes can be determined and the interval of each mode remains fixed. That means t_a–t_0, t_b–t_a, t_c–t_b, and t_d–t_c are fixed with the controlled drive signals. Moreover, from (15) and (16), it is noted that *A* and *B* are the matrices consisting of the component parameters of the converter inherently and do not depend on $V_{\rm in}$ and $V_{\rm out}$. Therefore, for the specific parameters, matrices *A* and *B* are constant. Similar to (32), when the input voltage varies to $V_{\rm ink}$ and output voltage varies to $V_{\rm outk}$, the input matrix $U_k = [V_{\rm ink}, V_{\rm outk}]^T$ and the initial conditions $X_k(0)$ of all variables for the designed converter is (36), shown at the bottom of next page.

Assume that the output voltage varies proportionally according to the input voltage. Based on this assumption, $V_{\rm ink} = kV_{\rm in}, V_{\rm outk} = kV_{\rm out}$ and the input matrix $U_k = kU$, where *k* is a proportional coefficient. By substituting $U_k = kU$ into (36), (37) is derived at the bottom of the next page.

Note from (32) and (37), the difference between (32) and (37) is only the coefficient *k*. So, (38) is obtained

$$X_k\left(0\right) = kX\left(0\right). \quad (38)$$

By substituting (33)–(35) into (38), respectively, (39)–(41) are obtained

$$X_{k①1}\left(0\right) = kX_{①1}\left(0\right) = 0 \quad (39)$$

$$X_{k④4}\left(0\right) = kX_{④4}\left(0\right) = 0 \quad (40)$$

$$X_{k②7}\left(0\right) = kX_{②7}\left(0\right) = 0 \quad (41)$$

where $X_{k①1}(0)$ represents the initial value of the first variable of *X*(*t*) in Mode ①, $X_{k④4}(0)$ is the initial value of the fourth variable of *X*(*t*) in Mode ④ and $X_{k②7}(0)$ is the initial value of the seventh variable of *X*(*t*) in Mode ② with the input voltage of $kV_{\rm in}$ and the output voltage of $kV_{\rm out}$.

From (39), (42) is obtained. From (40), (43) is obtained. Similarly, (44) is obtained from (41)

$$v_{ds\_ctrlk}\left(t_0\right) = u_{CFk}(t_0) = X_{k①1}\left(0\right) = 0 \quad (42)$$

$$v_{ds\_SRk}\left(t_c\right) = -u_{Crk}(t_c) = -X_{k④4}\left(0\right) = 0 \quad (43)$$

$$i_{Lrk}\left(t_a\right) = X_{k②7}\left(0\right) = 0 \quad (44)$$

where $v_{ds\_ctrlk}(t_0)$ is the drain voltage value of the control FET at $t = t_0, v_{ds\_SRk}(t_c)$ is the drain voltage value of the SR at $t = t_c, i_{Lrk}(t_a)$ is the current value of the inductor L_r at $t = t_a$, and $u_{\rm CFk}$ and $u_{\rm Crk}$ are the voltage of the capacitances C_F and C_r, respectively, with the input voltage $kV_{\rm in}$ and output voltage $kV_{\rm out}$.

According to Fig. 9, (42) indicates that the optimal ZVS turn-on of the control FET is obtained at $t = t_0$. Equation (43) indicates that the optimal ZVS condition of the SR is obtained at $t = t_c$. Equation (44) indicates that ZCS condition of the SR occurs at $t = t_a$. So, with the fixed drive signals, the gate drive voltage can always match well with the drain voltage of the power FETs over a wide input voltage range when the output voltage follows the input voltage proportionally.

$$\begin{bmatrix} X_{①}\left(0\right) \\ X_{②}\left(0\right) \\ X_{③}\left(0\right) \\ X_{④}\left(0\right) \end{bmatrix} = \begin{bmatrix} -e^{A_{①}\cdot(t_a-t_0)} & \mathrm{I} & 0 & 0 \\ 0 & -e^{A_{②}\cdot(t_b-t_a)} & \mathrm{I} & 0 \\ 0 & 0 & -e^{A_{③}\cdot(t_c-t_b)} & \mathrm{I} \\ \mathrm{I} & 0 & 0 & -e^{A_{④}\cdot(t_d-t_c)} \end{bmatrix}^{-1} \cdot \begin{bmatrix} A_{①}^{-1}\cdot\left(e^{A_{①}\cdot(t_a-t_0)}-\mathrm{I}\right) \\ A_{②}^{-1}\cdot\left(e^{A_{②}\cdot(t_b-t_a)}-\mathrm{I}\right) \\ A_{③}^{-1}\cdot\left(e^{A_{③}\cdot(t_c-t_b)}-\mathrm{I}\right) \\ A_{④}^{-1}\cdot\left(e^{A_{④}\cdot(t_d-t_c)}-\mathrm{I}\right) \end{bmatrix} \cdot B \cdot U \quad (32)$$

$$\begin{bmatrix} X_{k①}\left(0\right) \\ X_{k②}\left(0\right) \\ X_{k③}\left(0\right) \\ X_{k④}\left(0\right) \end{bmatrix} = \begin{bmatrix} -e^{A_{①}\cdot(t_a-t_0)} & \mathrm{I} & 0 & 0 \\ 0 & -e^{A_{②}\cdot(t_b-t_a)} & \mathrm{I} & 0 \\ 0 & 0 & -e^{A_{③}\cdot(t_c-t_b)} & \mathrm{I} \\ \mathrm{I} & 0 & 0 & -e^{A_{④}\cdot(t_d-t_c)} \end{bmatrix}^{-1} \cdot \begin{bmatrix} A_{①}^{-1}\cdot\left(e^{A_{①}\cdot(t_a-t_0)}-\mathrm{I}\right) \\ A_{②}^{-1}\cdot\left(e^{A_{②}\cdot(t_b-t_a)}-\mathrm{I}\right) \\ A_{③}^{-1}\cdot\left(e^{A_{③}\cdot(t_c-t_b)}-\mathrm{I}\right) \\ A_{④}^{-1}\cdot\left(e^{A_{④}\cdot(t_d-t_c)}-\mathrm{I}\right) \end{bmatrix} \cdot B \cdot U_k \quad (36)$$

IV. Proposed Voltage Following Control

A. Proposed Voltage Following Control

The conventional hysteresis control and proposed voltage following control are given in Fig. 11. In Fig. 11(a), with the conventional hysteresis control, the output voltage $V_{\rm out}$ falls to the lower limit V_L at t_{M0} so that the control signal $v_{\rm ctrl}$ sets high to turn on the converter. Observed from the gate drive voltage v_{gs}, the converter operates at fixed switching frequency f_s when the converter is ON and the modulation frequency f_M is much lower than the switching frequency f_s. $V_{\rm out}$ keeps increasing until it reaches the upper limit V_H. At $t = t_{M1}, v_{\rm ctrl}$ sets low to shut down the converter. During the time $[t_{M1}, t_{M2}]$, there is no power delivered in the converter and $V_{\rm out}$ keeps decreasing till the next modulation cycle. In Fig. 11(b), with the voltage following control, the reference voltage $V_{\rm ref}$ follows the input voltage proportionally, which leads to the lower limit of the output voltage V_L varies proportionally according to the input voltage. So, the output voltage can follow the input voltage proportionally if the ripple of the output voltage is not taken into consideration.

Fig. 12 shows structure diagram of the proposed voltage following control. The proposed control strategy is based on the voltage proportional module and hysteresis control. With the voltage proportional module, the reference voltage $V_{\rm ref}$ follows the input voltage proportionally. In addition, the isolation of $V_{\rm in}$ and $V_{\rm ref}$ is realized. With the hysteresis control, the output voltage follows $V_{\rm ref}$ proportionally. So, the function that the output voltage follows the input voltage proportionally can be realized. In Fig. 12, a digital isolator is used to realize the isolation of the control signal and a time delay module is used to create the same delay time as the digital isolator. CON1 and CON2 represent the drive signals of the control FET and the SR FET, respectively

Although the output voltage can follow the input voltage proportionally when the converter operates in the open-loop status with the rated load, the converter under the open-loop status is not suitable to be used as the DCX directly. In the open-loop status, the change of the load will have an effect on the resonant status of the converter and then the output voltage. Typically, as a DCX, the output voltage should controlled independent with the load condition. Therefore, the closed-loop control needs to be applied to ensure that the output voltage remains stable at the fixed input voltage.

B. Realization of the Proposed Voltage Following Control

With the hysteresis control, the voltage regulation is achieved by comparing the output voltage feedback to the reference voltage $V_{\rm ref}$. The comparator provides the control signal $v_{\rm ctrl}$ to modulate the converter ON and OFF. With this control strategy, the upper limit of the output voltage V_H and the lower limit of the output voltage V_L are

$$V_H = \frac{R_2+R_3}{R_2}\left(\frac{R_4\cdot V_{CH}}{R_4+R_5}+\frac{R_5\cdot V_{ref}}{R_4+R_5}\right)\approx\frac{R_2+R_3}{R_2}\cdot\frac{R_5\cdot V_{ref}}{R_4+R_5} \tag{45}$$

$$V_L = \frac{R_2+R_3}{R_2}\left(\frac{R_4\cdot V_{CL}}{R_4+R_5}+\frac{R_5\cdot V_{ref}}{R_4+R_5}\right)\approx\frac{R_2+R_3}{R_2}\cdot\frac{R_5\cdot V_{ref}}{R_4+R_5} \tag{46}$$

where V_{CH} and V_{CL} represent the high level and low level of the comparator output voltage, respectively, and the value of V_{CL} is close to zero. From (45) and (46), the output voltage is proportional to the reference voltage $V_{\rm ref}$ if the ripple of the output voltage is not taken into consideration. So, in order to control the output voltage to change proportionally with the input voltage, the reference voltage $V_{\rm ref}$ needs to be controlled to follow the input voltage proportionally.

Fig. 13 shows the detailed voltage proportional circuit. It consists of the scaling operation circuit, the liner optical coupling, and the differential amplifier. The functions of this circuit are given as follows: 1) realizing the function that the reference voltage $V_{\rm ref}$ follows the input voltage proportionally; and 2) realizing the isolation of the voltage $V_{\rm in}$ and $V_{\rm ref}$.

Based on the previous analysis, the reference voltage of the hysteresis control follows the input voltage proportionally which leads to the proportional variation of the output voltage with the input voltage. Then, the gate drive voltage can match well with the drain voltage of the power FETs over a wide input voltage range. The hard-switching of the SR FET and the reverse conduction problem of the eGaN HEMTs are minimized.

V. Experimental Verification and Discussion

To verify the functionality of the proposed control, an 18–24 V input, 18-W output, 10-MHz prototype of the DCX is built. Fig. 14 gives the photograph of the prototype. The parameters of the power stage and control stage are given in Tables III and IV, respectively. The air-core inductors from Coilcraft are used as the resonant inductance. EPC2001 from EPC is chosen as thepower FETs. The Tektronix DPO3040 oscilloscope is used in the experiment. The Tektronix P6139Bs are used as the probes and these probes are set in the full bandwidth of 300 MHz.

Fig. 15 shows the measured drain voltage and gate drive voltage waveforms of the SR FET with different input voltage

$$\begin{bmatrix} X_{k①}(0) \\ X_{k②}(0) \\ X_{k③}(0) \\ X_{k④}(0) \end{bmatrix} = \begin{bmatrix} -e^{A_{①}\cdot(t_a-t_0)} & \mathrm{I} & 0 & 0 \\ 0 & -e^{A_{②}\cdot(t_b-t_a)} & \mathrm{I} & 0 \\ 0 & 0 & -e^{A_{③}\cdot(t_c-t_b)} & \mathrm{I} \\ \mathrm{I} & 0 & 0 & -e^{A_{④}\cdot(t_d-t_c)} \end{bmatrix}^{-1} \cdot \begin{bmatrix} A_{①}^{-1}\cdot\left(e^{A_{①}\cdot(t_a-t_0)}-\mathrm{I}\right) \\ A_{②}^{-1}\cdot\left(e^{A_{②}\cdot(t_b-t_a)}-\mathrm{I}\right) \\ A_{③}^{-1}\cdot\left(e^{A_{③}\cdot(t_c-t_b)}-\mathrm{I}\right) \\ A_{④}^{-1}\cdot\left(e^{A_{④}\cdot(t_d-t_c)}-\mathrm{I}\right) \end{bmatrix} \cdot B\cdot k\cdot U \tag{37}$$

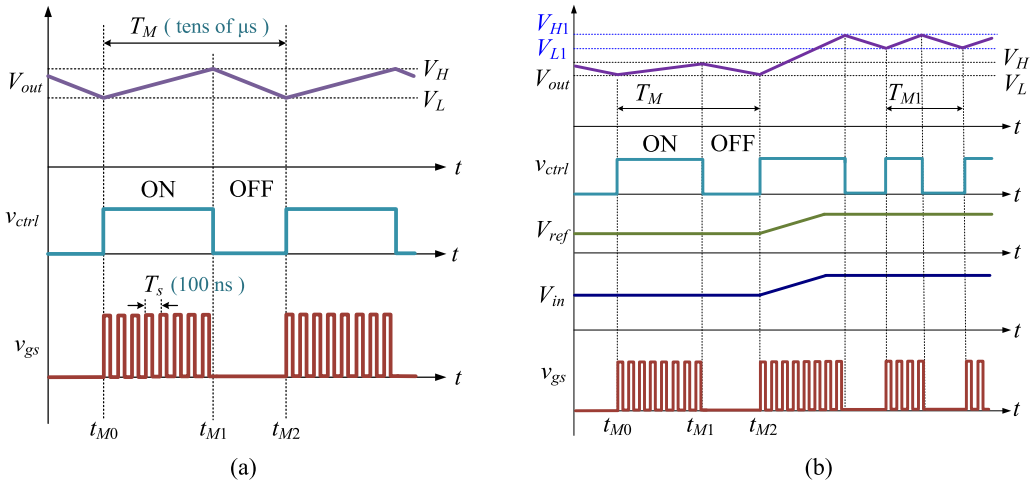


Fig. 11. Key waveforms of different control. (a) Conventional hysteresis control. (b) Proposed voltage following control.

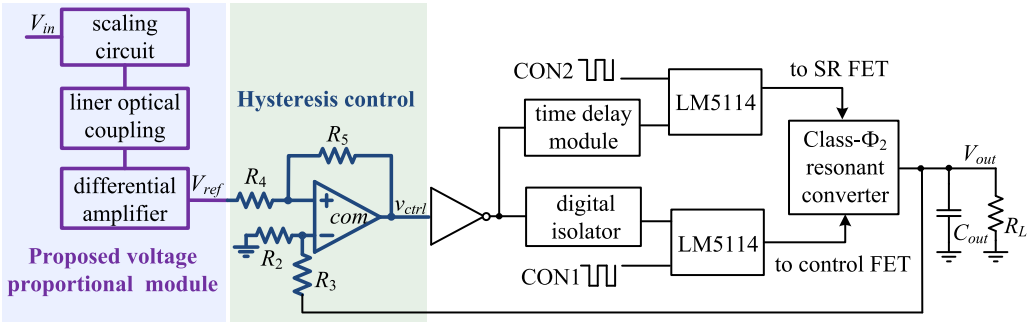


Fig. 12. Structure diagram of the voltage following control.

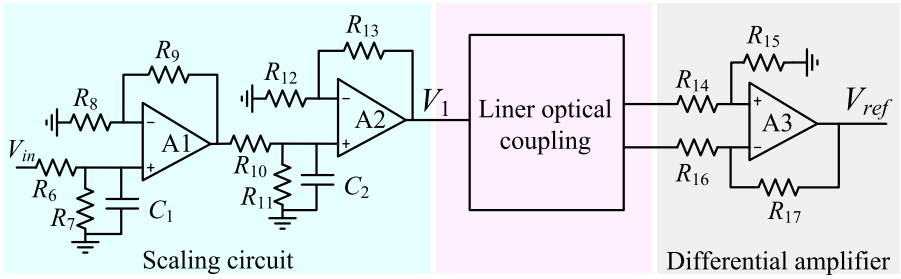


Fig. 13. Detailed voltage proportional circuit.

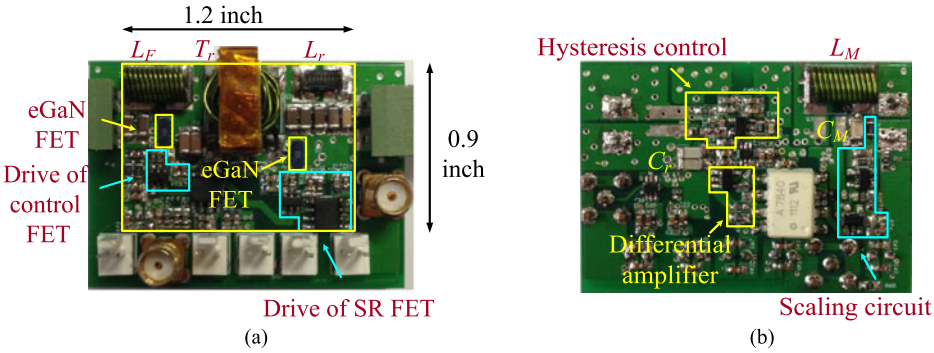


Fig. 14. Photograph of the prototype. (a) Top view. (b) Bottom view.

TABLE III
POWER STAGE COMPONENT VALUES

L_F	2222SQ-221 (Coilcraft)	L_M	2222SQ-221 (Coilcraft)
L_r	A10T(Coilcraft)	C_M	268 pF
C_r	670 pF	C_S	4 μF
C_{in}	94 μF	C_{out}	188 μF
n_1: n_2	4:2	Core	ER 14.5/3/7 (TDG TP5)

TABLE IV
CONTROL STAGE COMPONENT VALUES (KΩ)

R_2	16	R_3	56
R_4	1	R_5	100
R_6, R_8	15	R_7, R_9	1
R_{10}, R_{12}	12	R_{11}, R_{13}	1
R_{14}, R_{16}	7.5	R_{15}, R_{17}	3

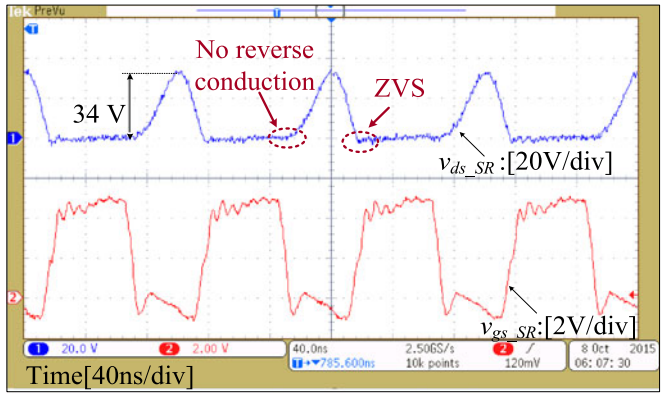
when the voltage following control is used. From Fig. 15(a), it is observed that zero reverse conduction and ZVS of the SR FET can be achieved at 18 V input. In Fig. 15(b) and (c), when the input voltage reaches 20 and 24 V, respectively, the zero reverse conduction and ZVS of the SR FET can still be achieved. The waveforms of the SR FET agree well with the theoretical analysis.

The measured voltage waveforms of the control FET with different input voltage are given in Fig. 16. From Fig. 16(a), it is observed that the reverse conduction time of the control eGaN HEMT is nearly zero when the input voltage is 18 V. In Fig. 16(b) and (c), when the input voltage increases to 20 and 24 V, respectively, the reverse conduction time of the control eGaN HEMT is still close to zero. From Fig. 16, it is noticed that the drive voltage matches well with the drain voltage of the control FET over a wide input voltage range.

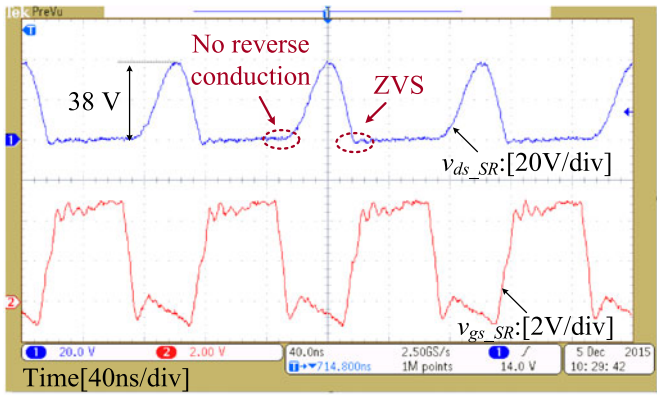
Fig. 17 gives the closed-loop efficiency with the input voltage of 18 and 24 V. The peak efficiency is 86.9% at full load when the input voltage is 18 V. It is observed that as the output current decreases from 2 to 0.25 A, the efficiency decreases from 86.9% to 85% (with the output current of 0.75 A) and then increase to 86.6% at 18 V input. Similarly, as the output current decreases from 2 to 0.25 A at 24 V input, the efficiency decreases from 86.3% to 85.2% (with the output current of 1 A) and then increase to 86.7%.

Fig. 18 gives the closed-loop efficiency of the converter with different output power. In Fig. 18(a), it is noted that as output power decreases from 18 to 12 W, the efficiency decreases from 86.9% to 86.2% at 18 V input and decreases from 85.5% to 85.2% at 24 V input. In Fig. 18(b), as the output power decreases from 9 to 3 W, the efficiency increases from 85.5% to 86.7% at 24 V input. The reason for this phenomenon is that the modulation frequency of the voltage following control varies depending on the output power.

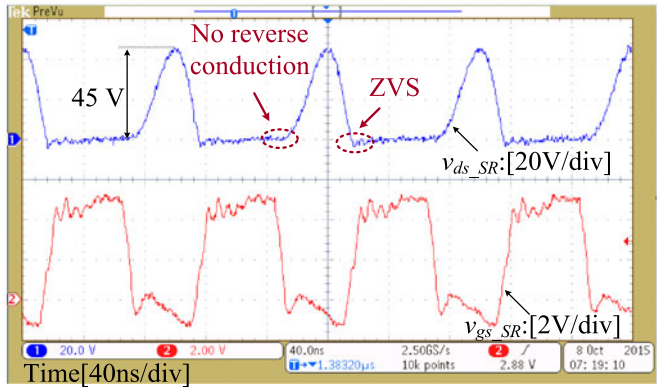
Fig. 19 gives the efficiency comparison when the output power of the converter is 18 W. In Fig. 19, the modeling calculation efficiency at 18 V input is 87.4% and the efficiency



(a)



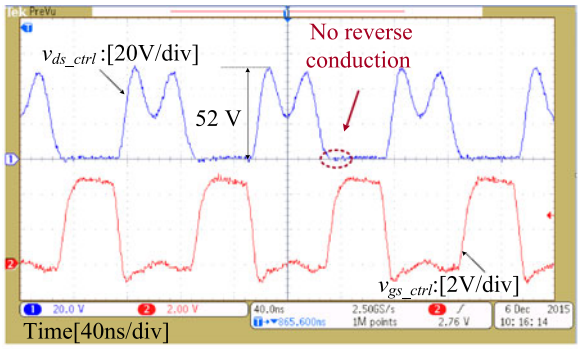
(b)



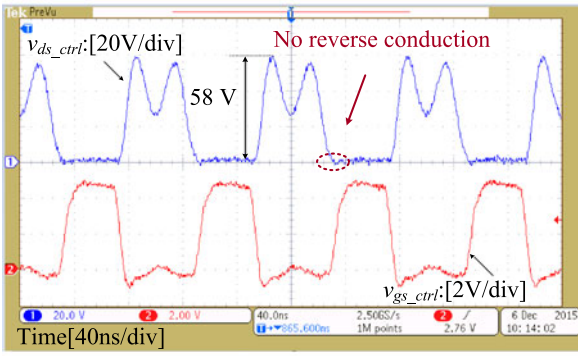
(c)

Fig. 15. Measured waveforms of the SR FET with different input voltage: $P_o = 18$ W and $f_s = 10$ MHz. (a) $V_{\text{in}} = 18$ V. (b) $V_{\text{in}} = 20$ V. (c) $V_{\text{in}} = 24$ V.

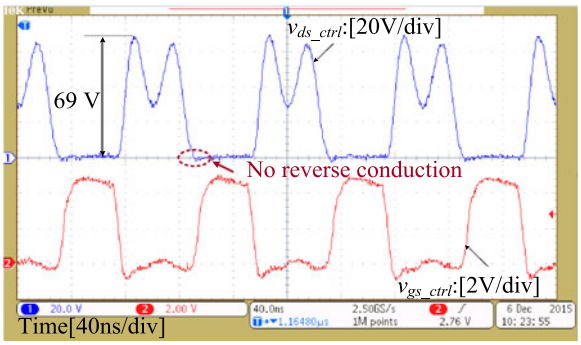
decreases to 86.3% when the input voltage reaches 24 V. When the voltage following control is used, the measured efficiency at 18 V input is 86.9% and it decreases to 85.5% at 24 V input. Compared to the conventional hysteresis control, the proposed voltage following control achieves significant efficiency improvement over a wide voltage input range. In Fig. 19, it is observed that the efficiency is 79.9% at 24 V input with the conventional hysteresis control. It increases to 85.5% as the voltage following control is applied. The efficiency improvement is 5.6% for the reason that the zero reverse conduction of the power FETs and ZVS of the SR FET are achieved.



(a)



(b)



(c)

Fig. 16. Measured waveforms of the control FET with different input voltage: $P_o = 18$ W and $f_s = 10$ MHz. (a) $V_{\text{in}} = 18$ V. (b) $V_{\text{in}} = 20$ V. (c) $V_{\text{in}} = 24$ V.

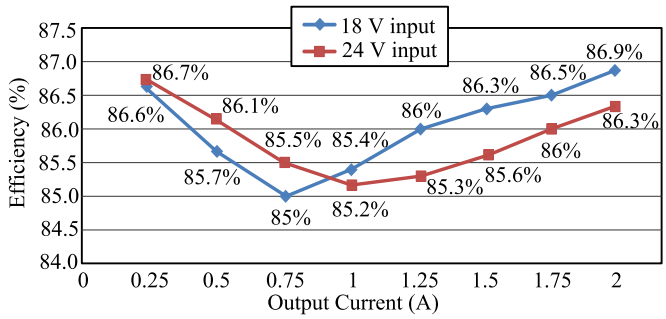


Fig. 17. Closed-loop efficiency (the gate drive loss included) at 18 and 24 V input.

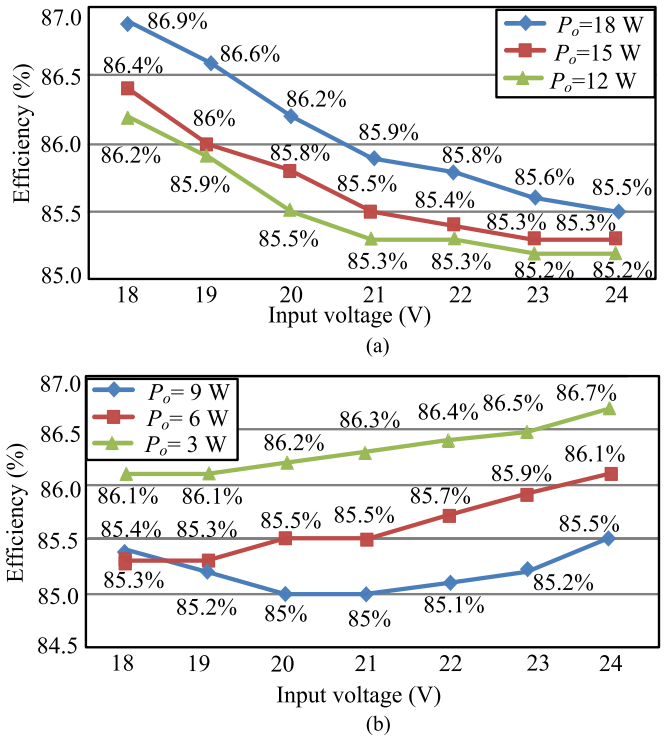


Fig. 18. Closed-loop efficiency (the gate drive loss included) with different output power. (a) $P_o > 9$ W. (b) $P_o < 9$ W.

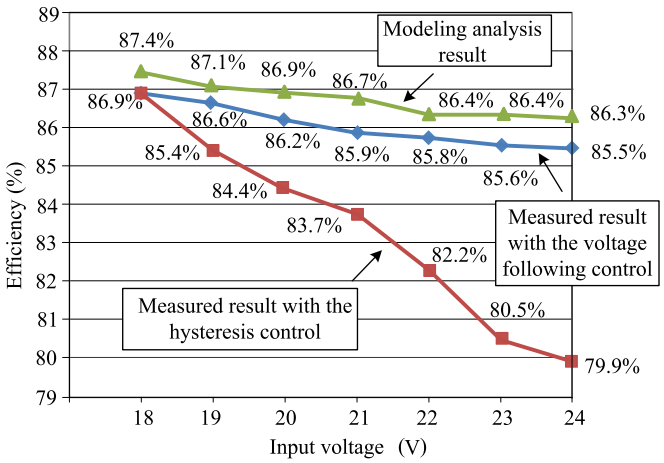


Fig. 19. Closed-loop efficiency comparison (the gate drive loss included): $P_o = 18$ W.

VI. Conclusion

For the isolated class-Φ_2 converter with the conventional hysteresis control, the gate drive voltage can hardly match efficiently with the drain voltage of the power FETs with the variation of the input voltage. It results in high reverse conduction loss and switching loss seriously at high frequency, especially for the eGaN HEMTs due to the reverse conduction mechanism. The state-space method is used to prove that the gate drive voltage matches well with the drain-to-source voltage of the power FETs over a wide input voltage range when the output voltage

follows the input voltage proportionally. The voltage following control is proposed and the output voltage follows the input voltage proportionally. The gate drive voltage matches well with the drain voltage of the power FETs over a wide input voltage range. ZVS of the SR FET can be achieved and the reverse conduction loss of the power FETs is minimized. Moreover, the main idea of the proposed voltage following control can be extended to other high frequency-isolated resonant converters, and the output power of the DCX can be designed from tens of watts to hundreds of watts according to the applications. An 18–24 V input, 18-W/2 A output, 10-MHz prototype of DCX is built to verify the functionality and benefits of the proposed control strategy. The efficiency is improved from 79.9% to 85.5% (an improvement of 5.6%) at 18 W output and 24 V input.

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