98.1%-Efficiency Hysteretic-Current-Mode Noninverting Buck–Boost DC-DC Converter With Smooth Mode Transition

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***Abstract*—A noninverting buck–boost dc–dc converter can work in buck, boost, or buck–boost mode. Hence, it provides a good solution when the input voltage may be higher or lower than the output voltage. However, a buck–boost converter requires four power transistors, rather than two. Therefore, its efficiency decreases, due to the conduction and switching losses of the two extra power transistors. Another issue of a buck–boost converter is how to smoothly switch its operational mode, when its input voltage approaches its output voltage. A hysteretic-current-mode noninverting buck–boost converter with high efficiency and smooth mode transition is proposed, and it was designed and fabricated using TSMC 0.35-μm CMOS 2P4 M 3.3 V/5V mixed-signal polycide process. The input voltage may range from 2.5 to 5 V, the output voltage is 3.3 V, and the maximal load current is 400 mA. According to the measured results, the maximal efficiency reaches 98.1%, and the efficiencies measured in the entire input voltage and loading ranges are all above 80%.**

***Index Terms*—Buck–boost, efficiency, hysteretic-current-mode (HCM), mode transition, switching regulator.**

I. Introduction

MANY portable devices have been introduced to the market in the past few decades, and these battery-powered devices, such as laptops and smartphones, provide more and more functions. However, the battery capacity did not grow as fast as the number of functions provided by these devices, so the operation time of portable devices decreases significantly with their increasing functions. Hence, development of efficient power management chips for extending the operation time of portable devices has drawn more and more attentions.

A Li-ion battery is the most popular battery for portable devices. In fact, because the output voltage of a Li-ion battery may gradually decrease with time (i.e., approximately from 4.2 to 2.7 V), it could be higher or lower than the required 3.3-V voltage, for example. This problem could be solved by using a noninverting buck–boost dc–dc converter [1], as illustrated in Fig. 1. However, there are four power switches in a noninverting buck–boost converter, while there are only two switches in a buck or boost converter. More power switches imply more conversion and switching losses. Hence, how to increase the conversion efficiency of buck–boost converters is an important topic.

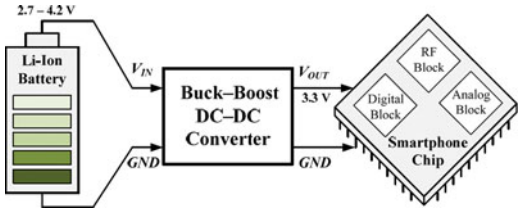

Fig. 1. Illustration of a buck–boost dc–dc converter applied on mobile applications.

Many control methods have been proposed for buck–boost converters [2]–[9]. For example, the converter in [4] works only in the buck–boost mode, so its maximal efficiency is only 72%. In [5], the converter can work in the buck, boost, or buck–boost mode, according to the relationship between its input and output voltages. Its maximal efficiency can reach 91.6%, but the efficiency in the buck–boost mode is the worst, as low as 34%, occurring when the input voltage approximates the output voltage. The converter in [6] works in either the buck or boost mode, but not the buck–boost mode, and its maximal efficiency is 92%, occurring when the input voltage is close to the output voltage. It adopts average-current-mode control, but its dual-loop control circuits require two sets of compensators (one of the compensators needs external components), which increases the cost and design complexity. In [7], the converter also works in the buck or boost mode only, where its mode selection is determined mainly by the relationship between the input and output voltages and partially by its duty cycle. Besides, both the pulse-width-modulation (PWM) and pulse-frequency-modulation (PFM) controls are included for achieving better efficiency over the entire loading range. Moreover, it also has control circuits to deal with the operation in the discontinuous conduction mode (DCM), in addition to the continuous conduction mode (CCM). As a result, its maximal efficiency can be boosted to 95% with the price of complicated mode selector and control circuits, i.e., higher cost and design complexity. The

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converter in [8] has four operational modes—buck, boost, and two buck–boost modes, and its mode selection also depends on the relationship between the input and output voltage. In those two buck–boost modes, its switching frequency is equivalently halved to reduce switching loss, and its maximal efficiency is 96%. Similarly, relatively complicated mode selector, control circuits, and external compensation components are required.

In addition to PWM and PFM, ripple-based controls have also been used in converters for decades, and it can be categorized into three different types—hysteretic control, constant on-/off-time control, and constant-frequency peak-/valley-voltage control [10]–[16]. Among them, the hysteretic-voltage control method has the highest efficiency and the lowest cost (i.e., no compensators and simple control circuit) [10]. However, it can only be applied to buck converters, and one main disadvantage is its poor line and load regulations. Its regulation issue can be improved by adopting compensators, which seems to sacrifice its advantage of low cost though. In fact, for an integrated power management chip, the cost of adding an opamp is negligible, but the cost of using external resistors and capacitors for the compensator is significant. For example, the area of the built-in compensator in this study, including an opamp, a resistor, a capacitor, and its capacitor multiplier circuit, is only 0.09 mm^2, which is around 2% of the total chip area. Notably, if a real on-chip capacitor is implemented without the capacitor multiplier circuit, the area is significantly increased to 0.25 mm^2. Hence, it is a trend to use fully built-in compensators for improving line/load regulations. Moreover, the hysteretic-voltage control cannot be applied to boost converters, because their output voltage and inductor current are out of phase. Instead, hysteretic-current control method with built-in compensators is typically used in boost converters. Nevertheless, it is difficult to apply the hysteretic-current control method to noninverting buck–boost converters, due to the issue of mode transition. The characteristics of the buck- and boost-mode operations are different, so their corresponding compensators and hysteretic-current control circuits are supposed to be different [17]. When the input voltage approaches the output voltage, the converter may keep jumping between the two sets of control circuits. However, each time to switch control circuit actually means a transient response, so the output voltage of the converter may oscillate [8], [18], [19]. The details will be further explained in Section II.

In this study, a hysteretic-current-mode (HCM) control method is proposed for noninverting buck–boost dc–dc converters to solve this issue, and its small-signal model is also analyzed. It is worth to mention that the operations of buck and boost modes in this study share the same set of control circuit, and smooth mode transition is achieved. Moreover, the operational mode is automatically determined by the HCM method, not depending on the relationship between the input and output voltage. Furthermore, it has a built-in compensator, and no external compensation components are required. The following sections are organized as follows. Section II describes the issue of mode transition, the block diagram of the proposed HCM noninverting buck–boost converter, and why the HCM method can improve efficiency. Section III analyzes the small-signal model of the proposed HCM buck–boost converter and shows the circuit implementation of its important blocks. Finally, the measured results are shown in Section IV, and a conclusion is given in Section V.

II. Proposed HCM Control Method

A. Mode Transition Issue

Because of the parasitic resistance of the inductor and power transistors, it cannot decide to work in the buck or boost mode by just comparing the input voltage V_{IN} with the output voltage V_{OUT}. Instead, it should compare ($V_{IN} - V_{PAR}$) with V_{OUT}, where V_{PAR} is the sum of voltage drops across those parasitic resistors. However, it is difficult to know the value of V_{PAR} exactly. Moreover, due to the delay time of the circuits, it is practically difficult to generate a duty ratio around 0–5% or 95–100%. Hence, the discontinuity in the extremely low and high duty-ratio ranges may result in larger output voltage ripples during this transition region (i.e., $V_{IN} \doteqdot V_{OUT}$) [18], [19]. To solve this issue, some work adds the buck–boost mode to deal with this transition region, but the efficiency in this mode is the worst among the three modes [2], [5]. Another method is to further divide this transition region into two submodes: fix the duty ratio of the buck (or boost) mode at 90% (or 10%) and modulate the duty ratio of the boost (or buck) mode according to V_{OUT} [8], but extra comparators and control circuits are required. In this study, a better control method is proposed. In fact, if ($V_{IN} - V_{PAR}$) is larger than V_{OUT}, the inductor current will increase when V_{IN} is connected to V_{OUT} through the inductor, which is defined as the initial phase in this study; otherwise, it will decrease in the initial phase. Therefore, the operational mode can be determined by the inductor current, rather than the relationship between V_{IN} and V_{OUT}. By using the proposed HCM method, there are still two operational modes only, and the efficiency achieves its maximum when V_{IN} approaches V_{OUT}. The detailed analysis will be derived later.

B. Block Diagram and Fundamentals of the Proposed HCM Noninverting Buck–Boost Converter

Fig. 2 shows the block diagram of the proposed HCM converter, where all the control circuits and the four power transistors are implemented into the chip. A proportional-integral (PI) compensator is adopted, and it compares the feedback signal V_{FB} with a reference voltage V_{REF}, and sends a control signal V_C to the hysteretic current controller. According to V_C, the hysteretic window circuit generates three corresponding boundary voltages (V_{IT}, V_{IM}, and V_{IB}) to form two hysteretic windows: V_{IB} is the lowest voltage among these three voltages, while V_{IT} is the highest one. The inductor current I_L is sensed and converted to a voltage signal V_S, which is then compared with V_{IT}, V_{IM}, and V_{IB} in the hysteretic current logic block to determine the operational mode. Then, its output signals are sent to the adaptive dead-time and gate driving circuits to generate the switching signals of the four power transistors. Moreover, to increase the efficiency at light load, zero-current detector (ZCD) and DCM controller, antiringing circuits, and adaptive

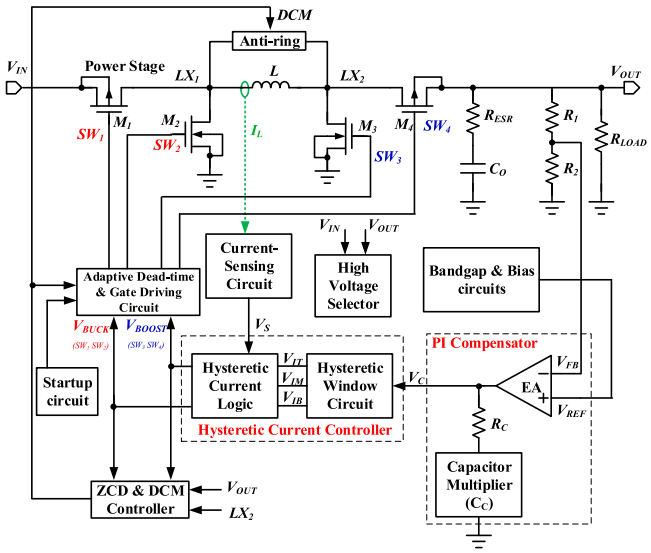

Fig. 2. System architecture of the proposed HCM buck–boost converter.

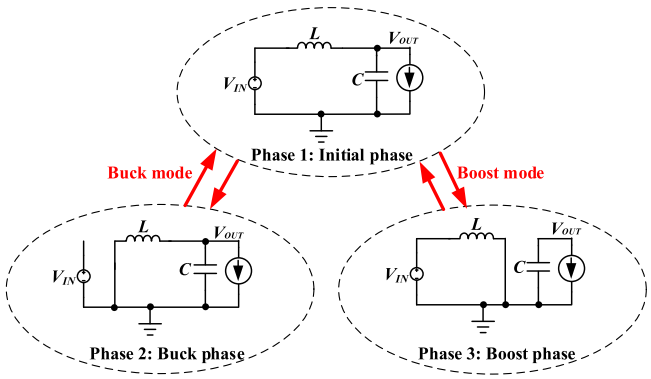

Fig. 3. Three phases of a noninverting buck–boost power stage.

dead-time circuits are also included. The ZCD is used to detect if the inductor current is reversed. If so, the DCM controller will turn OFF the corresponding power transistor to make the converter work in DCM. Furthermore, to avoid the oscillation between the inductor and capacitor in the power stage, the two terminals of the inductor would be shorted in DCM.

The power stage of the noninverting buck–boost converter has three different phases, as shown in Fig. 3. Phase 1 is called the initial phase, during which power transistors M_1 and M_4 are turned ON, and M_2 and M_3 are turned OFF. Phase 2 is called the buck phase, during which power transistors M_2 and M_4 are turned ON, and M_1 and M_3 are turned OFF. Similarly, Phase 3 is the boost phase, during which power transistors M_1 and M_3 are turned ON, and M_2 and M_4 are turned OFF. When the converter works in the buck mode, the power stage switches between Phases 1 and 2. When it works in the boost mode, it switches between Phases 1 and 3 instead. Notably, both V_S and I_L always decrease in the buck phase, while they increase in the boost phase. However, in the initial phase, I_L and V_S may increase or decrease, depending on whether (V_{IN}–V_{PAR}) is larger than V_{OUT} or not. If the inductor current increases in the initial phase, it

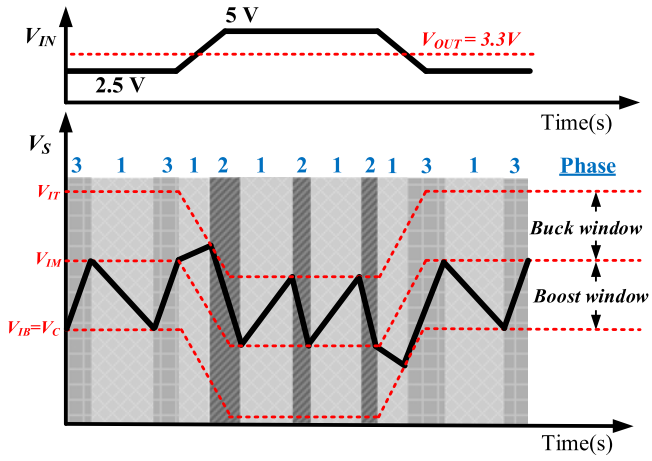

Fig. 4. Related waveforms of some important HCM signals.

should works in the buck mode, which means V_S stays between V_{IT} and V_{IM}. On the contrary, if the inductor current decreases in the initial phase, it should work in the boost mode, which means V_S is between V_{IM} and V_{IB}. Fig. 4 draws the related waveforms of the signals mentioned above. Notably, for a given load current, the hysteretic window will shift downward when V_{IN} increases, and the details will be further explained later.

C. Efficiency in the Transition Region

The efficiency of a converter is usually dominated by conduction loss and switching loss. If the buck–boost mode is inserted, the worst efficiency typically occurs when V_{IN} approaches V_{OUT}, because the conduction loss reaches its maximums at this time [2], [5]. The relationships between the average inductor current $I_{L(\mathrm{AVG})}$ and the load current I_{LOAD} in the buck, boost, and buck–boost modes can be expressed as [6]

$$\text{Buck}: \quad I_{L(\mathrm{AVG})} = I_{\mathrm{LOAD}} \tag{1a}$$

$$\text{Boost}: \quad I_{L(\mathrm{AVG})} = \frac{I_{\mathrm{LOAD}}}{1 - D_{\mathrm{BT}}} \tag{1b}$$

$$\text{Buck} - \text{Boost}: \quad I_{L(\mathrm{AVG})} = \frac{I_{\mathrm{LOAD}}}{1 - D_{\mathrm{BB}}} \tag{1c}$$

where $D_{\mathrm{BK}}, D_{\mathrm{BT}}$, and D_{BB} are the duty ratios in the buck, boost, and buck–boost mode, respectively. When V_{IN} approaches V_{OUT}, $D_{\mathrm{BK}}, D_{\mathrm{BT}}$, and D_{BB} approaches to 1, 0, and 0.5, respectively. It means that $I_{L(\mathrm{AVG})}$ is the same as I_{LOAD} in the buck and boost modes when $V_{\mathrm{IN}} = V_{\mathrm{OUT}}$, but $I_{L(\mathrm{AVG})}$ is twice of I_{LOAD} in the buck–boost mode. In other words, excluding the buck–boost mode is a good way to enhance efficiency.

Moreover, when D_{BK} (or D_{BT}) approaches 1 (or 0), the converter stays in the initial phase most of time. In the initial phase, the instantaneous inductor current $i_L(t)$ and its changing rate $\mathrm{d}i_L(t)/\mathrm{d}t$ can be expressed as

$$\frac{di_L(t)}{dt} = \frac{(V_{\mathrm{IN}} - V_{\mathrm{PAR}}) - V_{\mathrm{OUT}}}{L} \tag{2a}$$

$$i_L(t) = \frac{1}{L}\int [(V_{\mathrm{IN}} - V_{\mathrm{PAR}}) - V_{\mathrm{OUT}}]dt + I_0 \tag{2b}$$

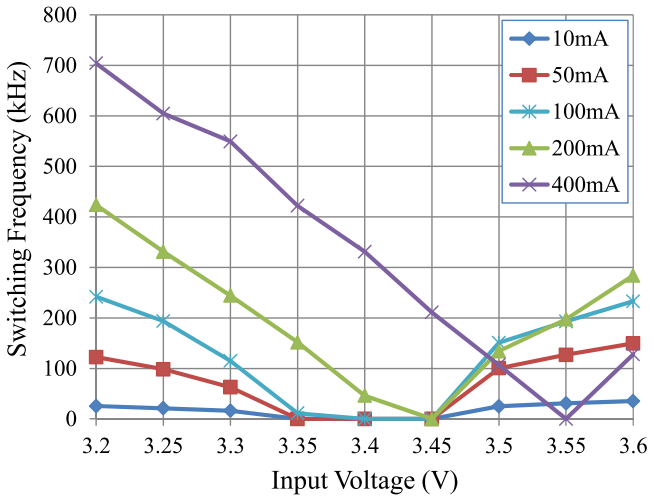

Fig. 5. Plot of the switching frequency versus the input voltage for different load current.

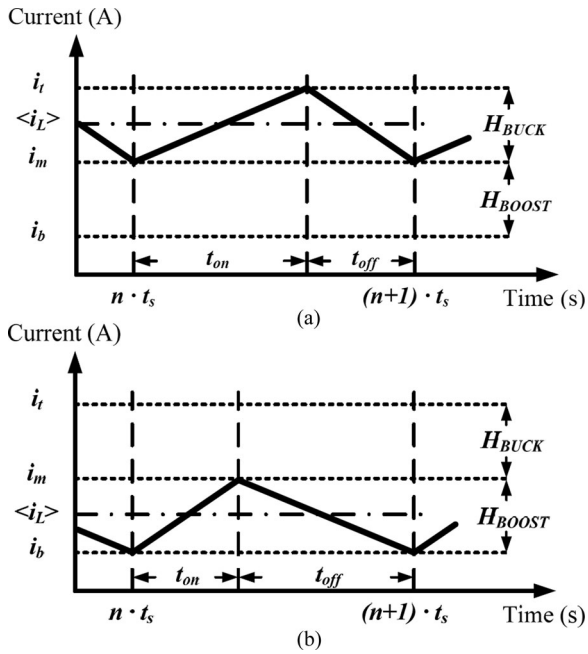

Fig. 6. Hysteretic current waveforms in (a) buck mode and (b) boost mode.

where L is the inductance in the power stage and I_0 is the initial inductor current in the beginning of the initial phase. When $(V_{\rm IN}–V_{\rm PAR})$ is the same as $V_{\rm OUT}$, $\mathrm{d}i_L(\mathrm{t})/\mathrm{dt}$ becomes zero and $i_L(\mathrm{t})$ remains at I_0, which should be the same as $I_{\rm LOAD}$ in steady states, i.e., $i_L(\mathrm{t}) = I_{\rm LOAD}$. It means that the converter stays in the initial phase forever at this particular condition, and, hence, no switching losses exist. Fig. 5 plots the switching frequency $f_{\rm SW}$ versus $\mathrm{V_{IN}}$ for different $I_{\rm LOAD}$ from simulations. When $(V_{\rm IN}–V_{\rm PAR})$ gradually approaches $V_{\rm OUT}$, $|\mathrm{d}i_L(\mathrm{t})/\mathrm{dt}|$ decreases, which in turn decreases $f_{\rm SW}$ to zero finally. In addition, because $V_{\rm PAR}$ is the product of $I_{\rm LOAD}$ and the sum of parasitic resistance, the corresponding input voltage for zero switching frequency increases with increasing $I_{\rm LOAD}$.

Furthermore, the conduction loss also reaches its minimum at $f_{SW} = 0$, which can be proved as follows. Let $I_{\rm H}$ and $I_{\rm L}$ denote the peak and valley value of a steady-state inductor current waveform in CCM, respectively, and then, its average value can be expressed as

$$I_{L(\mathrm{AVG})} = \frac{I_H + I_L}{2}. \tag{3}$$

The conduction loss is proportional to both $I_{\rm LOAD}$ and the root-mean-square of the inductor current $I_{L(\mathrm{RMS})}$ and the latter one can be calculated as

$$\begin{aligned} I_{L(\mathrm{RMS})} &= \sqrt{\frac{1}{T}\int_0^T i_L(t)^2 dt} = \sqrt{\frac{1}{T}\int_0^{DT} \left(I_L + \frac{I_H - I_L}{DT}\cdot t\right)^2 dt} \\ &\quad + \sqrt{\frac{1}{T}\int_{DT}^{T} \left[I_H - \frac{I_H - I_L}{(1-D)T}\cdot (t - DT)\right]^2 dt} \\ &= \sqrt{\frac{I_H^2 + I_L^2 + I_H I_L}{3}} \geq I_{L(\mathrm{AVG})} \end{aligned} \tag{4}$$

where D is the duty ratio and T is the switching period. When $f_{\rm SW}$ reduces to zero, the current ripple diminishes (i.e., $I_H = I_L$) and $I_{L(\mathrm{RMS})}$ reaches its minimum $I_{L(\mathrm{RMS_{min}})}$

$$I_{L(\mathrm{RMS\,min})} = I_{L(\mathrm{AVG})} = I_{\rm LOAD}. \tag{5}$$

Hence, its conduction loss also reaches its minimum at $f_{\rm SW} = 0$. As a result, the maximum efficiency occurs when $(V_{\rm IN} - V_{\rm PAR})$ is the same as $V_{\rm OUT}$.

III. Small-Signal Analysis and Circuit Implementation

A. Small-Signal Analysis

Since the proposed converter works only in the buck and boost mode and share the same compensator, the HCM small-signal models in both the buck and boost modes should be analyzed [20]–[23]. Fig. 6(a) and (b) shows the steady-state HCM current waveforms in CCM for the buck and boost mode, respectively. In fact, the main idea of HCM is to control current, rather than voltage signals. Hence, the voltage signals are all converted to current signals in Fig. 6, where the instantaneous inductor current i_L corresponds to V_S, and i_t, i_m, and i_b corresponds to $V_{\rm IT}, V_{\rm IM}$, and $V_{\rm IB}$, respectively. It can be found that i_L is limited by a fixed hysteretic window $H_{\rm BUCK}$ or $H_{\rm BOOST}$, and the switching period can be expressed as

$$t_s = t_{\rm on} + t_{\rm off}. \tag{6}$$

The instantaneous on-time and off-time ($t_{\rm on}$ and $t_{\rm off}$) in the buck and boost modes can be derived as follows:

Buck	Boost	
$t_{\rm on} = \frac{2L(i_t - \langle i_L\rangle)}{V_{\rm in} - V_{\rm out}}$	$t_{\rm on} = \frac{2L(i_m - \langle i_L\rangle)}{V_{\rm in}}$	(7)
$t_{\rm off} = \frac{L(i_t - i_m)}{V_{\rm out}}$	$t_{\rm off} = \frac{L(i_m - i_b)}{V_{\rm out} - V_{\rm in}}$	(8)

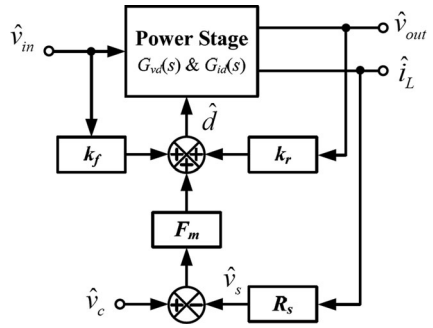

Fig. 7. Small-signal model of the HCM-controlled power stage.

where $\langle i_L \rangle$ represents the time-varying average inductance current, and $V_{\rm in}$ and$V_{\rm out}$ are the instantaneous input and output voltages, respectively.

For the small-signal analysis, every variable can be written as a summation of its dc and perturbation terms

$$t_s = T_s + \hat{t}_s, t_{\rm off} = T_{\rm off} + \hat{t}_{\rm off}, \text{ and } t_{\rm on} = T_{\rm on} + \hat{t}_{\rm on} \quad (9)$$

$$i_t = I_t + \hat{i}_t, i_m = I_m + \hat{i}_m, i_b = I_b + \hat{i}_b, \text{ and } \langle i_L \rangle = I_L + \hat{i}_L \quad (10)$$

$$V_{\rm in} = V_{\rm IN} + \hat{v}_{\rm in} \text{ and } V_{\rm out} = V_{\rm OUT} + \hat{v}_{\rm out}. \quad (11)$$

Substitute (9)-(11) into (7) and (8), and remove the dc terms and the second-order ac terms. Then, (7) and (8) can be rewritten as

$$\text{Buck}: \ \hat{t}_{\rm on} = \frac{2L(\hat{i}_t - \hat{i}_L) - T_{\rm on}(\hat{v}_{\rm in} - \hat{v}_{\rm out})}{V_{\rm IN} - V_{\rm OUT}} \quad \text{Boost}: \ \hat{t}_{\rm on} = \frac{2L(\hat{i}_m - \hat{i}_L) - T_{\rm on}\hat{v}_{\rm in}}{V_{\rm IN}} \quad (12)$$

$$\hat{t}_{\rm off} = \frac{-T_{\rm off}\hat{v}_{\rm out}}{V_{\rm OUT}} \quad \left| \hat{t}_{\rm off} = \frac{-T_{\rm off}(\hat{v}_{\rm out} - \hat{v}_{\rm in})}{V_{\rm OUT} - V_{\rm IN}} \right. . \quad (13)$$

Notably, because the sizes of hysteretic windows are fixed in this design, the perturbation terms of $(\hat{i}_m - \hat{i}_b)$ and $(\hat{i}_t - \hat{i}_m)$must be zero. Moreover, the small-signal duty cycle can be expressed as

$$D + \hat{d} = \frac{T_{\rm ON} + \hat{t}_{\rm on}}{T_S + \hat{t}_s} \quad (14a)$$

$$\hat{d} = \frac{D'\hat{t}_{\rm on} - D\hat{t}_{\rm off}}{T_S} \quad (14b)$$

where $D' = 1 - D$. Substituting (12) and (13) into (14b) results in

Buck:

$$\hat{d} = \left[\frac{2D'L(\hat{i}_t - \hat{i}_L) - D'T_{\rm on}(\hat{v}_{\rm in} - \hat{v}_{\rm out})}{V_{\rm IN} - V_{\rm OUT}} + \frac{DT_{\rm off}\,\hat{v}_{\rm out}}{V_{\rm OUT}} \right] \cdot \frac{1}{T_S} \quad (15)$$

TABLE I
MODEL PARAMETERS OF HCM BUCK AND BOOST MODES

Parameters	Buck	Boost
$\hat{v}_c$	$R_s\hat{i}_t$	$R_s\hat{i}_m$
F_m	$\frac{2D'D}{R_s H_{\rm BUCK}}$	$\frac{2D'D}{R_s H_{\rm BOOST}}$
k_f	$-\frac{D}{V_{\rm IN}}$	$-\frac{1}{V_{\rm OUT}}$
k_r	$\frac{D}{V_{\rm OUT}}$	$\frac{D'}{V_{\rm OUT}}$

TABLE II
DUTY-DERIVED TRANSFER FUNCTIONS IN BUCK AND BOOST MODES

	Buck	Boost
$G_{\rm vd}(s) = \frac{\hat{v}_{\rm out}}{\hat{d}}$	$V_{\rm IN}\frac{R}{s^2LCR + sL + R}$	$\frac{V_{\rm IN}}{D'^2}\cdot\frac{(RD'^2 - sL)}{s^2LCR + sL + RD'^2}$
$G_{\rm id}(s) = \frac{\hat{i}_L}{\hat{d}}$	$V_{\rm IN}\frac{(1 + sCR)}{s^2LCR + sL + R}$	$\frac{V_{\rm IN}}{D'}\cdot\frac{(2 + sCR)}{s^2LCR + sL + RD'^2}$

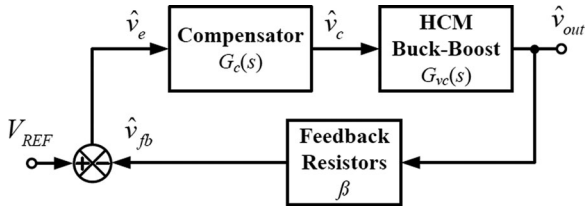

Fig. 8. Small-signal model of the whole system.

Boost:

$$\hat{d} = \left[\frac{2D'L(\hat{i}_m - \hat{i}_L) - D'T_{\rm on}\,\hat{v}_{\rm in}}{V_{\rm IN}} + \frac{DT_{\rm off}\,(\hat{v}_{\rm out} - \hat{v}_{\rm in})}{V_{\rm OUT} - V_{\rm IN}} \right] \cdot \frac{1}{T_S}. \quad (16)$$

In steady-state operations, the hysteretic windows ($H_{\rm BUCK}$ and $H_{\rm BOOST}$) and the conversion ratio can be expressed as

$$\text{Buck}: \ \frac{1}{H_{\rm BUCK}} = \frac{L}{DT_S(V_{\rm IN} - V_{\rm OUT})} \quad \text{Boost}: \ \frac{1}{H_{\rm BOOST}} = \frac{L}{DT_S V_{\rm IN}} \quad (17)$$

$$\frac{1}{D'} = \frac{V_{\rm IN}}{V_{\rm IN} - V_{\rm OUT}} \quad D' = \frac{V_{\rm IN}}{V_{\rm OUT}} \quad (18)$$

$$\frac{D}{V_{\rm OUT}} = \frac{1}{V_{\rm IN}} \quad \frac{1}{D} = \frac{V_{\rm OUT}}{V_{\rm OUT} - V_{\rm IN}}. \quad (19)$$

Therefore, (15) and (16) can be rewritten as

$$\text{Buck}: \hat{d} = \frac{2D'D}{H_{\rm BUCK}}(\hat{i}_t - \hat{i}_L) - \frac{D}{V_{\rm IN}}(\hat{v}_{\rm in}) + \frac{D}{V_{\rm OUT}}(\hat{v}_{\rm out}) \quad (20)$$

$$\text{Boost}: \hat{d} = \frac{2D'D}{H_{\rm BOOST}}(\hat{i}_m - \hat{i}_L) - \frac{1}{V_{\rm OUT}}(\hat{v}_{\rm in}) + \frac{D'}{V_{\rm OUT}}(\hat{v}_{\rm out}). \quad (21)$$

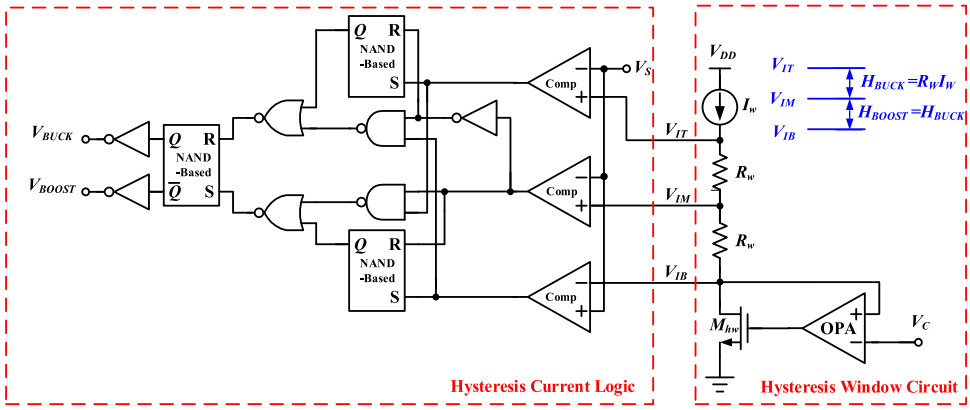

Fig. 9. Hysteretic current controller circuits.

On the other hand, the small-signal model of the HCM control is shown in Fig. 7, and its duty cycle is derived as

$$\hat{d} = F_m(\hat{v}_c - R_s\hat{i}_L) + k_f(\hat{v}_{\rm in}) + k_r(\hat{v}_{\rm out}). \tag{22}$$

By comparing (20) and (21) to (22), it can be found that each parameter in (22) can be mapped to a coefficient in (20) and (21). Table I lists the mapping results, where R_s is the sensing gain of the inductor current.

By assuming that the input voltage is fixed, i.e., $\hat{v}_{\rm in} = 0$, the control-to-output transfer function of the HCM converter $G_{\rm vc}(s)$ can be derived from Fig. 7

$$G_{\rm vc}(s) = G_{\rm vd}\frac{\hat{d}}{\hat{v}_c} \Rightarrow$$

$$G_{\rm vc}(s) = \frac{\hat{v}_{\rm out}}{\hat{v}_c} = \frac{F_m \cdot G_{\rm vd}}{1 - k_r \cdot G_{\rm vd} + F_m \cdot R_s \cdot G_{\rm id}} \tag{23}$$

where $G_{\rm vd}$ is the duty-to-output-voltage transfer function. Table II lists these transfer functions for the buck and boost modes, where R is the load resistance, C is the capacitance of the power stage, and $G_{\rm id}$ is the duty-to-inductor-current transfer function.

According to [20], if the design condition $F_m \cdot R_s \cdot G_{\rm id} >> (1–k_r \cdot G_{\rm vd})$ is satisfied, (23) can be further simplified as

$$G_{\rm vc}(s) = \frac{G_{\rm vd}}{R_s \cdot G_{\rm id}}. \tag{24}$$

As a result, the control-to-output transfer functions of the HCM converter for the buck and boost modes are

Buck:

$$G_{\rm vc}(s) = G_{\rm vc0}\frac{1}{\left(1 + \frac{s}{\omega_{p1\_\rm BK}}\right)} \tag{25a}$$

where $G_{\rm vc0} = \frac{R}{R_s}$ and $\omega_{p1\_\rm BK} = \frac{1}{RC}$

Boost:

$$G_{\rm vc}(s) = G_{\rm vc0}\frac{\left(1 - \frac{s}{\omega_{z(\rm RHP)}}\right)}{\left(1 + \frac{s}{\omega_{p1\_\rm BT}}\right)} \tag{25b}$$

where $G_{\rm vc0} = \frac{RD'}{2R_S}$, $\omega_{p1\_\rm BT} = \frac{2}{RC}$, and $\omega_{z(\rm RHP)} = \frac{RD'^2}{L}$.

Fig. 8 shows the small-signal model of the whole converter system, including the HCM buck–boost stage, feedback

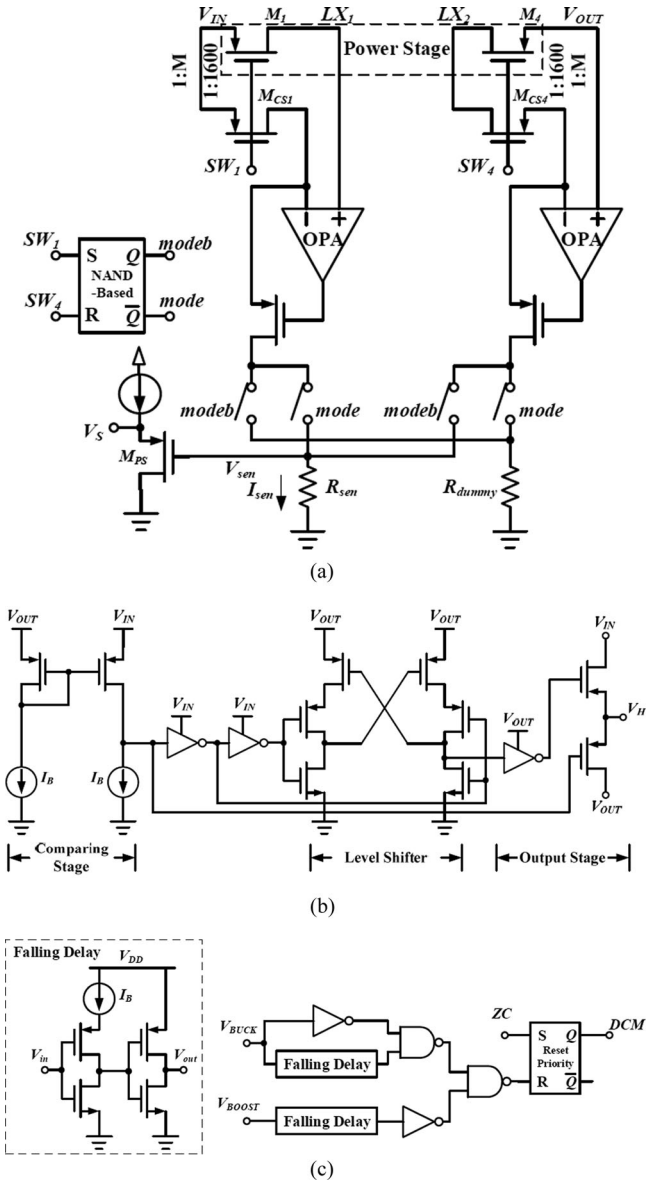

Fig. 10. (a) Inductor current sensing circuit. (b) High-voltage selector. (c) DCM controller.

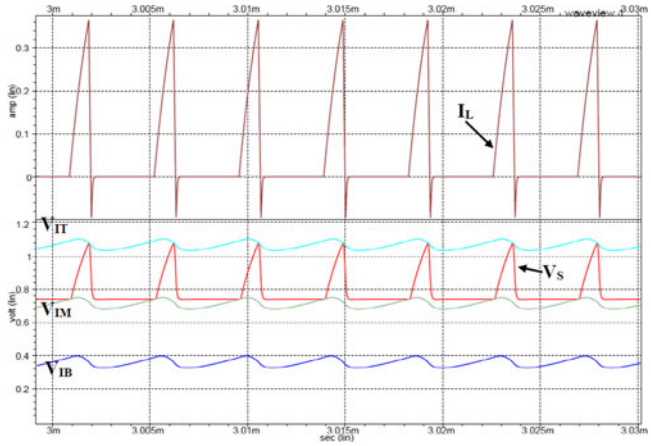

Fig. 11. Simulated steady-state waveforms of the signals of hysteretic window and inductor current in the DCM of the buck mode.

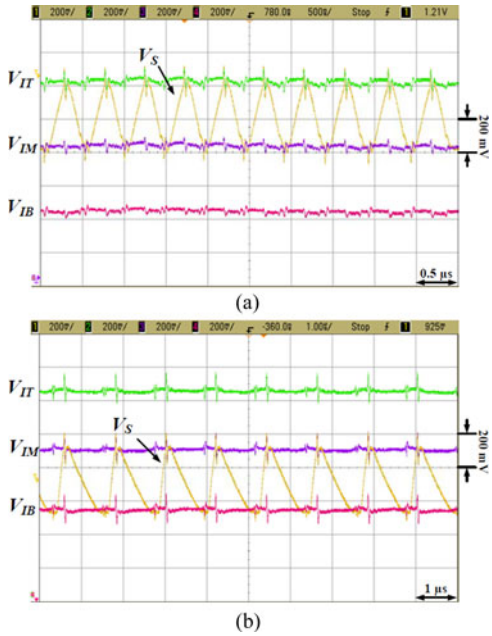

Fig. 12. Measured waveforms of hysteretic current windows with the sensed inductor current in the (a) buck and (b) boost modes.

resistors, and a compensator $G_c(s)$. The feedback resistors are composed of two resistors only, so it does not induce any pole or zero in frequency response. From (25a) and (25b), there is always a pole (ω_{p1_BK} or ω_{p1_BT}) in the buck and boost modes, while there is a right-hand-plane (RHP) zero $\omega_{z(\mathrm{RHP})}$ only in the boost mode. An RHP zero is typically undesired, because it may cause instability issue, which occurs when it is located around the unity-gain frequency of the system. Fortunately, the impact of the RHP zero in this design can be ignored, because it is much higher than the system bandwidth. Therefore, a PI compensator, rather than a complicated proportional-integral-derivative (PID) compensator, is enough and then chosen.

B. Circuit Implementation

Fig. 9 shows the circuit of the hysteretic current controller, including hysteretic window circuits and hysteretic current logic.

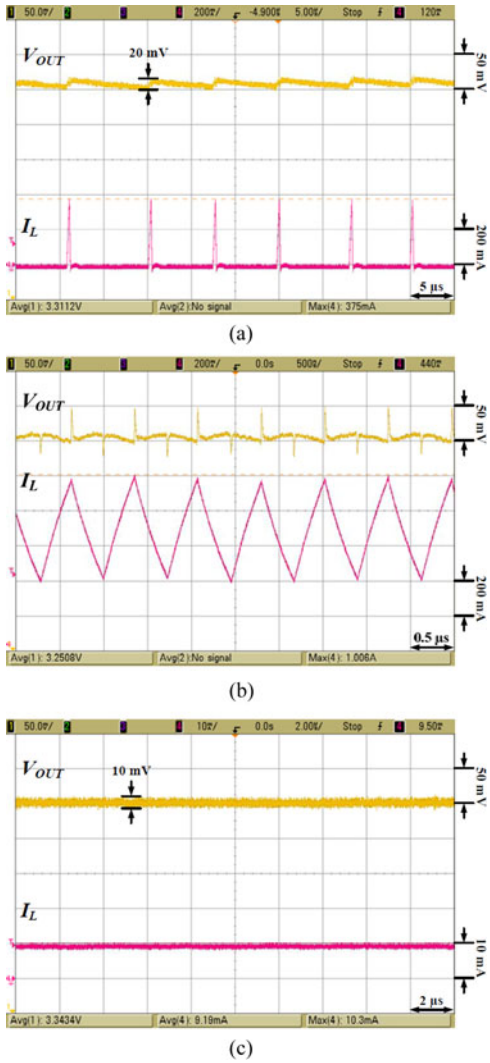

Fig. 13. Measured steady-state V_{OUT} and I_{L} waveforms. (a) DCM and buck mode @$V_{\mathrm{IN}} = 5$ V and $I_{\mathrm{LOAD}} = 10$ mA. (b) CCM and boost mode @$V_{\mathrm{IN}} = 2.5$ V and $I_{\mathrm{LOAD}} = 350$ mA. (c) Stay in the initial phase @$V_{\mathrm{IN}} = 3.35$ V and $I_{\mathrm{LOAD}} = 10$ mA.

$\mathrm{V_{IB}}$ is actually a buffered voltage of $\mathrm{V_C}$, and the offset voltage between the two successive boundary voltages is generated by passing a current I_{W} through a resistor R_{W}. As long as I_{W} and R_{W} are constant, the sizes of hysteretic windows, $\mathrm{H_{BUCK}}$ and $\mathrm{H_{BOOST}}$, are fixed. The algorithm of operational mode selection can be explained in the circuit level as well. Assume that the converter works in the boost mode initially when V_{IN} approaches V_{OUT}. When V_S gets larger than V_{IM}, the converter changes from the boost phase to the initial phase. Then, if the inductor current increases in the initial phase, i.e., $(\mathrm{V_{IN}} - \mathrm{V_{PAR}}) > \mathrm{V_{OUT}}$, V_S goes to the buck window and the converter works in the buck mode in the next cycle. On the contrary, V_S stays in the boost window and the converter still works in the boost mode. In addition, the hysteretic window would move upward or downward during transient responses. When either V_{IN} or I_{LOAD} changes, V_{OUT} changes immediately, which changes the output of the PI compensator V_{C}. Notably, the lowest boundary voltage of the hysteretic window $\mathrm{V_{IB}}$ is

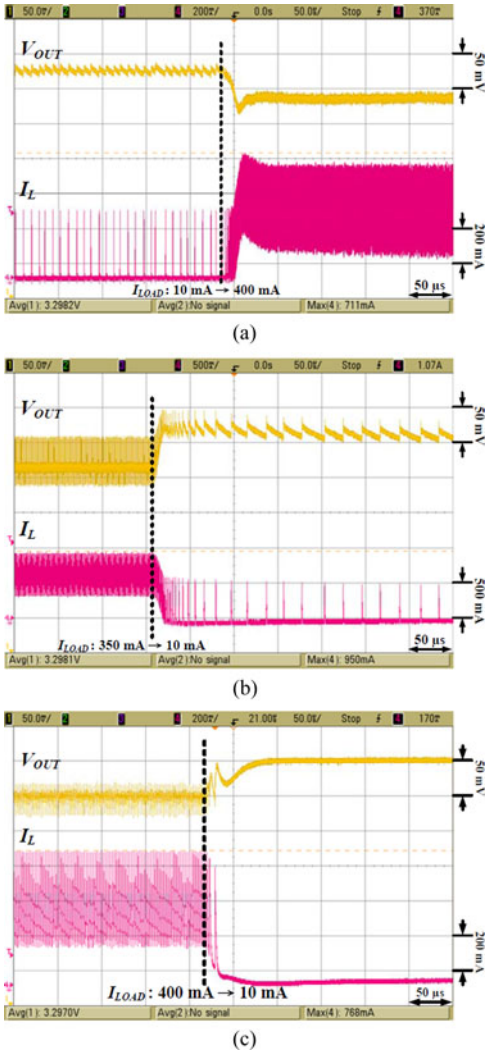

Fig. 14. Measured transient response. (a) $V_{\rm IN} = 5$ V, $I_{\rm LOAD} = 10 \rightarrow 400$ mA. (b) $V_{\rm IN} = 2.5$ V, $I_{\rm LOAD} = 300 \rightarrow 10$ mA. (c) $V_{\rm IN} = 3.35$ V, $I_{\rm LOAD} = 400 \rightarrow 10$ mA.

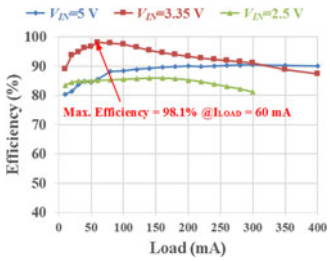

Fig. 15. Measured efficiency as a function of $I_{\rm LOAD}$ for three different $V_{\rm IN}$ values.

the same as $V_{\rm C}$, so the window moves upward/downward if $V_{\rm C}$ increases/decreases. However, the window size, i.e., $(V_{\rm IT} - V_{\rm IM})$ and $(V_{\rm IM} - V_{\rm IB})$, remains the same.

Fig. 10(a) shows the adopted full-cycle inductor current sensing circuit [24]. The opamps are used to make the drain–source voltage of the sensing transistors, $M_{\rm CS1}$ and $M_{\rm CS4}$, the same as that of the power transistors, M_1 and M_4. When the converter works in the buck mode, M_4 is always turned ON. Hence, $M_{\rm CS4}$

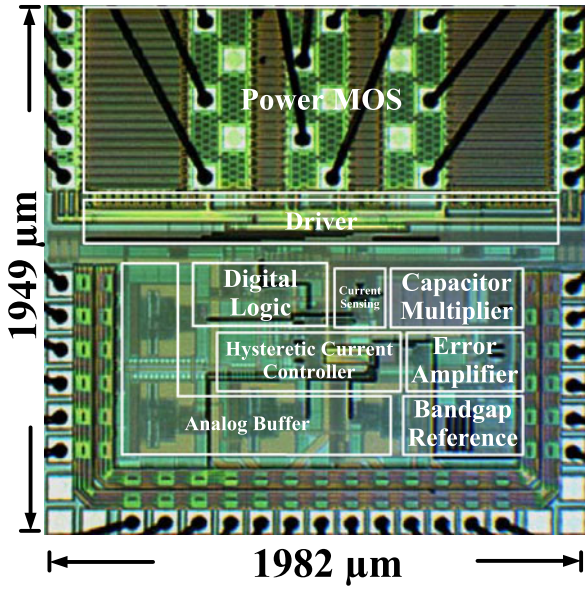

Fig. 16. Chip microphotograph.

is chosen for sensing the inductor current, and any signal/current from $M_{\rm CS1}$ is sent to a dummy path. Contrarily, when the converter is in the boost mode, $M_{\rm CS1}$ is chosen instead. The sensed current is converted to a voltage signal $V_{\rm sen}$ by passing through resistor $V_{\rm sen}$. Then, $V_{\rm sen}$ is level-shifted to V_S by a source follower $M_{\rm PS}$, before sending to the hysteretic current controller. Hence, the hysteretic windows would not get too low in DCM. Besides, most control circuits are powered by $V_{\rm IN}$, except for the antiringing and ZCD circuits. The ZCD circuit compares $V_{\rm OUT}$ with the voltage at node $\rm LX_2$, and the antiring circuit shorts nodes $\rm LX_1$ and $\rm LX_2$ together. Because both $V_{\rm OUT}$ and the voltage at $\rm LX_2$ may be higher than $V_{\rm IN}$, the higher voltage between $V_{\rm IN}$ and $V_{\rm OUT}$ should be selected to power them. Fig. 10(b) shows the circuit of the high voltage selector, which is modified from the circuit in [25]. Rather than traditional gate terminals, the source terminals are used as the inputs in the comparing stage. Fig. 10(c) shows the circuits of the DCM controller, whose functions are to turn OFF the corresponding power transistors and to turn ON the antiringing circuit, when the inductor current starts to reverse. The output signal of the DCM controller (DCM) is triggered by the ZCD output signal (ZC). The node voltage $\rm LX_2$ and $V_{\rm OUT}$ are compared in the ZCD to detect if the current is reversed: signal ZC is set to "1" when $\rm LX_2$ is lower than $V_{\rm OUT}$. However, $\rm LX_2$ is definitely lower than $V_{\rm OUT}$ in the boost phase, so some logics are designed to force ZC to "0" in the boost phase. In addition, signal DCM may be set to "1" mistakenly in the beginning of the initial phase, due to the comparator and circuit delays. Hence, the circuit of the falling delay block is used to create a longer delay only at the falling edge of its input signal, and it is achieved by only limiting the PMOS current in the first inverter. As a result, signal ZC is ignored in the beginning of the initial phase for avoiding false operations. Fig. 11 shows the simulated steady-state waveforms in the DCM of the buck mode. The sensed signal $V_{\rm S}$ is always within the hysteretic window, even in DCM.

TABLE III
PERFORMANCE COMPARISON

Parameter	This Work	TPE'14 [2]	TPE'13 [5]	TPE'12 [6]	ISSCC'11 [26]	TPE'10 [8]
Technology (μm)	0.35	0.18	0.35	0.35	0.5	0.25
Inductor (H)	$1\ \mu$	$1\ \mu$	$18\ \mu$	$4.7\ \mu$	$2.2\ \mu$	$4.7\ \mu$
Capacitor (F)	$10\ \mu$	$33\ \mu$	$47\ \mu$	$22\ \mu$	$10\ \mu$	$47\ \mu$
V_{IN} Range (V)	2.5–5	2.7–5.5	2.5–5	2.3–5	3–5.5	2.7–4.5
V_{OUT} (V)	3.3	2–5	3.3	3.3	3.6	3.3
I_{LOAD} max.(mA)	400	2000	300	400	1200	500
Switching Frequency	$\leq$ 1.66 MHz	2.5 MHz	500 kHz	500 kHz	2 MHz	700 kHz
Light Load Efficiency (%)	80.4 @10 mA	88 @400 mA	34 @50 mA	76 @50 mA	78 @600 mA	86 @100 mA
Peak Efficiency (%)	98.1	91	91.6	92	90.7	96
Proposed Control Method and/or Techniques	HCM	Automatic mode switching and dynamic sizing	Feed-forward and mode- selector	Average current mode	Error-averaged sense FET- based current sensing	Reduced average inductor current
Operational Modes	Buck/Boost	Buck/Buck-Boost/ Boost	Buck/Buck-Boost/ Boost	Buck/Boost	Buck/Buck-Boost/ Boost	Buck/2 buck-boost sub-modes/ Boost
Compensator Type	PI	PID	PID	PI	PI	PID
Fully built-in compensator	Yes	No	No	No	N/A	No

IV. MEASURED RESULTS

The proposed HCM noninverting buck–boost converter was designed and fabricated using TSMC 0.35-μm CMOS 2P4M 3.3/5V mixed-signal polycide process. The output voltage is set to 3.3 V, the input voltage range is 2.5–5 V, and the maximal $I_{\rm LOAD}$ is 400 mA. According to the measured results, the maximal measured switching frequency $f_{\rm SW}$ is 1.66 MHz.

Figs. 12(a) and (b) shows the measured HCM-related signals in the buck and boost mode, respectively. The inductor-current-sensed signal $V_{\rm S}$ is confined between $V_{\rm IT}$ and $V_{\rm IM}$ in the buck mode, while it is confined between $V_{\rm IM}$ and $V_{\rm IB}$ in the boost mode. Besides, the two hysteretic windows are both around 400 mV height. Fig. 13(a)–(c) shows the measured steady-state waveforms of $V_{\rm OUT}$ and $I_{\rm L}$. When $V_{\rm IN}$ is 5 V and $I_{\rm LOAD}$ is only 10 mA, the converter works in DCM of the buck mode. Similarly, when $V_{\rm IN}$ is decreased to 2.5 V and $I_{\rm LOAD}$ is increased to 350 mA, the converter works in CCM of the boost mode. Except for the switching noise, the output voltage ripple is only 20 and 15 mV in Fig. 13(a) and (b), respectively. Fig. 13(c) shows the measured waveforms when $V_{\rm IN}$ is around 3.35 V and $I_{\rm LOAD}$ is 10 mA. It can be found that the converter always stays in the initial phase (i.e., $f_{\rm sw} = 0$), and there are no ripples on $V_{\rm OUT}$ and $I_{\rm L}$.

Fig. 14(a) shows the transient response when $V_{\rm IN}$ is 5 V and $I_{\rm LOAD}$ changes from 10 to 400 mA, Fig. 14(b) shows the transient response when $V_{\rm IN}$ is 2.5 V and $I_{\rm LOAD}$ changes from 400 to 10 mA, and Fig. 14(c) shows the transient response when $V_{\rm IN}$ is 3.35 V and $I_{\rm LOAD}$ changes from 400 to 10 mA. The slew rate of the load current is $64\ {\rm mA}/\mu s$. The recovery times in all cases are less than or around 50 μs, and their undershoot/overshoot voltages are less than or around 50 mV. Notably, when $I_{\rm LOAD}$ decreases to 10 mA in Fig. 14(c), there are no ripples on the waveforms, i.e., the conditions of $f_{\rm sw} = 0$ is achieved. Fig. 15 plots the measured efficiency versus the load current for different $V_{\rm IN}$, and the maximum efficiency is 98.1%, occurring when $V_{\rm IN}$ is 3.35 V and $I_{\rm LOAD}$ is 60 mA. As analyzed in Section II, both the switching loss and $f_{\rm sw}$ would gradually reduce to zero when $V_{\rm IN}$ (or $V_{\rm IN}$–$V_{\rm PAR}$) approaches $V_{\rm OUT}$, and the conduction loss reaches its minimum at $f_{\rm sw} = 0$. Besides, the conduction loss is also proportional to $I_{\rm LOAD}$, so the efficiency should increase with the decreasing $I_{\rm LOAD}$. Nevertheless, the efficiency at extremely light load drops, because the current consumption of the control circuits becomes significant with regard to the extremely small load current. Therefore, the conversion efficiency reaches its maximum when $V_{\rm IN}$ is close to $V_{\rm OUT}$ and the load current is relatively small.

The line and load regulations of the proposed converter is around 0.55 %/V and 4.6 %/A, respectively. Fig. 16 shows the chip microphotograph, and the chip area is $1.95 \times 1.98\ {\rm mm}^2$. Table III compares the performance of the proposed HCM noninverting buck–boost converter with some recent published buck–boost papers. The proposed HCM converter has the highest maximal efficiency, and the light-load efficiency is only lower than those of [2] and [8]. However, the light-load efficiency in [2] and [8] was measured with 400- and 100-mA load current, respectively, and both of them are one-fifth of their maximal load currents. Instead, our light-load efficiency was measured with $I_{\rm LOAD} = 10$ mA, which is only one-fortieth of our maximal load current. In the other words, the proposed converter still can achieve remarkable efficiency at light load.

V. CONCLUSION

An HCM control method for noninverting buck–boost converters with smooth mode transition was proposed, and its small-signal model was also analyzed. In addition, the corresponding hysteretic current controller circuit was also proposed. The operational mode is automatically chosen by the relationship between the sensed inductor current and the hysteretic window, rather than the relationship between $V_{\rm IN}$ and $V_{\rm OUT}$. Moreover, when $V_{\rm IN}$ approaches $V_{\rm OUT}$, the switching loss can be eliminated completely to achieve its maximal efficiency. According to the measured results, the maximal efficiency of the proposed HCM noninverting buck–boost converter achieves 98.1%, and the minimal efficiency is still above 80%. To be concluded, the

proposed HCM method can effectively improve the conversion efficiency of the noninverting buck–boost converter over the entire input voltage and loading ranges.

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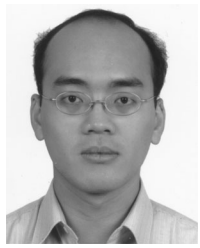

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