Three-Level TAIPEI Rectifier—Analysis of Operation, Design Considerations, and Performance Evaluation

Yungtaek Jang, *Fellow, IEEE*, Milan M. Jovanović, *Fellow, IEEE*, Misha Kumar, and Juan M. Ruiz

***Abstract*—A new low-cost three-phase four-switch three-level zero-voltage-switching (ZVS) discontinuous-current-mode power-factor-correction boost rectifier, for short named the three-level TAIPEI rectifier, that achieves a low input-current total harmonic distortion (THD) and features ZVS of all the switches is introduced. Since in the proposed rectifier the voltage stress of the four switches is equal to one-half of the output voltage, the rectifier can utilize switches with a lower voltage rating that, generally, have lower conduction losses. To reduce the switching-frequency range and maximize the light-load efficiency, the control is implemented by a combination of variable-switching frequency and phase-shift pulse-width modulation control. Detailed design guidelines for and performance evaluation of a three-phase 6-kW prototype designed for the line-to-line voltage range from 340 $V_{\rm RMS}$ to 520 $V_{\rm RMS}$ are presented. The prototype rectifier exhibits efficiency in the 96%–98% range and achieves less than 5% input-current THD over the entire nominal input-voltage range (380–480 $V_{L-L,\rm RMS}$) and above 50% of full load.**

***Index Terms*—Boost converter, discontinuous-conduction mode (DCM), frequency foldback, power factor correction (PFC), TAIPEI rectifier, three level, three phase, zero-voltage switching.**

I. Introduction

ACHIEVING high efficiency in high-voltage applications is a major design challenge that requires the optimization of conduction and switching losses through a careful selection of the converter topology and switching device characteristics. Generally, switching losses can be reduced and virtually eliminated by resorting to a variety of resonant or soft-switching topologies [1]–[9], whereas the conduction losses can be minimized by employing multilevel topologies that enable the use of switches with lower voltage ratings that generally exhibit lower conduction losses [10]–[15]. Furthermore, employing topologies with a reduced number of active switches usually results in a more cost effective design [1]–[7], [16]–[23].

Recently, a low-cost, three-phase, two-switch, zero-voltage-switching (ZVS), discontinuous-current-mode (DCM), power-factor-correction (PFC) boost rectifier, for short named the TAIPEI rectifier, that achieves a low input-current total harmonic distortion (THD) and features ZVS of all the switches without any additional soft-switching circuitry was introduced [24]. When designed for Japanese/U.S. nominal three-phase line-to-line voltage 200/240 $V_{\rm RMS}$ where 650-V MOSFETs can be used for the two switches, this minimum-component rectifier exhibits excellent performance with the input-current THD below 5% and efficiency in the 96%–97% range, as reported in [25]. However, because the output voltage of the TAIPEI rectifier designed to work with European/U.S nominal line-to-line voltage 380/480 $V_{\rm RMS}$ must be at least around 800 V and because the voltage stress of the switches is equal to the output voltage, the rectifier must be implemented with switches that are rated at least 1000 V. As documented in [24], by employing commercially available silicon carbide (SiC) MOSFET switches [26], the rectifier exhibits excellent performance with a full-load efficiency of approximately 98%. However, a relatively high price of SiC switches diminishes the cost effectiveness of the circuit making it less attractive in 380-/480-V applications.

In this paper, a low-cost, three-level, ZVS, DCM, PFC boost rectifier that can utilize switches with a lower voltage rating is proposed. In this three-level TAIPEI rectifier, which employs only four switches, the voltage stress across all the switches is clamped to one half of the output voltage. To further optimize the efficiency by limiting the switching frequency range, a combination of variable-switching frequency and phase-shift pulse-width modulation (PWM) control is employed. The performance evaluation of the proposed three-level TAIPEI rectifier was performed on a three-phase 6-kW prototype designed for the line-to-line voltage range from 340 to 520 $V_{\rm RMS}$.

II. Three-Phase Three-Level TAIPEI Rectifier

Fig. 1 shows the proposed three-phase three-level ZVS PFC DCM boost rectifier. The input of the circuit consists of three boost inductors L_1, L_2, and L_3 coupled to three capacitors C_1, C_2, and C_3 connected in the Y ("star") configuration and the three-phase input terminals through an EMI filter (not shown in Fig. 1). The common point of the capacitors *N* is connected to the midpoint between serially connected switch pairs S_1 and S_2 and S_3 and S_4 and also to the midpoint of split output capacitors C_{O1} and C_{O2}. The midpoint of serially connected switches S_1 and S_2 is connected to output capacitor C_{O1} through clamping diode D_{C1} so that the voltage across switch S_2 is clamped to the voltage across capacitor C_{O1}, which is one-half of output voltage V_O. Similarly, the midpoint of serially connected switches

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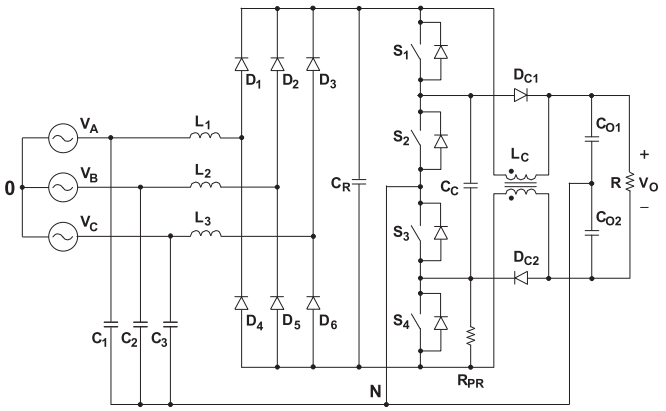

Fig. 1. Proposed three-phase three-level ZVS PFC DCM boost rectifier.

S_3 and S_4 is connected to output capacitor C_{O2} through clamping diode D_{C2} and the voltage across switch S_3 is also clamped to one-half of output voltage V_O. Clamping capacitor C_C that is connected between the midpoints of the two pairs of serially connected switches is precharged to its steady-state average voltage of one-half of the output voltage through the loop consisting of capacitor C_{O2}, the body diode of switch S_2, precharge resistor $R_{\rm PR}$, and a winding of coupled inductor L_C. Capacitor C_R that is used to reset the boost-inductor currents is connected across the serially connected pairs of switches and is decoupled from the output by coupled inductor L_C. Its average voltage is equal to the output voltage since the average voltage across the windings of L_C is zero. The voltages across switches S_1 and S_4 are clamped to the difference of the voltages across capacitor C_R and C_C through the body diodes of switch S_4 and switch S_1, respectively. Since this difference is equal to one-half of the output voltage, the voltages across all four switches in the circuit in Fig. 1 are clamped to one-half of the output voltage. Generally, any kind of switch that is capable of conducting current in both directions and blocking voltage in one direction such as for example a MOSFET or an IGBT with an antiparallel diode is suitable for this application.

To achieve a low input-current THD, high power factor (PF), and a wide-load range soft switching of the switches, the circuit in Fig. 1 must operate in DCM with a low-bandwidth output-voltage control. This control can be implemented by employing various modulation strategies of switches S_1–S_4. Fig. 2(a) shows timing waveforms of the four switches of the circuit in Fig. 1 for conventional switching-frequency modulation. In the switching-frequency modulation in Fig. 2(a), two pairs of switches S_1 and S_2 and S_3 and S_4 are switched in a complementary fashion with a small dead time t_D between their commutation instants to enable the pair of switches that is about to turn on to achieve ZVS. Since dead time t_D is very small in comparison with switching period T_S, the effect of the dead time is negligible, i.e., it can be assumed that the duty cycle of each switch is approximately 50%. Because the switches of each pair operate with the identical gate signals as shown in Fig. 2(a), this modulation scheme is identical to that of the two-level two-switch ZVS DCM PFC TAIPEI rectifier [24].

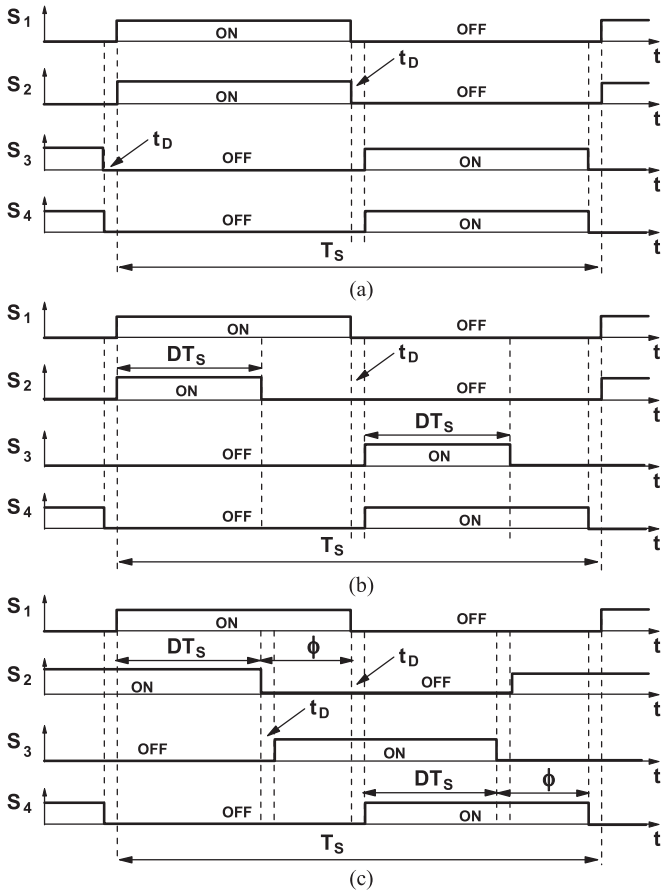

Fig. 2. Gating waveforms of switches S_1–S_4 for: (a) frequency control; (b) PWM control; (c) phase-shift PWM control.

Fig. 2(b) shows another modulation method of the switches in the circuit in Fig. 1. In this modulation approach, outer switches S_1 and S_4 are switched at a constant frequency in a complementary fashion with a small dead time, i.e., with approximately 50% duty ratio. The duty ratio of inner switches S_2 and S_3, whose turn-on instants are synchronized with the turn on instants of S_1 and S_4, respectively, is PWM to provide regulation of the output. While the rectifier output voltage can be fully regulated by this constant-frequency PWM control, the rectifier exhibits increased input-current THD and loses ZVS of switches S_1 and S_4 when the duty cycle becomes small. However, by properly combining switching-frequency modulation and PWM, a low THD and wide ZVS range can be achieved with a reduced frequency range, which brings about efficiency improvements at light loads. Namely, since in the output-voltage-regulated converter in Fig. 1, the switching frequency increases as the load decrease, the frequency range can be reduced by employing switching-frequency modulation over the load range from full load down to a predetermined level at light load and resorting to the constant-frequency PWM for the loads below this level. Moreover, by keeping the turn-on times of switches S_2 and S_3 constant and decreasing the switching frequency proportional to the load, i.e., by implementing frequency foldback PWM control, additional reduction of switching-related losses at light loads can be achieved.

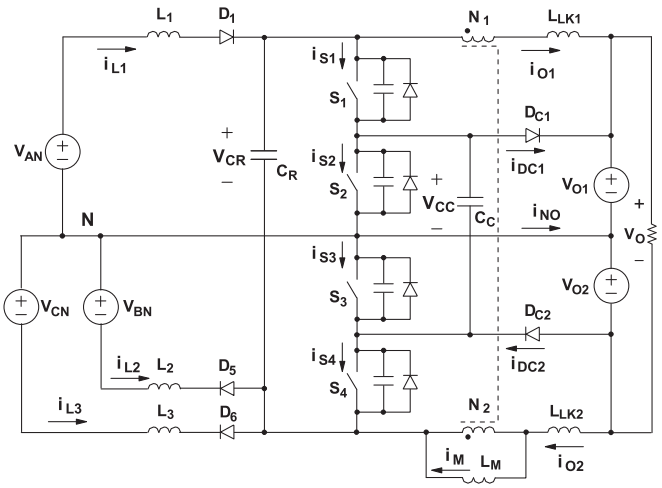

Fig. 3. Simplified circuit diagram of the proposed three-phase boost power stage showing reference directions of currents and voltages. The model is valid for 60° segment where $V_{\rm AN} > 0$ and $V_{\rm BN} < V_{\rm CN} < 0$.

Constant-frequency PWM control of the rectifier in Fig. 1 can also be implemented by employing the phase-shift PWM illustrated in Fig. 2(c). In this modulation method, each pair of switches S_1 and S_4 and S_2 and S_3 is switched at a constant frequency in a complementary fashion with a fixed duty ratio of approximately 50%. The PWM is achieved by a phase shift of the switching instants of the outer switch S_1 and S_4 pair with respect to the corresponding switching instants of the inner switch S_2 and S_3 pair. In this phase-shift PWM, the output voltage is maximum when phase-shift angle φ is zero and is zero when phase-shift angle φ is 180°, i.e., $T_S/2$. By combining the switching-frequency modulation and phase-shift PWM, a control method for the three-level TAIPEI rectifier that provides a low THD and wide ZVS range with a reduced switching-frequency range can be implemented.

III. Analysis of Operation

Fig. 3 shows a simplified model of the circuit in Fig. 1 along with reference directions of currents and voltages. To simplify the analysis of operation, it is assumed that ripple voltages of the input and output filter capacitors shown in Fig. 1 are negligible so that the voltage across the input and output filter capacitors can be represented by constant-voltage source $V_{\rm AN}, V_{\rm BN}, V_{\rm CN}, V_{O1}$, and V_{O2}. Also, it is assumed that in the on-state, semiconductors exhibit zero resistance, i.e., they are short-circuits. However, the output capacitances of the switches are not neglected in this analysis. Coupled inductor $L_{\rm C}$ in Fig. 1 is modeled as a two-winding ideal transformer with magnetizing inductance L_M and leakage inductances $L_{\rm LK1}$ and $L_{\rm LK2}$. It should be noted that the average voltage across flying capacitor C_R is equal to output voltage $V_O = V_{O1} + V_{O2}$ and the average voltage across clamping capacitor C_C is equal to one half of output voltage V_O. The circuit diagram of the simplified rectifier is shown in Fig. 3. The reference directions of currents and voltages in Fig. 3 correspond to the 60° segments of a line cycle when $V_{\rm AN} > 0, V_{\rm BN} < 0$, and $V_{\rm CN} < 0$.

To further facilitate the explanation of the operation, Fig. 4 shows topological stages of the circuit in Fig. 3 during a switching cycle, whereas Fig. 5 shows the power-stage key waveforms. As can be seen from the gate-drive timing diagrams of switches S_1–S_4 in Fig. 5, in this explanation a combination of switching-frequency modulation and phase-shift PWM is used. In Fig. 5, switches S_1 and S_4 and switches S_2 and S_3 operate in a complimentary fashion with a short dead time between their commutation instants, i.e., with a fixed duty ratio of approximately 50%. This gating strategy enable ZVS of the switches that are about to turn on. The output-voltage regulation is primarily done by frequency control, except at light loads and/or high-input voltages where phase-shift PWM control is used.

As shown in Figs. 4(a) and 5, before switch S_2 is turned OFF at $t = T_1$, inductor current i_{L1} flows through switches S_1 and S_2. The slope of inductor current i_{L1} is equal to $V_{\rm AN}/L_1$ and the peak of the inductor current at $t = T_1$ is approximately

$$I_{L1(\rm PK)} = \frac{V_{\rm AN}}{L_1} \times DT_S \tag{1}$$

where $V_{\rm AN}$ is the line-to-neutral voltage and T_S is the switching period. Because the dead time between turn-off of switch S_1 and turn-on of switch S_4 is very small in comparison with switching period T_S, the effect of the dead time is neglected in (1). During the time period between T_0 and T_1, current i_{O1} decreases at a rate of $-V_{O1}/(L_M + L_{\rm LK1})$, while current i_{O2} increases at a rate of $(V_{\rm CR} - V_{O1})/(L_M + L_{\rm LK2})$. Magnetizing current i_M is the difference between currents i_{O1} and i_{O2}. It should be noted that the magnetizing inductance value of coupled inductor L_M is designed to be sufficiently large so that the ripple current of the coupled inductor does not significantly affect rectifier operation. As shown in Fig. 1, the two windings of inductor L_C are coupled in such a way as to cancel the magnetic fluxes from the differential current of the two windings so that the large magnetizing inductance can be obtained by a small gap in the core without saturation. Since the effect of the current ripple of currents i_{O1} and i_{O2} is negligible, they are not further discussed, although they are shown in the topological stages in Fig. 4.

At $t = T_1$, when switch S_2 is turned OFF, inductor current i_{L1} starts charging the output capacitance of switch S_2, as shown in Fig. 4(b). Because the sum of the voltages across switch S_2 and switch S_3 is clamped to clamping capacitor voltage $V_{\rm CC}$, the output capacitance of switch S_3 discharges at the same rate as the charging rate of the output capacitance of switch S_2. This period ends when the output capacitance of switch S_2 is fully charged and clamping diode D_{C1} starts to conduct at $t = T_2$, as shown in Figs. 4(c) and 5. After $t = T_2$, switch S_3 is turned ON with ZVS.

Because clamping diode D_{C1} is forward biased, inductor current i_{L1} begins to linearly decrease. The slope of inductor current i_{L1} is equal to $(V_{\rm AN} - V_{O1})/L_1$ and the inductor current at $t = T_3$ is approximately

$$i_{L1}\,|_{t=T3} = \frac{V_{\rm AN} - (1-2D)\,V_{O1}}{2L_1} \times T_S. \tag{2}$$

At $t = T_3$, when switch S_1 is turned OFF, inductor current i_{L1} starts charging the output capacitance of switch S_1, as shown in

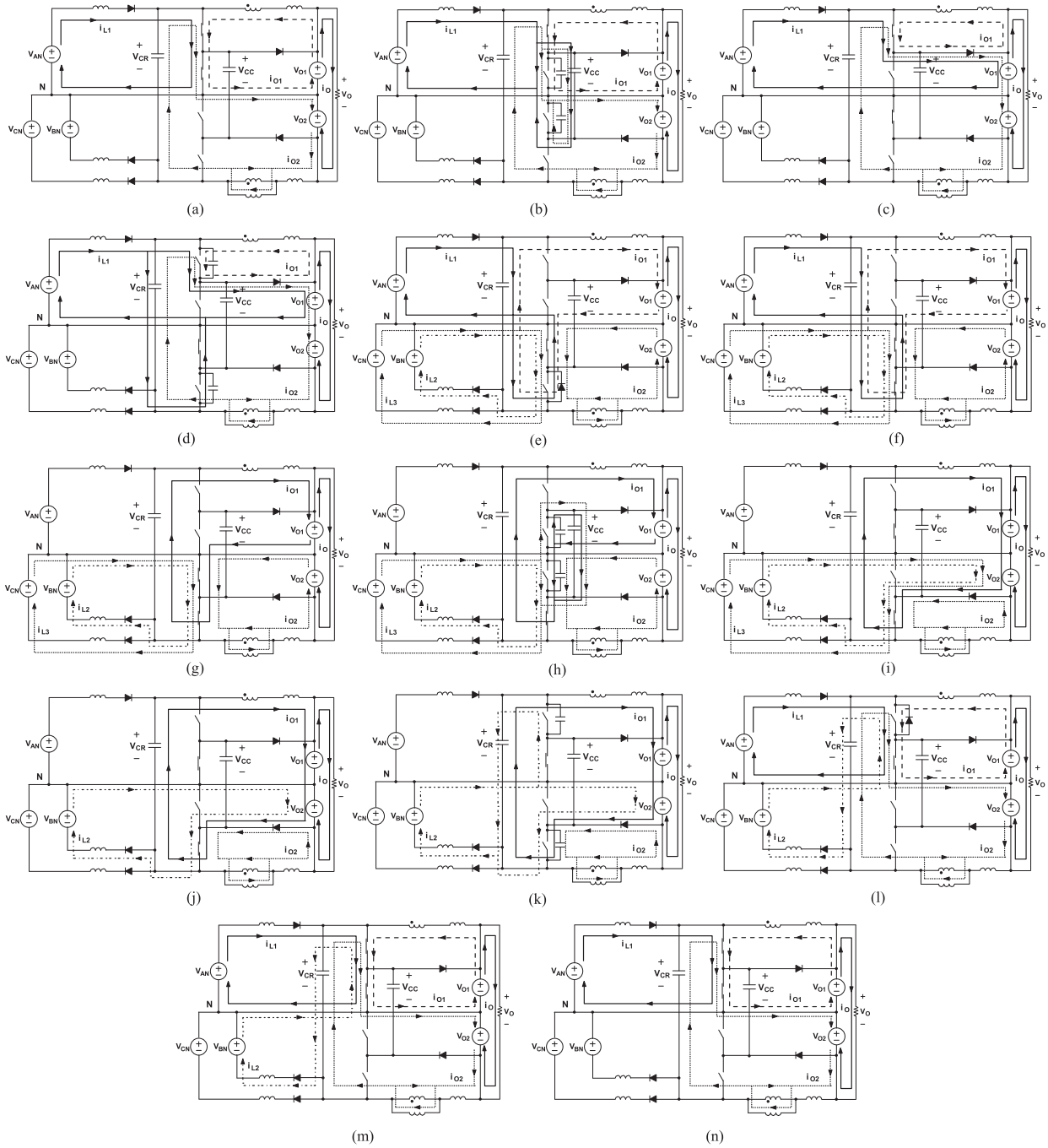

Fig. 4. Topological stages of the proposed rectifier when $V_{\rm AN} > 0$, $V_{\rm BN} < 0$, and $V_{\rm CN} < 0$. (a) $[T_0 - T_1]$. (b) $[T_1 - T_2]$. (c) $[T_2 - T_3]$. (d) $[T_3 - T_4]$. (e) $[T_4 - T_5]$. (f) $[T_5 - T_6]$. (g) $[T_6 - T_7]$. (h) $[T_7 - T_8]$. (i) $[T_8 - T_9]$. (j) $[T_9 - T_{10}]$. (k) $[T_{10} - T_{11}]$. (l) $[T_{11} - T_{12}]$. (m) $[T_{12} - T_{13}]$. (n) $[T_{13} - T_{14}]$.

Fig. 4(d). Because the sum of the voltages across switch S_1 and switch S_4 is clamped to the voltage difference between flying capacitor voltage $V_{\rm CR}$ and clamping capacitor voltage $V_{\rm CC}$, the output capacitance of switch S_4 discharges at the same rate as the charging rate of the output capacitance of switch S_1. This period ends when the output capacitance of switch S_4 is fully discharged and the antiparallel body diode of switch S_4 starts to conduct at $t = T_4$, as shown in Figs. 4(e) and 5. At $t = T_5$, switch S_4 is turned ON with ZVS and inductor current i_{L1} is commutated from the antiparallel body diode of switch S_4 to the switch, as illustrated in Fig. 4(f). Because the body diode of switch S_4 is forward biased and switch S_3 is ON, inductor currents i_{L2} and i_{L3} begin to linearly increase after $t = T_4$. At $t = T_5$, switch S_4 is turned ON with ZVS and inductor currents i_{L2} and i_{L3} are commutated from the antiparallel body diode of switch S_4 to the switch, as illustrated in Fig. 4(f). This period ends when inductor current i_{L1} decreases to zero at $t = T_6$. To maintain DCM operation, minimum voltage $V_{\rm CR(MIN)}$ across flying capacitor C_R, which is equal to output voltage V_O, is

$$V_{\rm CR(MIN)} = \frac{V_{\rm AN(PK)}}{1-D} = \frac{\sqrt{2}}{\sqrt{3}\,(1-D)} \times V_{L-L,\rm RMS} \qquad (3)$$

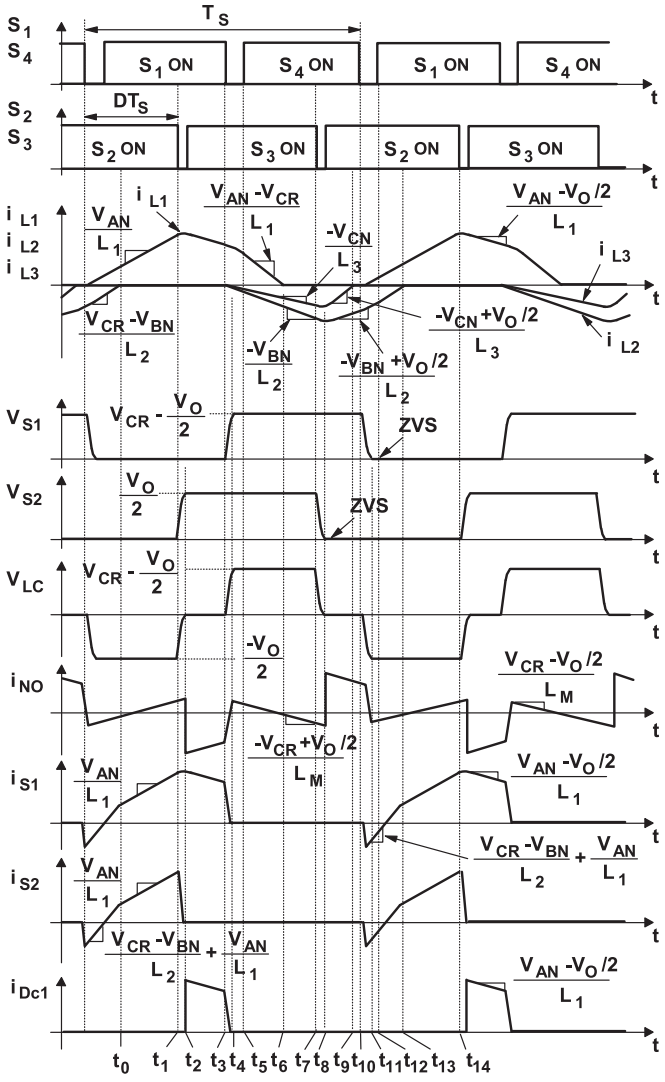

Fig. 5. Key waveforms of the proposed rectifier when $V_{\rm AN} > 0, V_{\rm BN} < 0$, and $V_{\rm CN} < 0$.

where $V_{\rm AN(PK)}$ is the peak line-to-neutral voltage. It should also be noted that because during the T_4–T_6 interval inductor currents i_{L2} and i_{L3} flow in the opposite direction from inductor current i_{L1}, the average current through switches S_3 and S_4 is reduced so that the switches in the proposed rectifier exhibit reduced power losses.

During the time period between $t = T_6$ and $t = T_7$, inductor currents i_{L2} and i_{L3} continue to flow through switches S_3 and S_4, as illustrated in Fig. 4(g). As shown in Fig. 5, the slopes of inductor currents i_{L2} and i_{L3} during this period are equal to $-V_{\rm BN}/L_2$ and $-V_{\rm CN}/L_3$, respectively. The peaks of the inductor currents at the moment when switch S_3 turns off at $t = T_7$ are approximately

$$I_{L2(\rm PK)} = -\frac{V_{\rm BN}}{L_2} \times DT_S \tag{4}$$

and

$$I_{L3(\rm PK)} = -\frac{V_{\rm CN}}{L_3} \times DT_S. \tag{5}$$

As it can be seen in (1), (4), and (5), the peak of each inductor current is proportional to its corresponding input voltage as long as duty cycle D and switching period T_S are constant during one-half of the line cycle.

After switch S_3 is turned OFF at $t = T_7$, inductor currents i_{L2} and i_{L3} start to simultaneously charge the output capacitance of switch S_3 and discharge the output capacitance of switch S_2, as shown in Fig. 4(h). This period ends at $t = T_8$ when the output capacitance of switch S_3 is fully charged and clamping diode D_{C2} starts to conduct at $t = T_8$, as shown in Figs. 4(i) and 5. After $t = T_8$, switch S_2 is turned ON with ZVS.

Because clamping diode D_{C2} is forward biased, inductor currents i_{L2} and i_{L3} begin to linearly increase. This period ends when inductor current i_{L3} reaches zero at $t = T_9$. The slopes of inductor currents i_{L2} and i_{L3} are equal to $(-V_{\rm BN} + V_{O2})/L_2$ and $(-V_{\rm CN} + V_{O2})/L_3$, respectively. Inductor current i_{L2} at $t = T_{10}$ when switch S_4 turns off is approximately

$$i_{L2}\,|_{t=T10} = \frac{-V_{\rm BN} + (1-2D)\,V_{O2}}{2L_2} \times T_S. \tag{6}$$

At $t = T_{10}$, when switch S_4 is turned OFF, inductor current i_{L2} starts charging the output capacitance of switch S_4, as shown in Fig. 4(k). Because the sum of the voltages across switch S_1 and switch S_4 is clamped to the voltage difference between flying capacitor voltage $V_{\rm CR}$ and clamping capacitor voltage $V_{\rm CC}$, the output capacitance of switch S_1 discharges at the same rate as the charging rate of the output capacitance of switch S_4. This period ends when the output capacitance of switch S_1 is fully discharged and the antiparallel body diode of switch S_1 starts to conduct at $t = T_{11}$, as shown in Figs. 4(l) and 5. At $t = T_{12}$, switch S_1 is turned ON with ZVS and inductor currents i_{L2} is commutated from the antiparallel body diode of switch S_1 to the switch, as illustrated in Fig. 4(m). Because switches S_1 and S_2 are ON, inductor current i_{L1} begins to linearly increase after $t = T_{11}$. During period T_{12}–T_{13}, increasing inductor current i_{L2} continues to flow through switches S_1 and S_2, as shown in Fig. 4(m). Finally, after inductor current i_{L2} reaches zero at $t = T_{13}$, a new switching cycle begins, as shown in Fig. 4(n).

Since in the circuit shown in Fig. 1, the charging current of each boost inductor during the time when the related switch is on is proportional to its corresponding phase voltage and its discharging current proportional to the difference of flying capacitor voltage $V_{\rm CR}$ and the corresponding phase voltage, as shown in the inductor-current waveforms in Fig. 5, average inductor current $< I_{L(\rm AVG)} >_{Ts}$ of each boost inductor during a switching cycle is

$$\left\langle I_{L(\rm AVG)} \right\rangle_{Ts} = \frac{T_S}{32L} \times \left(\frac{2\,(1+4D^2)\,V_{\rm CR} \times \sqrt{2}V_{L-N,\rm RMS}\sin\omega t - (1-2D)^2 V_{\rm CR}^2}{V_{\rm CR} - \sqrt{2}V_{L-N,\rm RMS}\sin\omega t} \right) \tag{7}$$

where $L = L_1 = L_2 = L_3$, and ω is the angular frequency of the line voltage. For maximum duty cycle $D_{\rm MAX} = 0.5$, average inductor current $< I_{L(\rm AVG)} >_{Ts,D=0.5}$ of each boost inductor

during a switching cycle is

$$\left\langle I_{L(\mathrm{AVG})}\right\rangle_{Ts,D=0.5}=\frac{T_S}{8L}\left(\frac{V_{\mathrm{CR}}\times\sqrt{2}V_{L-N,\mathrm{RMS}}\sin\omega t}{V_{\mathrm{CR}}-\sqrt{2}V_{L-N,\,\mathrm{RMS}}\sin\omega t}\right). \tag{8}$$

By defining input-to-output voltage conversion ratio M as

$$M=\frac{V_O}{\sqrt{2}V_{L-N,\mathrm{RMS}}} \tag{9}$$

and recalling that the voltage across flying capacitor C_R is equal to output voltage V_O, i.e., $V_{\mathrm{CR}}=V_O$, average inductor current $<I_{L(\mathrm{AVG})}>_{Ts}$ in (7) can be rewritten as

$$\left\langle I_{L(\mathrm{AVG})}\right\rangle_{Ts}=\frac{V_O T_S}{32L}\left(\frac{2\left(1+4D^2\right)\sin\omega t-(1-2D)^2M}{M-\sin\omega t}\right) \tag{10}$$

i.e., for $D_{\mathrm{MAX}}=0.5$

$$\left\langle I_{L(\mathrm{AVG})}\right\rangle_{Ts,D=0.5}=\frac{V_O T_S}{8L}\left(\frac{\sin\omega t}{M-\sin\omega t}\right). \tag{11}$$

The current distortion of the average inductor current in (11) is brought about by the denominator term ($M-\sin\omega t$) and it is dependent on voltage-conversion ratio M. It should be noted that the current distortion of the average inductor current is also dependent on duty cycle D if duty cycle D is less than 0.5 as shown in (10).

Fig. 6 shows calculated average boost inductor current $<I_{L(\mathrm{AVG})}>_{Ts}$ with duty cycle $D=0.5$, $D=0.2$, and $D=0.1$ for various input-to-output voltage conversion ratios M. The harmonic content of the average inductor currents shown in Fig. 6 is summarized in Table I. As can be seen from Table I, the third harmonic is the dominant distortion component. However, since in the three-wire power systems, the neutral wire is not available (or not connected), the line currents cannot contain the triplen harmonics (the third harmonic and the odd multiples of the third harmonic). As a result, the proposed circuit exhibits a very low THD and high PF since according to Table I, the remaining harmonics contribute less than 3% of total current distortion up to $D=0.2$. It should be noted that since the line currents cannot contain the third harmonic, the third harmonic of the inductor currents flow through filter capacitors C_1–C_3.

Finally, it should be noted that the proposed rectifier automatically balances the voltages across the two output capacitors, i.e., no additional voltage-balancing circuit is required. Natural voltage balancing is achieved because in the circuit in Fig. 1, the average voltages V_{O1} and V_{O2} across capacitors C_{O1} and C_{O2} are equal to the average voltages across corresponding serially connected switch pairs S_1 and S_2 and S_3 and S_4 since the average voltages across the windings of inductor L_C are zero. Because switch pairs S_1 and S_2 and S_3 and S_4 are operated symmetrically, their average voltages are equal to $V_{\mathrm{CR}}/2$ so that $V_{O1}=V_{O2}=V_{\mathrm{CR}}/2$. It should be also noted that clamping voltage V_{CC} is equalized to V_{O2} through clamping diode D_{C2} whenever switch S_2 is turned ON. Clamping voltage V_{CC} is also equalized to V_{O1} through clamping diode D_{C1} when switch S_3 is turned ON. As a result, the voltages across capacitors C_C, C_{O1}, and C_{O2} are equal to one-half of output voltage V_O.

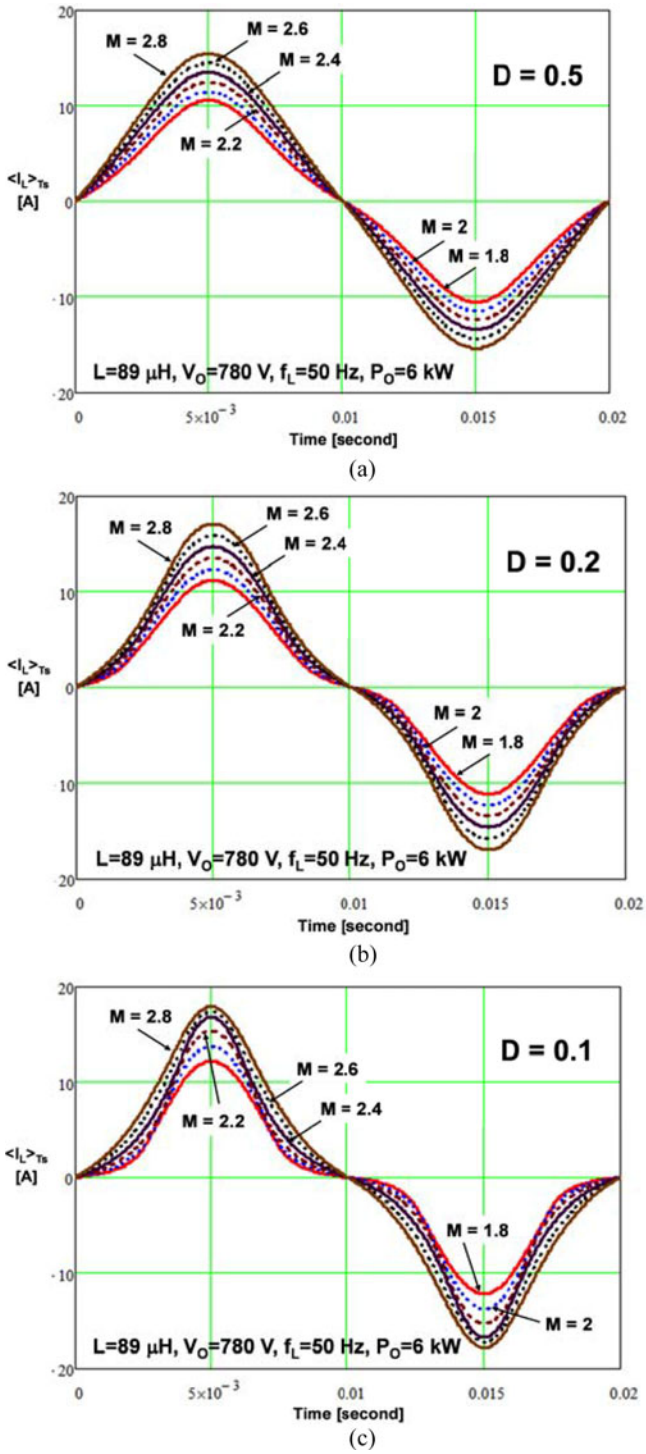

Fig. 6. Calculated average boost inductor current $<I_{L(\mathrm{AVG})}>_{Ts}$ for various input-to-output voltage conversion ratios M and: (a) $D=0.5$; (b) $D=0.2$; (c) $D=0.1$.

IV. Design Considerations

In this section, design guidelines for the proposed rectifier are outlined using the example prototype circuit that is evaluated in Section V. The evaluation prototype of the 6-kW three-phase three-level TAIPEI rectifier has been designed and built according to the following key specifications:

TABLE I
THD AND HARMONICS OF AVERAGE BOOST INDUCTOR CURRENTS SHOWN IN FIG. 6

	$D = 0.5$			$D = 0.2$			$D = 0.1$		
M	THD [%]	3rd [%]	5th–99th [%]	THD [%]	3rd [%]	5th–99th [%]	THD [%]	3rd [%]	5th–99th [%]
1.8	14.93	14.75	1.14	25.04	24.27	1.81	40.21	36.98	8.16
2	12.64	12.53	0.67	24.08	23.38	2.06	40.52	36.92	10.56
2.2	10.97	10.9	0.6	23.44	22.79	2.1	39.28	35.55	11.26
2.4	9.7	9.65	0.72	22.84	22.25	1.58	35.0	31.97	11.04
2.6	8.7	8.66	0.78	22.11	21.57	1.85	28.45	26.84	6.87
2.8	7.89	7.85	0.81	21.15	20.65	2.11	23.9	23.0	4.26

Input voltage $V_{\rm IN}$: three-phase, three-wire, 340–520 $V_{L-L,\rm RMS}$.

Output voltage V_O: 780 $V_{\rm DC}$.

Output power P_O: 6 kW at nominal input (380–480 $V_{L-L,\rm RMS}$), 5.4 kW at $V_{\rm IN} = 340V_{L-L,\rm RMS}$.

Efficiency η: >97% above 50% load.

Input-current THD: $< 5\%$.

PF: $< 98\%$.

Power density (PD): > 25 W/in^3.

A. Switching-Frequency Selection

Because the proposed rectifier employs variable switching-frequency control, both its minimum and maximum switching frequency, i.e., its frequency range, need to be selected. Generally, the selection of the minimum switching frequency is based on the tradeoff between efficiency and size, i.e., power density, whereas the maximum frequency is primarily determined considering limitations imposed by high-frequency switching losses and/or gate-drive capability.

In this design, the minimum frequency, which occurs at the minimum input voltage and full load is set at 20 kHz, which is about the lowest frequency that can make the prototype meet the specified power density. The maximum frequency is set to 250 kHz to primarily limit the switching frequency related losses. With the 250-kHz limit, the prototype rectifier can regulate the output voltage at high line down to 10% load. For loads below 10% of the full load, the burst mode or PWM operation can be applied.

B. Boost Inductor Design

Based on derivations in [24], the approximate value of boost inductance $L = L_1 = L_2 = L_3$ is given by

$$L \approx \frac{3 \cdot V_O^2}{8 \cdot f_S \cdot M \cdot P_O} \times \frac{0.48}{M - 0.92} \tag{12}$$

where P_O is the output power and M is defined in (9).

For selected switching frequency of 20 kHz at full load of 6 kW and the minimum nominal input voltage 380 $V_{L-L,\rm RMS}$, the required value of the boost inductors is approximately $L = 170$ μH. When selecting the core material for the boost inductors, it should be taken into consideration that the rectifier operates in DCM so that the pulsating currents of the boost inductors produce significantly higher core losses compared to those in continuous-conduction-mode operation. In addition, to achieve a low THD, it is necessary to maintain constant slopes of the boost-inductor currents, i.e., it is desirable that inductance value does not change with the inductor current. As a result, ferrite cores with an air gap are the best choice since they offer the lowest core loss and their permeability does not significantly change under the varying magnetic field strength.

To provide packaging flexibility, the boost inductor in each phase of the prototype circuit is implemented by two inductors connected in series. Each inductor was built using a pair of ferrite cores (PQ-40/40, 3C96) with 45 turns of Litz wire (Φ 0.1 mm, 180 strands) and 8.5-mm gaps at inner and outer legs to achieve inductance of 85 μH. The Litz wire was used to reduce the fringing-effect-induced winding loss near the gap of the inductor cores. For this inductor design, the maximum flux density which occurs at full load and the minimum input voltage is approximately 0.32 T.

C. Coupled-Inductor Design

The magnetizing inductance of coupled inductor L_C should be sufficiently large so that the ripple current in the coupled inductor does not significantly affect the rectifier operation. As shown in Fig. 1 by the "dot" convention, the two windings of inductor L_C are coupled so that the magnetic fluxes from the differential current of the two windings are cancelled. As a result, a large magnetizing inductance can be obtained by a small gap in the core without saturation.

Coupled inductor L_C was built using a pair of ferrite cores (ETD-54/28/19, 3C96) with 62 turns of Litz wire (Φ 0.1 mm, 150 strands) for each winding and 0.2-mm gap. The measured magnetizing and leakage inductances are approximately 3 mH and 182 μH, respectively. Peak magnetizing current $I_{M(\rm PK)}$ that occurs when the switching frequency is minimum is given by

$$I_{M(\rm PK)} = \frac{V_O}{8 \cdot L_M \cdot f_{S(\rm MIN)}} \tag{13}$$

where L_M is the magnetizing inductance of coupled inductor L_C and $f_{S(\rm MIN)}$ is the minimum switching frequency at full load and the minimum input voltage. According to (13), the maximum peak-to-peak magnetizing current at full load (6 kW) and the minimum input voltage ($380V_{L-L,\rm RMS}$) is approximately 1.63 A. The maximum flux density at steady-state operation is approximately 0.28 T, which gives plenty of margin from the saturation flux of the ferrite core.

D. Input Capacitor Selection

Input capacitors C_1–C_3 provide filtering of the switching-frequency ripple of the boost inductor currents and a path for their low-frequency triplen harmonics. Since the magnitude of the triplen harmonic component is much smaller than that of the ac component of the boost-inductor currents, the rating of the input capacitors is essentially determined by the RMS value of the ac component of the peak boost inductor current that occurs at full load and low line. Since in this design, the maximum RMS current of capacitors C_1–C_3 is approximately 5.5 A, a 5-μF low-ESR film capacitor (1300 Vdc/600 Vac, 10.5 A at

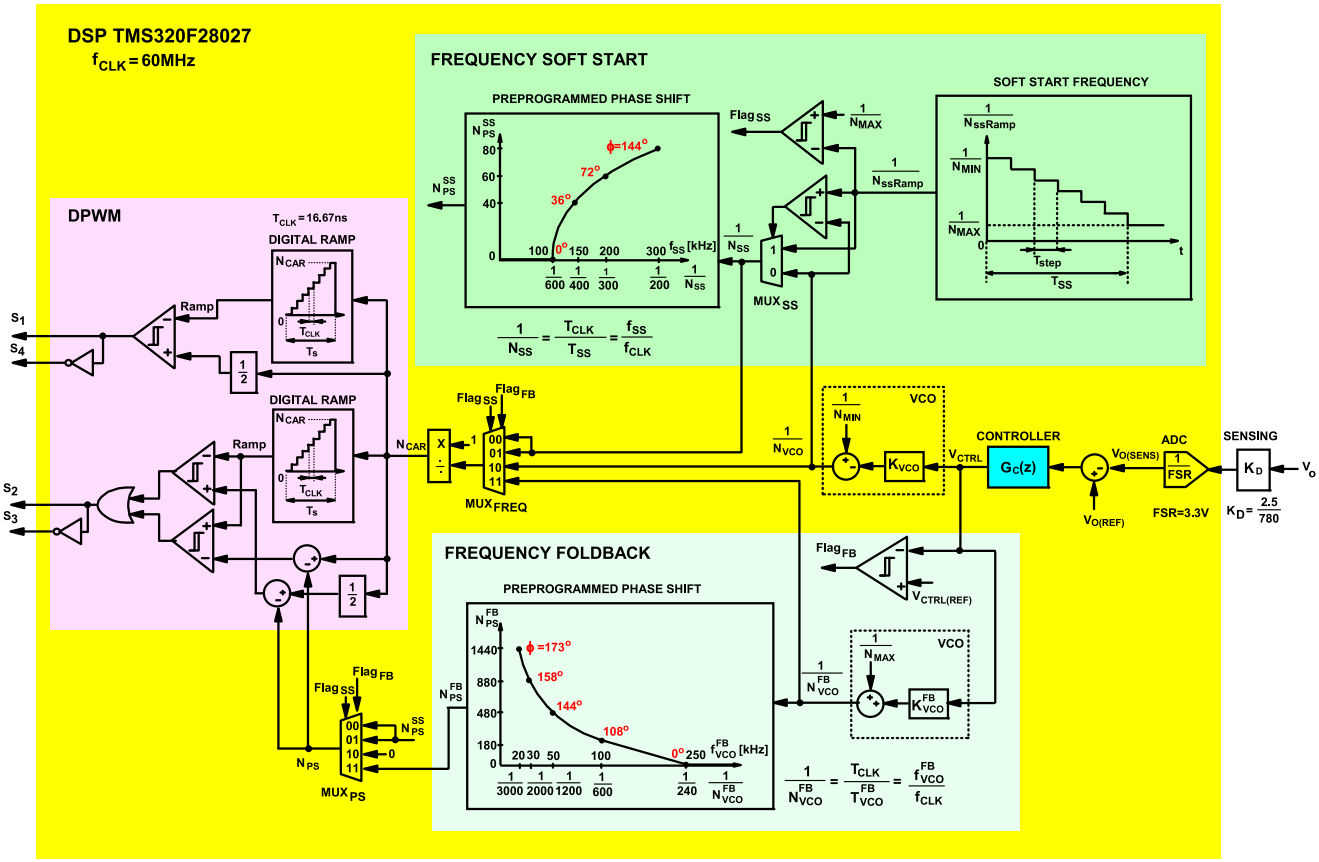

Fig. 7. Simplified block diagram of the DSP-based controller employed in prototype circuit of the proposed rectifier.

20 kHz, 10 A at 100 kHz, ESR = 9.8 mΩ) was used for each of input filter capacitors C_1, C_2, and C_3.

E. Selection of Other Capacitors

The peak current of flying capacitor C_R is equal to the sum of the ac components of the peak boost inductor current and the peak magnetizing current of coupled inductor L_C. Since in this design, the RMS value of the sum does not exceed 11 A, two 5-μF parallel-connected film capacitors (1300 Vdc/600 Vac, 10.5 A at 20 kHz, 10 A at 100 kHz) were used for flying capacitor C_R.

The current through clamping capacitor C_C is insignificant because the majority of the clamping current flows through clamping diodes D_{C1} and D_{C2} to the output capacitors. A 1-μF film capacitor (875 Vdc, 5 A at 20 kHz) was used for clamping capacitor C_C.

Three 560-μF/450-Vdc capacitors connected in parallel were used for output capacitors C_{O1} and C_{O2}. Because of additional filtering by the leakage inductance of coupled inductor L_C and capacitor C_R, the RMS current through output capacitors C_{O1} and C_{O2} is small.

F. Semiconductor Device Selection

Because the voltage stress of switches S_1–S_4 is approximately equal to one-half of output voltage V_O, i.e., it is around 390 V, it is necessary to use switches that are rated at least 500 V to maintain desirable design margin of 20%. The switches conduct the peak current of approximately 32 A. As a result, in the prototype circuit a IPW65R041CFD MOSFET (V_{DS} = 650 V, R_{DS} = 0.041 Ω, C_{OSS} = 400 pF, Q_{rr} = 1.9 μC) from Infineon was used for each switch.

Since input diodes D_1–D_6 must block the peak voltage that is approximately equal to output voltage V_O, i.e., it is around 780 V, and conduct the peak current (approximately 16 A), an C4D20120D diode (V_{RRM} = 1200 V, I_{FAVM} = 20 A) from Cree was used for each diode.

G. Control Implementation

The control of the prototype rectifier was implemented by TMS320F28027 DSP from TI. Since the rectifier naturally provides tracking of the average inductor current with the corresponding phase voltage, this DSP control consists only of a low-bandwidth feedback loop that regulates the output voltage.

Fig. 7 shows a simplified block diagram of the controller. As it can be seen in Fig. 7, variable-frequency control is implemented by a voltage-controlled oscillator (VCO) whose frequency is determined by the output V_{CTRL} of voltage controller G_{C} which processes the error between sensed output voltage $V_{O(\mathrm{SENS})}$ and its reference $V_{O(\mathrm{REF})}$. In addition, the controller implements soft start and frequency-foldback control by employing a combination of frequency modulation and phase-shift PWM. Although soft-start control can be implemented by switching-frequency control alone, i.e., by slowly decreasing

the switching frequency from the maximum frequency toward the required control frequency, combining it with PWM control enables more controllable and smooth start up. However, the frequency foldback control that is used to extend the minimum-load regulation range and/or improve light-load efficiency requires PWM control. Namely, frequency-foldback mode, i.e., the operation where the switching frequency is decreased as the load is reduced, can only be implemented if PWM control is also employed to provide regulation at a reduced output power.

In the implementation in Fig. 7, the drive signals of switches S_1–S_4 are obtained by using digital pulse-width modulator (DPWM) with two identical synchronized digital carrier ramps that are generated by counting DSP clock periods $T_{\rm CLK}$. Since the carrier ramp period $T_S = N_{\rm CAR}T_{\rm CLK}$, where $N_{\rm CAR}$ is the number of clock periods, carrier frequency f_S is proportional to $1/N_{\rm CAR}$. As shown in Fig. 7, the ramp frequency is set by multiplexer $\rm MUX_{FREQ}$ that based on the state of soft-start flag $\rm Flag_{SS}$ and frequency-foldback flag $\rm Flag_{FB}$ selects either the frequency of VCO, or the frequency of frequency-foldback $\rm VCO^{FB}$, or the frequency of the soft-start circuit. The number of clock periods $N_{\rm CAR}$ is obtained by finding the reciprocal value of the $\rm MUX_{FREQ}$ output.

The VCO transfer function is set by the selection of its maximum frequency $f_{\rm MAX}$, i.e., minimum count number $N_{\rm MIN}$, and gain $K_{\rm VCO}$. According to Fig. 7, the VCO output is given by

$$\frac{1}{N_{\rm VCO}} = \frac{1}{N_{\rm MIN}} - K_{\rm VCO}\cdot V_{\rm CTRL}. \tag{14}$$

Since

$$\frac{1}{N_{\rm VCO}} = T_{\rm CLK}\cdot f_{\rm VCO} = \frac{f_{\rm VCO}}{f_{\rm CLK}} \tag{15}$$

and

$$\frac{1}{N_{\rm MIN}} = T_{\rm CLK}\cdot f_{\rm MAX} = \frac{f_{\rm MAX}}{f_{\rm CLK}} \tag{16}$$

relationship in (14) can be written as

$$\frac{f_{\rm VCO}}{f_{\rm CLK}} = \frac{f_{\rm MAX}}{f_{\rm CLK}} - K_{\rm VCO}\cdot V_{\rm CTRL}. \tag{17}$$

As it can be seen from (17), the normalized frequency of the VCO with respect to $f_{\rm CLK}$ is a linear function of control voltage $V_{\rm CTRL}$ with negative slope $K_{\rm VCO}$. As a result, the VCO frequency increases as the control voltage decrease, i.e., as the load current decreases.

The drive signals of complementary switches S_1 and S_4 that always operate with 50% duty cycle are obtained by comparing the carrier ramp with one-half of its count value $N_{\rm CAR}$, i.e., with $0.5N_{\rm CAR}$, as shown in Fig. 7. The drive signals of complementary switches S_2 and S_3 that also always operate with 50% duty cycle but also can be phase shifted with respect to switches S_1 and S_4 are obtained by comparing the carrier ramp with $0.5N_{\rm CAR} - N_{\rm PS}$ and $N_{\rm CAR} - N_{\rm PS}$, where $N_{\rm PS}$ is proportional to phase shift φ, i.e., $N_{\rm PS} = (\varphi/360)N_{\rm CAR}$. Since the $N_{\rm PS}$ range is from 0 to $0.5N_{\rm CAR}$, phase shift φ is in the 0°–180° range. The $N_{\rm PS}$ value that is selected by $\rm MUX_{PS}$ is determined either by the soft start or frequency foldback circuit. The reason for the ramp comparison with two levels is to preserve 50% duty cycle of switches S_2 and S_3 during phase-shift operation. Namely, the ramp comparison with $0.5N_{\rm CAR} - N_{\rm PS}$ defines the beginning of the off time, whereas the comparison with $N_{\rm CAR} - N_{\rm PS}$ defines its end. Since the difference between the two levels is $0.5N_{\rm CAR}$, i.e., it is equal to one-half of the digital ramp height, the drive signals for switches S_2 and S_3 operate with 50% off time, i.e., with 50% duty cycle.

The frequency foldback circuit is activated at light loads whenever output of the controller $V_{\rm CTRL}$ falls below reference level $V_{\rm CTRL(REF)}$ and frequency foldback flag $\rm Flag_{FB}$ is set to 1. The frequency foldback circuit consists of the frequency-foldback VCO, $\rm VCO^{FB}$, and the preprogramed phase shift as a function of the VCO's frequency. The $\rm VCO^{FB}$ transfer function is set by the selection of its minimum frequency, i.e., maximum count number $N_{\rm MAX}$ and gain $K^{\rm FB}_{\rm VCO}$. It should be noted that opposite from VCO, $\rm VCO^{FB}$ is set up to decrease the frequency as the load decreases, i.e., its normalized frequency is a linear function of control voltage $V_{\rm CTRL}$ with positive slope $K_{\rm VCO}$ given by

$$\frac{f^{\rm FB}_{\rm VCO}}{f_{\rm CLK}} = \frac{f_{\rm MIN}}{f_{\rm CLK}} + K^{\rm FB}_{\rm VCO}\cdot V_{\rm CTRL}. \tag{18}$$

In the frequency-foldback mode, the output voltage is regulated by the phase-shift modulation illustrated in Fig. 2(c) by employing open-loop control where the phase shift is preprogramed as a function of the foldback frequency. Generally, any relationship where the phase shift is monotonically increasing as the foldback frequency decreases can be used.

Fig. 7 shows preprogramed phase shift dependence on the foldback frequency. As can be seen, the phase shift increases as the foldback frequency decreases. The phase-shift dependence on frequency shown in Fig. 7 is obtained by assuming a linear relationship between phase-shift count $N^{\rm FB}_{\rm PS}$ and switching-period count $N^{\rm FB}_{\rm VCO}$, i.e.,$N^{\rm FB}_{\rm PS} = 0.5(N^{\rm FB}_{\rm VCO} - 240)$, where $240 < N^{\rm FB}_{\rm VCO} < 3000$, which corresponds to the 250–20-kHz foldback-frequency range. In the prototype circuit, the maximum phase shift of $\varphi = \frac{N^{\rm FB}_{\rm PS}}{N^{\rm FB}_{\rm VCO}}\cdot 360^\circ = \frac{1440}{3000}\cdot 360^\circ = 173^\circ$ was set at minimum frequency $f^{\rm FB}_{\rm VCO} = 20$ kHz. This phase shift corresponds to the minimum duty cycle of $D_{\rm MIN} = \frac{(180^\circ - 173^\circ)}{360^\circ} \approx 0.02$.

The start up of the circuit is managed by the soft-start circuit which gradually decreases the switching frequency from the maximum frequency down to that required by the regulation loop. As shown in Fig. 7, soft-start frequency $1/N_{\rm SSRamp}$ is decreased by increasing switching period count $N_{\rm SSRamp}$ from $N_{\rm MIN}$ to $N_{\rm MAX}$ by one count every time step $t_{\rm step}$. For a given frequency range, i.e., for given $N_{\rm MIN}$ and $N_{\rm MAX}$, the duration of time step $t_{\rm step}$ is determined by desired maximum soft-start duration $T_{\rm SS}$, as $t_{\rm step} = T_{\rm SS}/(N_{\rm MAX} - N_{\rm MIN})$. In the experimental prototype circuit, the frequency soft-start range is from 300 ($N_{\rm MIN} = 200$) to 20 kHz ($N_{\rm MAX} = 3000$) and $t_{\rm step} =$ 2 ms which results in $T_{\rm SS} = 5.6$ s.

As shown in Fig. 7, during the soft-start normalized soft-start frequency $1/N_{\rm SSRamp} = f_{\rm SS}/f_{\rm CLK}$ is compared with VCO's normalized frequency $1/N_{\rm VCO} = f_{\rm VCO}/f_{\rm CLK}$ and the higher

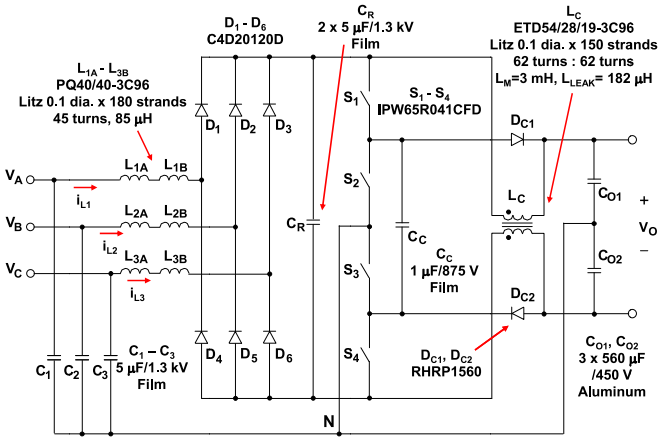

Fig. 8. Experimental prototype circuit of the proposed rectifier.

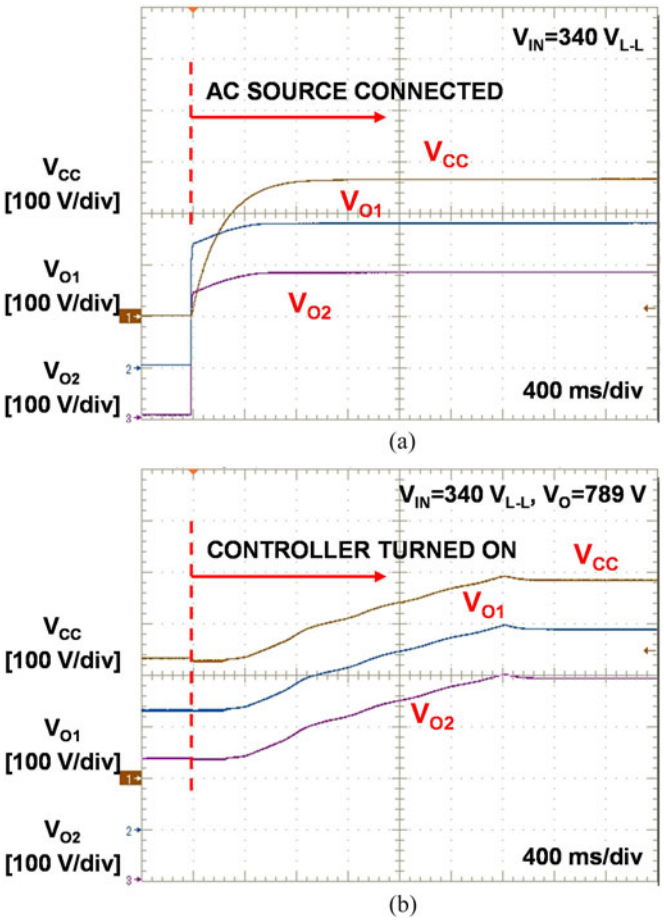

Fig. 9. Measured voltage waveforms of clamping capacitor C_C and output capacitors C_{O1} and C_{O2} during start up: (a) after ac source is connected and (b) after controller is turned on. Time scale is 400 ms/div.

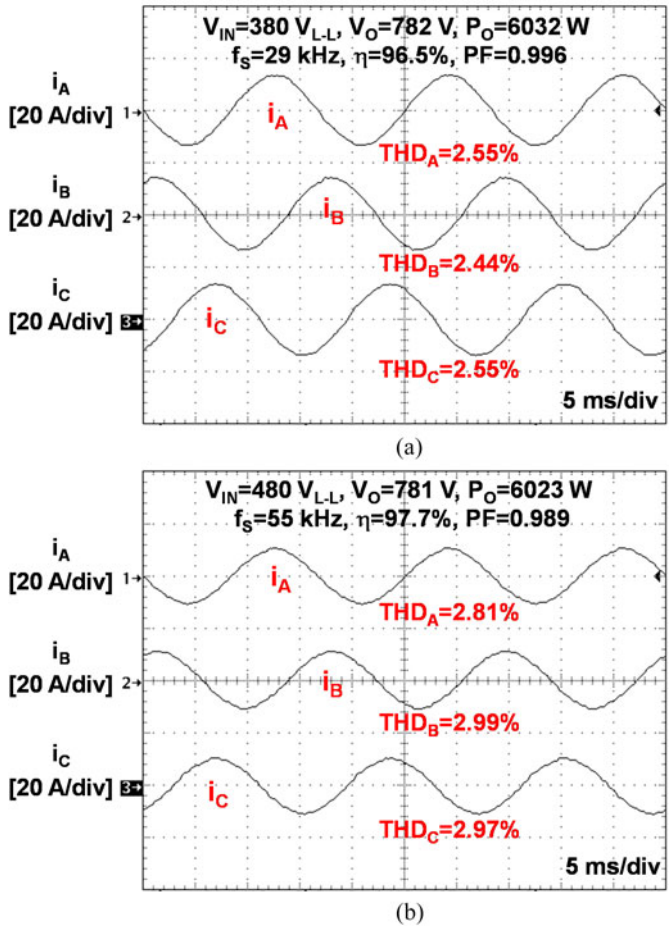

Fig. 10. Measured input-current waveforms at full power for three-phase line-to-line RMS input voltage: (a) 380 V and (b) 480 V. Time scale is 5 ms/div.

frequency is selected by $\mathrm{MUX_{SS}}$ which is then passed to the DPWM since during start up $\mathrm{Flag_{SS}} = 0$ and $\mathrm{Flag_{FB}} = 0$. Generally, at start up, the VCO frequency is at the minimum until the controller starts responding by decreasing its output and the VCO frequency starts increasing. Since at the beginning of start up the soft-start frequency is greater than the frequency of VCO, the soft-start circuit determines the switching frequency. When the frequency of VCO becomes larger than the decreasing soft-start frequency, the control loop determines the switching frequency. This implementation of soft start offers seamless transition from the soft start control to the feedback-loop control.

Furthermore to enable as smooth as possible soft-start control, the open-loop phase-shift control is also implemented alongside the frequency-modulation control. As shown in Fig. 7, the preprogramed soft-start phase shift is maximum at the maximum soft-start frequency and decreases as the soft-start frequency decreases. The phase-shift dependence on frequency shown in Fig. 7 is obtained by assuming a linear relationship between phase-shift count $N_{\mathrm{PS}}^{\mathrm{SS}}$ and switching-period count N_{SS}, i.e., $N_{\mathrm{PS}}^{\mathrm{SS}} = -0.2(N_{\mathrm{SS}} - 600)$, where $200 < N_{\mathrm{SS}} < 3000$, which corresponds to the 300–20-kHz soft-start frequency range. In the prototype circuit, the maximum phase shift of $\varphi = \frac{N_{\mathrm{PS}}^{\mathrm{SS}}}{N_{\mathrm{SS}}} \cdot 360^\circ = \frac{80}{200} \cdot 360^\circ = 144^\circ$ was set at maximum frequency $f_{\mathrm{SS}} = 300$ kHz. This phase shift corresponds to the minimum duty cycle of $D_{\mathrm{MIN}} = \frac{(180^\circ - 144^\circ)}{360^\circ} = 0.1$.

The controller is design by applying analog-redesign approach, i.e., by designing controller G_C in the s-domain and

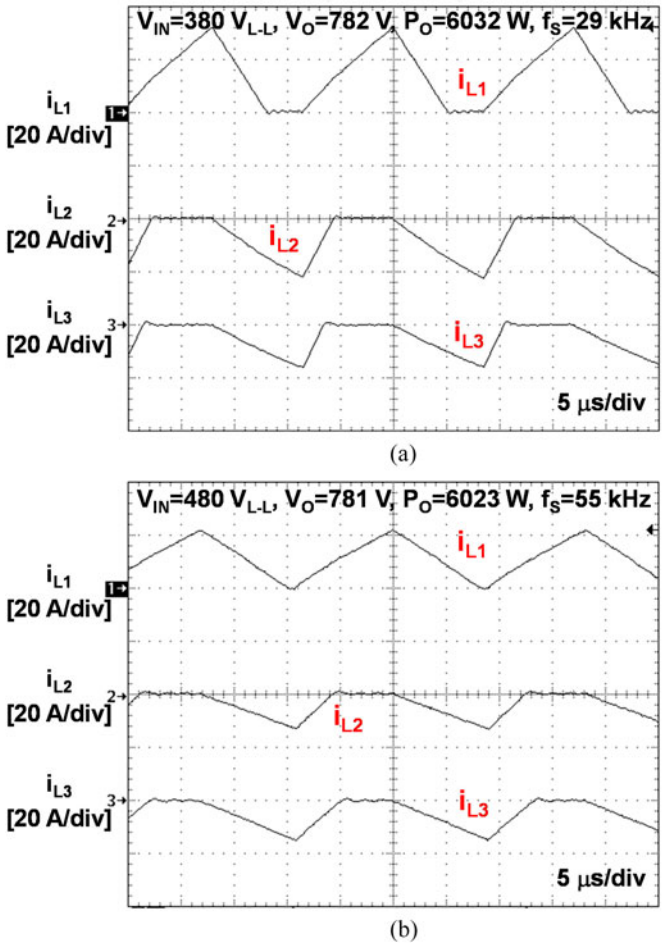

Fig. 11. Measured waveforms of inductor currents i_{L1}, i_{L2}, and i_{L3} at full power for three-phase line-to-line RMS input voltage: (a) 380 V; and (b) 480 V.

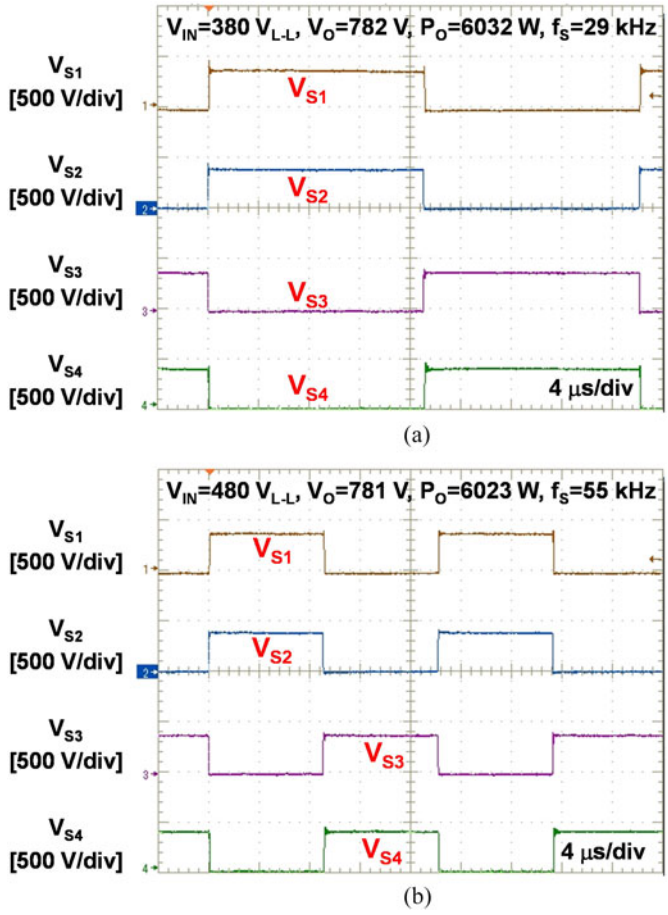

Fig. 12. Measured waveforms of switch voltages V_{S1}, V_{S2}, V_{S3}, and V_{S4} for three-phase line-to-line RMS input voltage: (a) 380 V; and (b) 480 V.

mapping it in the z-domain. The equivalent s-domain voltage-loop gain of the control loop of the experimental converter is

$$T_V(s) = K_D \cdot \frac{1}{\text{FSR}} \cdot G_C(s) \cdot K_{\text{VCO}} \cdot G_{\text{PS}}(s) \cdot e^{-sT_D} \approx K_D \cdot \frac{1}{\text{FSR}} \cdot G_C(s) \cdot K_{\text{VCO}} \cdot G_{\text{PS}}(s) \quad (19)$$

where K_D is the sensing gain of the output voltage, FSR is the full-scale range of analog-to-digital (ADC) converter, $G_{\text{PS}}(s)$ is the low-frequency power-stage small-signal transfer function, and e^{-sT_D} is the total digital-loop delay that includes ADC conversion time, DSP computational time, and the delayed update of DPWM to achieve synchronization to the resetting of DPWM ramp. Since in the experimental circuit, the sampling frequency $f_{\text{SAMPL}} = 25$ kHz is much greater than the desired 10-Hz bandwidth of the loop, the digital-loop delay can be neglected since it has no measurable effect on the voltage-loop phase margin.

For a resistive load, power stage small-signal transfer function $G_{\text{PS}}(s)$ is a single-pole transfer function

$$G_{\text{PS}}(s) = K_{\text{PS}} \frac{1}{1 + \frac{s}{2 \cdot \pi \cdot f_{\text{PO}}}}. \quad (20)$$

By using small-signal measurements, it was estimated that for the experimental circuit at full power of 6 kW and at line-to-line voltage of 380 V, power-stage gain $K_{\text{PS}} = 0.052$ and power-stage pole frequency $f_{\text{P0}} = 0.4$ Hz.

To compensate the loop, two-pole one-zero controller, i.e., PI controller with high-frequency pole, was used. The controller's s-domain transfer function is

$$G_C(s) = \frac{K}{s} \left(\frac{1 + \frac{s}{2 \cdot \pi \cdot f_Z}}{1 + \frac{s}{2 \cdot \pi \cdot f_P}} \right). \quad (21)$$

To obtain 10-Hz bandwidth, the controller parameters were selected as $K = 36$, $f_Z = 2$ Hz, and $f_P = 2$ kHz.

Since the sampling frequency in the prototype circuit is $f_{\text{SAMPL}} = 25$ kHz, the controller's z-domain transfer function obtained by bilinear (Tustin's) transformation that is coded in the DSP is

$$G_C(z) = 0.201 \cdot \frac{2.882 + 1.448 \cdot 10^{-3} \cdot z^{-1} - 2.881 \cdot z^{-2}}{1 - 1.598 \cdot z^{-1} + 0.598 \cdot z^{-2}}. \quad (22)$$

Finally, it should be noted that the control signals at the output of the DSP controller are coupled to the gate-to-source voltage of the corresponding switches with SI8235 drivers from Silicon Labs and that the output overvoltage protection and switch

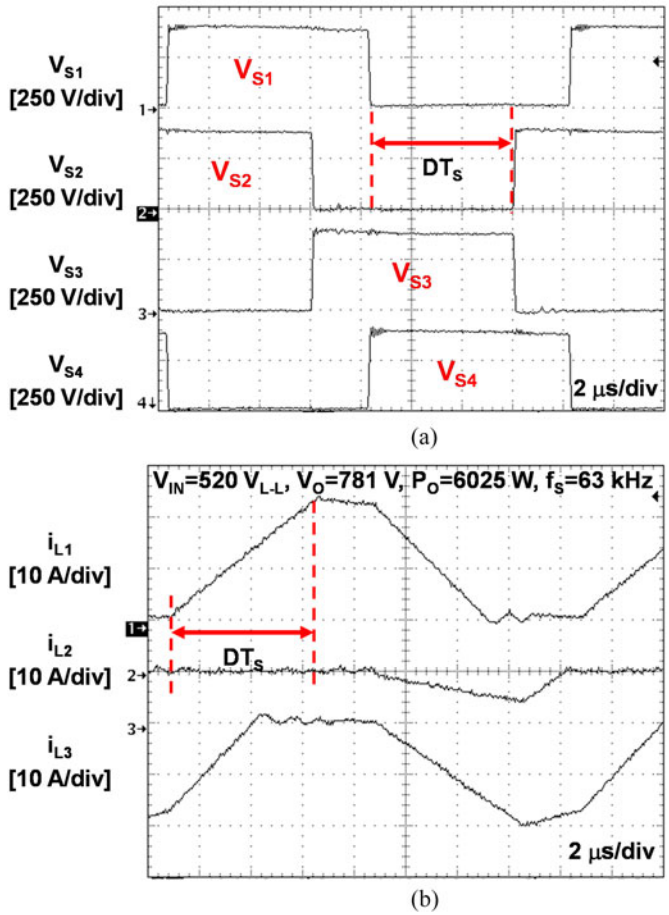

Fig. 13. Measured waveforms at full power for three-phase line-to-line RMS input voltage 520 V of: (a) switch voltages V_{S1}, V_{S2}, V_{S3}, and V_{S4}; (b) inductor currents i_{L1}, i_{L2}, and i_{L3}. It should be noted that phase shift between switch pairs S_1 and S_4 and S_2 and S_3 is increased to reduce switching frequency at above nominal input voltage 480 V.

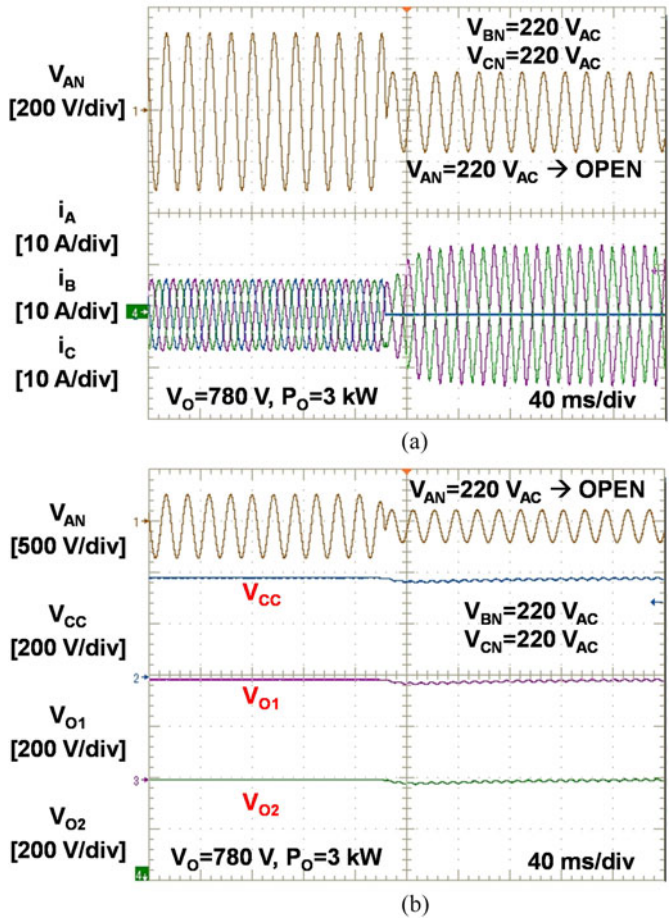

Fig. 14. Measured (a) input current waveforms and (b) voltage waveforms of clamping capacitor C_C and two serially connected output capacitors C_{O1} and C_{O2} with phase A voltage waveform when rectifier delivers 3 kW from three-phase line that initially has balanced 380 V_{L-L}. After transient command, phase A line is disconnected.

current overcurrent protection are implemented outside the DSP, i.e., by using analog comparators. Current-sensing transformers with turns ratio 1:100 were used for sensing current of the switches.

V. Experimental Results

The performance of the proposed rectifier was evaluated on a 6-kW prototype circuit that was designed according to the key specifications listed in Section IV. Fig. 8 shows the power-stage schematics of the experimental prototype circuit along with the component information.

Fig. 9 shows the measured voltage waveforms of clamping capacitor C_C and two serially connected output capacitors C_{O1} and C_{O2} during start up. Because voltages across those capacitors limit the peak voltage stresses of the primary switches, voltages V_{CC}, V_{O1}, and V_{O2} should always be equal to one half of the output voltage even during the start up. Fig. 9(a) shows the V_{CC}, V_{O1}, and V_{O2} voltage waveforms immediately after the ac source is connected and Fig. 9(b) shows the same waveforms after the controller is subsequently turned on. As it can be seen from Fig. 9(a) and (b), during the entire start-up period, voltages V_{O1}, V_{O2}, and V_{CC} are equal to one-half of the output voltage.

Fig. 10(a) and (b) shows the measured input-current waveforms of the experimental circuit operating at full power from 380 $V_{L-L,\mathrm{RMS}}$ and 480 $V_{L-L,\mathrm{RMS}}$ input, respectively. It should be noted that input currents i_A, i_B, and i_C are measured between the three-phase ac source and the input EMI filter of the rectifier which is not shown in Fig. 8. The measured full-power THDs of the input currents are below 3% for both input voltages. Fig. 11 shows the measured current waveforms of boost inductors L_1, L_2, and L_3 at full power. The measured waveforms and the ideal waveforms in Fig. 5 differ during the time intervals when the inductor currents are supposed to be zero. This difference is caused by the parasitic resonance of the junction capacitances of the reverse-biased input bridge rectifiers D_1–D_6 with the boost inductors. This current ringing increases slightly the THD of the input current and, if necessary, can be minimize by selecting rectifiers with smaller junction capacitances. Fig. 12 shows the waveforms of the drain voltages of switches S_1–S_4. It can be seen that all the switch voltages are well clamped to one half of output voltage V_O.

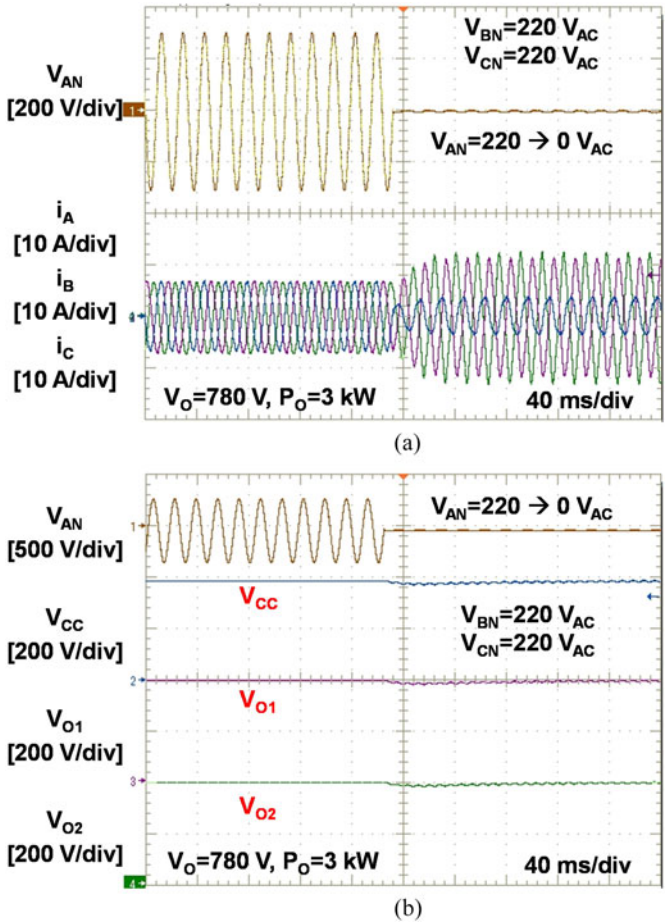

Fig. 15. Measured (a) input current waveforms and (b) voltage waveforms of clamping capacitor $C_{\rm C}$ and two serially connected output capacitors C_{O1} and C_{O2} with phase A voltage waveform when rectifier delivers 3 kW from three-phase line that initially has balanced 380 V_{L-L}. After transient command, one phase voltage drops to zero.

The output-voltage regulation in the prototype circuit is implemented by a combination of variable-switching-frequency and phase-shift PWM control. The phase-shift PWM control is employed at light load and can also be employed at high-input voltage to limit the switching-frequency range. Fig. 13(a) shows the waveforms of the drain voltages of switches S_1–S_4 at full power and 520 $V_{L-L,\rm RMS}$ input. As it can be seen from Fig. 13(a), in the phase-shift mode, each pair of switches S_1 and S_4 and S_2 and S_3 is switched in a complementary fashion with a fixed duty ratio of approximately 50% with the switching instants of the outer switch S_1 and S_4 pair phase shifted with respect to the corresponding switching instants of the inner switch S_2 and S_3. Fig. 13(b) shows the measured current waveforms of boost inductors L_1, L_2, and L_3 that correspond to voltage waveform shown in Fig. 13(a). The measured waveforms shown in Fig. 13(a) and (b) match well with the ideal waveforms shown in Fig. 5.

The operation of the circuit with unbalanced line voltages is illustrated in Figs. 14 and 15. Fig. 14(a) shows input-current waveforms of the experimental circuit with phase A open. Even under this extreme unbalanced condition, the measured THD of the remaining two phases is below 10%. Fig. 14(b) shows the measured voltage waveforms of clamping capacitor C_C and two serially connected output capacitors C_{O1} and C_{O2} during the same transient of phase A open. As it can be seen from Fig. 14(b), during the entire transient period, voltages V_{O1}, V_{O2}, and $V_{\rm CC}$ are well balanced and equal to one half of the output voltage. Fig. 15(a) and (b) illustrates operation of the circuit with one phase shorted (voltage of phase A set to zero). Under this unbalanced condition, the measured THD of the line currents is still well below 10% and voltages V_{O1}, V_{O2}, and $V_{\rm CC}$ are well balanced and equal to one-half of the output voltage as show in Fig. 15(b).

TABLE II
MEASURED THD [%] OF THE PROPOSED RECTIFIER

	Output Power [kW]						
Input Voltage [V_{L-L}]	0.5	1	2	3	4	5	6
380	4.51	4.33	3.91	3.18	3.05	2.78	2.54
480	13.32	9.77	5.48	4.95	4.62	4.39	2.81

TABLE III
MEASURED PF [%] OF THE PROPOSED RECTIFIER

	Output Power [kW]						
Input Voltage [V_{L-L}]	0.5	1	2	3	4	5	6
380	72.07	89.56	96.37	98.33	99.01	99.3	99.55
480	69.97	84.87	93.76	96.95	98.12	98.46	98.89

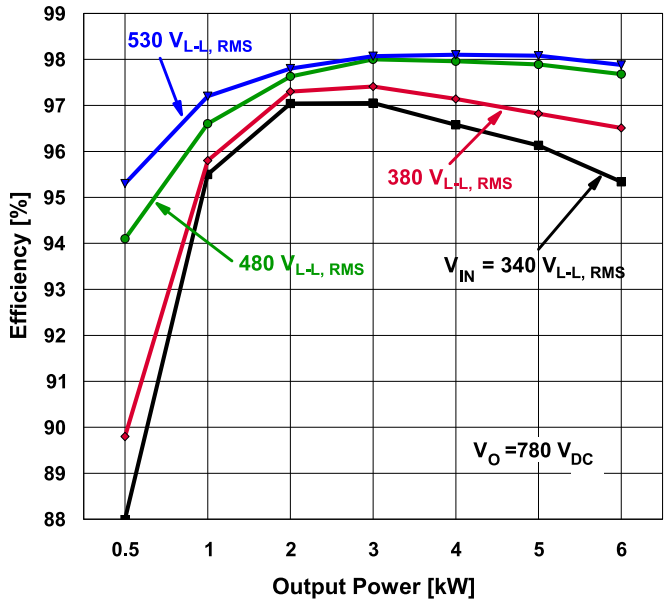

Fig. 16. Measured efficiencies of the experimental prototype as functions of output power.

Tables II and III show measured THD and PF at nominal input voltages, respectively. The proposed rectifier achieves less than 5% input-current THD at the nominal input

($380/480 V_{L-L,\mathrm{RMS}}$) and above 50% of the full load. The THD at lighter load can be further improved by employing a low junction capacitance rectifiers in the input bridge.

Finally, the measured efficiencies of the proposed rectifier as a function of the output power for 340 $V_{L-L,\mathrm{RMS}}$, 380 $V_{L-L,\mathrm{RMS}}$, 480 $V_{L-L,\mathrm{RMS}}$, and 520 $V_{L-L,\mathrm{RMS}}$ input are plotted in Fig. 16. The measured peak efficiency at 480 $V_{L-L,\mathrm{RMS}}$ is 98.0%, whereas the peak efficiency at 380 $V_{L-L,\mathrm{RMS}}$ is 97.4%. For both input voltages, the peak efficiency occurs at half load.

VI. Summary

In this paper, a new three-phase four-switch three-level ZVS PFC DCM boost rectifier has been introduced and its analysis of operation, design considerations, and performance evaluation have been presented. In the proposed rectifier, all semiconductor switches operate with ZVS and their off-state voltage is always clamped to one-half of the output voltage. To reduce the switching-frequency range and maximize the light-load efficiency, the control is implemented by a combination of variable-switching frequency and phase-shift PWM control.

The proposed soft-switched rectifier exhibits efficiency in the 96%–98% range and achieves less than 5% input-current THD over the nominal input (380–480 $V_{L-L,\mathrm{RMS}}$) and above 50% of the full load. The performance evaluation was done on a three-phase 6-kW prototype designed for the 340–520-$V_{L-L,\mathrm{RMS}}$ line-voltage range. The measured full-load input-current THD at 380 $V_{L-L,\mathrm{RMS}}$ and 480 $V_{L-L,\mathrm{RMS}}$ were 2.5% and 2.9%, respectively. The measured peak efficiency at 480 $V_{L-L,\mathrm{RMS}}$ is 98.0%, whereas the peak efficiency at 380 $V_{L-L,\mathrm{RMS}}$ is 97.4%.

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