Maximum Boost Control of Diode-Assisted Buck–Boost Voltage-Source Inverter With Minimum Switching Frequency

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***Abstract*—Diode-assisted buck–boost voltage-source inverter achieves high voltage gain by introducing a switch-capacitor based high step-up dc–dc circuit between the dc source and inverter bridge. As for the unique structure, various pulse width modulation (PWM) strategies are developed with regard to the chopped intermediate dc-link voltage. In order to maximize voltage gain and increase efficiency, this paper proposes a novel PWM strategy. It regulates the average value of intermediate dc-link voltage in one switching time period (T_s) the same as the instantaneous maximum value of three-phase line voltage by controlling the front boost circuit. Then, the equivalent switching frequency of power devices in the inverter bridge can be reduced to $1/3f_s(f_s = 1/T_s)$. The operating principle and closed-loop controller design are analyzed and verified by simulations and experiments. Compared with existing PWM strategies, the new control strategy demonstrates less power device requirement and higher efficiency in high voltage gain applications. It is a more competitive topology for wide range dc/ac voltage regulation in renewable energy applications. Furthermore, with new control strategy, the dc-side inductor current and capacitor voltage contains six-time line-frequency ripples. To overcome the undesired influence of low frequency ripples, it is also suitable for 400–800 Hz medium frequency aircraft and vessel power supply system.**

***Index Terms*—Closed-loop control, dc/ac conversion, high efficiency, minimum switching frequency, modulation strategy, voltage gain.**

I. Introduction

GIVEN the efficiency and environmental benefits of emerging solar and fuel cell technology, the distributed generation systems based on the renewable energy sources have rapidly developed in recent years [1]–[3]. In photovoltaic (PV) systems, it is difficult to realize a series connection of the PV cells without incurring a shadow effect [3]. Fuel cells and lightweight battery power supply systems are promising in future hybrid electric vehicle, more-electric aircraft and vessel. However, the obvious characteristic of these dc sources is low voltage supply with wide range voltage drop. Power electronic interface has to regulate the amplitude and frequency to obtain required high ac utility voltage. These applications raise stringent requirements for power converters such as low cost, high efficiency and wide range voltage buck–boost regulation ability. Traditional voltage-source inverter (VSI) can only perform buck voltage regulation. Thus, various novel and improved dc–ac topologies with buck–boost capability as well as the related control methods have been proposed to solve the issues [4]–[19].

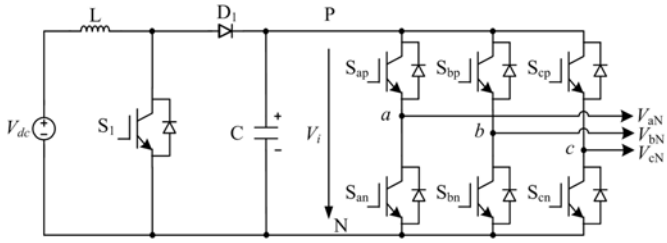

Fig. 1. Conventional two-stage buck–boost VSI.

Traditional two-stage VSI shown in Fig. 1 obtains the required output voltage by introducing dc–dc boost circuit in the front. In view of additional power conversion stage increasing cost and lowering efficiency, a family of *Z*-source inverter [4]–[6] introduces a unique impedance network between the dc source and the inverter bridge. It achieves the desired output voltage that is larger than the available dc source voltage by adopting shoot-through (ST) operation mode. *Z*-source inverter provides a potential cheap and single-stage power conversion. However, the ST state limits the modulation index and accompanies large ST current. Literature [7] makes comparison between traditional VSI and *Z*-source inverter based on electric vehicle driver system. The results reveal that *Z*-source inverter demonstrates low cost and high efficiency under relatively low voltage boost ratio range (1–2).

Although both of them can boost output voltage to any desired value without upper limitation in theory, the degradation of efficiency and increasing requirement of switching devices are prominent under high voltage gain. Literature [8] proposed diode-assisted buck–boost VSI and related modulation strategy. The main circuit is shown in Fig. 2. It extends voltage gain and avoids extreme boost duty ratio by introducing a

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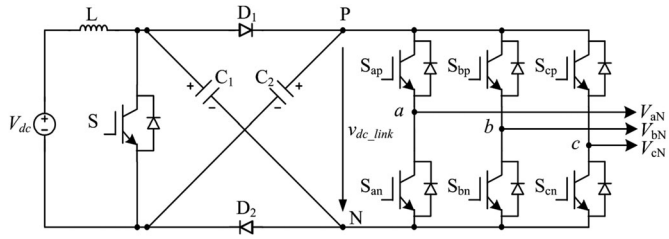

Fig. 2. Diode-assisted buck–boost VSI.

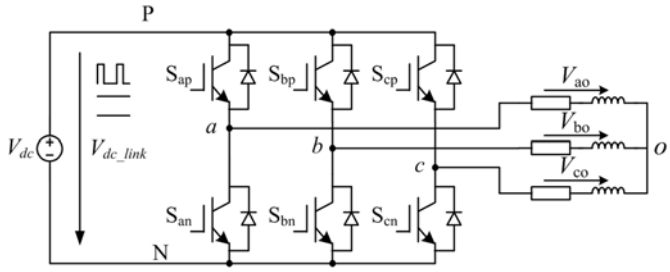

Fig. 3. Three-phase VSI.

switch-capacitor based high step-up dc–dc circuit between the dc source and inverter bridge. The diodes are naturally conducting to perform capacitive charging in parallel and discharging in series to achieve high voltage gain. In view of chopped intermediate dc-link voltage, the front boost circuit and inverter bridge needs coordinate control. The existing typical modulation strategy in [8] just utilizes intermediate dc-link voltage for ac output in the duration when the two capacitors are connected in series. Therefore, it has the drawback of relatively low dc-link voltage utilization. In order to increase voltage gain as well as to reduce voltage stress of switching devices, Zhang and Liu [9] proposed the improved PWM strategy to further utilize the intermediate dc-link voltage for ac output in the duration when the two capacitors are connected in parallel. It increases the dc-link voltage utilization and reduces the voltage stress of switching devices. However, it introduces the additional switching transient and increases the switching frequency. In order to achieve the increased efficiency as well as to maximize the voltage gain, this paper proposes a novel modulation strategy. It regulates the average value of intermediate dc-link voltage in one switching time period T_s the same as the instantaneous maximum value of three-phase line voltage by controlling the front boost circuit. Then, the equivalent switching frequency of power devices in the inverter bridge can be reduced to $1/3f_s(f_s = 1/T_s)$. Compared with the existing modulation strategies, new proposed maximum boost control strategy contributes to less switching device requirement and higher efficiency in high voltage gain applications.

This paper first reviews the basic modulation principle of conventional three-phase VSI in Section II, and then proposes a novel modulation strategy for diode-assisted buck–boost VSI in Section III. The brief comparison between the novel modulation strategy and existing modulation strategies is conducted in Section IV. The closed-loop controller design of diode-assisted buck–boost VSI with new modulation strategy is investigated in Section V. Simulation and experimental verification are presented in Section VI. The conclusion of this study is outlined in the last section.

II. Modulation Principle of Conventional Three-Phase VSI

Fig. 3 shows the main circuit of conventional three-phase VSI. For VSI supplying three-phase balanced load, three-phase symmetrical output voltage and output power can be expressed

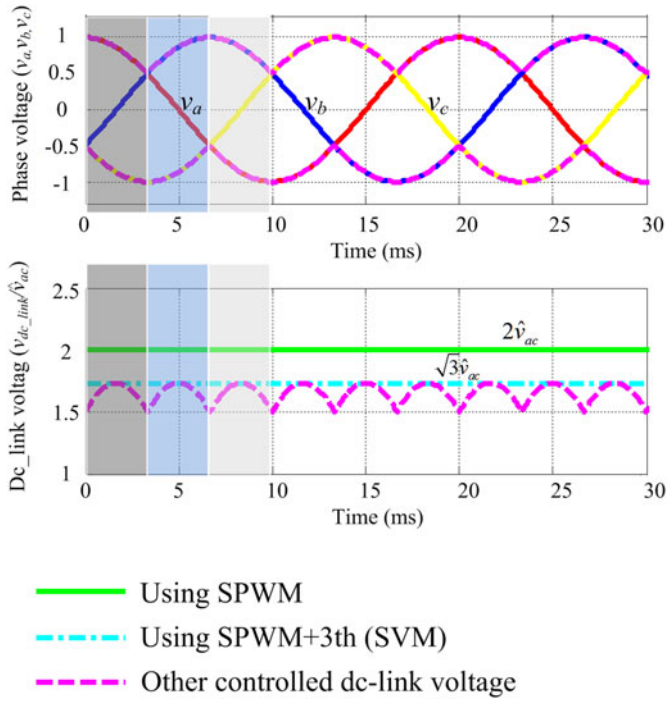

Fig. 4. Available dc-link voltage of the inverter bridge.

as follows:

$$\begin{cases} v_{\rm ao}(\omega t) = \hat{v}_{\rm ac} \cdot \cos(\omega t) \\ v_{\rm bo}(\omega t) = \hat{v}_{\rm ac} \cdot \cos\left(\omega t - \dfrac{2}{3}\pi\right) \\ v_{\rm co}(\omega t) = \hat{v}_{\rm ac} \cdot \cos\left(\omega t + \dfrac{2}{3}\pi\right) \end{cases} \tag{1}$$

$$P_o = \frac{3}{2} \cdot \hat{v}_{\rm ac} \cdot \hat{i}_{\rm ac} \cos(\varphi), \tag{2}$$

where $\hat{v}_{\rm ac}$ and $\hat{i}_{\rm ac}$ are the peak value of phase voltage and current, respectively. $\cos(\varphi)$ is the load power factor. $\omega = 2\pi f_{\rm line}$, and $f_{\rm line}$ is the fundamental frequency of output phase voltage.

Fig. 4 shows the output three-phase voltage and available minimum dc-link voltage for conventional three-phase VSI. For three-phase VSI using carrier wave-based sinusoidal pulse-width modulation (SPWM), the minimum constant dc-link voltage of inverter bridge is twice the peak value of output phase voltage $2\hat{v}_{\rm ac}$, which is the green solid line as shown in Fig. 4.

TABLE I
SWITCHING STATES OF POWER DEVICES IN THE INVERTER BRIDGE

Phase angle	$0° \le \theta \le 60°$	$60° \le \theta \le 120°$	$120° \le \theta \le 180°$	$180° \le \theta \le 240°$	$240° \le \theta \le 300°$	$300° \le \theta \le 360°$
Mod A	$S_{\rm ap}=1; S_{\rm an}=0$	$S_{\rm ap}S_{\rm an}=\rm PWM$	$S_{\rm ap}=0; S_{\rm an}=1$	$S_{\rm ap}=0; S_{\rm an}=1$	$S_{\rm ap}S_{\rm an}=\rm PWM$	$S_{\rm ap}=1; S_{\rm an}=0$
Mod B	$S_{\rm bp}S_{\rm bn}=\rm PWM$	$S_{\rm bp}=1; S_{\rm bn}=0$	$S_{\rm bp}=1; S_{\rm bn}=0$	$S_{\rm bp}S_{\rm bn}=\rm PWM$	$S_{\rm bp}=0; S_{\rm bn}=1$	$S_{\rm bp}=0; S_{\rm bn}=1$
Mod C	$S_{\rm cp}=0; S_{\rm cn}=1$	$S_{\rm cp}=0; S_{\rm cn}=1$	$S_{\rm cp}S_{\rm cn}=\rm PWM$	$S_{\rm cp}=1; S_{\rm cn}=0$	$S_{\rm cp}=1; S_{\rm cn}=0$	$S_{\rm cp}S_{\rm cn}=\rm PWM$

The fundamental frequency of three-phase output voltage $f_{\rm line}$ is 50 Hz for this analysis. Using SPWM with third harmonic injection or space vector modulation to increase dc-link voltage utilization, the minimum constant dc-link voltage is $\sqrt{3}\hat{v}_{\rm ac}$, which is the blue dot-dash line as shown in Fig. 4. Besides, there is another available dc-link voltage which is the instantaneous maximum value of the three-phase line voltage. It is the magenta dashed line shown in Fig. 4 which changes with six-time the line frequency and can be expressed as follows:

$$V_{\rm dc\_link}(\omega t) = \sqrt{3}\cdot\hat{v}_{\rm ac}\cdot\cos\left(\theta-\frac{\pi}{6}\right) \tag{3}$$

where $\theta = \omega t\%(\pi/3)$.

If the average dc-link voltage of the inverter bridge in one switching time period T_s can be accurately controlled as the time-varying six-pulse magenta dashed line shown in Fig. 4, the upper switch in the leg of the maximum phase voltage ($v_{\rm max}$) and the lower switch in the leg of minimum phase voltage ($v_{\rm min}$) are always turned on, and the upper and lower switches in the rest phase leg ($v_{\rm mid}$) are controlled with PWM signal. The switching states of three-phase VSI in each sextant are listed in Table I. Taking the first sextant for example, the instantaneous dc-link voltage is the line voltage ($v_{\rm ao}-v_{\rm co}$). Thus, $S_{\rm ap}$ and $S_{\rm cn}$ are always turned on; $S_{\rm bp}$ and $S_{\rm bn}$ are controlled with PWM to regulate the output phase voltage v_b. In each sextant, only one phase leg operates under complementary PWM mode. The corresponding duty ratio of upper and lower switch $d_{\rm Sip}, d_{\rm Sin}$ are expressed as (4). The equivalent switching frequency of power devices in the inverter bridge can be reduced to $1/3f_s (f_s = 1/T_s)$

$$\begin{cases} d_{\rm Sip}(\omega t) = \dfrac{v_{\rm mid}(\omega t)-v_{\rm min}(\omega t)}{v_{\rm max}(\omega t)-v_{\rm min}(\omega t)} \\ d_{\rm Sin}(\omega t) = 1-d_{\rm Sip}(\omega t) \end{cases} \tag{4}$$

where in each sextant, $v_{\rm min}(\omega t)$ is minimum of output three-phase voltage; $v_{\rm max}(\omega t)$ is maximum of output three-phase voltage; $v_{\rm mid}(\omega t)$ is middle of output three-phase voltage; *i* representing the phase leg of middle voltage $v_{\rm mid}(\omega t)$, changes between *a*, *b*, and *c*.

For conventional two-stage buck–boost VSI, in the intermediate dc-link, there is a large aluminum electrolytic capacitor to absorb current harmonics with pulse frequency, and to compensate the transient difference between the power requirement of the inverter bridge and the output power of the front boost circuit [13]. Therefore, the intermediate dc-link voltage is always kept constant by adjusting the fixed boost duty ratio in steady state. It is difficult or impossible to control the intermediate dc-link voltage like six-pulse waveform.

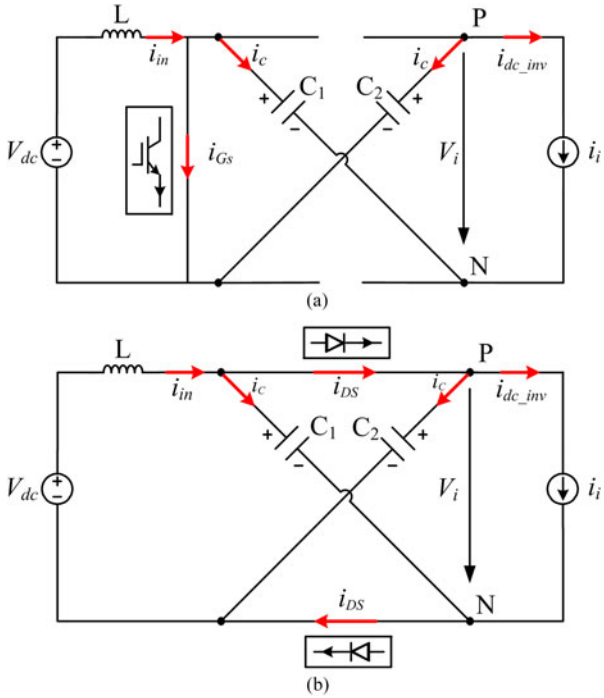

Fig. 5. Equivalent circuit of diode-assisted buck–boost VSI viewed from the dc link of the inverter bridge. (a) During S_1 = ON interval. (b) During S_1 = OFF interval.

III. NOVEL MODULATION STRATEGY OF DIODE-ASSISTED BUCK–BOOST VSI

The operation principles of diode-assisted buck–boost VSI have been described in literature [8], [9]. Fig. 5 shows two equivalent circuits seen from the dc link of the inverter bridge according to the switching state of S. When S is turned on, the inductor absorbs energy from the dc source and both capacitors are connected in series to supply the inverter bridge $v_{\rm dc\_link} = 2V_C$. When S is turned off, the energy accumulated in the inductor is transferred to capacitors and both capacitors are connected in parallel to supply the inverter bridge $v_{\rm dc\_link} = V_C$. Thus, the average intermediate dc-link voltage in one switching time period is

$$\bar{v}_{\rm dc\_link} = \frac{1}{T_s}\cdot\left(\int_0^{d_{\rm son}\cdot T_s} 2V_C\,dt + \int_{d_{\rm son}\cdot T_s}^{T_s} V_C\,dt\right) = (1+d_{\rm son})\cdot V_C \tag{5}$$

where $d_{\rm son}$ is the on-state duty ratio of switching device S.

The voltage gain of diode-assisted buck–boost VSI is defined as the ratio of the output peak phase voltage over half of

dc-source voltage

$$G = \frac{\hat{v}_{\rm ac}}{V_{\rm dc}/2} = \frac{2\hat{v}_{\rm ac}}{V_{\rm dc}}. \tag{6}$$

With the existing PMW strategies presented in [8] and [9], the average value of $v_{\rm dc\_link}$ in one switching time period T_s is constant for given output ac reference voltage. In order to reduce the switching commutations of power devices in the inverter bridge, which is in favor of the converter with high efficiency, it is possible to adjust the boost duty ratio $d_{\rm son}$ to regulate the average value of $v_{\rm dc\_link}$ to meet (3). For simple analysis, it is assumed the capacitance of C_1 and C_2 is large enough and the voltage is almost constant in steady state. Seen from (5), the average dc-link voltage of the inverter bridge in one switching time period T_s can be regulated intermediately by adjusting boost duty ratio

$$(1 + d_{\rm son}(\omega t)) \cdot V_C = \sqrt{3} \cdot \hat{v}_{\rm ac} \cdot \cos\left(\theta - \frac{\pi}{6}\right) \tag{7}$$

where $\theta = \omega t \% (\pi/3)$.

In steady state, the capacitor voltage V_C is related to the average value of duty ratio of S = ON, which can be expressed as

$$V_{C1} = V_{C2} = V_C = \frac{V_{\rm dc}}{1 - d_{\rm avg}}. \tag{8}$$

In which, the average value of the boost duty ratio $d_{\rm avg}$ can be calculated by integrating $d_{\rm son}(\omega t)$ in (7) in one sextant

$$\begin{aligned} d_{\rm avg} &= \frac{3}{\pi} \cdot \int_0^{\pi/3} \left(\sqrt{3} \cdot \frac{\hat{v}_{\rm ac}}{V_C} \cdot \cos\left(\omega t - \frac{\pi}{6}\right) - 1\right) \cdot d\omega t \\ &= \frac{3\sqrt{3}}{\pi} \cdot \frac{\hat{v}_{\rm ac}}{V_C} - 1. \end{aligned} \tag{9}$$

Solving (7)–(9), the expressions of capacitor voltage and duty ratio of S can be derived as follows:

$$V_C = \left(\frac{1}{2} + \frac{3\sqrt{3}}{4\pi} G\right) \cdot V_{\rm dc} \tag{10}$$

$$\begin{aligned} d_{\rm son}(\omega t) &= \frac{\pi}{3}(1 + d_{\rm avg}) \cdot \cos\left(\theta - \frac{\pi}{6}\right) - 1 \\ &= \frac{2\sqrt{3}\pi G \cdot \cos\left(\theta - \frac{\pi}{6}\right)}{2\pi + 3\sqrt{3}G} - 1 \end{aligned} \tag{11}$$

$$d_{\rm avg} = \frac{3\sqrt{3}G - 2\pi}{3\sqrt{3}G + 2\pi} - 1. \tag{12}$$

When diode-assisted buck–boost VSI operates under boost mode, the duty ratio of S always meets $d_{\rm son} \geq 0$. So, *G* should be larger than 1.486 from (11).

From (7), the intermediate dc-link voltage $(1 + d_{\rm son}(\omega t)) \cdot V_C$ in one switching time period T_s is the maximum value of three-phase output line voltage ($v_{\rm max} - v_{\rm min}$). With regard to the chopped intermediate dc-link voltage, the switching transient of the power devices in one phase leg with PWM control also needs some modification. For existing PMW strategies presented in [8] and [9], at any switching instant, there is only one switch to commutate. When S is commutating, the inverter bridge always outputs zero-voltage vector which indicates no influence on the three-phase loads. In order to meet this requirement, the improved modulation strategies in [9] introduce one additional switching instant to fully utilize the intermediate dc-link voltage to improve voltage gain and reduce the voltage stress of power devices. However, the aforementioned requirement is not essential for the operation of diode-assisted buck–boost VSI. The compulsory requirement is that S and D_1, D_2 in the front boost circuit, the upper switches $S_{\rm ip}$ and lower switches $S_{\rm in}$ (i = *a,b,c*) in the inverter bridge need to turned complementary on and off with each other.

With regard to the chopped intermediate dc-link voltage, the switching transient of the power devices in one phase leg with PWM control has two possible conditions. It is either during S = ON interval or during S = OFF interval. Fig. 6 shows the drive and output waveforms of diode-assisted buck–boost VSI with novel modulation strategy in one switching time period in the first sextant. For the symmetry, the drive signal of new control strategy in other sextant can be obtained similarly. As shown in Fig. 6(a), $S_{\rm ap}$ and $S_{\rm cn}$ are always turned on. Thus, $v_{\rm an}$ is the same as the intermediate dc-link voltage and $v_{\rm cn}$ is zero. The switches $S_{\rm bp}$ and $S_{\rm bn}$ commutate during S = ON interval, when the intermediate dc-link voltage is twice the capacitor voltage $v_{\rm dc\_link} = 2V_C$. $v_{\rm bn}$ changes between $2V_C$ and zero at the instant of $S_{\rm bp}S_{\rm bn}$ commutation. At this moment, the output phase voltage $v_{\rm mid}$ is relatively small and twice capacitor voltage during S = ON interval is enough for generating $v_{\rm mid}$. As shown in Fig. 6(b), the switches $S_{\rm bp}$ and $S_{\rm bn}$ commutate during S = OFF interval, the intermediate dc-link voltage is once the capacitor voltage $v_{\rm dc\_link} = V_C$.$v_{\rm bn}$ changes among $2V_C, V_C$ and zero at the instant of $S_{\rm bp}, S_{\rm bn}$ and S, D_1, D_2 commutation. At this moment, the output phase voltage $v_{\rm mid}$ is relatively large. Both twice capacitor voltage $2V_C$ during S = ON interval and once capacitor voltage V_C during S = OFF interval are used for generating $v_{\rm mid}$. As shown in Fig. 3, the three-phase voltage $v_{\rm ao}, v_{\rm bo}, v_{\rm co}$ can be calculated as follows:

$$v_{\rm io} = v_{\rm iN} - v_{\rm oN} (i = a, b, c). \tag{13}$$

And the instantaneous three-phase voltage meets

$$v_{\rm ao} + v_{\rm bo} + v_{\rm co} = 0. \tag{14}$$

Substituting (13) into (14), the natural-to-zero voltage is obtained as follows:

$$v_{\rm oN} = \frac{1}{3}(v_{\rm an} + v_{\rm bn} + v_{\rm cn}). \tag{15}$$

where $v_{\rm ao}, v_{\rm bo}, v_{\rm co}$ are the line-to-natural voltage; $v_{\rm an}, v_{\rm bn}, v_{\rm cn}$ are the line-to-zero voltage; $v_{\rm oN}$ are the natural-to-zero voltage.

In the first sextant, the output three-phase voltage meets $v_{\rm max} = v_{\rm ao}, v_{\rm mid} = v_{\rm bo}, v_{\rm min} = v_{\rm co}$. As shown in Fig. 6(a) and (b), according to volt–second balance principle, the duty ratio of upper switch $d^*_{\rm Sip}$ and output voltage of phase B $v_{\rm mid}$ meet

$$v_{\rm mid} - v_{\rm min} = d^*_{\rm Sip}(\omega t) \cdot 2V_C \tag{16}$$

$$v_{\rm mid} - v_{\rm min} = d_{\rm son}(\omega t) \cdot 2V_C + (d^*_{\rm Sip}(\omega t) - d_{\rm son}(\omega t)) \cdot V_C. \tag{17}$$

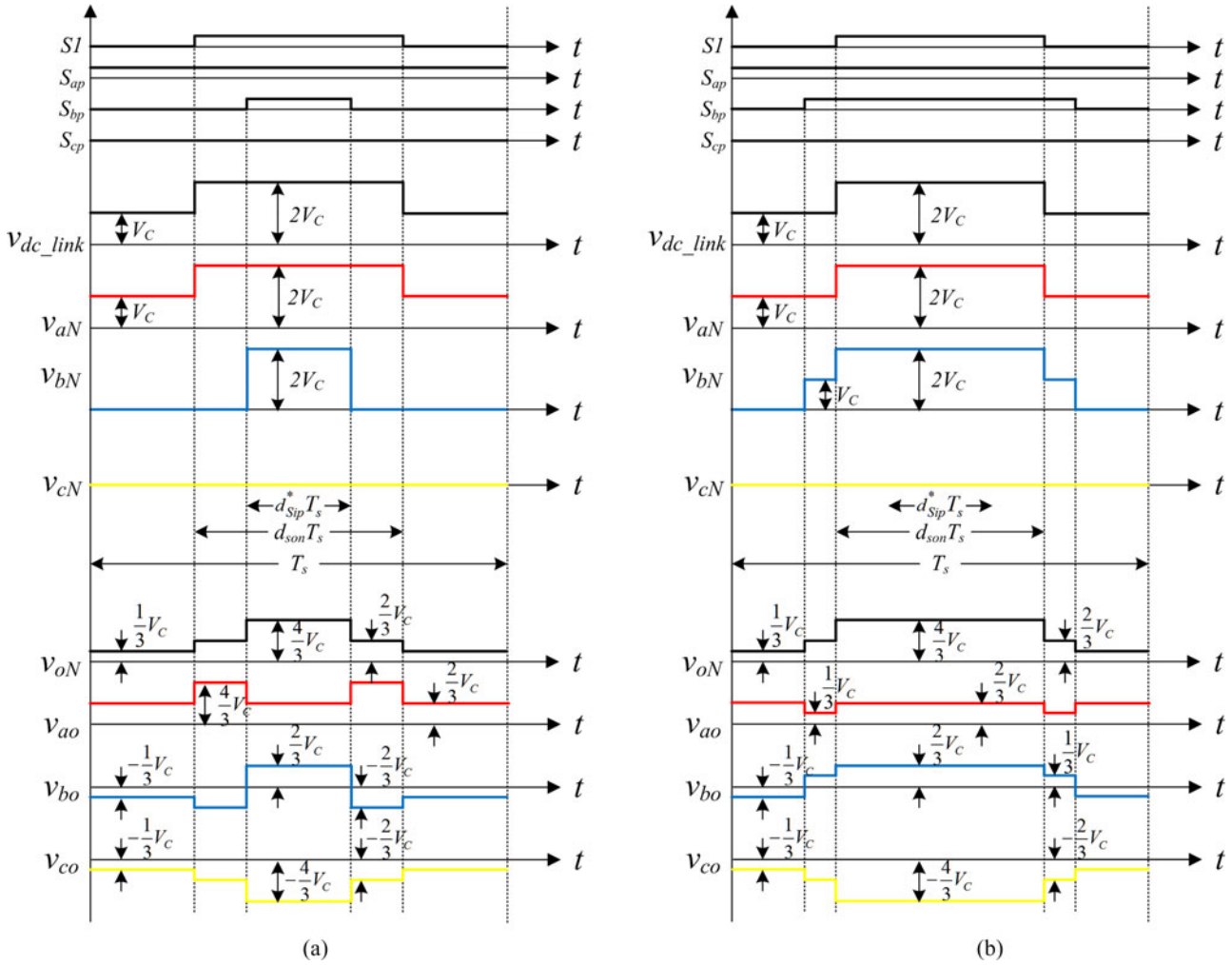

Fig. 6. Drive and output waveforms of diode-assisted buck–boost VSI with novel modulation strategy. (a) Switching transient of $S_{\rm ip}$ during S = ON interval. (b) Switching transient of $S_{\rm ip}$ during S = OFF interval.

From (3) and (4), the output voltage of phase B $v_{\rm mid}$ also meets

$$v_{\rm mid} - v_{\rm min} = d_{\rm Sip}(\omega t) \cdot (1 + d_{\rm son}(\omega t)) \cdot V_C. \qquad (18)$$

Solving (16)–(18), the expression of the corresponding duty ratio of upper and lower switches $d^*_{\rm Sip}$, $d^*_{\rm Sin}$ in (4) can be rewritten as (19).

Fig. 7 shows the equivalent drive waveform of carrier wave-based PWM approach for diode-assisted buck–boost VSI with the aforementioned maximum boost control. The six-pulse line $d_{\rm son}$ compared with the triangle carrier wave is adopted to control the duty ratio of switching device S. Three modulation waveforms are compared with the triangle carrier wave to produce the gate signals for switching devices in each phase leg of the inverter bridge (19) as shown bottom of the next page. where in each sextant, $v_{\rm min}(\omega t)$ is minimum of three-phase voltage; $v_{\rm max}(\omega t)$ is maximum of three-phase voltage; $v_{\rm mid}(\omega t)$ is middle of three-phase voltage; i representing the phase leg of middle voltage $v_{\rm mid}(\omega t)$, changes between a, b, and c.

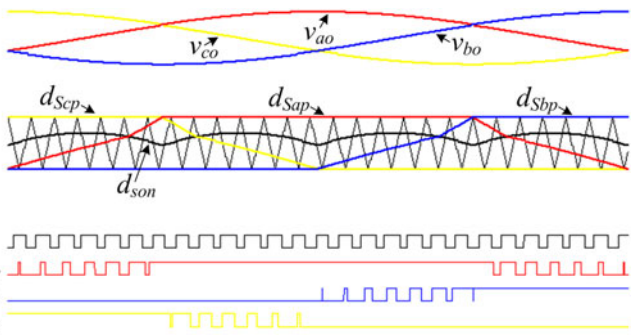

Fig. 7. Equivalent control waveform of carrier wave-based PWM.

IV. Comparison of Modulation Strategies

As for diode-assisted buck–boost VSI, using existing modulation strategy in [8], the switching frequency of power devices in the front boost circuit and the inverter bridge both are $f_s (f_s = 1/T_s)$. Only twice intermediate capacitor voltage $2V_C$ during S = ON interval is fully utilized for ac output. Therefore, the modulation index of inverter bridge M_i is limited by

TABLE II
EXPRESSIONS OF VOLTAGE STRESS AND SWITCHING FREQUENCY OF POWER DEVICES FOR DIODE-ASSISTED BUCK–BOOST VSI WITH DIFFERENT PWM STRATEGIES

		Switches in front boost circuit		Switches in the inverter bridge	
Modulation Scheme	Voltage gain	($V_{\rm sf}/V_{\rm dc}$)	Switching frequency	Voltage stress ($V_{\rm si}/V_{\rm dc}$)	Switching frequency
Existing PWM in [8]	$\frac{4}{\sqrt{3}}\cdot\frac{d_{\rm son}}{1-d_{\rm son}}$	$\frac{4+\sqrt{3}G}{4}$	f_s	$\frac{4+\sqrt{3}G}{2}$	f_s
Improved PWM in [9]	$\frac{2}{\sqrt{3}}\cdot\frac{1+d_{\rm son}}{1-d_{\rm son}}$	$\frac{2+\sqrt{3}G}{4}$	f_s	$\frac{2+\sqrt{3}G}{2}$	$2f_s$
Maximum boost PWM	$\frac{2\pi}{3\sqrt{3}}\cdot\frac{1+d_{\rm avg}}{1-d_{\rm avg}}$	$\frac{2\pi+3\sqrt{3}G}{4\pi}$	f_s	$\frac{2\pi+3\sqrt{3}G}{2\pi}$	$\frac{1}{3}f_s$

the on-state duty ratio of the switching device S ($d_{\rm son}$) in the front boost circuit. The corresponding voltage gain is

$$G=\frac{2}{1-d_{\rm son}}\cdot M_i \quad \left(0\le M_i\le\frac{2}{\sqrt{3}}d_{\rm son}\right). \tag{20}$$

Using improved modulation strategy in [9], in order to eliminate the influence of switching commutation of power devices in the front boost circuit on the three-phase load, the inverter bridge outputs zero-voltage vector during this instant. Therefore, it introduces the additional switching commutation in the inverter bridge. The switching frequency of power devices in the front boost circuit and the inverter bridge are f_s and $2f_s$, respectively. However, the advantage is that the chopped intermediate dc-link voltage is fully utilized for ac output. The voltage gain is

$$G=\frac{1+d_{\rm son}}{1-d_{\rm son}}\cdot M_i \quad \left(0\le M_i\le\frac{2}{\sqrt{3}}\right). \tag{21}$$

Using the aforementioned novel modulation strategy, the switching frequency of power devices in the front boost circuit and the inverter bridge are f_s and $1/3f_s$, respectively. The duty ratio of S ($d_{\rm son}$) in front boost circuit is always changing with the time. However, the average value of boost duty ratio ($d_{\rm avg}$) is fixed in steady state. From (6), (9), and (10), the voltage gain of diode-assisted buck–boost VSI is

$$G=\frac{2\pi}{3\sqrt{3}}\cdot\frac{1+d_{\rm avg}}{1-d_{\rm avg}}. \tag{22}$$

According to the operation principle of diode-assisted buck–boost VSI, the voltage stress across the switching devices in the front boost circuit $V_{\rm sf}$ is the same as the capacitor voltage V_C and voltage stress of the switching devices in the inverter stage $V_{\rm si}$ is the maximum intermediate dc-link voltage which is twice the capacitor voltage ($2V_C$) during S = ON interval. Substituting the boost duty ratio in (20)–(22) into (8), the

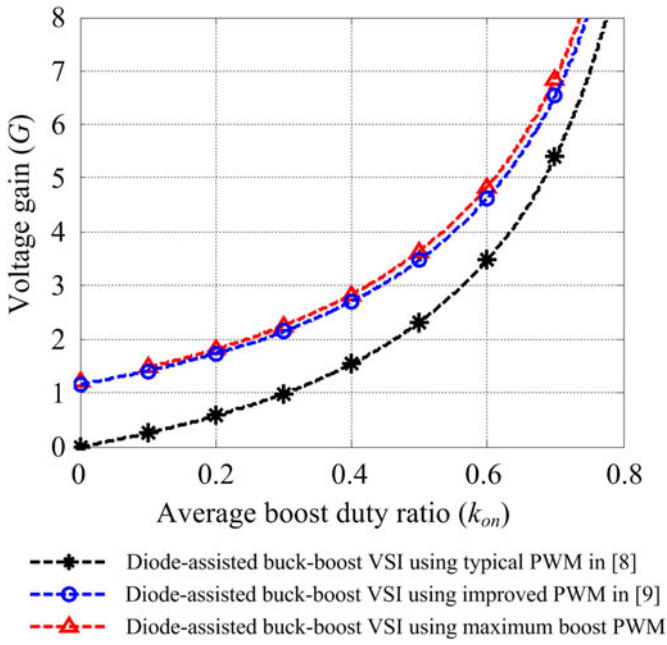

Fig. 8. Voltage gain of diode-assisted buck–boost VSI with different modulation strategies.

voltage stress of power devices for diode-assisted buck–boost VSI can be expressed by given voltage gain G. With existing PWM strategies in [8] and [9] and the aforementioned novel modulation strategy, the expressions of voltage gain, voltage stress, and switching frequency of power devices for diode-assisted buck–boost VSI are listed in Table II.

The voltage gain and voltage stress comparison of power devices for diode-assisted buck–boost VSI with different PWM strategies is shown in Figs. 8 and 9, respectively. Evidently, diode-assisted buck–boost VSI with the maximum boost modulation strategy demonstrates the maximum voltage boost

$$\begin{cases} d^*_{\rm Sip}(\omega t)=\dfrac{(1+d_{\rm son}(\omega t))}{2}\cdot\dfrac{v_{\rm mid}(\omega t)-v_{\rm min}(\omega t)}{v_{\rm max}(\omega t)-v_{\rm min}(\omega t)} & 0\le\dfrac{v_{\rm mid}(\omega t)-v_{\rm min}(\omega t)}{v_{\rm max}(\omega t)-v_{\rm min}(\omega t)}\le\dfrac{2\cdot d_{\rm son}(\omega t)}{1+d_{\rm son}(\omega t)} \\ d^*_{\rm Sip}(\omega t)=(1+d_{\rm son}(\omega t))\cdot\dfrac{v_{\rm mid}(\omega t)-v_{\rm min}(\omega t)}{v_{\rm max}(\omega t)-v_{\rm min}(\omega t)}-d_{\rm son}(\omega t) & \dfrac{2\cdot d_{\rm son}(\omega t)}{1+d_{\rm son}(\omega t)}\le\dfrac{v_{\rm mid}(\omega t)-v_{\rm min}(\omega t)}{v_{\rm max}(\omega t)-v_{\rm min}(\omega t)}\le 1 \\ d^*_{\rm Sin}(\omega t)=1-d^*_{\rm Sip}(\omega t) \end{cases} \tag{19}$$

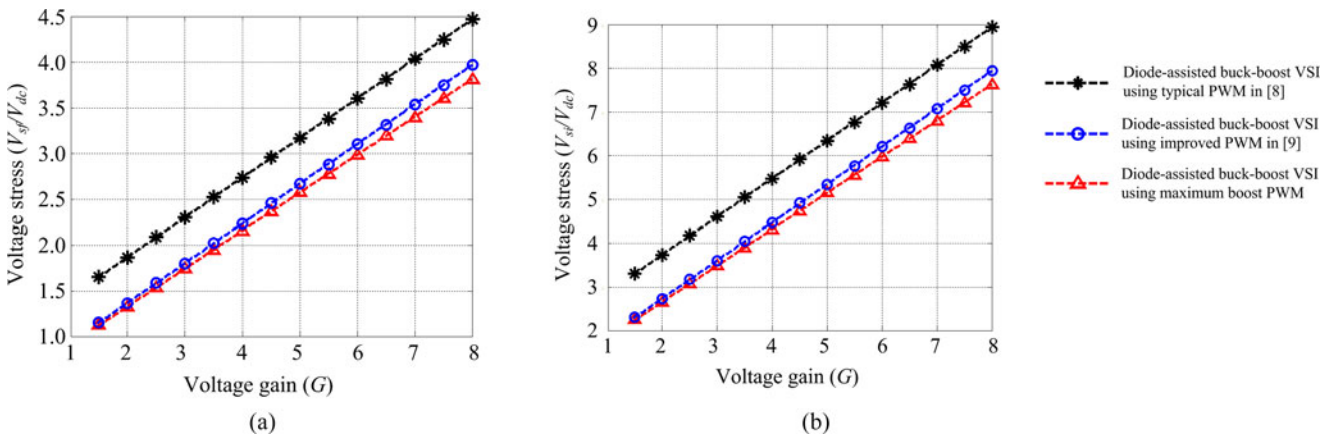

Fig. 9. Voltage stress of switches for diode-assisted buck–boost VSI with different modulation strategies. (a) Switches in front boost circuit. (b) Switches in the inverter bridge.

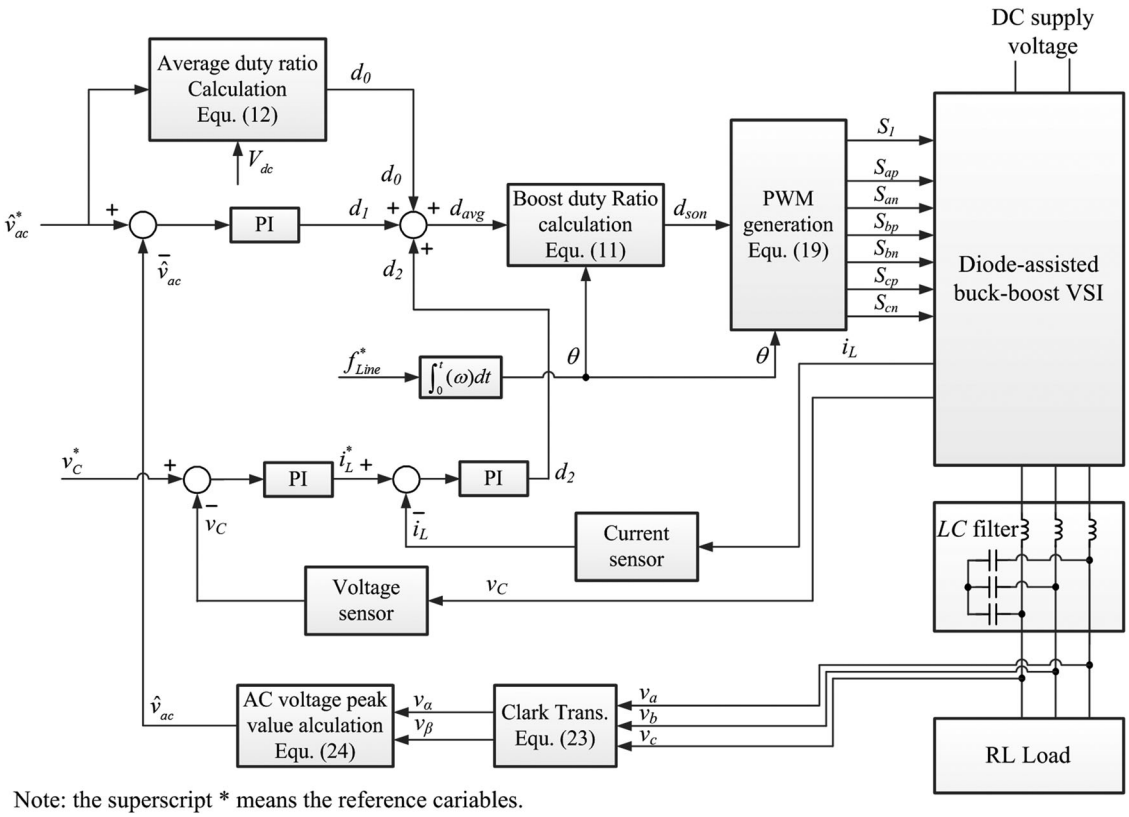

Fig. 10. Control system diagram of diode-assisted buck–boost VSI with maximum boost control.

capability, minimum voltage stress, and minimum switching frequency of power devices under the same voltage gain, which is in favor of reducing the cost and power loss of semiconductor devices, as compared with existing modulation strategies in [8] and [9].

V. Closed-Loop Controller Design

For diode-assisted buck–boost VSI with existing PWM strategies in [8] and [9], there are two control degrees of freedom: The boost duty ratio in the front boost circuit $d_{\rm son}$ and equivalent modulation index of inverter bridge M_i. The intermediate capacitor voltage is controlled by $d_{\rm son}$ and the output voltage is controlled by M_i, using separate closed loops with linear PI controller. However, with the aforementioned maximum boost modulation strategy, there is only one control freedom $d_{\rm son}$ for both intermediate capacitor voltage and output ac voltage regulation [18], [19]. Furthermore, there are some special requirements for the main circuit parameters design. The boost inductance and intermediate capacitance are designed larger enough to limit the six-time line-frequency ripples to the desired range. The ac-side *LC* filter is designed to filter the high switching frequency ripples, which is the same as conventional three-phase VSI.

Fig. 10 shows the closed-loop control system diagram, which consists of the dc-side dual-loop capacitor voltage control and the ac output voltage control. For given ac output voltage reference $\hat{v}_{\rm ac}^*$, the reference capacitor voltage v_C^* is calculated by (10). The relationship between voltage gain *G* and boost duty ratio $d_{\rm avg}$ expressed in (22) has obvious nonlinear characteristics, which deteriorate the transient response of output voltage. In order to overcome this problem, the feedforward control technique with the reference voltage $\hat{v}_{\rm ac}^*$ and input voltage $V_{\rm dc}$ is introduced to generate the related voltage gain *G* by (6) and calculate the approximate average value of boost duty ratio d_0 by (12). That is beneficial to achieve good transient performance. Instead of the ac component, the amplitude of three-phase voltage is feedback because it is dc component. After detecting the three-phase line voltages, the there-phase voltages $v_{\rm ao}, v_{\rm bo},$ and $v_{\rm co}$ are transformed into the two-axis stationary reference frame v_α and v_β according to

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{23}$$

where factor 2/3 is included which means that the amplitude of a voltage vector equals the peak value of the output phase voltage.

And then, the amplitude of output three-phase voltage $v_{\rm ac}$ can be calculated by

$$\hat{v}_{\rm ac} = \sqrt{v_\alpha^2 + v_\beta^2}. \tag{24}$$

The output of PI controller d_1 drives the amplitude of three-phase voltage to zero steady-state error.

For the front boost circuit, the voltage gain and frequency characteristic of boost duty ratio to intermediate capacitor voltage are similar as conventional boost dc–dc circuit. The typical dual-loop controller is applied to deal with the nonminimum phase system characteristic and obtain the good dynamic response. The output of PI controller d_2 drives the intermediate capacitor voltage to follow V_C^*.

The phase angle θ determines the sector at which the reference voltage vector is located. The instantaneous boost duty ratio $d_{\rm son}$ is calculated based on $d_{\rm avg}$ and θ according to (11). Then, the PWM module generates S signal for boost circuit and six PWM signals for the inverter bridge according to (19).

The state-space averaged model and small-signal perturbation provide the tools for good understanding of circuit performance and parameter selection of PI controller. For diode-assisted buck–boost VSI supplying three-phase balanced load, the output ac side is transferred to dc side and simplified as a dc resistive load connected with the high switching frequency *LC* filter [17]. Fig. 11 shows the dc-side equivalent circuit considering the influence of ac-side three-phase balanced load. The equivalent load resistor is calculated based on power balance

$$R_e = \frac{18}{\pi^2} \cdot R_L. \tag{25}$$

Taking all the inductor current ($i_L, i_{\rm Lf}$) and capacitor voltage ($v_C, v_{\rm Cf}$) as the state variables and using the state-space

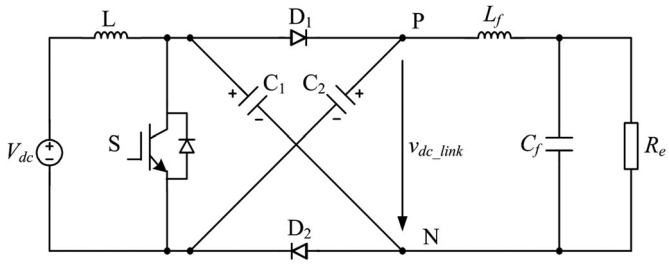

Fig. 11. DC-side equivalent circuit.

averaging method in one switching time period (T_s), the state equations of dc-side equivalent circuit can be expressed as (26).

Performing small signal perturbation at the equilibrium operation point, the transfer function expressions of control to boost inductor current, intermediate capacitor voltage, and output voltage perturbations are as (27)–(29).

It can be observed from (27)–(29) that the transfer function of boost duty ratio to intermediate capacitor voltage $G_{v_C}(s)$ and output voltage $G_{v_{\rm Cf}}(s)$ contains the right half-plane (RHP) zero. With RHP zero, the expected voltage falls before rising to the reference when the step increase of control command is given [18]. This nonminimum phase system exhibits a worse dynamic response and causes oscillation. Therefore, inner current loop is essential to deal with such an influence and obtain the good response.

Fig. 12 shows the block diagram of closed-loop controller of dc-side equivalent circuit. $C_i(z)$, $C_{v_C}(z)$, and $C_{v_{\rm Cf}}(z)$ are the typical digital PI controller with antiwindup correction expressed in (30). H_i and H_v are the coefficients of current and voltage sampling units, respectively. $(1-e^{-T_s s})/s$ is zero order hold. $e^{-T_d s}$ is time delay. $G_{i_L}(s)$, $G_{v_C}(s)$, and $G_{v_{\rm Cf}}(s)$ are the control to state variable transfer functions expressed in (27)–(29). $G_{i_L}(s)$ is the minimum phase system transfer function. And the total phase delay is 90. Therefore, the inner current regulator $C_i(z)$ is easily designed to meet the bandwidth requirement. $G_{vcf}(s)$ provides the guidance for parameters design of PI controller for three-phase ac output voltage. Applying the formula for Mason's rule, the inner current closed-loop transfer function is derived as (31). Once the current loop is designed, it can be treated as a new power stage for the outer voltage loop

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \\ \frac{di_{\rm Lf}}{dt} \\ \frac{dv_{\rm Cf}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-d_{\rm Son}}{L} & 0 & 0 \\ \frac{1-d_{\rm Son}}{2C} & 0 & -\frac{1+d_{\rm Son}}{2C} & 0 \\ 0 & \frac{1+d_{\rm Son}}{L_f} & 0 & \frac{1+d_{\rm Son}}{L_f} \\ 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f R_e} \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_C \\ i_{\rm Lf} \\ v_{\rm Cf} \end{bmatrix} + \begin{bmatrix} L \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot V_{\rm dc} \tag{26}$$

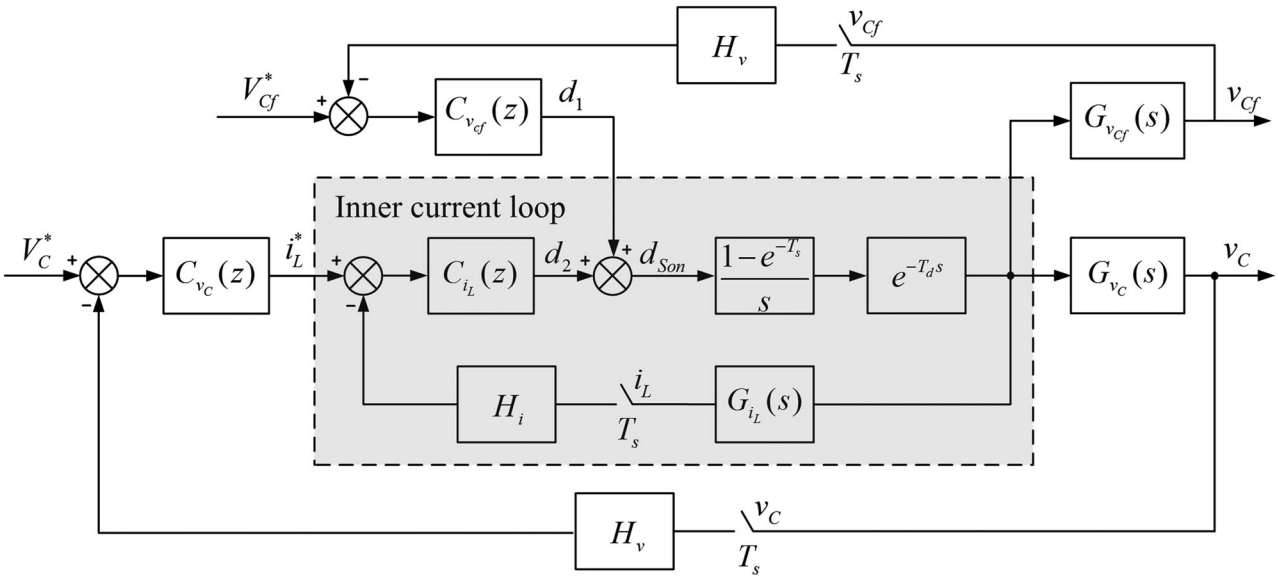

Fig. 12. Block diagram of closed-loop controller for dc-side equivalent circuit.

$$G_{i_L}(s) = \frac{\hat{i}_L(s)}{\hat{d}_{\rm Son}(s)} = \frac{a_{13}\cdot s^3 + a_{12}\cdot s^2 + a_{11}\cdot s + a_{10}}{b_4\cdot s^4 + b_3\cdot s^3 + b_2\cdot s^2 + b_1\cdot s + b_0} \quad (27)$$

$$G_{v_C}(s) = \frac{\hat{v}_C(s)}{\hat{d}_{\rm Son}(s)} = \frac{a_{22}\cdot s^2 + a_{21}\cdot s + a_{20}}{b_4\cdot s^4 + b_3\cdot s^3 + b_2\cdot s^2 + b_1\cdot s + b_0} \quad (28)$$

$$G_{v_{\rm Cf}}(s) = \frac{\hat{v}_{\rm Cf}(s)}{\hat{d}_{\rm Son}(s)} = \frac{a_{32}\cdot s^2 + a_{31}\cdot s + a_{30}}{b_4\cdot s^4 + b_3\cdot s^3 + b_2\cdot s^2 + b_1\cdot s + b_0} \quad (29)$$

where the numerator and denominator coefficients are

$$a_{13} = \frac{2CL_fC_fR_eV_{\rm dc}}{1-D_{\rm Son}},\ a_{12} = \frac{2L_fV_{\rm dc}(C+(1+D_{\rm Son})C_f)}{1-D_{\rm Son}},$$

$$a_{11} = \frac{2R_LV_{\rm dc}[C+(1+D_{\rm Son})C_f]}{1-D_{\rm Son}} + \frac{2L_fV_{\rm dc}(1+D_{\rm Son})}{(1-D_{\rm Son})R_e},$$

$$a_{10} = \frac{4(1+D_{\rm Son})V_{\rm dc}}{1-D_{\rm Son}}, a_{23} = -\frac{2(1+D_{\rm Son})LL_fC_fV_{\rm dc}}{(1-D_{\rm Son})^2},$$

$$a_{22} = \frac{-2LL_fV_{\rm dc}(1+D_{\rm Son}))}{(1-D_{\rm Son})^2R_e} + \frac{R_LC_fV_{\rm dc}\left[(1-D_{\rm Son})L_f-(1+D_{\rm Son})L\right]}{(1-D_{\rm Son})},$$

$$a_{21} = \frac{V_{\rm dc}[(1-D_{\rm Son})^2L_f-(1+D_{\rm Son})(3-D_{\rm Son})L]}{(1-D_{\rm Son})^2},$$

$$a_{20} = V_{\rm dc}R_e, a_{32} = \frac{2LCR_eV_{\rm dc}}{(1-D_{\rm Son})},$$

$$a_{31} = -\frac{2LV_{\rm dc}(1+D_{\rm Son})^2}{(1-D_{\rm Son})^2},\ a_{30} = 2R_eV_{\rm dc},$$

$$b_4 = 2LCL_fC_fR_e,\ b_3 = 2LCL_f,\ b_2 = [(1+D)^2LC_f + 2LC + (1-D)^2L_fC_f]R_e,\ b_1 = (1+D)^2L + (1-D)^2L_f,\ b_0 = (1-D)^2R_e.$$

design. The closed-loop transfer functions of capacitor voltage and filtered output voltage are derived as (32) and (33)

$$G_c(z) = K_p + K_iT_s\cdot\frac{z}{z-1} \quad (30)$$

$$T_{i_L}(s) = \frac{C_i(s)\cdot G_{i_L}(s)}{1+H_i\cdot C_i(s)\cdot G_{i_L}(s)} \quad (31)$$

$$T_{v_C}(s) = \frac{C_{v_C}(s)\cdot T_{i_L}(s)\cdot G_{v_C}(s)}{G_{i_L}(s)+H_{v_C}\cdot C_{v_C}(s)\cdot T_{i_L}(s)\cdot G_{v_C}(s)} \quad (32)$$

$$T_{v_{C_f}}(s) = \frac{C_{v_{\rm Cf}}(s)\cdot T_{i_L}(s)\cdot G_{v_{C_f}}(s)}{C_{i_L}(s)\cdot G_{i_L}(s)+H_{v_{\rm Cf}}\cdot C_{v_{\rm Cf}}(s)\cdot T_{i_L}(s)\cdot G_{v_{C_f}}(s)}. \quad (33)$$

VI. Simulation and Experimental Verification

Numerical simulations using MATLAB/Simulink have been performed to verify the proposed maximum boost modulation strategy and the theoretical analysis. The main circuit parameters are: $V_{\rm dc} = 120$ V, $L = 8$ mH, $C_1 = C_2 = 500$ μF, $L_f = 400$ μH, $C_f = 25$ μF, $R_{\rm Load} = 40-80$ Ω, $L_{\rm load} = 2$ mH. The switching time period T_s is 100 μs.

Fig. 13 shows the drive signals, intermediate dc-link voltage, and output waveforms for diode-assisted buck–boost VSI with the aforementioned modulation strategy to obtain the maximum voltage gain and minimum switching frequency under the output reference voltage of $\hat{v}_{\rm ac} = 310$ V. As for the unfiltered phase voltage shown in Fig. 13(b). The positive and negative half-period waveforms are not symmetric with each other. As is illustrated in Fig. 6, during $v_a = v_{\max}$ interval,

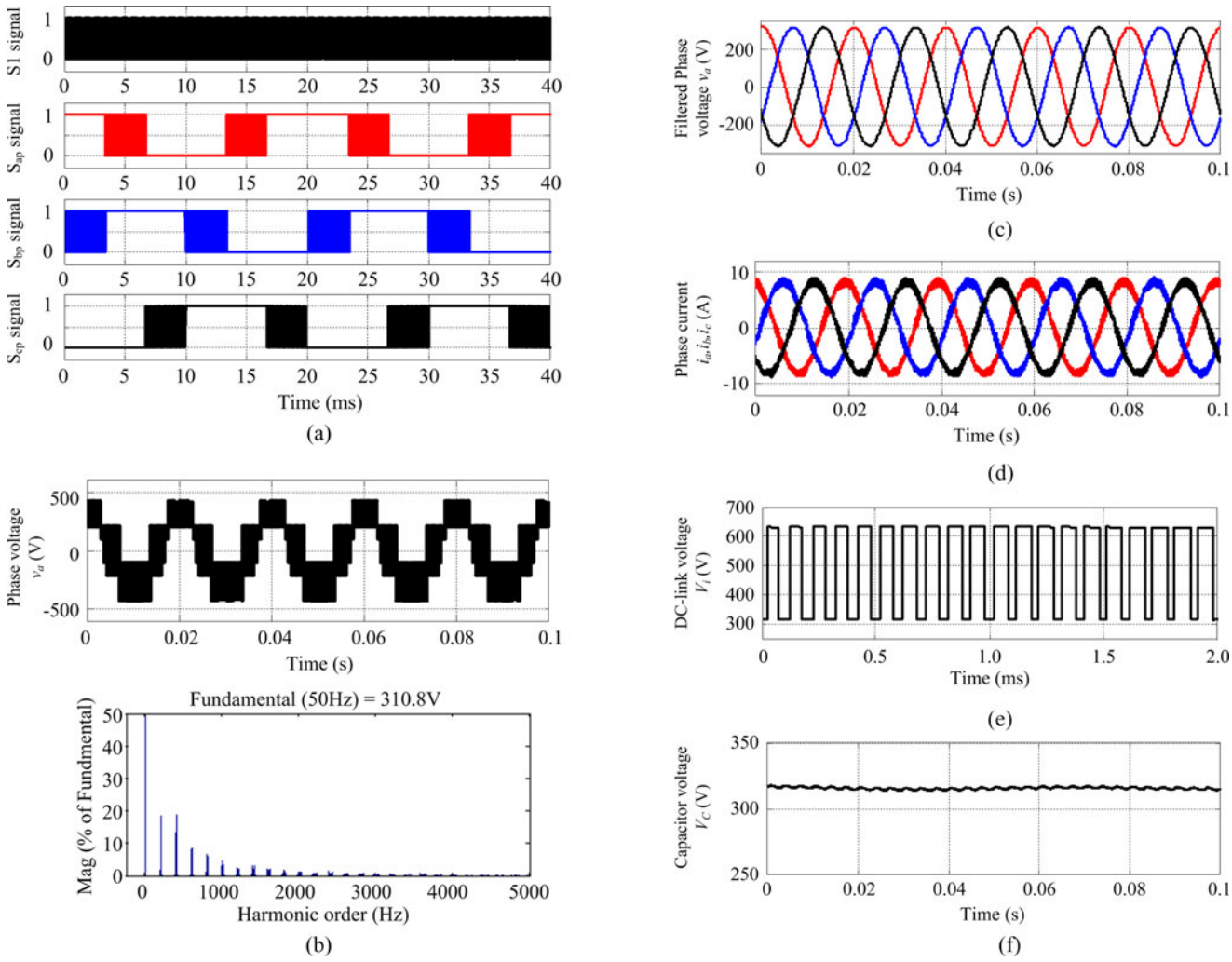

Fig. 13. Simulation results for diode-assisted buck–boost VSI with novel PWM strategy. (a) Drive signal. (b) Output phase voltage and spectrum analysis. (c) Filtered output phase voltage. (d) Output line current. (e) Intermediate dc-link voltage. (f) Capacitor voltage.

when only twice capacitor voltage during S = ON interval are used to generate $v_{\rm mid}, v_{\rm ao}$ changes between $2/3V_C$ and $4/3V_C$. When both twice capacitor voltage during S = ON interval and once capacitor voltage during S = OFF interval are used to generate $v_{\rm mid}, v_{\rm ao}$ changes between $1/3V_C$ and $2/3V_C$. During $v_a = v_{\rm min}$ interval, $v_{\rm ao}$ always changes among $-1/3V_C, -2/3V_C$, and $-4/3V_C$ in one switching time period. However, the output phase voltage merely contains fundamental wave and harmonics with switching frequency multiplication in theory. According to volt–second balance principle, the unsymmetry does not influence ideal fundamental sinusoidal voltage. According to (6) and (10), the voltage gain $G = 5.18$, and the capacitor voltage $V_C = 317$ V calculated in theory are identical to the simulation results. Compared with the existing PWM strategies, diode-assisted buck–boost VSI with novel modulation scheme achieves the maximum voltage gain as well as minimum voltage stress and switching frequency of power devices.

A laboratory prototype rated at 2.5 kW was built to confirm the proposed maximum boost PWM strategy with the Infineon power devices. The main control board is designed based on DSP28335. Fig. 14 shows a photograph of the test platform. A programmable dc power supply is arranged as the dc source to simulate the *V–I* characteristics of fuel cells and solar arrays. A Y-type three-phase *RL* load is connected to the ac side of the inverter. HIOKI 3390 power analyzer simultaneously measures the input dc power and ac output power to perform efficiency analysis. The time duration of each switching instant is precalculated in DSP28335. The conditioning board performs logic operations to generate gate signals of power devices according to the requirement of the output voltage vector. The specifications for the experimental prototype are listed in Table III. The key parameters of closed-loop controllers are

$$G_{i_L}(z) = 0.072 + 0.0031 \bullet z/(z-1);$$
$$G_{v_C}(z) = 0.05 + 0.019 \bullet z/(z-1);$$
$$G_{\rm vcf}(z) = 0.035 + 0.02z/(z-1)$$

For diode-assisted buck–boost VSI with aforementioned modulation strategy, the main circuit parameters are carefully designed with the consideration of six-time line-frequency ripples. However, the dc-side inductor steady state current

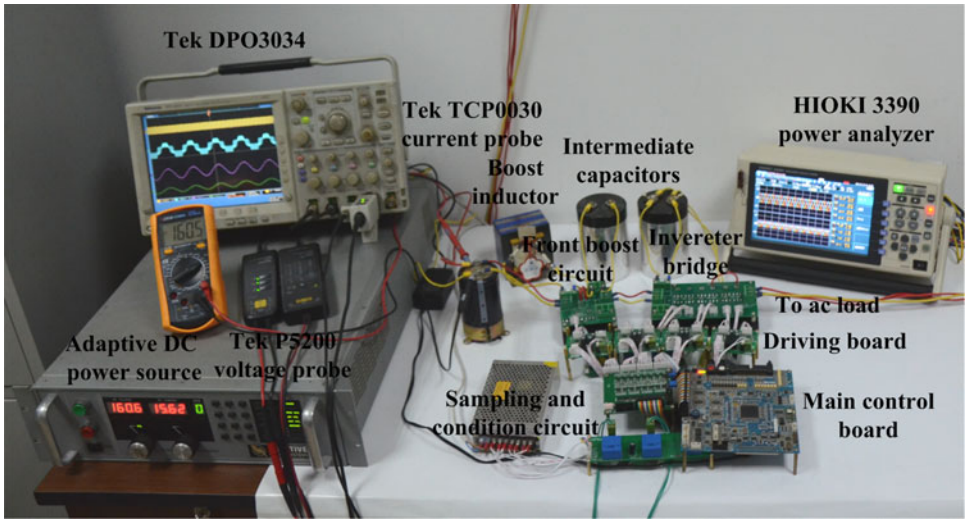

Fig. 14. Diode-assisted buck–boost VSI test platform.

TABLE III
SPECIFICATIONS FOR THE EXPERIMENTAL PROTOTYPE

Switching device	S	IGBT (IGW40T120)
	D_1 and D_2	DIODE (IDP30E120)
	S_{ap}, S_{an}, S_{bp}, S_{bn}, S_{cp}, S_{cn}	IGBT (IGW25N120) and DIODE (IDP18E120)
Passive components	L	8 mH
	C_1 and C_2	500 μF
Three-phase EMI filer	L_f	400 μH
	C_f	35 μF
Three-phase RL load	R_{load}	80–600 Ω
	L_{load}	2 mH
Switching time period	T_s	100 μs
Current sensor	H_i	0.1
Voltage sensor	H_v	0.01

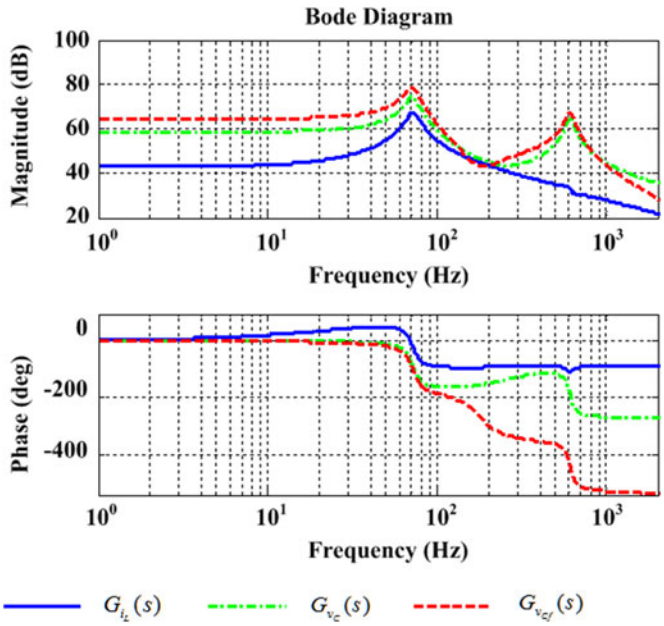

Fig. 15. Frequency characteristic of control to inductor current, intermediate capacitor voltage, and output voltage.

inevitably contains 300 Hz low frequency ripples for 50 Hz ac output. Fig. 15 shows the frequency characteristic of control to inductor current and intermediate capacitor voltage and filtered output voltage. In order to suppress the undesired influence of low frequency ac components, the bandwidth of inner current loop is designed below 300 Hz. Fig. 16 shows the designed closed-loop frequency responses. The inner current loop is designed with 200 Hz bandwidth and 50° phase margin. The intermediate capacitor voltage loop and output voltage are designed with almost 30 Hz bandwidth and 60° phase margin, which is beneficial to reduce the voltage oscillatory.

Fig. 17 shows the experiment results for diode-assisted buck–boost VSI with the aforementioned maximum boost PWM strategy under the output reference voltage of $\hat{v}_{ac} = 310$ V. The maximum voltage gain of $G_{imax} = 5.18$ can be obtained. Fig. 17(a) shows the voltage waveforms of gate signals for power devices (S, S_{ap}, S_{bp}, and S_{cp}). During each sextant, the switches in the legs of maximum phase voltage and minimum phase voltage are fixed. Only switches in one phase leg are commutating with PWM. Fig. 17(b) shows the captured waveforms of the intermediate dc-link voltage, the output phase voltage before and after filtered, as well as the output current. The measured intermediate dc-link voltage changes between 319.6 and 639.3 V. The filtered output phase voltage is 220.3 V. All these measured values are a little larger than the theoretical values of 317.3, 634.6, and 220 V, respectively. This is due to the voltage drop of switching devices and the voltage loss of the dead zone in the inverter. Compared with existing modulation strategies, the maximum boost PWM strategy reduces intermediate dc-link capacitor voltage and switching frequency, which is a benefit for power devices.

The maximum boost PWM strategy introduces a six-time low-frequency ripples that is associated with the output line frequency in the dc-side inductor current and the capacitor

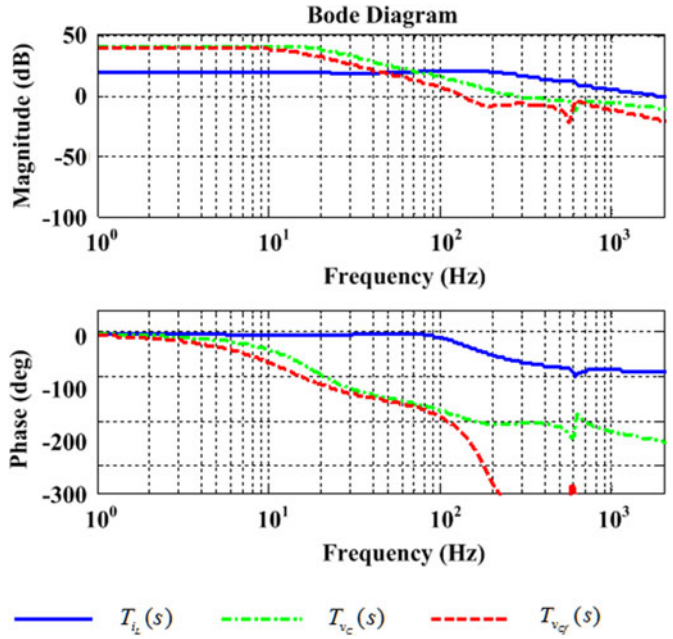

Fig. 16. Closed-loop frequency response of inductor current, intermediate capacitor voltage, and output voltage.

voltage. This will cause a higher requirement of the passive components when the output frequency is very low. In order to reduce the undesired influence of low frequency ripples, it is also suitable for 400–800 Hz medium frequency application of power supply system. Fig. 18 shows the experiment results for diode-assisted buck–boost VSI using the maximum boost modulation strategy under the input voltage of $V_{\rm in} = 50$ V and output reference voltage of $\hat{v}_{\rm ac} = 156$ V, $f_{\rm line} = 400$ Hz, switching time period $T_s = 50$ μs. The maximum voltage gain of $G_{i\max} = 6.2$ can be obtained. Fig. 16 shows the captured waveforms of the intermediate dc-link voltage, the output phase voltage before and after filtered, as well as the output current. The measured intermediate dc-link voltage changes between 157.2 and 314.3 V. The filtered output phase voltage is 110 V. All these measured values are a little larger than the theoretical value of 153.7, 307.3, and 110 V, respectively.

Fig. 19(a) and (b) shows the experimental results when the reference output voltage has a step change from $\hat{v}_{\rm ac} = 250$ V to $\hat{v}_{\rm ac} = 310$ V and back to $\hat{v}_{\rm ac} = 250$ V, respectively. As can be seen from the experimental results, the controller is very stable under steady-state operation and the step change response is also fast with acceptable response time. With controller design shown in Fig. 10, the output three-phase voltage has good transient performance. The output three-phase voltage follows the reference when the intermediate capacitor voltage $V_C = 256$ Vachieves new steady state $V_C = 318$ V.

Efficiency is an important criterion for designing a power converter in renewable energy application. The losses of power converter comprise semiconductor devices losses, passive components losses, controller and driver losses, etc. In which, the semiconductor devices losses are the dominating part. The insulated-gate bipolar transistor (IGBT) loss consists of turn-on and turn-off switching loss besides conduction loss. The power

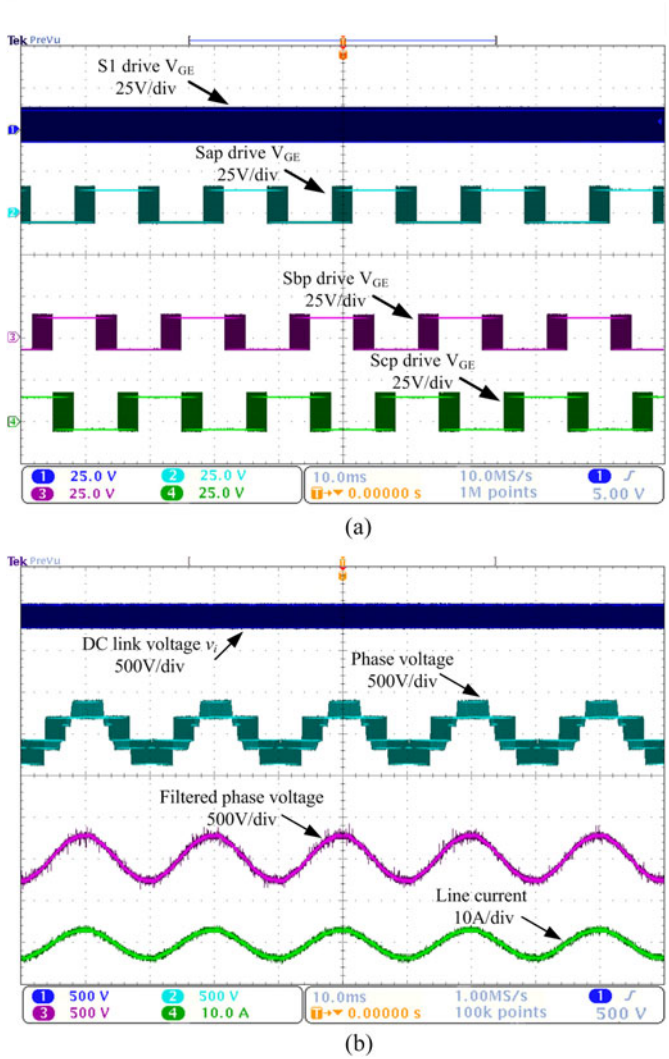

Fig. 17. Diode-assisted buck–boost VSI with maximum boost control ($V_{\rm dc} = 120$ V, $R_L = 80\ \Omega$, $f_{\rm line} = 50$ Hz). (a) Voltage waveforms of power device gate signals. (b) Waveforms of intermediate dc-link voltage, output voltage, and current.

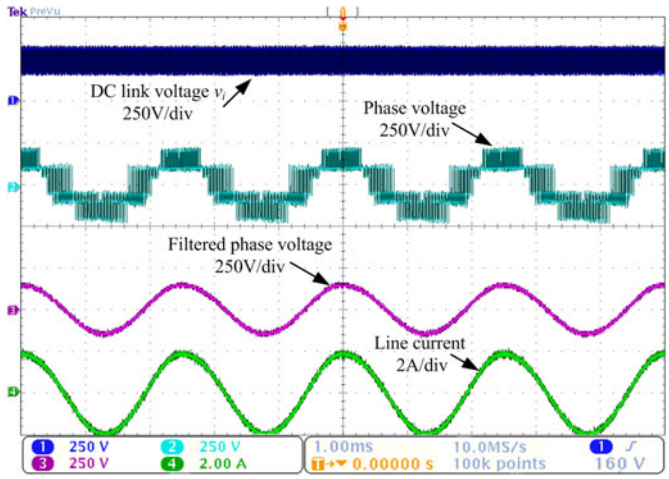

Fig. 18. Experiment waveforms of intermediate dc-link voltage, output voltage, and current for diode-assisted buck–boost VSI with maximum boost control ($V_{\rm dc} = 50$ V, $R_L = 80\ \Omega$, $f_{\rm line} = 400$ Hz).

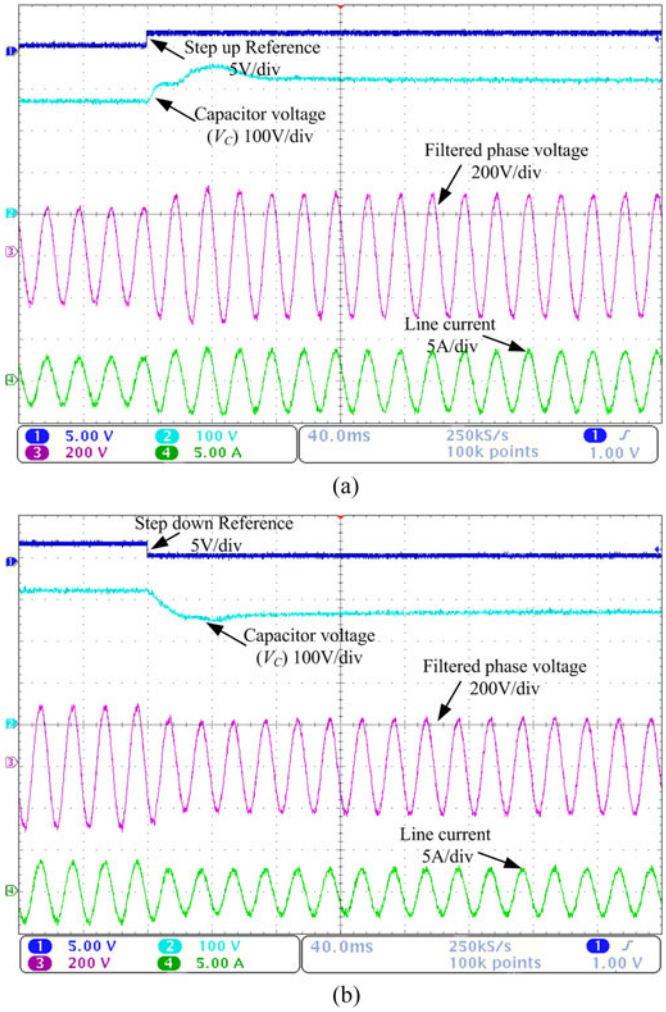

Fig. 19. Dynamic responses of diode-assisted buck–boost VSI with closed-loop maximum boost control under step change of output voltage reference ($V_{\rm dc} = 160$ V, $R_L = 80\Omega$). (a) Step up 250–310 V. (b) Step down 310–250 V.

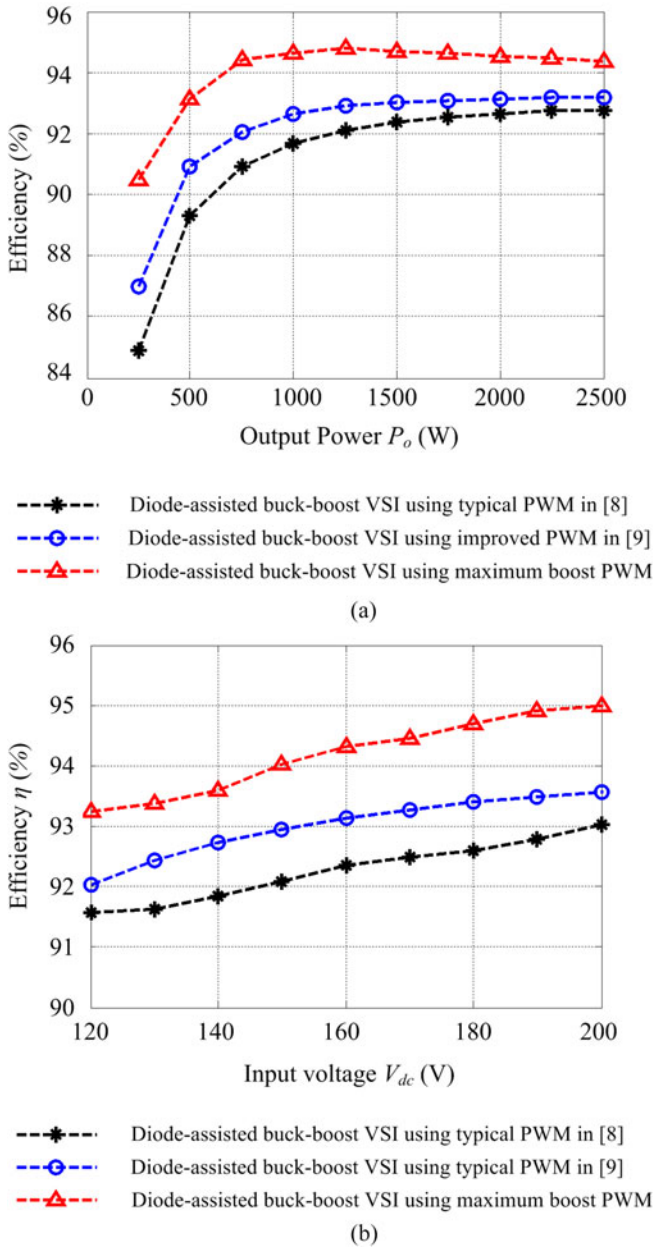

Fig. 20. Efficiency comparison of diode-assisted buck–boost VSI with different modulation schemes. (a) Efficiency versus output power ($V_{\rm dc} = 160$ V, $V_{\rm ac} = 311$ V, $P_o = 250 - 2500$ W). (b) Efficiency versus input voltage ($V_{\rm dc} = 120 - 200$ V, $V_{\rm ac} = 311$ V, $P_o = 2500$ W).

diode loss includes the reverse recovery loss and conduction loss because the turn-on loss is small enough to be neglected [22]. The switching loss model of semiconductor device can be expressed as follows [22]–[24]:

$$E_{\rm sw(on,off)} = (\alpha + \beta \cdot i_{\rm sw} + \gamma \cdot i_{\rm sw}^2)\frac{V_{\rm sw}}{V_{\rm ref}} \tag{34}$$

$$P_{\rm sw} = f_{\rm sw} \cdot (E_{\rm swon} + E_{\rm swoff}) \tag{35}$$

where $V_{\rm sw}$ is the blocking voltage; $i_{\rm sw}$ is the switched current; α, β, and γ are the device parameters from the manufacturer datasheet. $V_{\rm ref}$ is the reference voltage under which the device parameters are derived.

The conduction loss of power devices in the front boost circuit and inverter bridge can be expressed as follows:

$$P_{\rm con\_dc} = \frac{1}{T_s}\int_{t_1}^{t_2} v_{\rm con} \cdot i_{\rm con} dt \tag{36}$$

$$P_{\rm con\_inv} = \frac{1}{2\pi}\int_{\lambda_1}^{\lambda_2} d_{\rm con}\cdot @v_{\rm on} \cdot i_{\rm con} d\theta_r \tag{37}$$

where $v_{\rm con} = v_{\rm th} + r i_{\rm con}$ is on-state voltage drop. $v_{\rm th}$ is threshold voltage; r is on-state resistor. $i_{\rm con}$ is conduction current, $d_{\rm con}$ is conduction duration.

As indicated in (34) and (35), the switching loss of semiconductor device depends on the switching frequency ($f_{\rm sw}$), switched current ($i_{\rm sw}$), and blocking voltage ($V_{\rm sw}$). As for diode-assisted buck–boost VSI with maximum boost PWM strategy, the reduced switching frequency and voltage stress are beneficial to increase the efficiency. In order to quantify the improvement introduced by maximum boost PWM strategies, the aforementioned main circuit efficiency is measured under different output power and input voltage as a reference. Diode-assisted

buck–boost VSI with different modulation strategies operate with maximum boost control, respectively. Fig. 20 shows the efficiency comparison results when diode-assisted VSI operates at (a) $V_{\rm dc} = 160$ V, $V_{\rm ac} = 311$ V, $P_o = 250 - 2500$ W with the change of load resistance and (b) $V_{\rm dc} = 120 - 200$ V, $V_{\rm ac} = 311$ V, $P_o = 2500$ W with the change of the input voltage.

Compared with existing modulation strategies in [8] and [9], diode-assisted buck–boost VSI with maximum boost PWM strategy reduces the switching frequency and voltage stress of power devices in the inverter bridge. At the same time, with existing modulation strategies, at least one switching commutation takes place during S = ON interval in one switching time period (T_s) in each phase leg, the switching voltage is $V_{\rm sw} = 2V_C$. With maximum boost modulation strategy, in some switching time period, the power devices in the inverter bridge commutates during S = OFF interval as shown in Fig. 6(b), the switching voltage is $V_{\rm sw} = V_C$. Therefore, the switching loss of power device in the inverter bridge can be reduced to a large extent. That is the main reason why diode-assisted buck–boost VSI with maximum boost PWM strategy demonstrates best efficiency than other inverter system configurations. Especially, in low power application, the switching loss is the main part of semiconductor devices loss. Furthermore, the reduced switching frequency and voltage stress mean less silicon device requirements for power converter.

VII. Conclusion

The paper starts by analyzing the modulation principle of three-phase VSI and then proposes a new PWM strategy to achieve the instantaneous maximum utilization of intermediate dc-link voltage, as well as to reduce the switching frequency of power devices in diode-assisted buck–boost VSI. Simulation and experimental results are included to verify theoretical analysis. Compared with existing modulation strategies in [8] and [9], diode-assisted buck–boost with maximum boost control strategy reduces the voltage stress of switches and demonstrates the optimal efficiency. Therefore, it is a more promising and competitive topology for wide range voltage regulation in renewable energy applications. Furthermore, with the maximum boost control strategy, the dc-side inductor current and capacitor voltage contains six-times line frequency ripples. Therefore, it is also suitable for relatively high output line frequency, including 400–800 Hz medium frequency aircraft and vessel power supply system.

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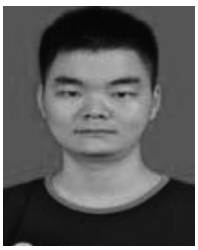

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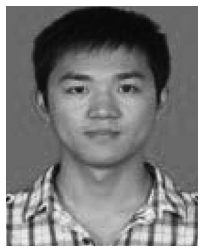

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