Interleaved Resonant Boost Inverter Featuring SiC Module for High-Performance Induction Heating

Héctor Sarnago, *Member, IEEE*, Óscar Lucía, *Senior Member, IEEE*, and José Miguel Burdío, *Senior Member, IEEE*

***Abstract*—Induction heating (IH) has become the technology of choice in many industrial, domestic, and medical applications due to its high efficiency and performance. This paper proposes an interleaved resonant boost inverter featuring SiC three-phase module to achieve high efficiency and performance IH power supply. The proposed converter achieves high efficiency by reducing the current through the devices, while the use of an interleaved full-bridge configuration reduces input current ripple and provides additional control degrees. The proposed converter has been designed, implemented, and tested experimentally, proving the feasibility of this proposal.**

***Index Terms*—Induction heating (IH), inverter, resonant power conversion.**

I. Introduction

INDUCTION heating (IH) [1] has become a key technology in recent years due to its benefits in terms of performance and efficiency when compared with classical heating methods. Advances in enabling technologies, including power electronics, digital control, and magnetic components, has enabled a significant breakthrough in IH technology, which has led to a number of relevant industrial [2]–[4], domestic [5]–[7], and medical applications [8].

Although alternative implementations using permanent magnets are being studied [9], usually IH systems rely on a power converter to generate an alternating magnetic field to heat the IH target. Fig. 1 summarizes the most common approaches when designing IH power supplies.

The first approach is the simplest one, requiring a rectifier, dc–dc conditioning, and medium-frequency inverter blocks. This is the most extended approach, with multiple variations, due to its simplicity and easy control. In some cases, the second approach is followed where the rectifier and dc–dc blocks are combined, leading to an integrated approach. Finally, in recent years, several direct ac–ac converters have been proposed [10]–[12], enabling the design of higher power density and performance solutions at the cost of a more complex design and control. In all the discussed approaches, the inverter is the core of the power converter and is commonly implemented using single-switch [13] or half-bridge [14], [15] topologies for low-medium power applications, and the full-bridge [16] topology for high-power applications. Although Si IGBT is the technology of choice, in recent years, wide bandgap devices [17], and specially SiC, have enabled significant advances in performance and play currently an important role in modern IH systems [18]–[20].

This paper proposes an interleaved boost resonant inverter topology [10], [21] in order to provide an efficient and high-performance IH power supply. The proposed topology achieves high efficiency by reducing the current through the power devices and inductor, while the use of an interleaved configuration enables reduced input current ripple. Besides, the boost full-bridge inverter provides additional control degrees, enabling fine output power control. The proposed converter takes advantage of a three-phase SiC module to achieve a high power density and performance implementation.

The remainder of this paper is organized as follows. Section II details the proposed topology, and Section III presents a thorough analytical model of the converter divided in an interleaved boost rectifier plus a resonant full-bridge inverter. Section IV provides a power loss model, including power loss in the main power devices as well as passive devices. Section V summarizes the main simulation and experimental results proving the feasibility of the proposed converter. Finally, Section VI draws the conclusions of this paper.

II. Direct AC–AC Interleaved Full-Bridge Converter

The proposed converter is depicted in Fig. 2. The main power supply $v_{\rm ac}$ is rectified by means of the half-bridge branch $R(S_{H,r}, S_{L,r})$. It is important to remark that a synchronous rectification has been implemented to improve efficiency, being possible to use a two-diode standard half-wave rectifier branch. Consequently, $S_{L,r}$ is activated during the positive mains voltage half-cycle and $S_{H,R}$ during the negative one. Two additional inverter branches $A(S_{H,A}, S_{L,A})$ and $B(S_{H,B}, S_{L,B})$ simultaneously perform a voltage boost function and generates the high-frequency current required for the induction heating (IH) application [21], [22].

The voltage boost function is achieved by means of the interleaved inductors $L_{s,A}, L_{s,B}$ and the dc-link capacitor C_s, whereas a full-bridge inverter topology provides the required high-frequency current i_o for the application. A series resonant tank has been implemented, composed of the equivalent IH load parameters, i.e., a series resistance R_L and inductance L_r and the resonant capacitor C_r. The applied resonant tank voltage v_o is defined by the inverter branches *A* and *B*,

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The authors are with the Department of Electronic Engineering and Communications, University of Zaragoza, Zaragoza 50018, Spain (e-mail: hsarnago@unizar.es; olucia@unizar.es; burdio@unizar.es).

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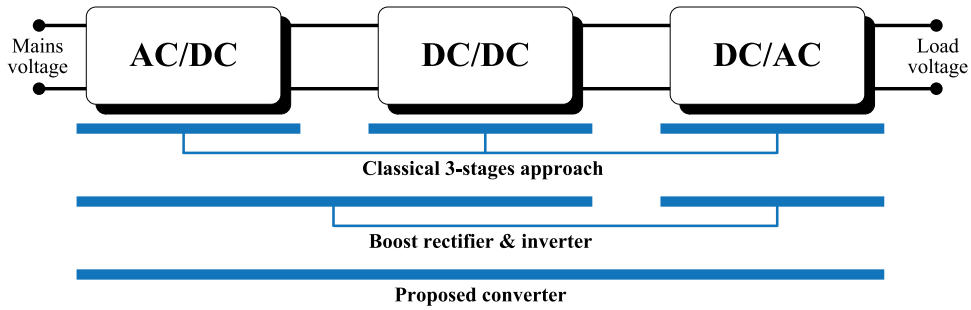


Fig. 1. Power converter alternative implementations diagram.

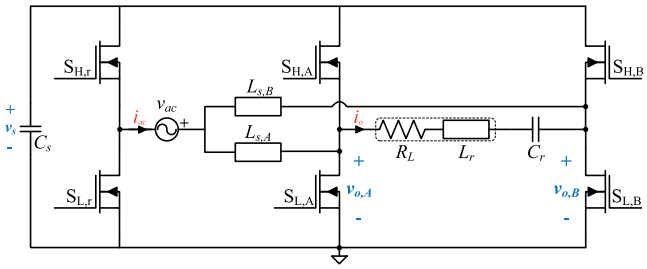


Fig. 2. Proposed converter schematic.

yielding $v_o = v_{o,A} - v_{o,B}$. Considering the structure of the proposed converter, a three-phase SiC MOSFET module is selected, yielding a compact and efficient implementation.

Fig. 3 shows the equivalent circuits of the proposed converter for the positive (a) and negative (b) mains cycle. From this figure, it can be seen that one device from each half-bridge branch is activated at all times. Besides, it is important to note that states III and VII occur when the duty cycle $D < 0.5$, whereas states IV and VIII apply when $D > 0.5$.

The main converter waveforms are shown in Fig. 4. A complementary activation of the rectifier branch with a mains period $T_{\rm ac} = 1/f_{\rm ac}$ is considered, and high-frequency switching for the inverter branches *A* and *B* period $T_{\rm sw} = 1/f_{\rm sw}$ is used. It is important to note that zero-voltage switching is achieved in the inverter devices, ensuring smooth and efficient operation. These conditions are detailed in Fig. 5, where the control signals, blocking voltage, and current through each device are shown, highlighting the ZVS switching margin.

Considering that the mains frequency is in the range of 50–60 Hz, and the switching frequency is in the range of the tens of kHz, i.e., $T_{\rm ac} >> T_{\rm sw}$, the mains voltage $v_{\rm ac}$ can be considered constant during a switching period. Consequently, the bus voltage v_s can be calculated as a function of the duty cycle $D_A = D_B$, where a fixed phase lag between branches *A* and *B* has been established, $\varphi_{AB} = 0.5\ = T_{\rm sw}$, yielding

$$v_s(t) = \begin{cases} \dfrac{v_{\rm ac}(t)}{D_A}, & v_{\rm ac}(t) \geq 0 \\ \dfrac{-v_{\rm ac}(t)}{1 - D_A}, & v_{\rm ac}(t) < 0 \end{cases} \tag{1}$$

Consequently, the duty cycle applied to the inverter branches *A* and *B* must be changed according to the mains sign to provide an input power factor close to 1. Fig. 6 shows the modulation parameters for a nominal duty cycle *D* defined as a function of the desired voltage boost ratio $D = 1 - |v_{\rm ac}/v_s|$. Consequently, $D_A = D_B = 1 - D$ is applied for the positive mains half-periods, whereas $DA{=}DB{=}D$ is applied for the negatives ones.

It is important to note the role and operation of the dc-link capacitor in the proposed converter. From the point of view of the equivalent inverter side, the inverter can be modeled as a pure resistor if constant modulation parameters are applied. By combining this fact with the use of a small dc-link capacitor, a mains power factor close to the unit can be achieved. In the case of the proposed converter, a capacitor large enough to filter the high-frequency harmonics but still providing a sinusoidal current consumption will be selected. As it can be observed in Fig. 6 and predicted by (1), the waveform of the dc-link capacitor voltage is proportional to the absolute value of the mains voltage, ensuring the input power factor close to one. Additionally, this effect will be appreciated in the experimental results.

III. Converter Analysis

The converter operation can be analyzed using the superposition principle assuming that the voltage ripple in the bus capacitor can be neglected as the sum of an interleaved boost rectifier and a resonant full-bridge inverter [21], as it is depicted in Fig. 7.

As it is shown Fig. 7., the dc-link voltage v_s can be controlled using the duty cycle of the branches *A* and *B*, whereas the applied output power to the IH load can be controlled either by the duty cycle or the switching frequency.

A. Equivalent Interleaved Boost Rectifier Stage

One of the main advantages of the interleaved boost rectifier stage is the ability to reduce the input current ripple $\Delta i_{\rm ac}$ being also possible to cancel the input ripple for a given conditions $(D = 0.5)$. In order to simplify the analysis without loss of generality, the analysis will be performed for $v_{\rm ac} > 0$, being possible to obtain the same results in the case of $v_{\rm ac} < 0$. Consequently, as it has been detailed in (1), $D_A = D_B = D = 1 - |v_{\rm ac}/v_s|$,

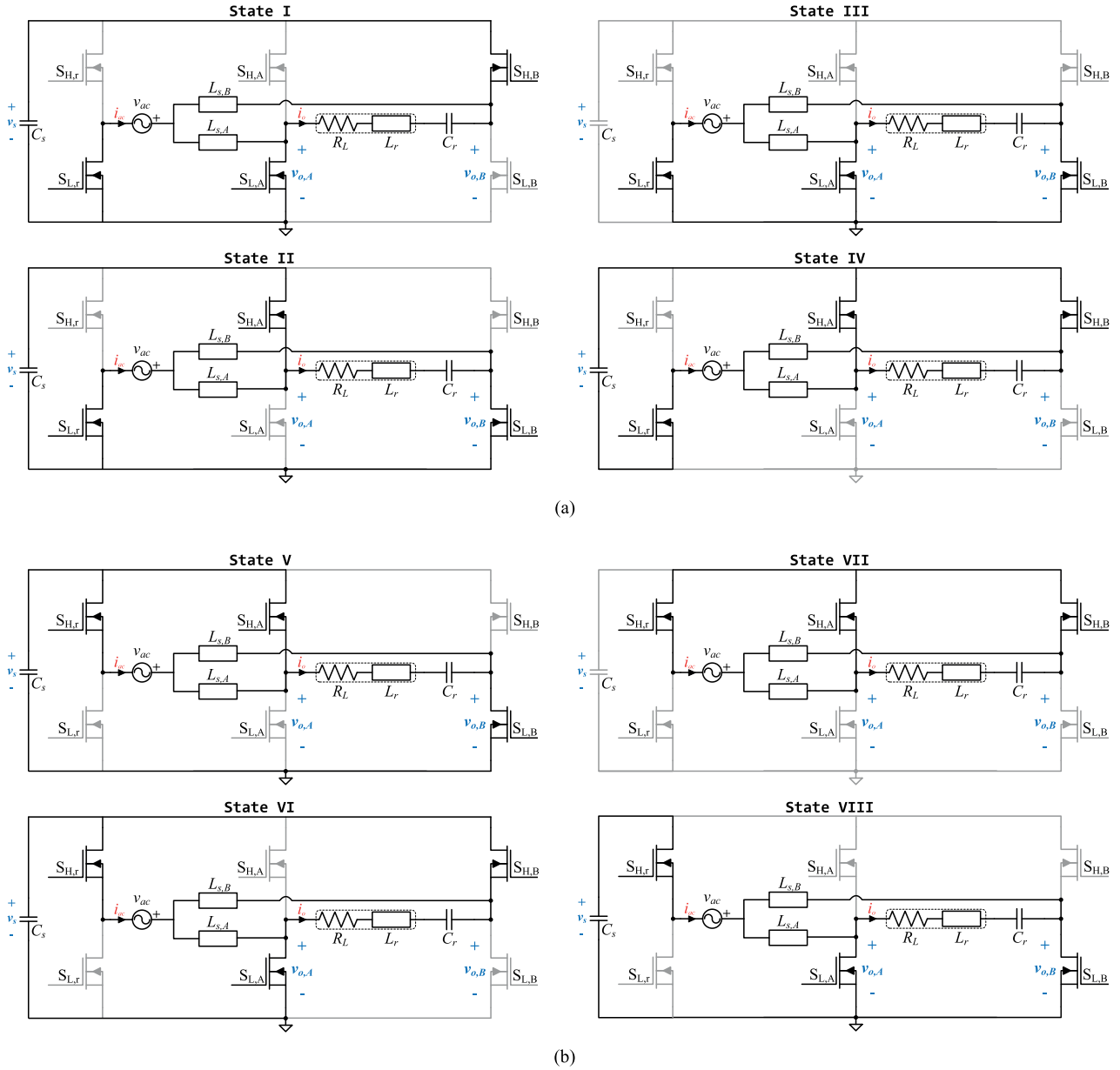


Fig. 3. Equivalent circuits of the proposed converter: (a) positive mains cycle and (b) negative mains cycle.

represent the equivalent interleaved boost rectifier stage duty cycle. It is important to note that the same duty cycle is considered in both interleaved branches ($DA = DB$) in order to obtain the required dc-link voltage.

In order to compute both the input current ripple and the interleaved branches current ripple, the equivalent circuit depicted in Fig. 8 has been considered.

The applied output voltage in each branch is

$$v_{o,A}(t) = \begin{cases} v_s, & 0 \le t < D_A T_{\rm sw} \\ 0, & D_A T_{\rm sw} < t \le T_{\rm sw} \end{cases} \quad (2)$$

$$v_{o,B}(t) = \begin{cases} v_s, & 0 \le t < (D_B - 1/2)\, T_{\rm sw} \\ 0, & D_B T_{\rm sw} < (t - T_{\rm sw}/2) \le T_{\rm sw} \end{cases} . \quad (3)$$

The current ripple in the branch A $\Delta i_{Ls,A}$ can be calculated as

$$\begin{aligned} \Delta i_{Ls,A} &= \frac{1}{L_{s,A}} \int_0^{D_A T_{\rm sw}} (v_{o,A} - v_{\rm ac}) dt \\ &= \frac{-1}{L_{s,A}} \int_{D_A T_{sw}}^{T_{sw}} (v_{o,A} - v_{\rm ac}) dt \end{aligned} \quad (4)$$

yielding $\Delta i_{Ls,A} = (v_{\rm ac}/f_{\rm sw} L_{s,A})(1 - D_A)$. Similar results can be obtained for the branch B, $\Delta i_{Ls,B} = (v_{\rm ac}/f_{\rm sw} L_{s,B})(1 - D_B)$. Assuming $L_{s,A} = L_{s,B} = L_s$, the mains input ripple $\Delta i_{\rm ac}$ can be obtained as the sum of both

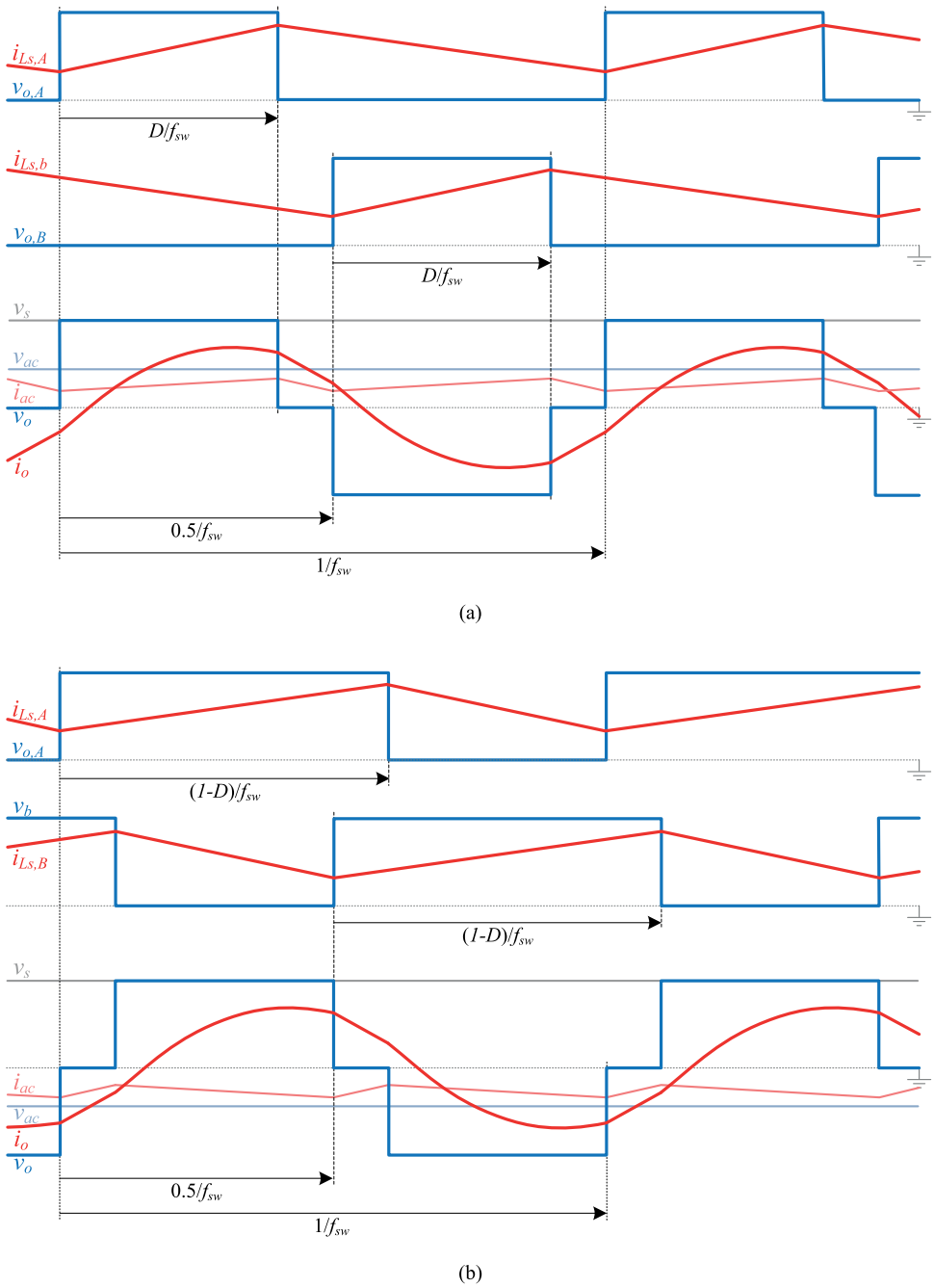


Fig. 4. Main waveforms of the proposed converter. Waveforms for (a) the positive mains half period and (b) the negative.

interleaved branches:

$$\begin{aligned}\Delta i_{\rm ac} &= \frac{1}{L_s}\int_0^{D_A T_{\rm sw}} (v_{o,A} - v_{\rm ac})dt \\ &\quad + \frac{1}{L_s}\int_0^{D_A T_{\rm sw}} (v_{o,B} - v_{\rm ac})dt \\ &= \frac{1}{L_s}\int_0^{D_A T_{\rm sw}} (v_{o,A} + v_{o,B}) - 2v_{\rm ac}dt \end{aligned} \tag{5}$$

where the sum of both branches voltage results in a periodic waveform with double the switching frequency. Depending on the value of the duty cycle, two scenarios are possible

$$\Delta i_{\rm ac} = \begin{cases} \dfrac{1}{L_s}\displaystyle\int_0^{D_A T_{\rm sw}} (v_s + 0) - 2v_{\rm ac}dt, & \text{for } D_A \le \frac{1}{2} \\ \dfrac{1}{L_s}\displaystyle\int_0^{(D_A - 1/2)T_{\rm sw}} (v_s + v_s) - 2v_{\rm ac}dt, & \text{for } D_A > \dfrac{1}{2} \end{cases} \tag{6}$$

yielding

$$\Delta i_{\rm ac} = \frac{T_{\rm sw} v_{\rm ac}}{L_s} \begin{cases} 2\left(\dfrac{1}{2} - D_A\right), & \text{for } D_A \le \dfrac{1}{2} \\ 2\left(\dfrac{1}{D_A} - 1\right)\left(D_A - \dfrac{1}{2}\right), & \text{for} D_A > \dfrac{1}{2} \end{cases} \tag{7}$$

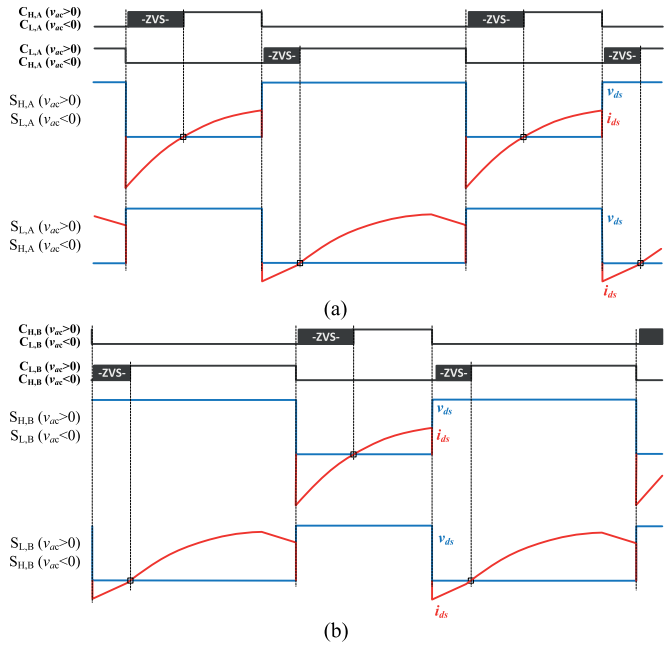


Fig. 5. Main waveforms highlighting the soft-switching ZVS operation for (a) the inverter branch A and (b) the inverter branch B.

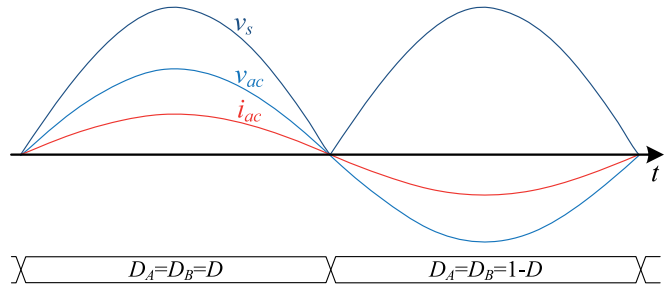


Fig. 6. Mains waveforms for a given nominal duty cycle D.

Fig. 9(a) shows the normalized ripple as a function of the duty cycle $\overline{\Delta i_{\rm ac}} = \Delta i_{\rm ac}/(T_{\rm sw} v_{\rm ac}/L_s)$, whereas Fig. 9(b) shows the ratio of the mains ripple and a phase ripple $\Delta i_{\rm ac}/\Delta i_{Ls,A} = \Delta i_{\rm ac}/\Delta i_{Ls,B}$. As it shown, the minimum mains ripple is achieved at 50% duty cycle, regardless the value of the boost inductance or switching frequency. It is also important to note that, as it has been derived in the previous expressions, the mains ripple occurs at a double switching frequency, simplifying the mains filter requirements. Additionally, since synchronous rectification is provided by $S_{H,r}$ and $S_{L,r}$, there is no minimum value for L_S in order to obtain a continuous conduction mode (CCM).

B. Equivalent Full-Bridge Series-Resonant Inverter

The full-bridge inverter topology is appropriate for medium-high output power levels [1] because of its efficiency and versatile control. In order to reduce switching losses, the operation above the resonant point is preferred, leading to ZVS turn-on transition which entails decreased switching losses and mitigated EMI issues.

Fig. 10 shows the main resonant converter waveforms, including the output voltage v_o, the load current i_o, and the resonant capacitor voltage v_{Cr}. Using a matrix notation, the state variable vector $x = [i_o, v_{Cr}]^T$ can be defined for each switching interval Δ_i, with $i = 0, \ldots, 3$. Each switching interval can be defined according to the modulation parameters as follows:

$$\Delta_0 = \Delta_2 = \left(\frac{1}{2} - \left|\frac{1}{2} - D\right|\right) T_{\rm sw} \tag{8}$$

$$\Delta_1 = \Delta_3 = \left(\left|\frac{1}{2} - D\right|\right) T_{\rm sw}. \tag{9}$$

The differential equations system that defines the dynamic of the converter is

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}\mathbf{x}(t) + \mathbf{B}v_o(t) \tag{10}$$

where

$$\mathbf{A} = \begin{bmatrix} -R_L/L_r & -1/L_r \\ 1/C_r & 0 \end{bmatrix} \qquad \mathbf{B} = \begin{bmatrix} 1/L_r \\ 0 \end{bmatrix}. \tag{11}$$

The temporal expression for each switching interval results

$$\mathbf{x}_{\rm i}(t) = e^{\mathbf{A}t}\mathbf{X}_{\rm i} + A^{-1}\left(e^{\mathbf{A}t} - \mathbf{I}\right)\mathbf{B}V_{o,i} \tag{12}$$

where the initial conditions for each interval X_i can be obtained as

$$\begin{bmatrix} \mathbf{X}_0 \\ \mathbf{X}_1 \\ \mathbf{X}_2 \\ \mathbf{X}_3 \end{bmatrix} = \begin{bmatrix} -e^{\mathbf{A}\Delta_o} & \mathbf{I} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & -e^{\mathbf{A}\Delta_1} & \mathbf{I} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & -e^{\mathbf{A}\Delta_2} & \mathbf{I} \\ \mathbf{I} & \mathbf{0} & \mathbf{0} & -e^{\mathbf{A}\Delta_3} \end{bmatrix}^{-1} \times \begin{bmatrix} \mathbf{A}^{-1}\left(e^{\mathbf{A}\Delta_o} - \mathbf{I}\right)\mathbf{B}v_s \\ \mathbf{0} \\ -\mathbf{A}^{-1}\left(e^{\mathbf{A}\Delta_o} - \mathbf{I}\right)\mathbf{B}v_s \\ \mathbf{0} \end{bmatrix}. \tag{13}$$

The applied output power can be computed as a function of the output voltage and the load current

$$P_o = \frac{1}{T_{\rm sw}}\int_0^{T_{\rm sw}} v_o i_o dt = \frac{v_s}{T_{\rm sw}}\left(\int_{\Delta_1} i_o dt - \int_{\Delta_3} i_o dt\right) \tag{14}$$

where the load current integral for a given switching interval can be obtained as a function of the resonant capacitor voltage at the beginning of each switching interval [23], yielding

$$P_o = \frac{v_s}{T_{\rm sw}} C_r \left((V_{C_r,1} - V_{C_r,0}) - (V_{C_r,3} - V_{C_r,2})\right). \tag{15}$$

Considering the symmetry of the system $X_2 = -X_0$ and $X_3 = -X_1$, the output power expression can be simplified as follows:

$$P_o = 2\frac{v_s}{T_{\rm sw}} C_r \left(V_{C_r,1} - V_{C_r,0}\right). \tag{16}$$

IV. Power Losses Analysis

The proposed converter is composed of six active power devices and additional passive elements. In this section, the main

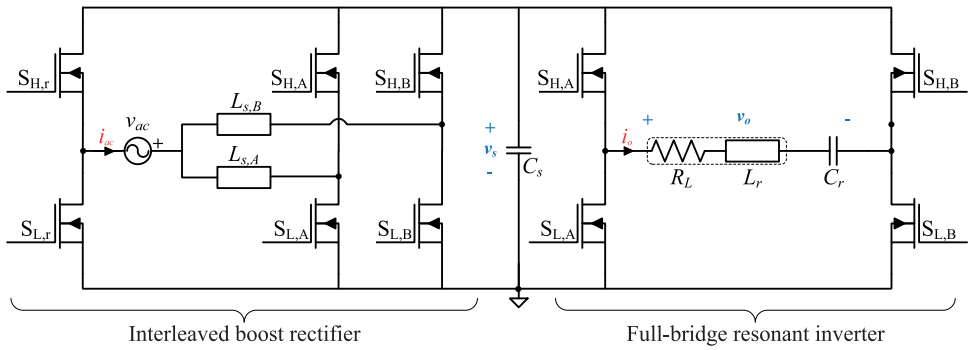


Fig. 7. Equivalent converter model for analysis by the superposition principle.

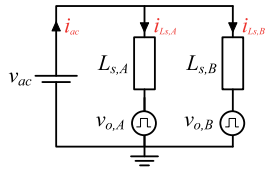


Fig. 8. Equivalent circuit for current ripple calculation.

power losses will be analyzed, with special emphasis in the active devices, where both conduction and switching losses will be detailed. In the case of the passive components, conduction losses will be considered. Fig. 11 shows an equivalent power loss schematic, where main conduction losses take place in the equivalent conduction resistance. In the case of the converter branches, i.e., *r, A*, and *B*, the complementary activation of the transistors yields to an equivalent transistor continuously activated. Additionally, the direct ac–ac operation of the converter equilibrates the power losses between both transistors of the same branches for a mains period, leading to a balanced 50% power loss distribution. Since there are always two active MOSFET devices and they are activated to maximize channel conduction, i.e., minimizing dead times, the proposed simplified model can be applied regardless the current flow direction.

A. Boost Inductors

In order to compute conduction power losses for each component, it is required to obtain the main root-mean-square (rms) current values as a function of the output power P_o and the mains rms voltage $V_{\mathrm{ac,rms}}$. In the case of the boost inductances, $L_{s,A} = L_{s,B} = L_s$, the equivalent conduction resistance has been divided into a low-frequency component $r_{Ls,\mathrm{LF}}$ (mains frequency), and a high-frequency component $r_{Ls,\mathrm{HF}}$ (switching frequency ripple). The low-frequency rms current, $I_{Ls,\mathrm{LF,rms}} = I_{Ls,A,\mathrm{LF,rms}} = I_{Ls,B,\mathrm{LF,rms}}$ can be directly related to the mains rms current, yielding $I_{Ls,LF,\mathrm{rms}} = I_{\mathrm{ac,rms}}/2$. By assuming an input power factor close to one and $P_i \approx P_o$

$$I_{Ls,LF,\mathrm{rms}} = \frac{P_o}{2V_{\mathrm{ac,rms}}}. \tag{17}$$

Besides, according to the previous analysis, the high-frequency rms current can be obtained by (18) as shown at the bottom of the page.

Leading to $I_{Ls,HF,\mathrm{rms}} = \Delta i_{Ls}/2\sqrt{3}$. Therefore, combining (18) with (4), the average rms value during a mains period results

$$\begin{aligned} I_{Ls,\mathrm{HF,rms}} &= \frac{1}{T_{\mathrm{ac}}}\int_0^{T_{\mathrm{ac}}} \frac{\Delta i_{Ls}(t)}{2\sqrt{3}}dt \\ &= \frac{V_{\mathrm{ac,rms}}2\sqrt{2}}{\pi}\frac{(1-D)\,T_{\mathrm{sw}}}{2\sqrt{3}L_s}. \end{aligned} \tag{19}$$

B. Resonant Capacitor

The equivalent series resistance of the resonant capacitor can be obtained from the loss factor, i.e., $\tan(\delta)$, leading to $r_{Cr} = \tan(\delta)/(2\pi f_{\mathrm{sw}} C_r)$. The entire rms load current $I_{o,\mathrm{rms}}$ flows through the resonant capacitor, and consequently, power losses can be directly computed. The output current can be easily computed from the output power as follows:

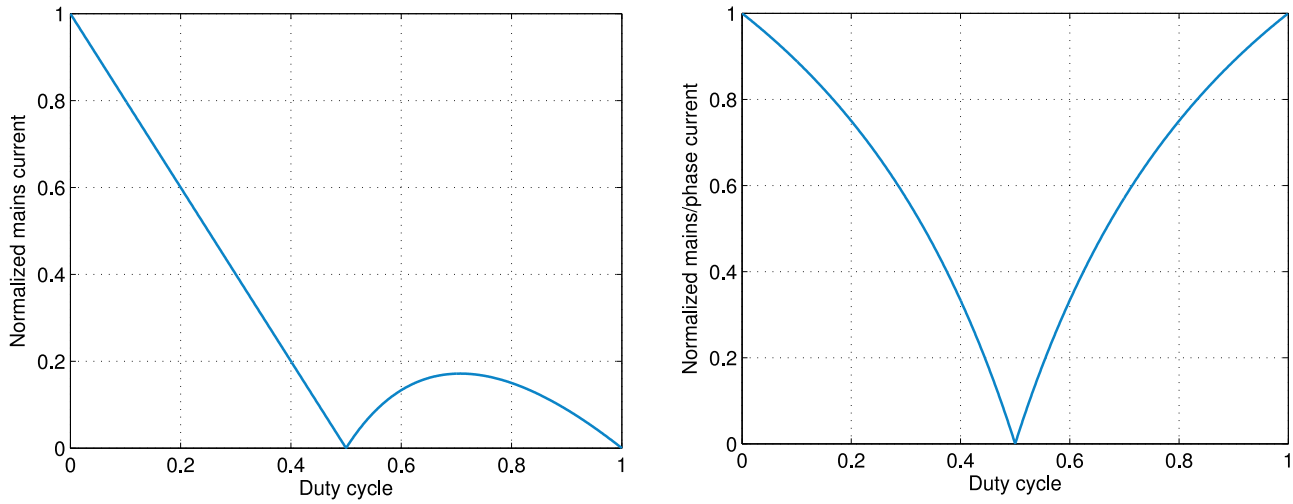
$$I_{o,\mathrm{rms}} = \sqrt{\frac{P_o}{R_L}}. \tag{20}$$

C. DC-Link Capacitor

Unlike the resonant capacitor, the dc-link current ripple fundamental frequency is twice the switching frequency. By neglecting the mains current ripple, the instantaneous current value in the dc-link capacitor is

$$i_{\mathrm{Cs}}(t) = \begin{cases} i_o - \frac{i_{\mathrm{ac}}}{2}, & 0 \le t < \left(\frac{1}{2} - \left|\frac{1}{2} - D\right|\right) T_{\mathrm{sw}} \\ 0, & \left|\frac{1}{2} - D\right| T_{\mathrm{sw}} < t \le T_{\mathrm{sw}}/2 \end{cases}. \tag{21}$$

$$I_{Ls,HF,\mathrm{rms}} = \frac{\Delta i_{Ls}}{2}\sqrt{\frac{1}{T_{\mathrm{sw}}}\int_0^{DT_{\mathrm{sw}}}\left(\frac{t}{DT_{\mathrm{sw}}} - 1\right)^2 dt + \frac{1}{T_{\mathrm{sw}}}\int_{DT_{\mathrm{sw}}}^{(1-D)T_{\mathrm{sw}}}\left(1 - \frac{t - DT_{\mathrm{sw}}}{(1-D)T_{\mathrm{sw}}}\right)^2 dt} \tag{18}$$



(a) (b)

Fig. 9 (a) Normalized mains current and (b) normalized mains current to phase current versus the duty cycle.

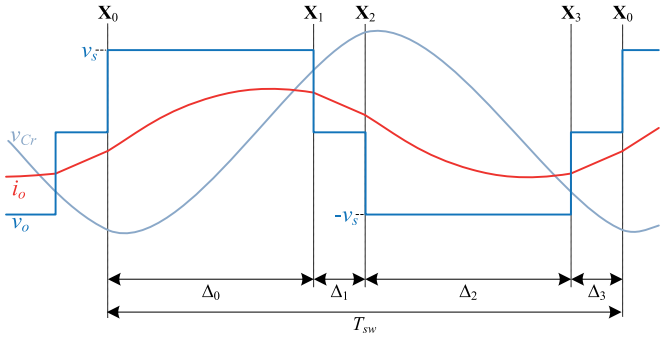


Fig. 10. Main resonant converter waveforms.

Both variables i_o and $i_{\rm ac}$ can be computed independently if $T_{\rm ac}>>T_{\rm sw}$ is considered. The rms value of i_o can be obtained by an energy balance analysis [24], whereas a constant value for a switching period is considered for $i_{\rm ac}$, yielding

$$I_{Cs,\rm rms} \approx \sqrt{\left(\sqrt{\frac{E_O - E_C - E_L}{R_L\,(T_{\rm sw}/2)}}\right)^2 + \left(\frac{i_{\rm ac}}{2}\sqrt{1-|1-2D|}\right)^2} \tag{22}$$

where

$$E_O = v_s C_r \left(V_{C_r,1} - V_{C_r,0}\right) \tag{23}$$

$$E_C = \frac{1}{2} C_r \left(V_{C_r,1}^2 - V_{C_r,0}^2\right) \tag{24}$$

$$E_L = \frac{1}{2} L_r \left(I_{o,1}^2 - I_{o,0}^2\right). \tag{25}$$

D. Rectifier Branch r

The mains current flows through the rectifier branch, and therefore, by neglecting the mains ripple and assuming high power factor, the rms current value $I_{r,\rm rms}$ results

$$I_{r,\rm rms} = I_{\rm ac,rms} = \frac{P_o}{V_{\rm ac,rms}}. \tag{26}$$

Considering the reduced mains frequency, switching losses in the rectifier branch can be neglected.

E. Inverter Branches A and B

Based on the symmetric modulation parameters, the rms current value are equivalent in both branches $I_{A,\rm rms} = I_{B,\rm rms}$. By neglecting the current ripple, this value can be obtained by the contribution of the boost and the resonant inverter stages, yielding

$$I_{A,\rm rms} = I_{B,\rm rms} = \sqrt{i_{o,\rm rms}^2 + \left(\frac{1}{2} i_{\rm ac,rms}\right)^2} = \sqrt{\frac{P_o}{R_L} + \frac{1}{4}\left(\frac{P_o}{V_{\rm ac,rms}}\right)^2}. \tag{27}$$

In order to decrease switching losses, a ZVS soft-switching behavior is preferred (see Fig. 12), eliminating turn-on losses. In order to compute the turn-off losses, a controlled current source is used to model the transistor current during the transition, whereas the transistor voltage is dominated by the equivalent device output capacitance $C_{\rm oss}$ [25].

Therefore, the turn-off switching losses $E_{\rm off}$ results

$$E_{\rm off} = \int_0^{t_{f,i}} i_{d,\rm off}(t) v_{ds}(t) dt \tag{28}$$

where

$$i_{d,\rm off}(t) = I_{d,\rm off}\left(1 - \frac{t}{t_{f,i}}\right) \tag{29}$$

$$v_{ds}(t) = \frac{1}{C_{\rm oss}(v_{ds}) + C_{\rm oss}(v_s - v_{ds})} \int I_{d,\rm off}\left(\frac{t}{t_{f,i}}\right) dt \tag{30}$$

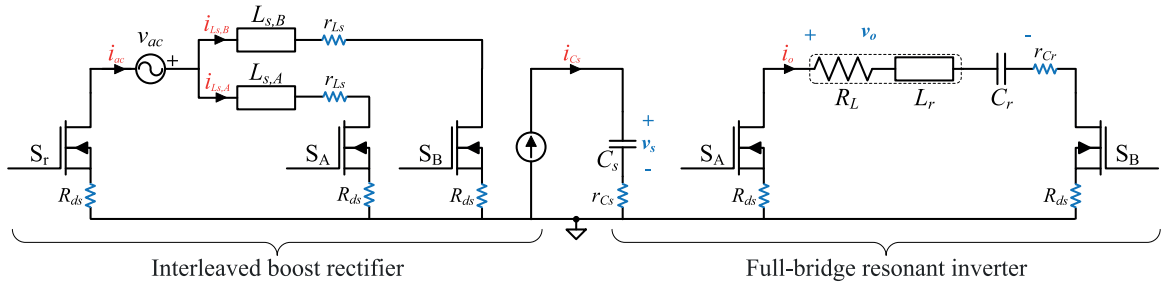


Fig. 11. Equivalent conduction losses model.

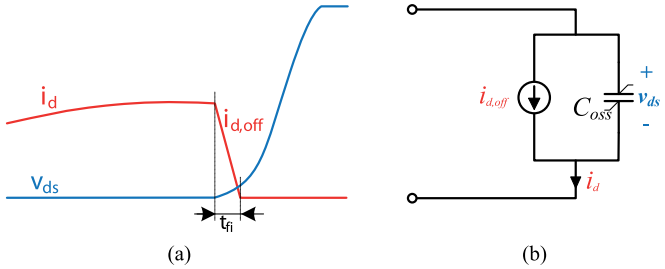


Fig. 12. Turn-off transition under ZVS soft-switching behavior. (a) Main waveforms and (b) equivalent model.

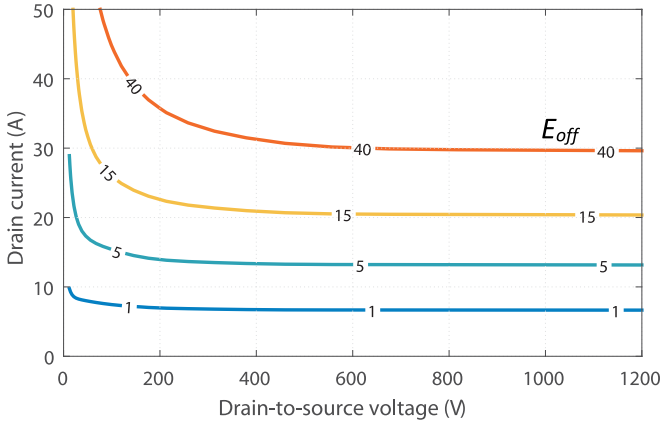


Fig. 13. Turn-off switching energy loss (μJ) as a function of drain current (A) and drain-to-source voltage (V).

and $I_{d,\text{off}}$ denotes the turn-off current. A turn-off losses energy diagram is depicted in Fig. 13 for the selected SiC power module.

The minimum turn-off current $I_{d,\text{off,min}}$, to ensure the charge/discharge of the output capacitance of the devices during the dead time t_{dt} results

$$I_{d,\text{off,min}} = \frac{\int_0^{v_s} C_{\text{oss}}(v) + C_{\text{oss}}(v_s - v)dv}{t_{dt}}. \tag{31}$$

Therefore, by applying the minimum turn-off current required to ensure the ZVS behavior, the soft-switching conditions result

$$\begin{cases} (I_{o,0} - |i_{Ls}/2|) < -I_{d,\text{off,min}} \\ (I_{o,1} - |i_{Ls}/2|) > I_{d,\text{off,min}} \end{cases}, \quad \text{for } D \leq \frac{1}{2}$$
$$\begin{cases} (I_{o,3} - |i_{Ls}/2|) < -I_{d,\text{off,min}} \\ (I_{o,2} - |i_{Ls}/2|) > I_{d,\text{off,min}} \end{cases}, \quad \text{for } D > \frac{1}{2}. \tag{32}$$

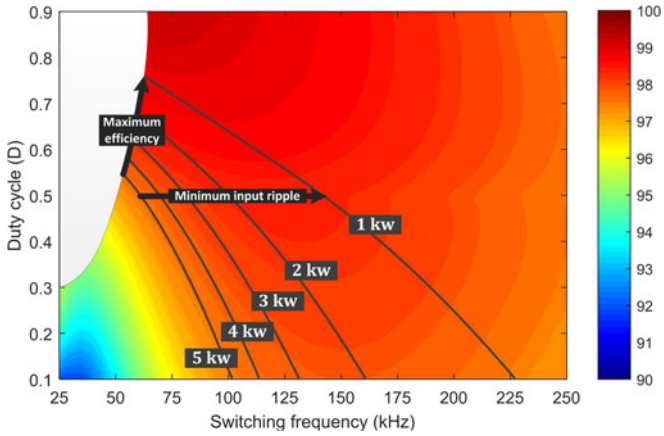


Fig. 14. Efficiency plane as a function of the control parameters.

V. Simulation and Experimental Results

In this section, the main simulation and experimental results are summarized. The proposed converter can be controlled using both the duty cycle, D, and the switching frequency f_{sw}. As it has been aforementioned, by holding the duty cycle to 50%, the minimum mains current ripple is achieved. However, it is important to note that the maximum efficiency can be achieved by varying simultaneously the duty cycle and the switching frequency. Both control strategies in order to minimize input current ripple or maximize efficiency have been represented in the efficiency diagram shown in Fig. 14. Depending on the application and required performance, either the efficiency or the input current ripple can be optimized accordingly. It is important to note that with both strategies, the efficiency slightly decays with reduced switching frequencies, mainly due to the higher current ripple which leads to additional losses.

The proposed converter has been designed and implemented to test the feasibility of this proposal. Table I summarizes the main design parameters and operational conditions. As shown in Fig. 15, the proposed converter has been implemented using a commercial three-phase SiC module (CCS050M12CM2) and controlled using an FPGA (XC6SLX45) for versatile modulation parameter control. A wide range of modulation strategies is enabled in order to allow the design space exploration and optimization. The main waveforms, including the mains voltage,

TABLE I
MAIN OPERATING RATINGS AND DESIGN PARAMETERS

Parameter	Value
Input voltage	230 Vrms
Output Power	1–5 kW
Switching frequency range	50–200 kHz
Duty range	0.3–0.75
IH load	
$L_{s,A} = L_{s,B}$	150 µH
R_L	22 Ω
L_r	70 µH
C_r	270 nF
Power devices	SiC module CCS050M12CM2
Digital control device	XC6SLX45

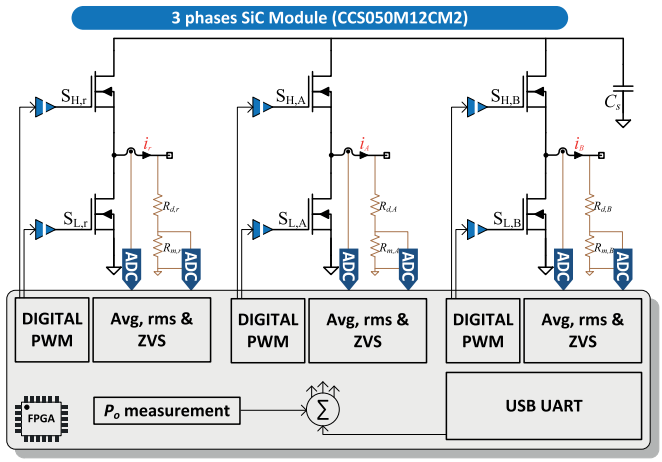


Fig. 15. Implementation diagram of the proposed converter.

operating at 100 kHz switching frequency have been depicted in Fig. 16.

Fig. 17 shows the main waveforms of the proposed converter close to the resonant frequency (50 kHz) and at a higher switching frequency (100 kHz) for 50% duty cycle. In these figures, the correct converter operation in the whole output power range can be observed. Besides, the main converter waveforms at 60 kHz for different duty cycles are shown in Fig. 18, showing its influence on the input current ripple.

Fig. 19 shows the detailed converter waveforms including the device control signals, and one half-bridge branch output current $i_{o,A}$ and output voltage $v_{o,A}$ to highlight the ZVS soft-switching operation for different operating conditions, including resonance at 50 kHz and $D = 50\%$ (a), higher switching frequency 100 kHz and $D = 50\%$, and asymmetric operation at 100 kHz, $D = 60\%$. In this figure, it can be seen that ZVS soft-switching conditions are achieved in the proposed converter operation range.

Finally, both simulated and measured converter efficiencies are shown in Fig. 20. Predicted values match the experimental ones, exhibiting efficiency above 97% in the whole operating range. To better understand the influence of each component,

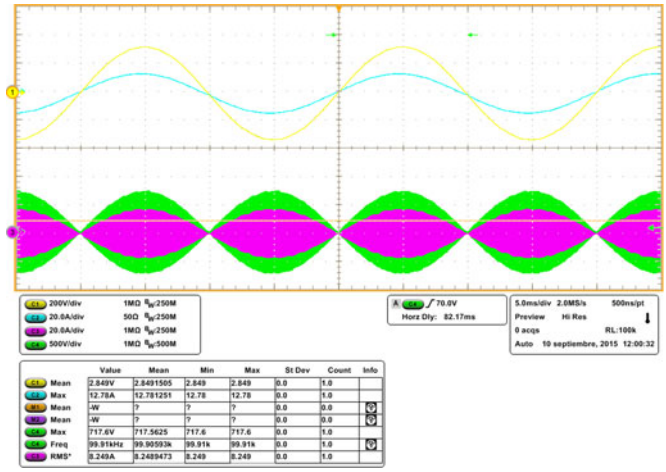


Fig. 16. Main waveforms at 100 kHz switching frequency and 50% duty cycle. From top to bottom: mains voltage $v_{\rm ac}$ (200 V/div), mains current $i_{\rm ac}$ (20 A/div), output voltage v_o (500 V/div), and load current i_o (20 A/div). Time 5 ms/div.

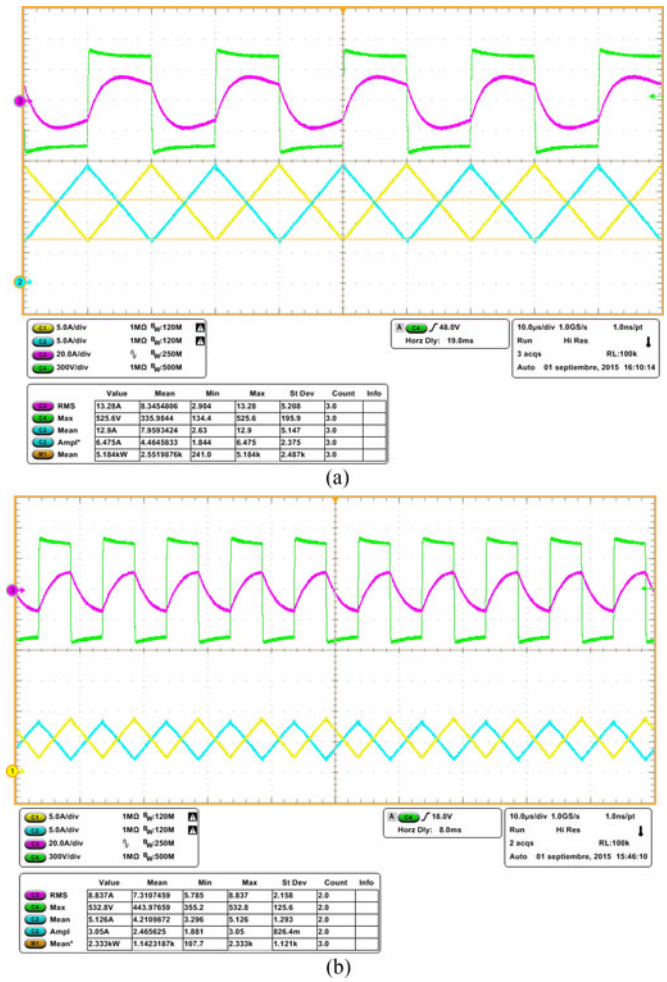


Fig. 17. Main converter waveforms at 50% duty cycle. Waveforms at (a) 50 kHz and (b) 100 kHz. From top to bottom: output voltage v_o (300 V/div), load current i_o (20 A/div), and lines current $i_{Lr,A}$,$i_{Lr,B}$ (5 A/div). Time 10 μs/div.

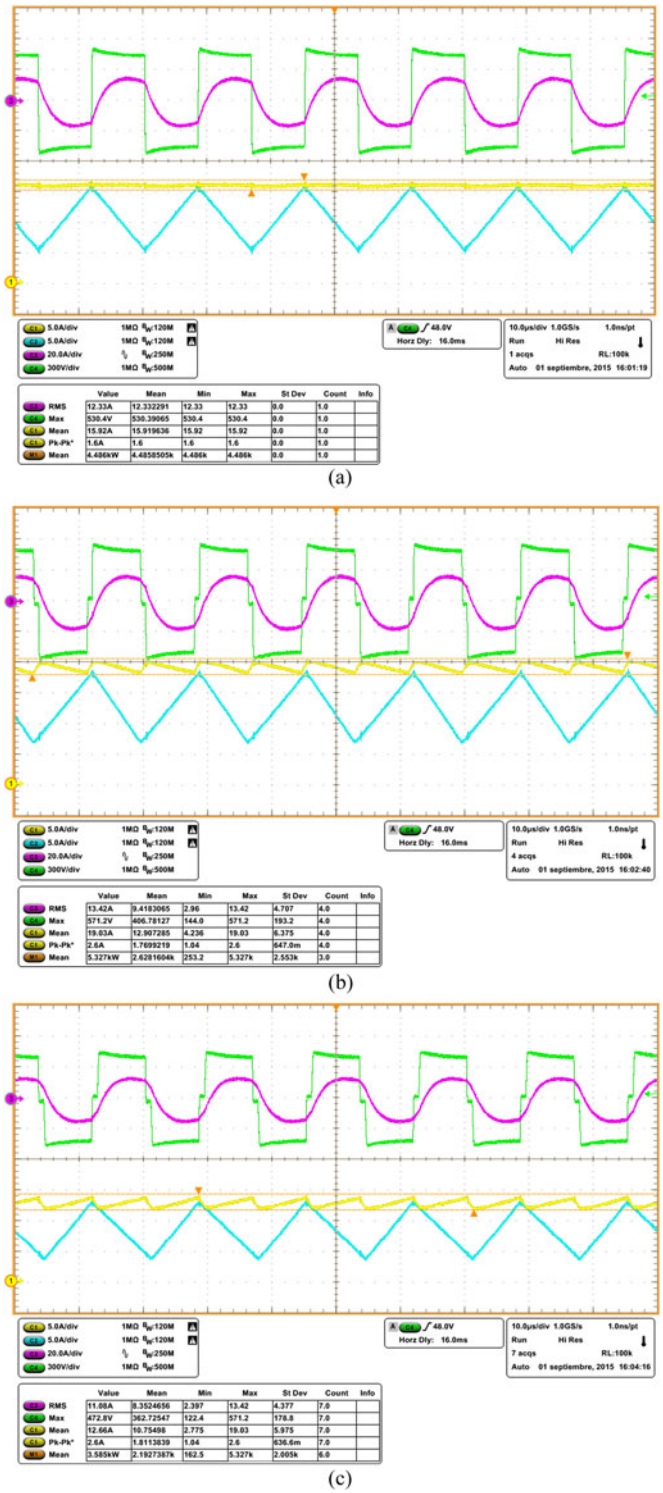


Fig. 18. Converter waveforms for different duty cycles at 60 kHz switching frequency. Waveforms for $D = 50\%$ (a), $D = 40\%$ (b), and $D = 60\%$ (c). From top to bottom: output voltage v_o (300 V/div), load current i_o (20 A/div), mains current $i_{\rm ac}$ (5 A/div), and phase current $i_{Lr,A}$ (5 A/div). Time 10 μs/div.

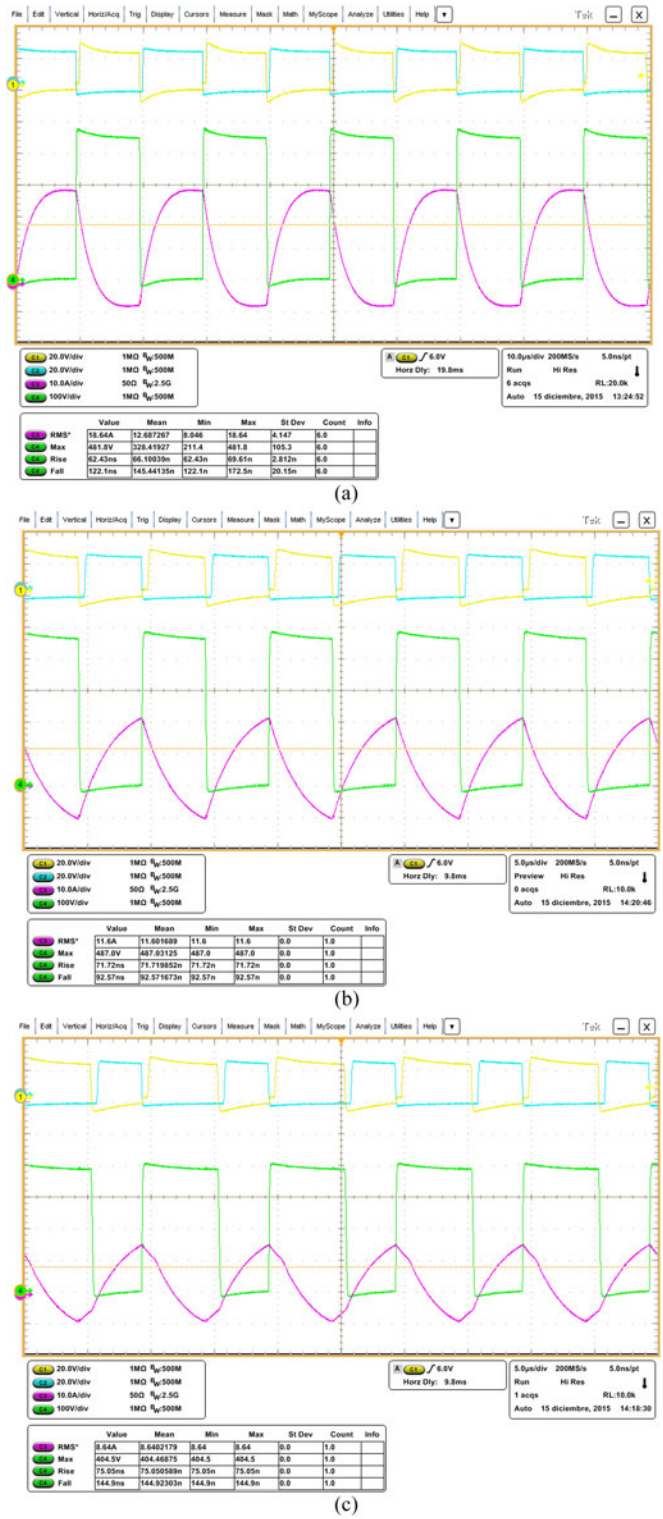


Fig. 19. Half-bridge branch waveforms highlighting ZVS soft-switching for different operating conditions: 50 kHz and $D = 50\%$ (a), 100 kHz and $D = 50\%$ (b), and 100 kHz and $D = 60\%$ (c). From top to bottom: control signals (20 V/div), half-bridge branch output voltage $v_{o,A}$ (100 V/div), and half-bridge branch output current $i_{o,A}$ (10 A/div). Time 5 μs/div.

a power loss distribution graph is shown in Fig. 21 for 5 kW output power. From this figure, it is clear that the main power loss contributions are due to the inductors and inverter branches—the focus of future efficiency optimizations.

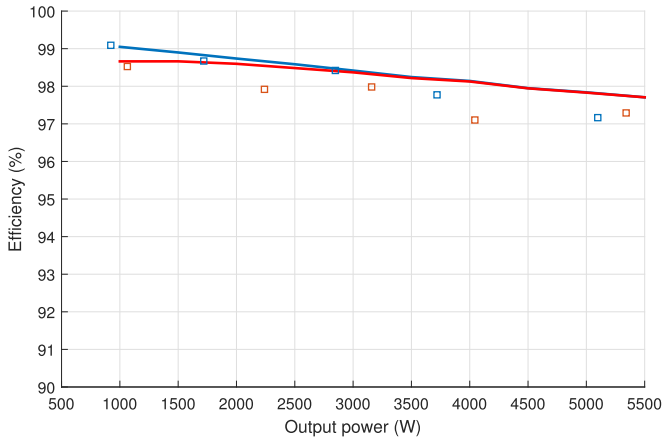


Fig. 20 Simulated (lines) and measured (dots) efficiency for the minimum input ripple and the maximum efficiency control strategies.

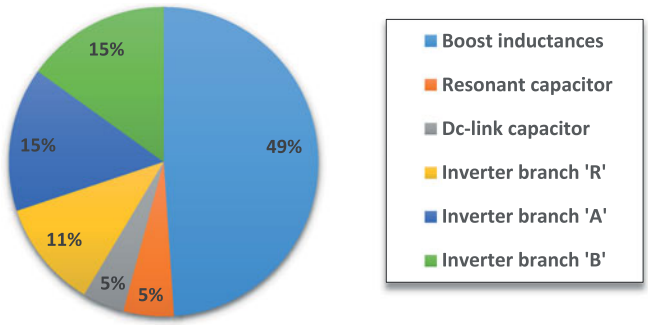


Fig. 21. Main analyzed power losses for the maximum output power (5 kW).

VI. Conclusion

In this paper, an interleaved boost resonant inverter for IH applications was proposed and deeply analyzed. The proposed converter enables high efficiency and high-performance operation, with improved control and reduced input current ripple.

An analytical model for the proposed converter was provided and a detailed power loss analysis was performed, enabling the converter design and optimization. The proposed converter was designed and implemented taking advantage of SiC technology, and the main experimental results proving the feasibility of this topology was discussed. As a conclusion, the interleaved boost resonant converter was proposed as a high-performance topology for industrial IH applications.

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Héctor Sarnago (S'09–M'15) received the M.Sc. degree in electrical engineering, and the Ph.D. degree in power electronics from the University of Zaragoza, Zaragoza, Spain, in 2010 and 2013, respectively.

He is currently a Senior Postdoctoral Researcher in the the Department of Electronic Engineering and Communications, University of Zaragoza. His current research interests include resonant converters and digital control for induction heating applications.

Dr. Sarnago is a Member of the Aragon Institute for Engineering Research (I3A).

Óscar Lucía (S'04–M'11–SM'14) received the M.Sc. and Ph.D. degrees (with Honors) in electrical engineering from the University of Zaragoza, Zaragoza, Spain, in 2006 and 2010, respectively.

During 2006 and 2007, he held a Research Internship at the Bosch and Siemens Home Appliances Group. Since 2008, he has been with the Department of Electronic Engineering and Communications, University of Zaragoza, where he is currently an Assistant Professor. During part of 2009 and 2012, he was a Visiting Scholar at the Center of Power Electronics Systems (CPES), Virginia Tech. His current research interests include resonant power conversion, wide-bandgap devices, and digital control, mainly applied to contactless energy transfer, induction heating, and biomedical applications. In these topics, he has authored or coauthored more than 50 international journal papers and 100 conference papers, and he has filed more than 25 patents.

Dr. Lucía is an active member of the Power Electronics (PELS) and Industrial Electronics (IES) societies. He was a Guest Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS in 2013 and 2015, respectively. He is currently an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE TRANSACTIONS ON POWER ELECTRONICS. He is a Member of the Aragon Institute for Engineering Research (I3A).

José Miguel Burdío (M'97–SM'12) received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Zaragoza, Zaragoza, Spain, in 1991 and 1995, respectively.

He has been with the Department of Electronic Engineering and Communications, University of Zaragoza, where he is currently a Professor, the Head of the Group of Power Electronics and Microelectronics, and the Director of the BSH Power Electronics Laboratory. During 2000, he was a Visiting Professor at the Center for Power Electronics Systems, Virginia Tech. He is the author of more than 80 international journal papers and over 200 papers in conference proceedings and the holder of more than 60 international patents. His current research interests include modeling of switching converters and resonant power conversion for induction heating and biomedical applications.

Dr. Burdío is a Senior Member of the Power Electronics and Industrial Electronics Societies. He is also a Member of the Aragon Institute for Engineering Research.