Experimental Investigation on the Effects of Narrow Junction Temperature Cycles on Die-Attach Solder Layer in an IGBT Module

Wei Lai, Minyou Chen, *Senior Member, IEEE*, Li Ran, *Senior Member, IEEE*, Shengyou Xu, Nan Jiang, Xuemei Wang, Olayiwola Alatise, *Member, IEEE*, and Philip Mawby, *Senior Member, IEEE*

***Abstract*—This paper presents a series of experiment results on the ageing effects of cyclic junction temperature variations (ΔT_j) of low amplitudes in power modules, to help the capturing of module reliability characteristics and the derivation of lifetime models in the future. Power cycling tests, for nonaged and aged modules, are designed to illustrate the failure mechanisms. Insulated gate bipolar transistor (IGBT) modules in actual converters are usually operated in a ΔT_j range up to 40 °C; therefore, tests are carried out to observe the effects of such narrow ΔT_j stress cycles on the module lifetime. It is found that the relatively minor stress cycles may not be able to directly initiate a crack but can contribute to the development of damage in the die attach solder layer due to stress concentration. Finite element analysis modeling is utilized to verify the stress concentration effect. The experiment results show that the effects of the narrow ΔT_j stress cycles are affected by the ageing status of the module and the stress level itself.**

***Index Terms*—Narrow junction temperature cycles, power cycling test, reliability, stress concentration, solder failure.**

NOMENCLATURE

$T_{j\max}$	Maximum of junction temperature.
$T_{j\min}$	Minimum of junction temperature.
ΔT_j	Amplitude of junction temperature cycle at the beginning of each test.
T_{jm}	Mean value of junction temperature cycle at the beginning of each test.
T_c	Case temperature.
$T_{c\max}$	Maximum case temperature.
$V_{\rm ce}$	IGBT on-stage voltage drop.
σ	Mean tensile stress.
$\sigma_{\rm crack-tip}$	Tensile stress at the tip of a crack.
a	Major diameter of the crack.
b	Minor diameter of the crack.
Rth	Thermal resistance between junction and case.
$R_{\rm th0}$	Initial thermal resistance between junction and case.
K	Rate of thermal resistance increase.
r_p	Plastic zone width.
DUT	Device under test.
Δvon-Mises	Difference of the maximum and minimum stresses at the crack tip during one cycle.

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W. Lai, M. Chen, S. Xu, and N. Jiang are with the State Key Laboratory of Power Transmission Equipment and System Security and New Technology, School of Electrical Engineering, Chongqing University, Chongqing 400044, China (e-mail: laiweicqu@126.com; mchencqu@126.com; sheng_you_xu@163.com; 1094326873@qq.com).

L. Ran was with the State Key Laboratory of Power Transmission Equipment and System Security and New Technology, School of Electrical Engineering, Chongqing University, Chongqing 400044, China. He is now with the School of Engineering, University of Warwick, Coventry, CV4 7AL, U.K. (e-mail: l.ran@warwick.ac.uk).

X. Wang is with the School of Electric Power, South China University of Technology, Guangzhou 510640, China (e-mail: 6543804@qq.com).

O. Alatise and P. Mawby are with the School of Engineering, University of Warwick, Coventry, CV4 7AL, U.K. (e-mail: o.alatise@warwick.ac.uk; p.a.mawby@warwick.ac.uk).

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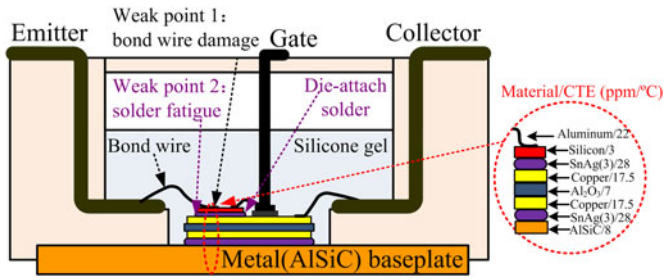

Fig. 1. Part of an IGBT module structure.

I. INTRODUCTION

INSULATED gate bipolar transistors (IGBTs) are now the main components in most power electronic systems, playing a key role in delivering flexible control of electric energy and efficient power conversion. However, semiconductor modules are one of the most vulnerable components [1], [2]; meanwhile, temperature is the predominant source of stresses causing module fatigue and has the most significant impact on reliability [3], [4]. Therefore, it is important to carry out electrical–thermal–mechanical analyses on the power modules in order to enhance the knowledge about their reliability characteristics.

In all converters, the junction temperature T_j fluctuates as the load condition varies. Due to temperature cycling, the mismatch of coefficients of thermal expansion (CTE) between adjacent layers and internal temperature gradients, a module can be subject to cyclic shear stresses, leading to fatigue damage. Part of an IGBT module structure is shown in Fig. 1, with two weak points

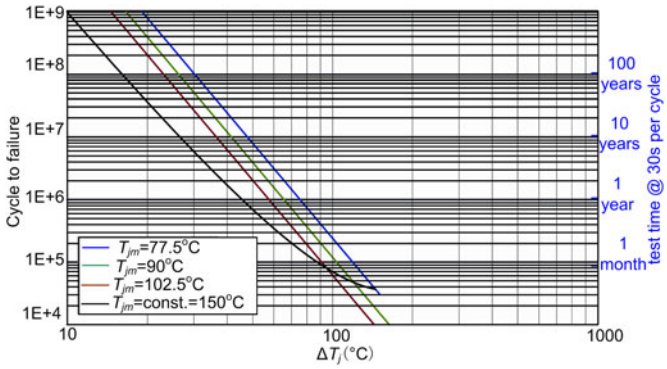

Fig. 2. Power cycling lifetime as a function of ΔT_j and T_{jm} [16].

at the interfaces. The most commonly observed failure modes are bond wire liftoff [5], [6] and solder delamination [7]–[9]. Depending on the cooling arrangement, the case temperature T_c may also fluctuate with the load condition and this is important when considering the thermomechanical wear out of the solder layer between the module base-plate and substrate. Huang and Mawby [10] show that the die-attach solder fatigue is usually more dominant while bond wire joints start to degrade when the junction temperature is above 200 °C. The failure mechanism of solder interconnections as well as microstructural observations of the primary cracks are reported in [11] with a junction temperature profile between 25 and 125 °C. Power cycling tests above $\Delta T_j = 80$ °C are used to account for thermal fatigue life behavior of different solder joint composition [12]. Previous studies of power cycling test focused on large ΔT_j (≥80 °C) [13]–[15] because the small ΔT_j ageing test would take a long time. But in an actual inverter ΔT_j is only about 40 °C. Wintrich *et al.* [16] indicate that a narrow power cycling test with $\Delta T_j = 30$ °C would take 30–100 years, as shown in Fig. 2. It is unrealistic to test to the end of lifetime under such stress conditions.

It is well known that stress concentration can be very high at a crack tip and decreases gradually away from the tip. It means that once there is the initial crack in the solder, the effects of the small ΔT_j may not be ignored. Normally, two basic types of accelerated ageing tests are used to analyze the failure mechanism and assess reliability of power modules. The first type is passive temperature cycling, where the modules under test are stressed by external changes of temperature [17]. The other type is power cycling, which is an active test because the stress is generated by the power losses inside the device [18]. The latter is more suitable to study the effects of narrow junction temperature cycles on the power modules in different stages of the ageing process. This paper mainly examines the effects and characteristics of the small ΔT_j stress cycles on the aged and unaged modules.

II. Power Cycling Tests

A. Power Cycling Test Rig

The main electrical circuit of the power cycling rig is shown in Fig. 3. Four IGBT single-chip modules (SKM50GB12T4, 50 A/1200 V) are connected in series to ensure that all chips are

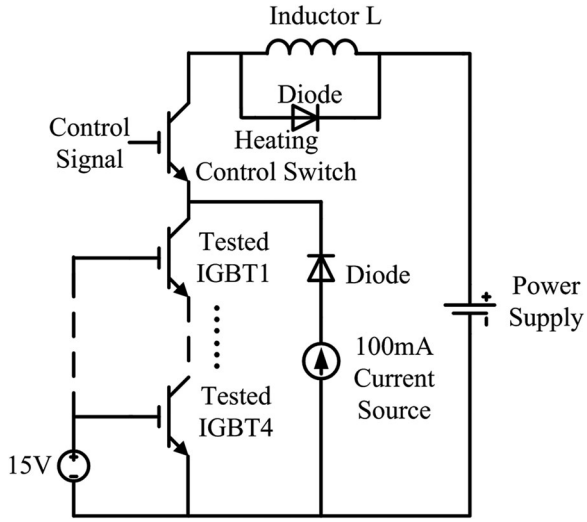

Fig. 3. Main circuit of power cycling test rig.

under the same cycling current, which is controlled using the remote current mode of the power supply. The control strategy of the rig keeps the maximum swing of the case temperature constant. This leads to ΔT_j varying as ageing proceeds. A 100 mA current source is connected through all modules, which are permanently gated on. In this setup, a heating up phase is initiated by closing the heating control switch. When the heating control switch turns off according to the set $T_{c\max}$, the IGBTs are then sent into a cooling phase, at which moment every IGBT module's $T_{j\max}$ is obtained by measuring the corresponding $V_{\rm ce}$. During cooling, the current going through the IGBTs is always 100 mA, therefore the measurements of $V_{\rm ce}$ will continually indicate the decaying junction temperature [19]–[21]. This temperature-sensitive electrical parameter (TSEP) method is verified in [22]. The module thermal resistance *R*th is obtained at the beginning of each cooling phase from the junction-above-case temperature and the power loss, which can be calculated from the voltage and current. The minimum junction temperature $T_{j\min}$ is obtained in a similar way at the end of the cooling phase and beginning of the next heating up phase. $T_{j\max}$ and $T_{j\min}$ define the stress level ΔT_j, which can be adjusted by the duty cycle and period of the heating control switch. But the stress level ΔT_j is not directly controlled to be constant because as the modules start to degrade this will cause the $T_{j\max}$ to be higher than before. An inductor is connected in the circuit to limit the current overshoot when the heating control switch turns on.

B. Large ΔT_j Power Cycling Tests

In actual applications, converters mainly operate under intermittent and/or variable-load conditions. The temperature swing on the die is typically situated between 10 and 40 °C [23], corresponding to a predicted lifetime greater than one million cycles. It would be therefore impossible to conduct lifetime testing under realistic stress conditions that are of interest. Previous studies of power cycling focus on large ΔT_j above 80 °C [14],

[15], [24] to shorten the test time. Therefore, large ΔT_j power cycling tests are designed to obtain the ageing-to-failure process of power modules and analyze the effect of thermomechanical wear out, as shown in Fig. 4. This will lay the theoretical foundation for the low ΔT_j study. Device degradation is monitored at the end of each heating phase by comparing the measured $V_{\rm ce}$ and thermal resistance of the module *R*th with their initial values.

According to (1), the increasing steady-state thermal resistance of the power module will lead to increasing junction temperature for the same case temperature, current, and voltage. This is verified in Fig. 4(a) and (b). Both the thermal resistance and junction temperature increase after 60 000 cycles, which take 28 days to complete. The heating time and cooling time are about 25 and 15 s, respectively, in each cycle. The higher junction temperature will lead to accelerated ageing of the module. Fig. 4(c) shows that when the die-attach solder has degraded, the bond wires start to degrade because the increased thermal resistance leads to the increase of junction temperature. The voltage changing trend agrees with previous research [25]

$$T_j - T_c = V_{\rm ce} \cdot I_c \cdot R_{\rm th}. \tag{1}$$

Comparing Fig. 4(a) and (c) shows that the solder degrades faster when ΔT_j is higher, which agrees with previous research [14], [15], [24]. The die-attach solder degrades before the bond wire degrades and the bond wire failure process lasts for about 3000 cycles from initial wear out to complete failure (Module wear out 3). This is because the junction temperature increases with the growth of the thermal resistance, which leads to bond wire liftoff. Therefore, bond wire liftoff is accelerated by solder cracking and the subsequent rise of junction temperature. The die-attach solder fatigue is the main failure mechanism, and it is necessary to analyze its process of development.

It is well known that the reliability of power semiconductor modules mainly suffers from fatigue and creep, which lead to the wear out of packaging materials. Fatigue is a progressive structural damage caused by a repeated oscillating stress below the yield stress of a material. The thermomechanical stress caused by the junction temperature cycling and CTE mismatch are the main reasons for the fatigue failure. Therefore, the solder wear-out process is divided into two stages, as shown in Fig. 4(c). First, it starts with dislocation movements, forming persistent slip bands that act as stress risers and nucleate microscopic cracks in stage ①; the threshold that defines the end of the stage and the start of stage ② is arbitrarily set as 0.5% increase from the initial thermal resistance value. Then macroscopic cracks will be initiated in the areas of stress concentration which is followed by incremental crack propagation and leads to final fatigue failure in stage ②. ΔT_j will vary as degradation proceeds due to the control strategy adopted for the test rig, which only keeps ΔT_c constant. Therefore, in stage ①, only large ΔT_j would be an issue while in stage ②with an initial crack both large and small ΔT_j may cause further damages.

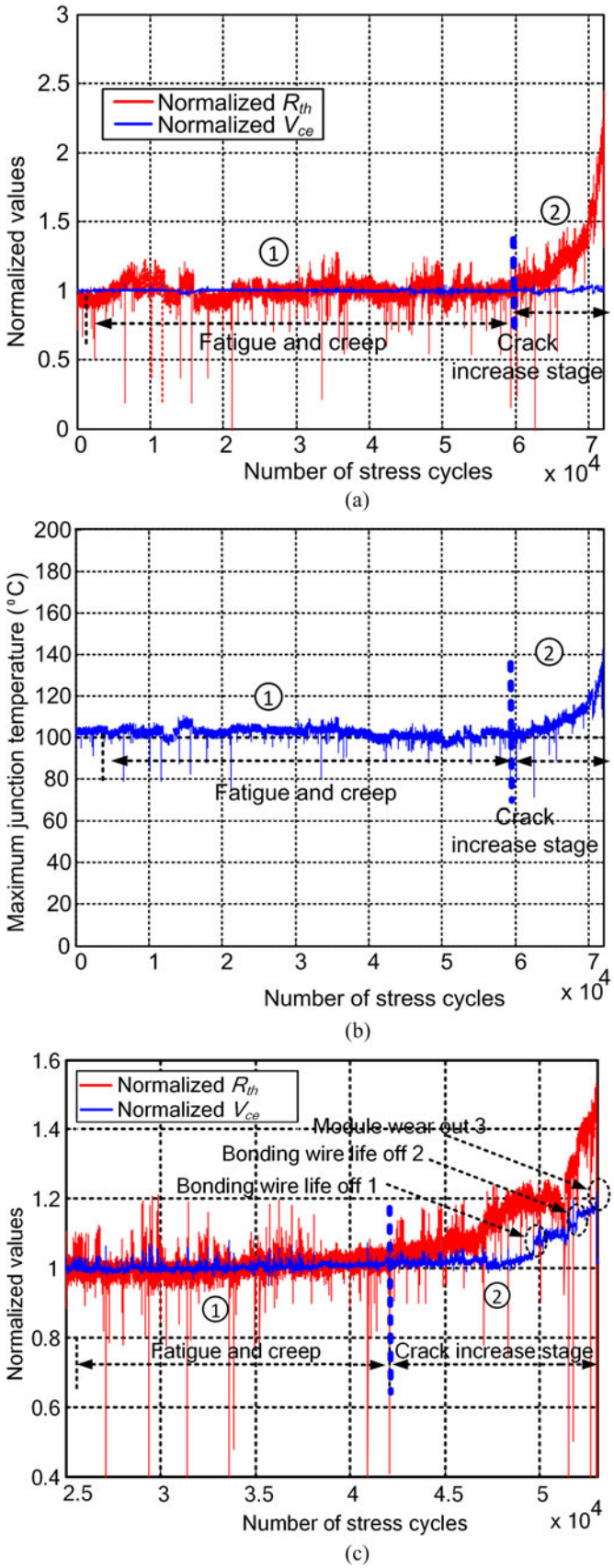

Fig. 4. Results of power cycling test. (a) Normalized *R*th and $V_{\rm ce}$ under $\Delta T_j = 71$ °C; (b) junction temperature under $\Delta T_j = 71$ °C; (c) normalized *R*th and $V_{\rm ce}$ under $\Delta T_j = 94.3$ °C.

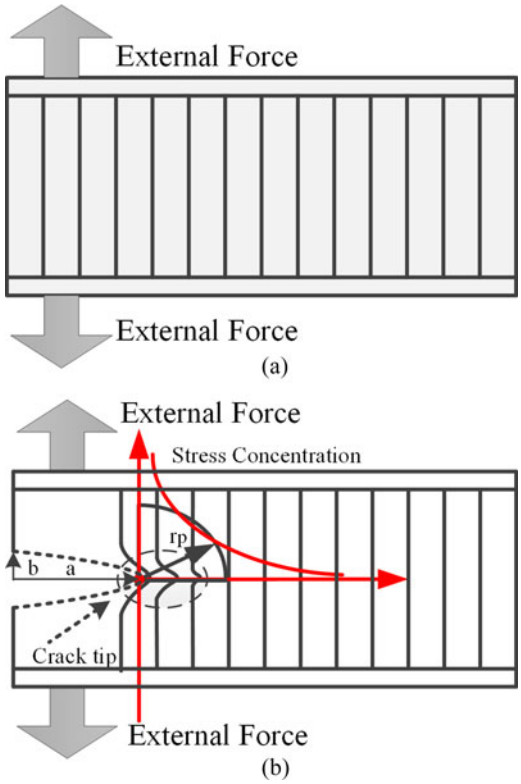

Fig. 5. Contour lines of stress (a) without and (b) with crack. (a) Contour lines of stress are uniform and parallel initially, producing a uniform stress which equals to the ratio of force and area. (b) The introduction of the crack causes the contour lines of stress to become nonuniform and nonparallel.

III. Stress Concentration Under Different Conditions

A. Stress Concentration

Most of the fractures initiate on the corners, where there is a local stress concentration. A stress concentration is usually due to geometric discontinuities located in an object. Geometric discontinuities cause an object to experience a local increase in the intensity of a stress field. Examples of shapes that cause such concentrations are cracks, sharp corners, holes, and changes in the cross-sectional area of the object. A material can fail via a propagating crack, when a concentrated stress exceeds the material's cohesive strength. High local stresses can cause objects to fail more quickly; therefore, an example is used to illustrate the principle as follows. The contour lines of stress before and after an initial crack introduction are shown in Fig. 5. Without the initial crack, the contour lines of stress are uniform and parallel, as shown in Fig. 5(a), producing a mean tensile stress σ which equals the ratio of force to area. However, it is changed with a crack, as shown in Fig. 5(b). The nonuniform distribution produces a crowding of force lines at the crack tip [26], but the contour lines of stress will become uniform and parallel again away from the crack tip meanwhile a plastic zone is produced at the crack tip [27], [28]. The higher density of force lines at crack tip produces an increased stress [29]–[32]. The larger the crack length is, the greater impact of stress concentration will be [26]. For a propagating crack, the stress at the tip must be greater than the strength of the material. Therefore, it can be completely different with or without an initial crack under the same conditions due to the stress concentration.

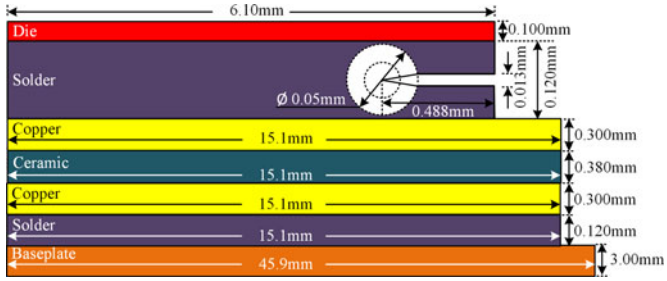

Fig. 6. Sizes of crack.

B. Simulation of Stress Concentration

ANSYS models with or without a crack are established to verify the stress concentration under narrow ΔT_j profiles. A crack, as shown in Fig. 6 whose width and length are 0.013 and 0.488 mm, respectively, is selected corresponding to an *R*th increase of about 10%. Test module geometry, materials, and junction temperature profiles are used in the model. The junction temperature profiles are obtained from power cycling test, as shown in Fig. 7(a) and (b). Fig. 7(c) shows that the contour lines of stress are uniform and parallel away from the corners of solder, while the stress is concentrated at the corner. The stress near the crack tip, rather than at the tip itself, is obtained in the simulation due to the singularity. Linear elastic stress analysis of sharp cracks predicts infinite stresses at the crack tip. In real materials, however, stresses at crack tips are finite [29]. Fig. 7(d), (e) and (f) shows that the stress is largest at and gradually drops away from the crack tip. Fig. 7(f) shows that the maximum stress is almost five times as large as the mean stress, which may cause the crack to propagate under $\Delta T_j = 40$ °C. The maximum stress when $T_j = 95$ °C with crack is more than double as compared to the case without crack, as shown in Fig. 7(a). The stress near the crack tip is larger than that when $T_j = 140$ °C by comparing Fig. 7(a) with Fig. 7(b). The results agree with previous results: the stress at the crack tip is much higher than σ [29]–[32], and the stress gradually drops away from the crack tip and approaches σ eventually. Moreover, the larger crack length is, the greater impact of stress concentration will be [26].

C. Effect of Different Stress Level on Power Module Solder Joint

Further simulation cases with the previous crack size are performed to obtain the stress distribution under different stress levels, as shown in Fig. 8. Fig. 8(a) and (b) shows that larger ΔT_j causes larger fatigue stress near the crack tip. Fig. 8(b) plots the Δvon-Mises as the difference of the maximum and minimum stresses near the crack tip. It shows that when $\Delta T_j \leq 10$ °C, the Δvon-Mises is so small (<45 MPa) that the crack would not progress, i.e., the rate of degradation is low. Bond wire failure

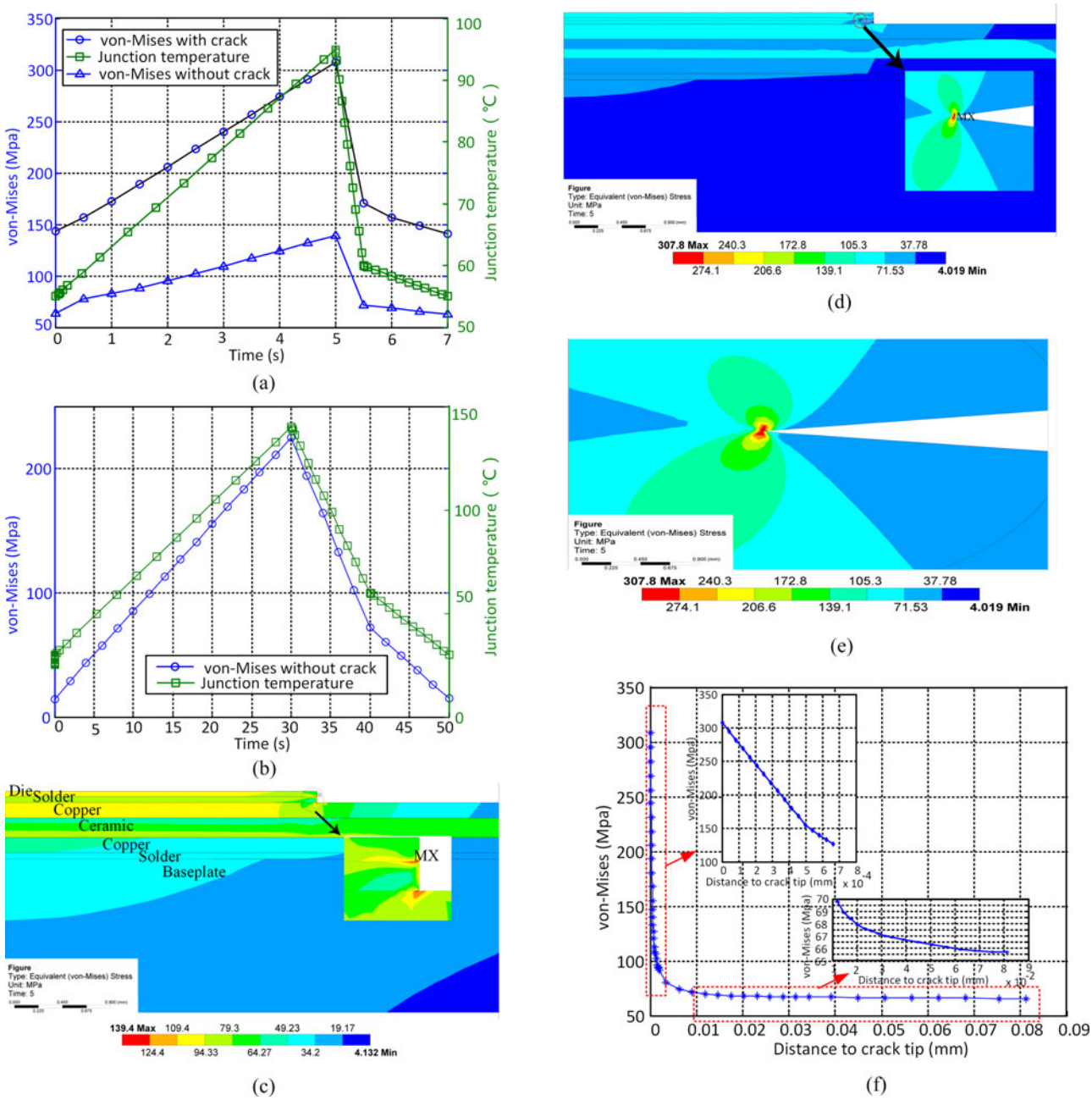

Fig. 7. Results of ANSYS simulation. (a) Junction temperature and stress under $\Delta T_j = 40$ °C. (b) Junction temperature and stress without preset initial crack under $\Delta T_j = 110$ °C. (c) Stress distribution without crack under $T_j = 95$ °C. (d) Stress distribution with crack under $T_j = 95$ °C. (e) Enlargement of the near crack tip for solder layer under $T_j = 95$ °C. (f) Stress away from crack tip.

and die-attach solder layer fatigue are mainly caused by the cyclic shear stress between adjacent layers due to the mismatch of the products of CTE and temperature. Therefore, the following narrow ΔT_j power cycling tests are mainly designed around 30–40 °C. Fracture mechanics applies to cracks that are infinitely sharp prior to loading. While laboratory specimens inevitably fall short of this ideality, it is possible to introduce cracks that are sufficiently sharp for practical purposes. The most efficient way to produce such a crack is through cyclic loading.

IV. Narrow ΔT_j Power Cycling Tests and Analysis of Thermal Resistance Characteristics

According to the simulation results, the effects of stress concentration are affected by the stress level for a preset initial crack. However, stress concentration does not distinctly exist without an initial crack. Therefore, not only power cycling tests should be conducted for aged and nonaged modules under the same conditions, but also the repeatability should be demonstrated. Experiments and Huang and Mawby [10] indicate that a 50% increase of *R*th would be an appropriate inflection point.

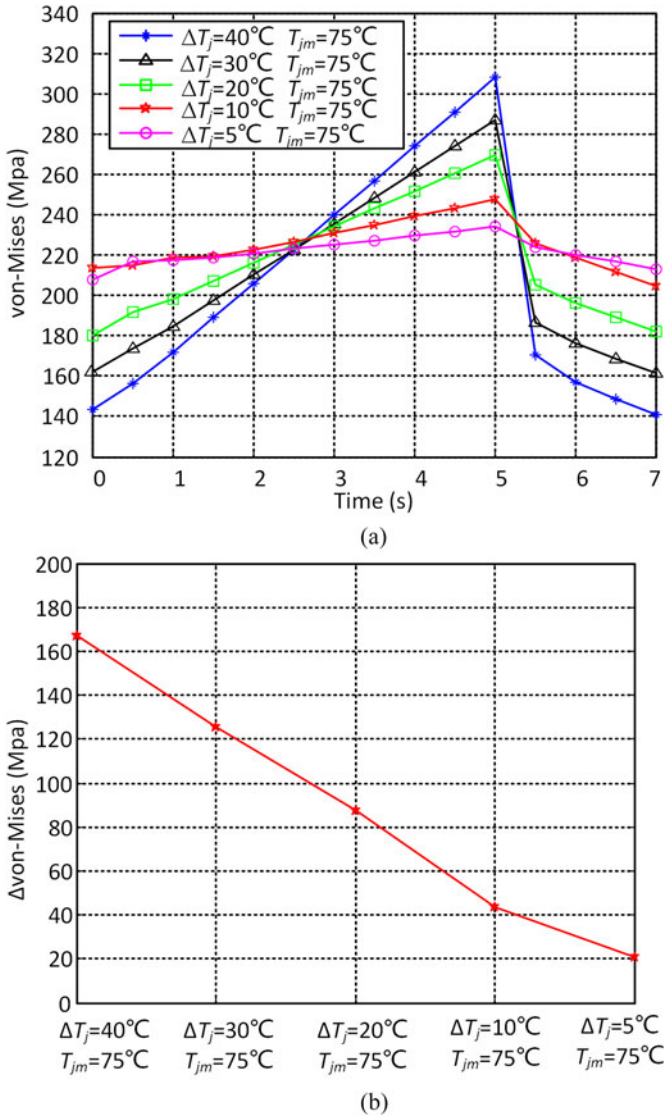

Fig. 8. Results of ANSYS simulation under different load profiles. (a) von-Mises under the different ΔT_j. (b) Δvon-Mises.

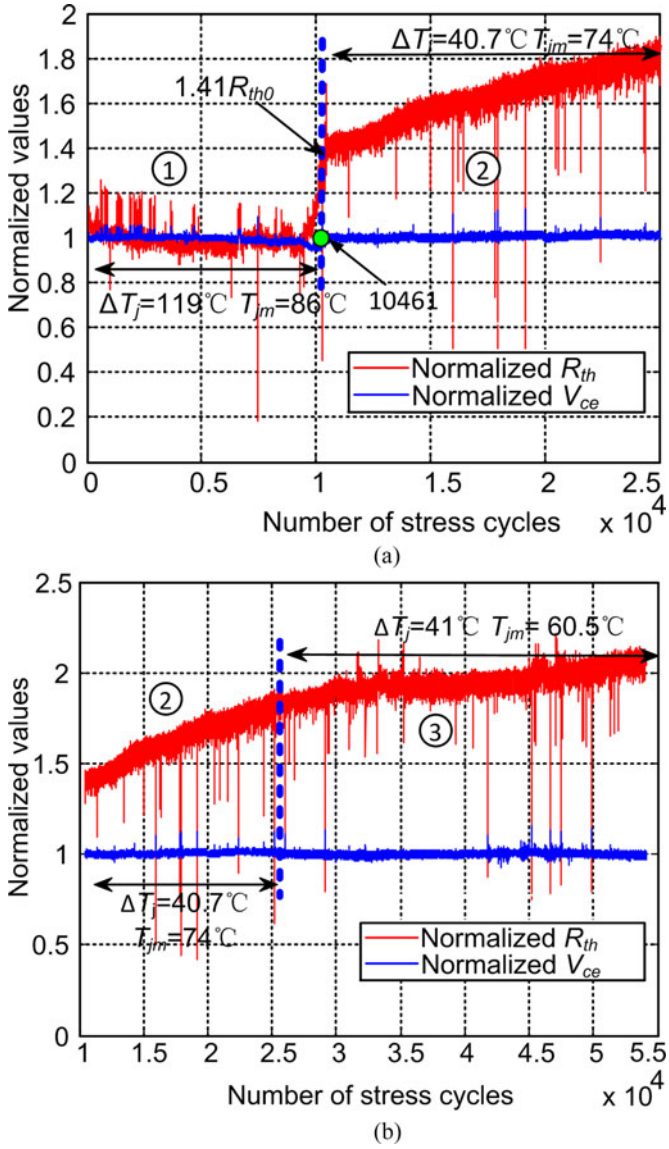

Fig. 9. Results of power cycling test under narrow ΔT_j. (a) Normalized *R*th in a new module under large ΔT_j. (b) Normalized *R*th in aged module under narrow ΔT_j.

Therefore, this paper mainly studies the behavior of *R*th between its initial value of a nonaged module and an increase of 50%. A series of power cycling tests are designed to verify the effects. In one test, four IGBTs have no complete same ΔT_j due to the difference of modules and setup place on the heat sink. One test is designed with four same type module in the series connection so that the earliest degraded module could be found to shorten the test time. The degraded module could be used for small ΔT_j test.

A. *Narrow ΔT_j Power Cycling Test 1*

The earlier discussion has shown the importance of obtaining the effects of narrow ΔT_j stress cycles on the solder layer in the second stage of power module ageing (with macroscopic cracks). In order to verify the effects, test plans which are completely different to previous power cycling tests are designed. Given the difficulty to wear out a new module, a staged test scheme is proposed in this study. Some new modules are first subject to large ΔT_j cycles to cause initial solder cracks. Once the thermal resistance reaches a preset value, which can change from test to test, the stress cycles will be reduced to the 30–40 °C range. The degradation level at which the changeover takes place can be controlled so that the effects the module's present condition on the further progress of ageing can be investigated.

The first test aims to show qualitatively, the respective effects of ΔT_j, the mean junction temperature T_{jm} and the present solder pad condition, as shown in Fig. 9. New modules are first subject to a sufficient number of stress cycles with $\Delta T_j = 119$ °C and $T_{jm} = 86$ °C to cause 41% increase of *R*th. This test is to prove for the first time the effect of narrow ΔT_j, stress cycles. Therefore, a seriously degrade state (41%) is selected. Further change of *R*th is monitored under $\Delta T_j \approx 40$ °C and

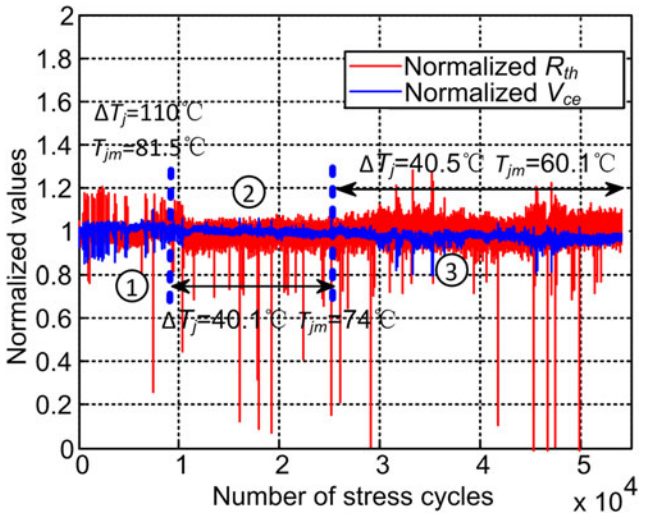

Fig. 10. Normalized *R*th in nonaged module under narrow ΔT_j.

$T_{\rm jm} = 74$ °C as the number of stress cycles increases. *R*th is normalized with respect to its initial value for the new module: $R_{\rm th0}$. Fig. 9(a) shows that the thermal resistance still increase under $\Delta T_j = 40.7$ °C and $T_{\rm jm} = 74$ °C, because once there is a crack the stress close to the crack tip is greater than the average stress applied to the solder layer due to stress concentration, meanwhile a plastic zone is formed around the tip. The module is more likely to further degrade than in the case without a crack. The number of cycles is set as 15 000 from stage ② to ③. Comparing Fig. 9(a) with Fig. 9(b) shows that the higher the mean junction temperature is, the faster the crack progresses. This is because the higher mean temperature leads to larger thermomechanical stress caused by the CTE mismatch, agreeing with the previous LESIT results [24]. The DUT's normalized collector–emitter voltage $V_{\rm ce}$ under the heating current and with temperature compensation [10] is also included in the plot to monitor the bond wire failure. In Fig. 9(a) and (b), $V_{\rm ce}$ does not change indicating that bond wire liftoff is not taking place due to the maximum junction temperature being still modest. Huang and Mawby [10] showed that the die-attach solder fatigue is the dominant failure mechanism while the bond wire starts to degrade when junction temperature is above 200 °C. Morozumi *et al*. [15] showed that cracks occur at the interface between the die and the bond wire when ΔT_j is more than about 100 °C.

B. Narrow ΔT_j Power Cycling Test 2

Test 2 is designed to show the effect of narrow ΔT_j on nonaged modules. First, the new modules are tested under large ΔT_j cycles, which are less stressful than in the first stage of the previous test. After that the test conditions are changed into the same conditions as stages ② and ③ in the previous test, which is shown in Fig. 10. The condition of a nonaged module, measured by the junction-to-case thermal resistance *R*th, hardly changes. The stress level is now lower in stage ①, and as a result, cracks are not formed, and the temperature cycling in stages ② and ③ has little effect. Comparing Fig. 9 with Fig. 10 confirms that the narrow ΔT_j stress cycles would only affect aged modules. As analyzed before once there is a crack in the solder layer, the stress close to the crack tip becomes greater than the overall average due to stress concentration meanwhile a plastic deformation zone is formed around the tip, causing progressive degradation. Therefore, it may be the case that narrow ΔT_j stress cycles should not be ignored for modules that are already aged.

C. Narrow ΔT_j Power Cycling Test 3

Test 3 is designed to verify the repeatability and show the effect of $T_{\rm jm}$ by using a different module. *R*th is first pushed up by 17% instead of 41%. The test results are shown in Fig. 11. The effect of further narrow ΔT_j stress cycles is again observed, as shown in Fig. 11(a), but is reduced when compared to the previous results for the same ΔT_j and $T_{\rm jm}$ on a more aged module [see Fig. 9(a)]. The ageing effect is still present when ΔT_j is reduced close to 30°C. If the thermal resistance is larger and the crack is longer, the stress concentration effect will be stronger. The on-state voltage does not change in the whole power cycling test from Fig. 11(a) and (b). Therefore, there is no bond wire failure. Fig. 11(c) shows the measured ΔT_j during the test. It shows that as the die-attach solder degrades, the thermal resistance increase leads to the increase of junction temperature, because the minimum junction temperature is fixed and the maximum case temperature is controlled.

D. Narrow ΔT_j Power Cycling Test 4

*R*th had been significantly increased in the previous tests. Therefore, test 4 is conducted to verify the effect of narrow ΔT_j from an even lower initial aged status. The modules are tested under four different stress levels. The results and test conditions are shown in Fig. 12. It shows that the narrow ΔT_j stress cycles still have effect on the slightly aged module (1.06 *R*th). According to the results, the degradation rate of thermal resistance depends on the current *R*th and further stress level. Tests below $\Delta T_j = 28$ °C were not performed due to the time limit; it took 28–40 days for each test performed.

The increase rates of thermal resistance in test 1, test 3, and test 4 are estimated for different stages and are listed in Table I. For the same stress condition, the increase rate of test 1 is generally greater than in test 3 and test 4. The thermal resistance is an indication of the total crack length. A longer crack length implies stronger stress concentration effect [33]. Therefore, a more degraded module would correspond to the greater increase rate of *R*th. It is observed that the rate in stage ③ of test 1 is smaller than that in stage ② of test 3, while the degradation in stage ③ of test 1 is faster than in stage ② of test 3. This shows the mean junction temperature effect in addition to ΔT_j. Comparing stages ② and ③ of test 3 clearly shows that the higher the stress level, the greater the increase rate. It also shows that the higher the mean junction temperature, the greater the increase rate.

E. Characteristics of Thermal Resistance

One more narrow ΔT_j test is designed to demonstrate the independence of further ageing on the history leading to the

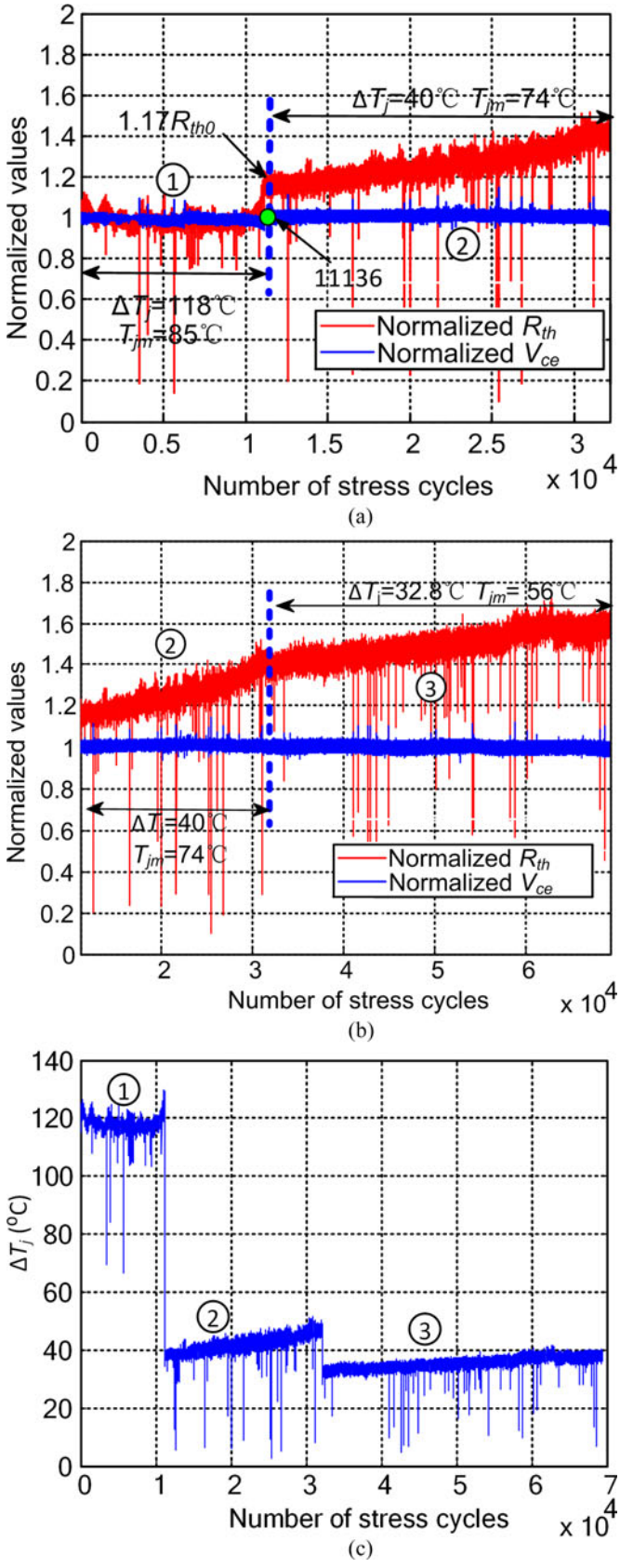

Fig. 11. Results of power cycling test under narrow ΔT_j. (a) Normalized *R*th in a new module under large ΔT_j. (b) Normalized *R*th in aged module under narrow ΔT_j. (c) ΔT_j in aged module.

TABLE I
*R*TH AVERAGE INCREASE RATE UNDER DIFFERENT CONDITIONS

Test Conditions and *R*th Increase Rate *K* (per 10 000 cycles)					
$\Delta T_j = 40.7$ °C	29%	$\Delta T_j = 41$ °C			
$T_{\rm jm} = 74$ °C		$T_{\rm jm} = 60.5$ °C	8%	*	*
$R_{\rm th} = 1.41R_{\rm th0}$		$R_{\rm th} = 1.78R_{\rm th0}$			
$\Delta T_j = 40$ °C	11.7%	$\Delta T_j = 32.5$ °C	5.44%	*	*
$T_{\rm jm} = 74$ °C		$T_{\rm jm} = 55.8$ °C			
$R_{\rm th} = 1.18R_{\rm th0}$		$R_{\rm th} = 1.40R_{\rm th0}$			
$\Delta T_j = 40$°C	8.95%	$\Delta T_j = 28$°C		$\Delta T_j = 34$°C	
$T_{\rm jm} = 74$ °C		$T_{\rm jm} = 54$ °C	1.91%	$T_{\rm jm} = 58$ °C	7.03%
$R_{\rm th} = 1.06R_{\rm th0}$		$R_{\rm th} = 1.20R_{\rm th0}$		$R_{\rm th} = 1.24R_{\rm th0}$	

∗Test results unavailable.

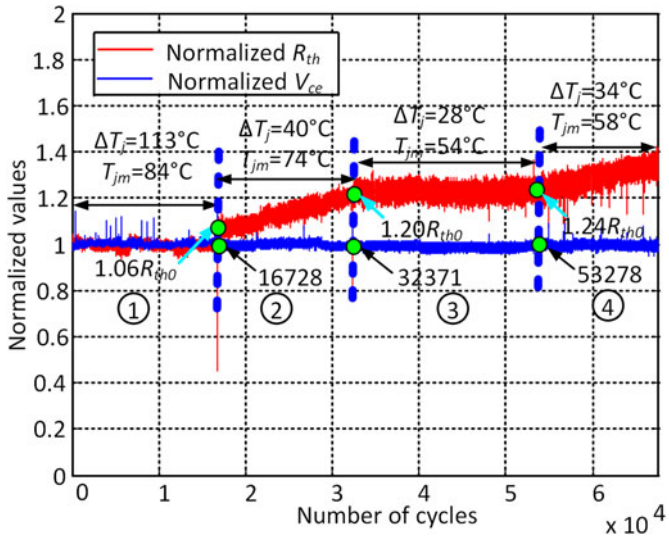

Fig. 12. Results of power cycling test under narrow ΔT_j.

present status of health. The results for two modules of the same type are shown in Fig. 13. The *R*th curve of module 1 reaches 17% increase before module 2 because their stress levels are different. Once their *R*th increase reached this level, the stress applied to them is reduced and set to the same for both modules ($\Delta T_j = 40$ °C and $T_{\rm jm} = 74$ °C). The further progression of ageing is apparently the same. For further stress cycles of $\Delta T_j = 40$ °C and $T_{\rm jm} = 74$ °C, the rate of *R*th increase is 7.19% every 10 000 cycles for Module 1 and 7.14% every 10 000 cycles for Module 2. This also indicates that not only the effect of the narrow ΔT_j stress cycles should be considered in the second stage of ageing but also the effect depends on the current health condition of the power module.

Next, other two new power modules are tested under different fatigue loading sequences. The results are shown in Fig. 14 and Table II. First, in the test both modules are brought to $R_{\rm th} = 1.17R_{\rm th0}$ with large ΔT_j stress cycles. Then, the test conditions in stage ② are changed to ($\Delta T_j = 40$ °C, $T_{\rm jm} = 74$ °C) for module 1 and ($\Delta T_j = 32.8$ °C, $T_{\rm jm} = 56$ °C) for module 2. After that the conditions are changed over between the two modules in stage ③. The results show that at the end of the process module 1 is degraded more than module 2, implying that once the junction-to-case thermal resistance *R*th has started

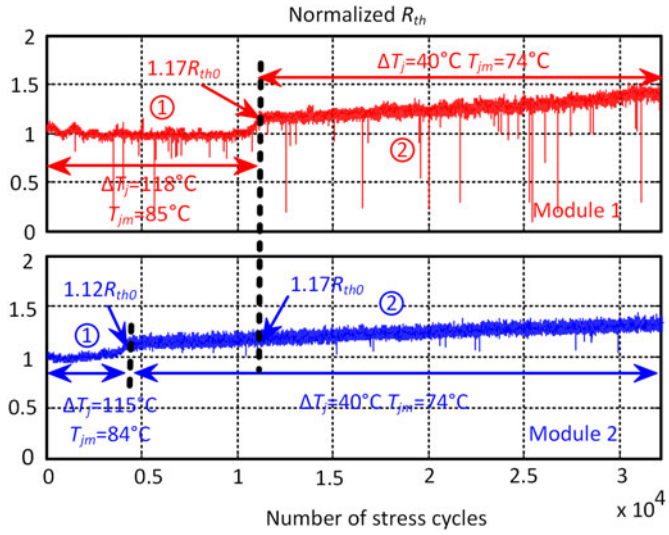

Fig. 13. Comparing the thermal resistance from two tests.

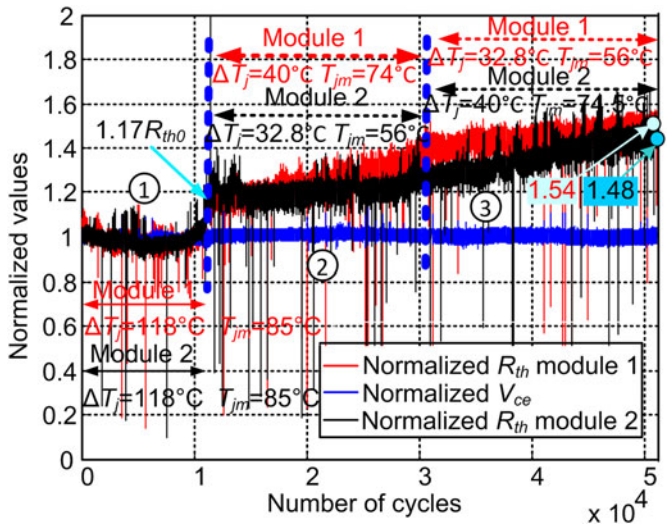

Fig. 14. Results of power cycling test under two test conditions.

TABLE II
*R*TH AVERAGE INCREASE RATE UNDER DIFFERENT CONDITIONS OF TWO MODULES.

	Stage ①			Stage ②		Stage ③	
Module number	Test Conditions and *R*th Increase Rate *K* (per 10 000 Cycles)						
Module 1	$\Delta T_j = 118$ °C $T_{\rm jm} = 85$ °C	$\Delta T_j = 40$ °C $T_{\rm jm} = 74$ °C	11.7%	$\Delta T_j = 32.8$°C $T_{\rm jm} = 56$ °C	5.44%		
Module 2	$\Delta T_j = 118$ °C $T_{\rm jm} = 85$ °C	$\Delta T_j = 32.8$ °C $T_{\rm jm} = 56$ °C	3.54%	$\Delta T_j = 40$ °C $T_{\rm jm} = 74.5$ °C	12.4%		

to increase; the further increase follows a nonlinear relationship with the health status of the module. The ageing process generally develops progressively faster and the sequence for different stress cycles to occur would affect the ageing consequence.

V. DISCUSSION AND CONCLUSION

A lifetime model is traditionally extracted from accelerated ageing tests under intensified stress conditions; the results are then extrapolated to the normal operation region of lesser stresses. More recent power module designs with improved reliability can only be tested in highly intensified stress conditions with, e.g., $\Delta T_j \geq 80$ °C, which can introduce considerable uncertainty in the extrapolation procedures. Linear accumulation is usually used to calculate the damage for a load profile. This lacks of experiment proof for power modules and has become questionable.

This study demonstrates the effect of narrow temperature excursions during power cycling on the IGBT module reliability from 28 to 40 °C. The effects of the narrow ΔT_j stress cycles on aged modules are only tested above 28 °C, and the initial cracks are established using large ΔT_j stress cycles. It has not been verified whether or not the small ΔT_j stress cycles themselves would eventually cause any cracks; if they would, it would take many cycles. The key step of this study is to quantify the ageing status of the power module through the measurement of its internal thermal resistance. This is then extended to investigate the dependence of the ageing process on the nature of the stress cycles and the present health condition. This is the first time to confirm the effects of narrow ΔT_j stress cycles, which can be significant on aged modules. In the next stage of work, an improved lifetime model will be attempted, including the effects of the narrow ΔT_j stress cycles and the dependence on key variables.

In conclusion, this study provides a new perspective, which indicates that fatigue life is not only related to the magnitudes of an extended range of temperature stress cycles but also dependent on the module health condition itself. A series of experiments are carried out to show the limitations of traditional thinking about the ageing process. The study also implies that the traditional stress life (*S–N*) curve should be improved to accurately predict the fatigue life in real complex loading conditions. The study shows that while the degradation rate of thermal resistance is affected by the current health condition and further stress levels, the history of the ageing process to reach the present status is apparently irrelevant. The study has shown that bond wire failure has not happened in all the tests, confirming the knowledge that this mechanism usually occurs when the die-attach solder layer is already in deep degradation and the junction temperature is very high. It is hoped that the study would help design engineers in developing converter systems that are expected to operate reliably over a long period of time subject to a large number of minor stress cycles. The study could also be usefully fed into the development of operational management techniques such as condition monitoring and prognosis.

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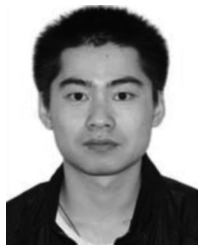

Wei Lai received the M.Sc. degree from Chongqing University of Technology, Chongqing, China, in 2012. He is currently working toward the Ph.D. degree in electrical engineering from the School of Electrical Engineering, Chongqing University, Chongqing.

He was a joint Ph.D. student funded by the China Scholarship Council at the University of Warwick, Coventry, U.K., from September 2013 to May 2015. His current research interests include the reliability of power modules, the application of power electronics for electric power generation, and the development of condition monitoring methods for power electronic converters.

Minyou Chen (M'05–SM'14) received the M.Sc. degree in control theory and engineering from Chongqing University, Chongqing, China, in 1987, and the Ph.D. degree in control engineering from the University of Sheffield, Sheffield, U.K., in 1998.

He is currently a Full Professor at Chongqing University. He is the author or coauthor of more than 180 papers. His current research interests include intelligent modeling and control, reliability of power modules, microgrid control, and state monitoring in power distribution systems.

Li Ran (M'98–SM'07) received the Ph.D. degree in power systems engineering from Chongqing University, Chongqing, China, in 1989.

He was a Research Associate with the Universities of Aberdeen, Nottingham and Heriot-Watt, at Aberdeen, Nottingham, and Edinburgh in the U.K., respectively. He became a Lecturer in Power Electronics with Northumbria University, Newcastle upon Tyne, U.K., in 1999, and was seconded to Alstom Power Conversion, Kidsgrove, U.K., in 2001. Between 2003 and 2012, he was with Durham University, U.K.. He joined the University of Warwick, Coventry, U.K., as a Professor in Power Electronics - Systems in 2012. His current research interests include the application of power electronics for electric power generation, delivery, and utilization.

Shengyou Xu received the Ph.D. degree in electrical engineering from Chongqing University, Chongqing, China, in 2013.

He was a Visiting Scholar at Durham University, Durham, U.K., in 2010. He is currently a Lecturer of Electrical Engineering at the School of Electrical Engineering, Chongqing University. His current research interests include the control of power system and the reliability of power module used in renewable energy systems.

Nan Jiang is currently working toward the M.Sc. degree in electrical engineering from Chongqing University, China.

She is currently involved in working on reliability of power electronic modules with a special interest in failure mechanisms of solder layer in IGBT modules based on FEM.

Xuemei Wang (M'12) received the M.Sc. degree in control engineering from the Central South University, Changsha, China, in 2004, and the Ph.D. degree in power electronics and power drives from South China University of Technology, Guangzhou, China, in 2009.

Her current research interests include multiphysics modeling of power semiconductor device, reliability of power modules, and nonlinear behavior of power converters.

Olayiwola Alatise (M'05) received the B.Eng. degree (with first-class honors) in electronic engineering from Newcastle University, in 2005, and the Ph.D. degree in microelectronics and semiconductors from Newcastle University, Newcastle upon Tyne, U.K., in 2008.

He was involved in studying mixed-signal performance enhancements in strained Si/SiGe metal–oxide–semiconductor field-effect transistors (MOSFETs). In June 2008, he joined the Innovation R&D Department, NXP Semiconductors, as a Development Engineer, where he designed, processed, and qualified discrete power trench MOSFETs for automotive applications and switched-mode power supplies. In November 2010, he became a Science City Research Fellow with the University of Warwick, Coventry, U.K., where since August 2012, he has been an Associate Professor of Electrical Engineering. His current research interests include investigating advanced power semiconductor materials and devices for improved energy conversion efficiency.

Philip Mawby (S'85–M'86–SM'01) received the B.Sc. and Ph.D. degrees in electronic and electrical engineering from the University of Leeds, Leeds, U.K., in 1983 and 1987, respectively.

His Ph.D. was focused on GaAs/AlGaAs heterojunction bipolar transistors for high-power radio frequency applications at the GEC Hirst Research Centre, Wembley, U.K. In 2005, he joined the University of Warwick, Coventry, U.K., as the Chair of Power Electronics. He was also with the University of Wales, Swansea, U.K., for 19 years and held the Royal Academy of Engineering Chair for power electronics, where he established the Power Electronics Design Center. He has been internationally recognized in the area of power electronics and power device research. He was also involved in the development of device simulation algorithms, as well as optoelectronic and quantum-based device structures. He has authored or coauthored more than 100 journal and conference papers. His current research interests include materials for new power devices and modeling of power devices and circuits.

Prof. Mawby has been involved in many international conference committees, including the ISPSD, EPE, and the ESSDERC. He is a Chartered Engineer, a Fellow of the IET, and a Fellow of the Institute Physics. He is a Distinguished Lecturer for the IEEE Electron Devices Society.