Dynamic Electrothermal Model of Paralleled IGBT Modules With Unbalanced Stray Parameters

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***Abstract*—Compared with single-module applications, unbalanced stray parameters come about frequently in the process of installing paralleled IGBT modules, which could result in some distinctions of current sharing and temperature distributions. To focusing on depicting this practical issue, a novel dynamic electrothermal model extended to paralleled systems is proposed in this paper to establish a comprehensive transient model to characterize the relations of power losses, junction temperature, and unbalanced parasitic elements. The model can describe the interactions of current distributions and thermal dissipations between paralleled modules. In addition, the variation of unbalanced temperature during transient process can be obtained with the proposed electrothermal model. First, the stray inductance parameters in the paralleled branches are analyzed in detail by finite-element-method simulation tool. And based on impedance analysis, an improved power loss model is built up, considering the interaction of paralleled devices. Moreover, by the method of resistor–capacitor networks extracted from numerical simulations of 3-D structural model, the transient thermal impedance of devices and cooling system is obtained for fast and accurate electrothermal cosimulation of the paralleled system. Experimental results are carried out to verify the proposed model and coincide with the theoretical analysis.**

***Index Terms*—Electrothermal model, insulated-gate-bipolar-transistor (IGBT) module, paralleled, stray parameters.**

I. Introduction

DURING the past decades, power semiconductor devices especially insulated-gate-bipolar-transistor (IGBT) power modules have found an important application in industry due to the excellent performance in high power converters. In order to scale up the current carrying capacity of power converters, the modules are commonly applied in paralleled connection when considering the cost and complexity of the power systems. One main issue about paralleled devices is how to obtain the best current sharing performance. However, there are always some unequal stray elements existing in the paralleled branches when mounting the devices because of some system restrictions. Since the operation performance of parallel power devices are strongly dependent on their junction temperatures and the parasitic parameters in the circuits [1]–[4], it is necessary to build the electrothermal model for paralleled modules to develop more reliable power converters and satisfy the power demands.

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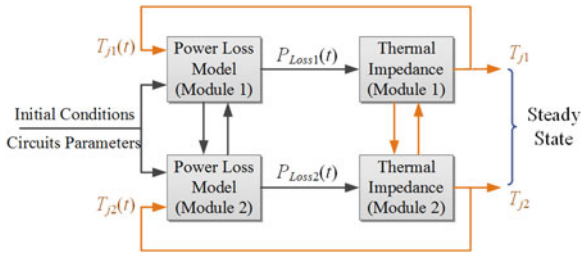


Fig. 1. Proposed electrothermal feedback networks for paralleled modules.

As illustrated in Fig. 1, the model structure of the paralleled system consists of feedback networks of interactional power loss models and thermal impedance. With initial conditions of the power circuits, the dissipations of each module P_{Loss1} and P_{Loss2} can be derived under certain junction temperature T_{j1} and T_{j2}. Then, the calculated losses are delivered to thermal models to calculate junction temperatures. After enough iterations of the transient flow, the steady-state junction temperatures can be obtained. Since most presented electrothermal models [5]–[10] are suitable for single module but do not consider the coaction of paralleled devices, an improved model specialized for paralleled IGBT modules should be proposed for system design. The circuit simulation tools like SABER or SPICE are widely employed to calculate the losses by simulating current and voltage waveforms based on physical models [11]–[13] or behavioral models [14]–[16]. For physical models, although simulation results match experimental data very well, accurate physical parameters extracted from the devices are difficult to be obtained and massive data are needed to be processed. The simulation speed of behavioral models is much faster, but it is hard to guarantee the calculation accuracy in variable operation situations without considering their physical mechanisms. Thus, based on equivalent circuits derived from physics, analytical models were proposed and proved to be fast, accurate, and suitable for data processing and loss calculations [17]–[20]. Temperature-dependent parameters can be acquired by typical measurements and diagrams from datasheet. Nevertheless, there are few papers that introduced this method into the analysis of paralleled modules. Therefore, in this paper, an improved analytical model of the power losses for paralleled modules is carried out to cooperate with thermal models. In addition to considering the variety of junction temperatures and stray parameters, the current distributions based on impedance analysis is included in the proposed loss models.

It is necessary to create a 3-D structural model of paralleled IGBT modules because the power dissipations generated

from the silicon chips diffuse to the cooling system in three dimensions. In [21] and [22], the authors proposed several solutions to the heat diffusion equations by employing mathematical methods. However, solving complexity is increasing when considering the sophisticated geometrical shape of the cooling systems. With increased operation speed of computers, the temperature distribution can be calculated by the finite-element method (FEM) [23]–[25], which is employed in commercial simulation tool, like ANSYS. However, it is difficult to cosimulate the thermal models with circuit simulation tools. For that reason, the models of thermal *RC* networks [23]–[26], which can be derived from FEM calculation results, are widely implemented because the thermal properties of the systems can be integrated into circuit simulation tools. Nevertheless, little attention has been paid to the analysis of temperature distributions in the paralleled modules on the same heat sink since the relative position of devices will affect the thermal coupling of the modules. In this paper, some efforts have been made to analyze the coupling in the thermal models with an innovative *RC* network.

Unlike single-module electrothermal model [5]–[10], unbalanced problems will arise significantly in paralleled modules since unbalanced stray parameters can induce current distribution problems significantly. Furthermore, unbalanced junction temperature will emerge during the transient process. However, there are fewer literatures focusing on depicting this practical issue. In this study, the electrothermal model is extended to paralleled systems, providing a comprehensive transient model to characterize the relations between unbalanced junction temperature and unbalanced stray inductance in practical installations. This is derived with the help of a detailed parallel-device model extended from single-device models and an improved thermal model by considering the thermal coupling between modules.

This paper is organized as follows. First, power circuits and stray parameters in the power circuits are analyzed in Section II. Then, an improved power loss models suitable for paralleled modules are described in Section III. Subsequently, a novel *RC* network of paralleled modules is proposed and the parameters extracted from the FEM simulation tool are presented in Section IV. Then, the electrothermal model of the total systems are established and verified by some experimental results in the Section V. The summarization is given in the final section.

II. Analysis of Stray Parameters

First, the parasitic elements in the system were calculated by establishing the physical models in the FEM software. It should be noted that stray inductance in the power circuits is the reason that causes voltage spikes at turn-off period and increases switching losses especially in high switching frequency and large power ratings. Consequently, the selected device ratings are higher to avoid failures, which means more cost of the whole systems. As shown in Fig. 2, a popular buck converter is selected as a study case in this study, which is widely applied in energy storage systems. The IGBTs below are in parallel to perform as a diode with zero driving voltages. Table I shows the basic parameters and components of the circuit. Usually,

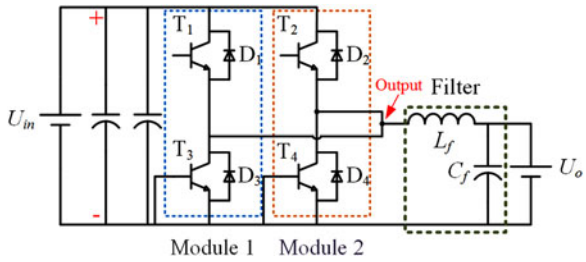


Fig. 2. Schematic diagram of buck converter with paralleled IGBT modules.

TABLE I
Parameters and Components of the Converter

Parameters	Symbols	Values
Input voltage	$U_{\rm in}$	250 V
Output voltage	U_o	150 V
Output current	I_o	30 A
Switching frequency	f_s	40 kHz
Filter inductor	L_f	150 μH
Filter capacitor	C_f	300 μF

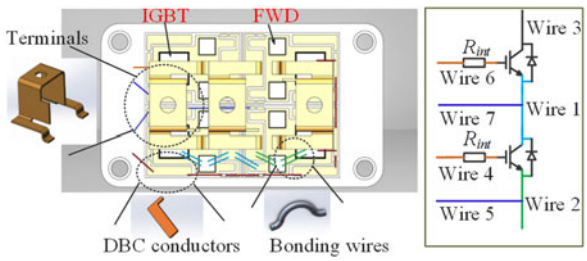


Fig. 3. Internal structure of an IGBT module (FF300R12KT4) and the equivalent connection schematic of this module.

the stray inductance is composed of two types: the internal part mainly distributed inside IGBT modules including in the terminals, bonding wires, and copper traces; the external stray inductance parasitizing connecting wires and bus bars in the power circuits. In order to model the parallel systems precisely, the stray inductance is calculated by the FEM tools first as follows.

In this study, a commercial half-bridge IGBT module FF300R12KT4 is employed and the packaging layout of this module is illustrated as the left picture of Fig. 3. There are four IGBT chips and eight free-wheeling diode (FWD) chips on the DBC substrate, which are connected by copper traces and terminals to external circuits. Each bonding wire that connects copper traces is in parallel connection to achieve high power capability and low stray inductance. Accordingly, the schematic diagram of this IGBT module is derived to simplify the model as shown in the right picture of Fig. 3. In order to obtain the values of stray inductance, some efforts have been made based on FEM tools [27] or some equations deriving from the electromagnetic theory [28], [29]. In this study, an FEM simulation tool ANSYS is applied for the stray parameters estimation since this method performs high calculation accuracy especially for complicated

TABLE II
STRAY INDUCTANCE OF INTERNAL MODULES AND EXTERNAL CONNECTION

Stray Inductance of Internal Modules			
Wire Number	Values(nH)	Wire Number	Values(nH)
1	3.57	5	16.3
2	14.7	6	11.9
3	10.8	7	15.9
4	29.5	-	-
Stray Inductance of External Modules			
Collector (bus bars)	15.0	Collector (wire:15 cm)	58.2
Emitter		17.2	
Gate		35.4	

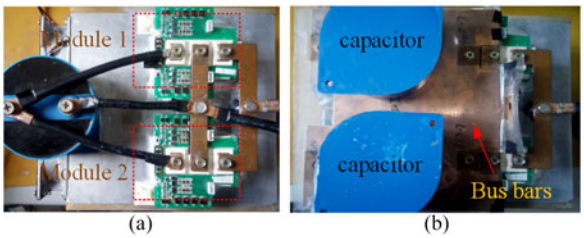


Fig. 4. Pictures of the paralleled system with (a) cylindrical wires or (b) bus bars connections.

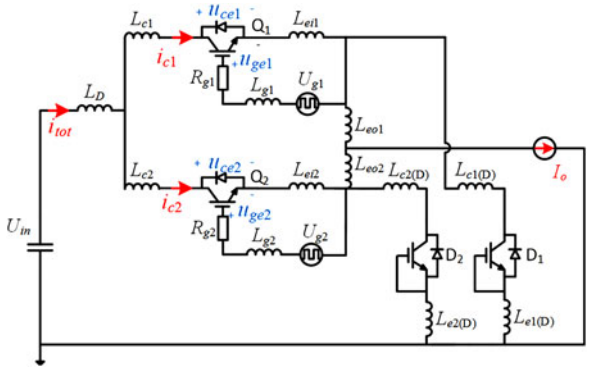


Fig. 5. Schematic diagram of buck converter with stray inductance in the top paralleled devices.

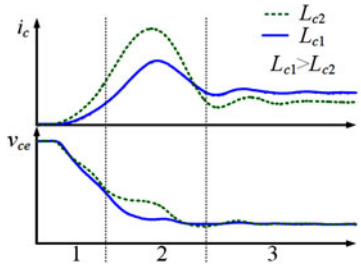


Fig. 6. Typical turn-on waveforms of paralleled modules with unbalanced stray inductance in the top paralleled devices.

structures. The frequency of the current source applied on the components is set as 1 MHz, which is associated with the duration of switching phases. Table II gives the calculation results of stray inductance in each equivalent wire in Fig. 3. The results indicate that the stray inductance in power circuits takes smaller part of the internal inductance when compared with that parasitizing the driving circuits.

The other partial stray inductance in the commutation circuits mainly exists in the outside connecting wires. There are two main alternative connecting ways: cylindrical wires or planar bus bars as shown in Fig. 4. The structure of the designed bus bars is built by two paralleled conducting plates, which are separated by a thin insulating layer made of PET material. As discussed in [30], a lumped parameter model can be employed to analyze the stray characteristic since the wavelength is far larger than the dimension of the bus bars. In addition, the diameter of the copper wires is selected as 1.2 cm to bear the designed current stress. In order to compare the stray inductance of cylindrical wires and bus bars, a 3-D FEM analysis is carried on to estimate the stray inductance individually. As shown in Table II, the results indicate that the structure of bus bars processes lower stray inductance than the copper wires, which is the reason why bus bars are widely employed in high power converters. However, in this study, the cylindrical wires are employed when considering the feasibility of measurements by current probes. After simulating the stray parameters in the circuits, a novel power loss model for parallel modules is presented in the following section.

III. PROPOSED ANALYTICAL LOSS MODEL FOR PARALLELED MODULES WITH UNBALANCED STRAY INDUCTANCE

A proposed analytical loss model, which is suitable for paralleled modules, is described detailedly in this section. Compared with single-module loss model, the interactions of paralleled modules, especially the distinction of current distributions, are emphasized when considering the diversity of stray inductance and junction temperature. The current sharing is analyzed based on the impedance of each branch in different source frequencies.

Based on the analysis of stray inductance in Section II, a detailed schematic diagram of the buck converter is shown in Fig. 5. The collector inductance L_c is equal to the summed inductance of internal Wire 3 and external inductance in the wire connecting collector and power supply. The gate inductance L_g can be obtained by adding the internal inductance on Wire 6 and Wire 7 to the external stray inductance in the driving circuit, and the internal emitter inductance $L_{\rm ei}$ is equal to partial inductance in Wire 1 and $L_{\rm eo}$ is the outside emitter inductance in the wire connecting emitter and the filter inductor. The letter "D" in parenthesis means the inductance in the paralleled FWDs. In respect that there is a filter inductor with high inductance value, the stray inductance in the filter loop has little influence on the transient mutation of switching waveforms. Thus, only the stray inductance in the emitter, collector, gate, and the switching loop is considered as depicted in the schematic diagram. Fig. 6 shows typical turn-on waveforms of the paralleled modules with unbalanced stray inductance in the collector. As studied in [16], the total losses of single module are usually classified

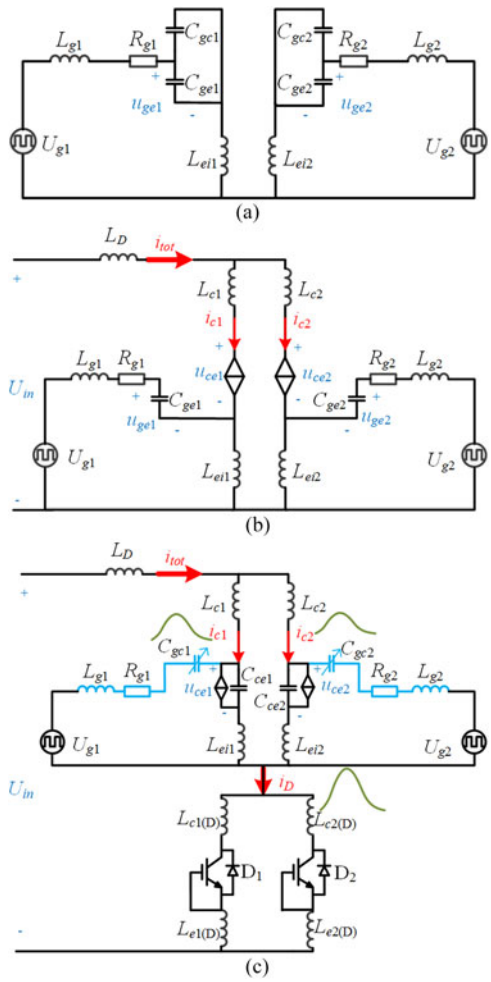


Fig. 7. Equivalent circuits of analytical models. (a) Equivalent circuit before $u_{\rm ge}$ reaches $U_{\rm th}$. (b) Equivalent circuit for stage 1. (c) Equivalent circuit for stage 2.

into switching losses, conduction losses, and blocking losses of IGBTs and FWDs. The blocking losses are not discussed in this paper since these partial losses account for a small proportion of the total power losses. The following is the detailed analysis of the power losses in paralleled modules.

A. Turn-On Switching Process

According to the mutations of collector current and collector–emitter voltage, the switching process is divided into three equivalent circuits as depicted in Fig. 7. As illustrated in Fig. 7(a), when a positive gate supply voltage is applied on the driving circuit, the collector current i_c keeps close to zero and the collector–emitter voltage $u_{\rm ce}$ remains the input voltage $U_{\rm in}$ before the gate–emitter voltage $u_{\rm ge}$ rises to the threshold voltage $U_{\rm th}$ since the internal MOS channel has not taken shape. After that, as demonstrated in Fig. 7(b), the collector current begins to increase toward the conduction current as the internal MOS channel starts to form and the electron current has an access to flow into the drift region. Meanwhile, the current of the paralleled FWDs falls to the turn-off state due to the constant load current at this short period. Moreover, $u_{\rm ce}$ turns to decrease because the sharp rise of the collector current results in an induced voltage across the stray inductance, which can be calculated by

$$u_{\rm ce1} = U_{\rm in} - L_D\frac{di_{\rm tot}}{dt} - (L_{c1}+L_{\rm ei1})\frac{di_{c1}}{dt} \quad (1)$$

$$u_{\rm ce2} = U_{\rm in} - L_D\frac{di_{\rm tot}}{dt} - (L_{c2}+L_{\rm ei2})\frac{di_{c2}}{dt} \quad (2)$$

where $u_{\rm ce1}$ and $u_{\rm ce2}$ are the collector–emitter voltage of Module 1 and Module 2, $U_{\rm in}$ is the input voltage, $i_{\rm tot}$ is the total current of paralleled modules, L_D is the total stray inductance in the input bus wires, L_{c1}, L_{c2} are the stray inductance in collector, $L_{\rm ei1}, L_{\rm ei2}$ are the stray inductance in internal emitter and i_{c1}, i_{c2} are the collector currents.

Since $u_{\rm ce}$ remains a high level, IGBT modules operate in the active region. The relation of i_c and $u_{\rm ge}$ can be defined as the following expressions [17]:

$$i_c = \frac{K_p}{2}(u_{\rm ge}-U_{\rm th})^2 \quad (3)$$

$$\frac{di_c}{dt} = K_p(u_{\rm ge}-U_{\rm th})\frac{du_{\rm ge}}{dt} = g_m\frac{du_{\rm ge}}{dt} \quad (4)$$

where K_p is the internal MOS channel conductance, $U_{\rm th}$ is the threshold voltage of the device and g_m is the transconductance, which can be derived from the transfer characteristic I_c–$U_{\rm ge}$ curves, which was tested by the Curve Tracer TEK 371A and a heating platform. These temperature-dependence parameters K_p, g_m affect the slope of di_c/dt at turn-on stage as investigated in [31].

Since the "Miller plateau" has not been formed in this period, the equivalent circuit can be simplified as Fig. 7(b). According to the Kirchhoff's voltage laws, the voltage $u_{\rm ge}$ can be expressed as

$$U_g = R_gC_{\rm ge}\frac{du_{\rm ge}}{dt} + L_gC_{\rm ge}\frac{d^2u_{\rm ge}}{dt^2} + u_{\rm ge} + L_e\frac{di_c}{dt} \quad (5)$$

where U_g is the positive value of the driving voltage, R_g is the driving resistor, L_g is the parasitic inductance in the driving circuit, and $C_{\rm ge}$ is the gate–emitter capacitor.

Assuming that

$$a = L_gC_{\rm ge} \quad (6)$$

$$b = R_gC_{\rm ge} + L_{\rm ei}g_m. \quad (7)$$

The voltage can be derived in two different expressions [18] by comparing the values of b^2 and $4a$ as the followings:

$$u_{\rm ge} = U_g - (U_g-U_{\rm th})e^{-\frac{b}{2a}t}\left(\cos\left(\sqrt{\frac{1}{a}-\left(\frac{b}{2a}\right)^2}\,t\right) + \frac{1}{\frac{2a}{b}\sqrt{\frac{1}{a}-(\frac{b}{2a})^2}}\sin\left(\sqrt{\frac{1}{a}-\left(\frac{b}{2a}\right)^2}\,t\right)\right)$$

when $b^2 < 4a$

$$u_{\rm ge} = U_g - (U_g-U_{\rm th})$$

$$\frac{\frac{2a}{b-\sqrt{b^2-4a}}e^{-\frac{t}{\frac{2a}{b-\sqrt{b^2-4a}}}}-\frac{2a}{b+\sqrt{b^2-4a}}e^{-\frac{t}{\frac{2a}{b+\sqrt{b^2-4a}}}}}{\frac{2a}{b-\sqrt{b^2-4a}}-\frac{2a}{b+\sqrt{b^2-4a}}}$$

when $b^2 > 4a$. (8)

In the study, $b^2>4a$ prevails and the secondary equation in (8) is used commonly in the model calculations. For paralleled IGBT modules, the stray inductance in emitter affects the slope of current increasing by changing the slope of the voltage $u_{\rm ge}$. Also, the junction temperature has an impact on the current change rating as K_p varies with temperature. The collector current of paralleled modules can be derived by substituting (8) into (3).

After the total current of each IGBT module excesses the output current, the FWDs (D1 and D2) begin to turn to the reverse recovery stage. As investigated in [32], the reverse recovery current is related to several parameters: the conduction current, the current slope, and junction temperatures, which can be modeled as presented in [33]. The detailed model of the reverse recovery current can be found in the previous work [34]. The recovery current of paralleled diodes merge to the connecting point, and then, is divided to the paralleled IGBTs according to the impedance of each branch. For the purpose of calculating current spikes in each IGBT, the angular frequency of this period should be calculated first as

$$\omega_p = 2\pi f_p = \frac{\pi}{t_{rr}} \tag{9}$$

where ω_p, f_p is the angular frequency and frequency of the collector current in this stage, $t_{\rm rr}$ is the duration of the reverse recovery current of FWDs.

As a consequence, the collector current of each IGBT can be calculated as

$$i_{c1} = i_D \cdot \frac{Z_2(\omega_p)}{Z_1(\omega_p)+Z_2(\omega_p)} + I_{c1} \tag{10}$$

$$i_{c2} = i_D \cdot \frac{Z_1(\omega_p)}{Z_1(\omega_p)+Z_2(\omega_p)} + I_{c2} \tag{11}$$

where $Z_1(\omega_p)$ and $Z_2(\omega_p)$ are the impedance of Module 1 branch composed of $L_{c1}, C_{\rm ce1}, L_{\rm ei1}, C_{\rm ge1}, R_{g1}$, and L_{g1} and Module 2 branch composed of $L_{c2}, C_{\rm ce2}, L_{\rm ei2}, C_{\rm ge2}, R_{g2}$, and L_{g2}, i_D is the total reverse recovery current, and I_{c1}, I_{c2} are the steady current for each branch. The values of the impedance from collector to emitter are estimated by calculated results of stray inductance and measured capacitors. As the voltage-controlled current in Fig. 7(c) is controlled by $u_{\rm ge}$ and $u_{\rm ge}$ changes little during the "Miller plateau," the current source can be treated as an open circuit when we analyzed the impedance of each branch. Meantime, the voltage $u_{\rm ce}$ drops to the saturating voltage rapidly because the Miller capacitance $C_{\rm gc}$ provides a path to decrease the voltage as explained in Fig. 7(c), which can be expressed as

$$\frac{du_{\rm ce}}{dt} = \frac{i_g}{C_{\rm gc}} = \frac{U_g - U_{pl}}{R_g C_{\rm gc}} \tag{12}$$

where U_{pl} is the value of the voltage $u_{\rm ge}$ at this period, i_g is the current through the driving circuit and $C_{\rm gc}$ is the gate–collector capacitor in this stage. Although the capacitance $C_{\rm gc}$ decreases nonlinearly with a function of the collector–emitter voltage during this period, a two-step function of the collector–emitter voltage can be implemented to simplify the calculation [19]. According to the test results by a 590 CV analyzer, $C_{\rm gc}$ is estimated as 1.6 nF when the voltage is higher than 4 V, otherwise the value is 4 nF.

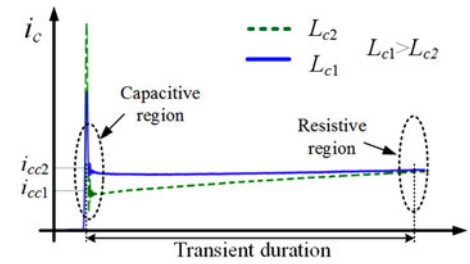


Fig. 8. Typical on-state current waveforms of paralleled modules with unbalanced stray inductance in the top paralleled devices.

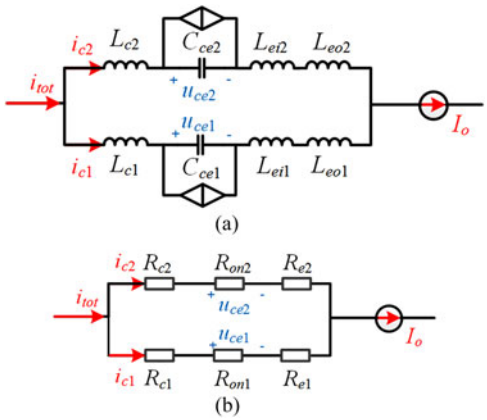


Fig. 9. (a) Equivalent circuit for the capacitive region. (b) Equivalent circuit for the end of the resistive region.

B. Conduction Process

As shown in Fig. 8, in the conduction process, there is a transient duration from reverse recovery to the resistive region where the collector current is in proportion to collector–emitter voltage. Since the current source is in high frequency at the start of the transient process, the stray resistors in emitter and collector have little influence on the current distribution. The impedance of each branch is different from that in stage 2 because $C_{\rm gc}$ becomes smaller in this region after "Miller plateau." In stage 2, the impedance of paralleled modules performs inductive, which means the branch with larger stray inductance will share less reverse recovery current. However, since the impedance shows capacitive when the capacitance $C_{\rm gc}$ decreases to a small value in Stage 3, the current sharing behaves the reverse pattern in this period. As depicted in Fig. 9(a), the current sharing can be expressed as

$$i_{\rm cc1} = I_o \cdot \frac{Z_{\rm on2}(\omega_p)}{Z_{\rm on1}(\omega_p)+Z_{\rm on2}(\omega_p)} \tag{13}$$

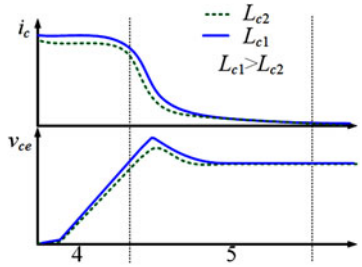


Fig. 10. Typical turn OFF waveforms of paralleled modules with unbalanced stray inductance in the power loop.

$$i_{\mathrm{cc2}} = I_o \cdot \frac{Z_{\mathrm{on1}}(\omega_p)}{Z_{\mathrm{on1}}(\omega_p) + Z_{\mathrm{on2}}(\omega_p)} \tag{14}$$

where i_{cc1} and i_{cc2} are the collector current in the paralleled modules in capacitive region, $Z_{\mathrm{on1}}(\omega_p)$ and $Z_{\mathrm{on2}}(\omega_p)$ are the corresponding impedance of paralleled modules at the start of transient duration. Since the capacitor C_{gc} becomes much smaller when compared with C_{ce}, it has little influence on the current sharing in this period. In contrast to the current sharing behaviors in stage 2, the branch with higher stray inductance performs less capacitive, which results in more current sharing.

In Fig. 8, the transient duration is the transient process between the capacitive region and the resistive region. During the transient duration, the branch impedance varies from capacitive to resistive, which results in the difference of the voltage drops on the stray inductance becomes smaller gradually. At the end of the transient duration, the slope of the current source is equal to the change rate of the current through the filter inductor, which leads to the branch impedance closed to be resistive as illustrated in Fig. 9(b). The current distribution is depended on the stray resistor R_{e1} in emitter, R_{c1} in collector and the on-state resistor R_{on}, which was derived from the output characteristic I_c–U_{ce} curves tested by the Curve Tracer TEK 371A and a heating platform. According to measurement results, R_{e1} and R_{c1} is about 50 $\mu\Omega$, which is smaller than R_{on} (3.4 mΩ at 20 °C). Therefore, the current diversity is inapparent in the resistive region when compared with that in the capacitive region. Although the impedance is resistive at the end of the transient duration, the current difference in capacitive region leads to a transient current sharing to resistive region.

C. Turn-Off Switching Process

The turn-off switching period can be divided into two different stages according to the voltage mutations as pictured in Fig. 10. First, the collector–emitter voltage u_{ce} rises up to the supply voltage because the gate pulse ceases and declines to the threshold voltage. Since the FWDs have not been turned on in this period, the collector current cannot be transferred from IGBTs to FWDs. The main factors that affect the slope du_{ce}/dt are the junction temperature and steady-state collector current at fixed supply voltage U_{DC} and driving circuits [35]. The expression for the slope is presented as

$$\frac{du_{\mathrm{ce}}}{dt} = \frac{1}{R_g C_{\mathrm{gc}}} \left(\frac{U_g - U_{\mathrm{off}}}{1 + (C_o / g_m R_g C_{\mathrm{gc}})} \right) \tag{15}$$

where U_{off} is the negative value of the driving voltage and C_o is the charge extraction capacitance as derived in [35]. It should be noted that du_{ce}/dt decreases with the increase of temperature and slightly rises when the collector current becomes larger, but is not influenced by the stray inductance in this stage as discussed in [35].

The FWDs turn ON after u_{ce} reaches the blocking voltage. Accordingly, the collector current declines dramatically to the tail current based on the theory in [36] and can be calculated by (3)–(8) as the analysis of Stage 1 during turn-on process. This rapid current change will induce a high voltage spike across the stray inductance, which can be depicted by (1) and (2). When the internal MOS turns OFF, the collector current turns into the tail current. Under high lifetime situation, this current can be expressed as follows [13]:

$$i_c = I_{\mathrm{tail}} \cdot e^{\left(-\frac{(1-\alpha_{p-n-p})t}{\tau_{\mathrm{tail}}}\right)} \tag{16}$$

where I_{tail} is the collector current at the start of the tailed stage, α_{p-n-p} is the common-base current gain of the transistor in the equivalent and τ_{tail} is the carrier transit time. The value of α_{p-n-p} and τ_{tail} can be obtained by fitting the test current waveforms.

The loss model of single module is investigated in previous work [34]. The temperature-dependent parameters have been tested by a heating platform and the transient waveforms are demonstrated and compared with measured results in [34]. In view of impedance analysis, the proposed analytical model can be employed to calculate losses in different stages for paralleled models under different stray inductance. The junction temperature should be known previously to determine parameter values. However, losses contribute to the temperature varying. Therefore, thermal models were established to obtain the junction temperature with certain power losses as the following section shows.

IV. Proposed Thermal Impedance Calculation Method for Paralleled Modules

In this section, a novel thermal model, including the interaction of paralleled modules, which are mounted on the same heat sink, is built to derive the relations between power losses and junction temperatures. The FEM simulation tool is used to obtain the thermal impedance of the proposed model. Furthermore, we analyzed the influence on thermal flow with different distances between mounted modules to give a more precise thermal model.

The lumped *RC* networks, which can be extracted from thermal dynamic curves, are widely utilized to analyze thermal characteristic since it is easy to be integrated into circuit simulation tools, such as SABER or MATLAB. In practical applications, IGBT modules are always mounted on a heat sink to keep the junction temperatures lower than the limiting temperature. According to the power dissipations of the devices in

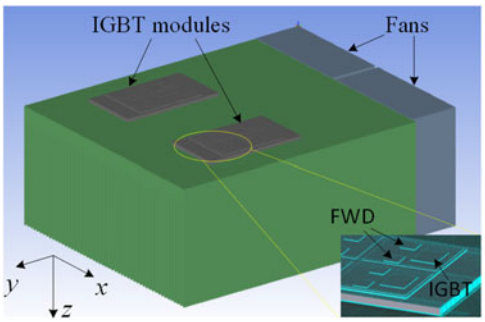


Fig. 11. Structure model of paralleled modules established in the FEM simulation tool.

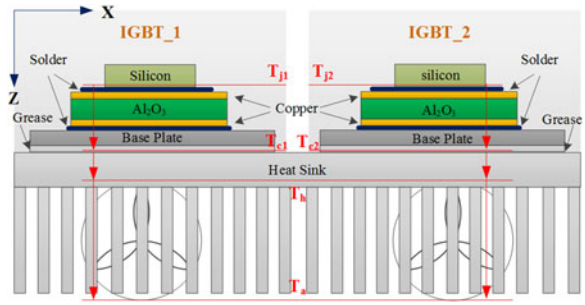


Fig. 12. Temperature distribution of the packaging layers in modules and the cooling system.

different operation conditions, heat sinks are always designed with various sizes. Also, force air or water cooling is typically implemented to improve the heat-sinking capability. In general, arbitrary geometrical shapes of heat sinks and varying surrounding fluid make the analytical methods [21], [22] for obtaining the transient thermal impedance more complicated. To solve these intricate problems, the numerical method with 3-D FEM simulation tools is widely employed, even though at the cost of more computer resources.

The model of the whole system was built in the FEM tool ICEPAK first, based on the dimensions and materials of the modules and heat sink. After that, a coarse meshing for the system and a denser meshing in the devices were implemented to get precise results. The transient curves of temperature distributions were obtained to derivate the *RC* networks of this system by numerical calculations. The schematic structure of the paralleled system is depicted in Fig. 11, which is composed of two IGBT modules and a cooling system with a heat sink and fans. The heat sink is cooled by forced air convection generated from two fans located at symmetrical position.

With a reasonable assumption that the materials are homogeneous and isotropic, the 3-D heat diffusion equation to describe the transient temperature in this system can be written as

$$\nabla(k_i \nabla T_i(x,y,z,t)) = \rho_i c_i \frac{\partial T_i(x,y,z,t)}{\partial t}, i = 1,2,\ldots,n \tag{17}$$

where T_i is the temperature for the *i*th layer, and k_i, ρ_i, *and* c_i are the thermal conductivity, the specific, and the material density, respectively, in the *i*th layer and *n* means the total number of layers. In the IGBT module, the heat source generated from the silicon layer mainly flows to the heat sink in the vertical direction as the *Z*-axis in Fig. 11. To get more accurate results, the meshing size in the vertical direction must be slimmer since the thickness of each layer is extremely thin compared with the length and the width as illustrated in Fig. 11. In addition, the rotation per minute (RPM) of the fans is set as 2500 to produce constant wind speed.

Fig. 12 illustrates the layers inside the modules and key temperature points of paralleled IGBT modules mainly in the vertical direction. Table III shows the thickness and thermal conductivity of each layer. It should be noted that the temperature distribution on the top surface of heat sink is diverse when the power losses of parallel modules are different, especially

TABLE III
THERMAL PARAMETERS AND THICKNESS OF EACH LAYER IN MODULES

Layer	Silicon	Solder	Copper	Al_2O_3	Baseplate
Thermal conductivity (W/(m∗K))	180	57	390	17	390
Thickness (μm)	300	100	400	380	3000

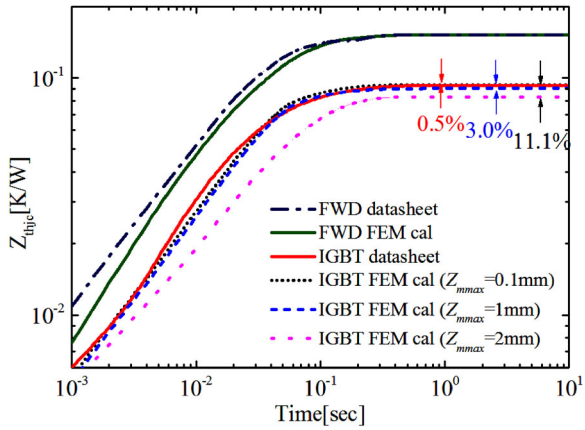


Fig. 13. Comparison of calculation results and datasheet of transient thermal impedance for IGBT chip and diode chip $\left(\text{Error}(\%) = \frac{|\text{calculation}-\text{datasheet}|}{\text{datasheet}} \times 100\%\right)$.

when the distance of the modules is longer. At the condition of certain power losses *P*, the transient thermal impedance Z_{th} can be derived by

$$Z_{\text{th}} = \frac{\Delta T}{P}. \tag{18}$$

By substituting the calculation results into (18), the transient thermal impedance curves from junction to case for both IGBT and FWD are derived and compared with device datasheet as shown in Fig. 13. The comparison indicates that the calculated steady impedance is in accordance with the provided data. Additionally, the meshing quality especially in perpendicular direction affects the calculation accuracy. Thermal impedance with different maximal element size $Z_{m\max}$ in *Z*-direction is calculated in the software. When $Z_{m\max}$ is set to be equal to the smallest size of the layers: 0.1 mm, the error is within 0.5%.

TABLE IV
PARAMETERS FOR THE TRANSIENT THERMAL IMPEDANCE FOR IGBT, FWD CHIPS, AND COOLING SYSTEM

Parameters of Thermal Impedance Internal Modules					
	i	1	2	3	4
IGBT	R_i (K/W)	0.024	0.027	0.030	0.011
	τ_i (s)	0.051	0.060	0.059	0.071
FWD	R_i (K/W)	0.039	0.043	0.048	0.018
	τ_i (s)	0.059	0.058	0.030	0.174
Parameters of Thermal Impedance for the Cooling System					
Grease	R_i (K/W)	0.078	-	-	-
	τ_i (s)	0.814	-	-	-
Heat sink Vertical P_v	R_i (K/W)	0.051	-	-	-
Heat sink ($D = 3.8$ cm)	τ_i (s)	54.41	-	-	-
Horizontal P_H	R_i (K/W)	0.087	0.018	-	-
Heat sink ($D = 3.8$ cm)	τ_i (s)	11.68	70.57	-	-
Middle P_M	R_i (K/W)	0.175	-	-	-
	τ_i (s)	66.40	-	-	-

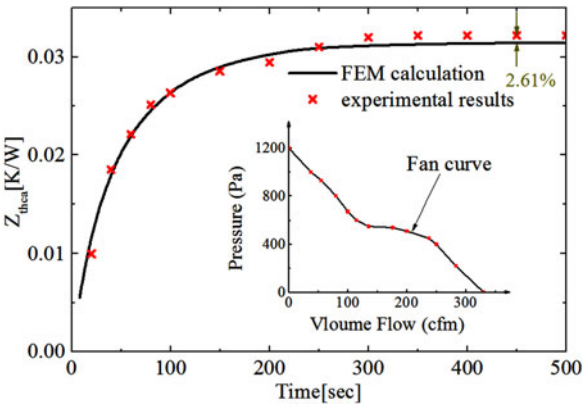


Fig. 14. Comparison of calculation and experimental results of transient thermal impedance for heat sink and the fan's nonlinear curve of pressure to volume flow.

However, the error increases to be 11.1% if $Z_{m\max}$ is set as 2 mm. Thereby, the meshing quality in *Z*-direction should be denser to get precise results.

Foster *RC* network is utilized to characterize the transient thermal impedance in a simple *RC* cascade form. The parameters of the *RC* network can be obtained facilely by the transient temperature curve. In general, the curve of $Z_{\rm th}$ versus time is fitted as a series of finite number of exponential terms as

$$Z_{\rm th} = \sum_{i=1}^{m} r_i \cdot \left(1 - e\left(-\frac{t}{\tau_i}\right)\right). \tag{19}$$

By applying user-defined functions in the data-fitting toolbox "*cftool*" in MATLAB, the parameters r_i and τ_i were obtained and listed in Table IV.

Moreover, the thermal impedance of heat sink used in this system was calculated and shown in Fig. 14. In the software ICEPAK, the IGBT chips are heated by constant power and the simulative model of the heat sink is established according to the real objects including the sizes and the materials as shown in Fig. 11. Also, the position, the distance, and the size of the fans can be specified as the same with the real objects. Since the heat sink is cooled by air force, the most important factor is the input fan flow rate, which is characterized by the nonlinear curve of pressure to volumetric flow as depicted in Fig. 14. The curve can be obtained in the datasheet of the fans. After these sets in the software, air speed through the fins of the heat sink can be calculated automatically. In order to measure the thermal impedance of the heat sink, we built a platform with the same dimensions of the simulative model. One of the paralleled modules in the buck converter as pictured in Fig. 2 was operating to generate power losses. According to the simulation results, the temperature-dependent power losses change little during the transient process of the thermal impedance of the heat sink because the transient duration of $Z_{{\rm th}jc}$ is much shorter than $Z_{{\rm th}ca}$ and the thermal resistance of the heat sink is much smaller than the thermal resistance of the modules. To verify the calculated thermal impedance, the temperature at the bottom boundary of the base plate was measured by a thermistance when a single module was operating. Although the temperature is distinct at the boundary and the center of the baseplate's button, the difference is slight according to the simulation results as shown in Fig. 15. Also, the fitting parameters of Foster network for the heat sink and grease were derived from the simulation results.

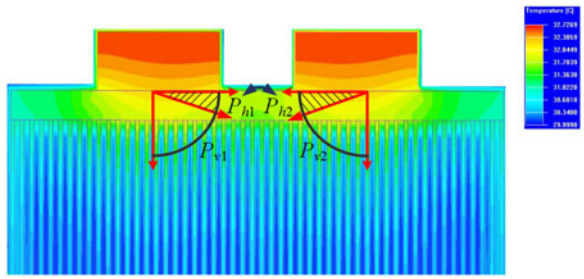


Fig. 15. Temperature distribution of a cut plane in a simplified model of paralleled blocks. The two blocks are heated by 50 W and the ambient temperature is 30 °C.

Most of thermal models proposed in papers [21]–[26] are suitable for a single module with high accuracy. However, for the paralleled IGBT modules mounted on the same heat sink, the interaction of the devices is hardly considered. In this study, the thermal distribution of two simplified block sources on the same heat sink was simulated and depicted in Fig. 15. There are two parts of heat flow: the most losses as P_{v1} and P_{v2} flow in the vertical direction and a small part as P_{h1} and P_{h2} flows in the horizontal direction. Fig. 16 gives the temperature distributions in the surface of the heat sink with two different distances of mounted modules in the moment of 500 s. The results show that smaller distance leads to less temperature distinction between the block center and the intermediate position of two modules, which cannot be explained by thermal models of single module. Therefore, an interacted *RC* network is introduced to illustrate the relation of the transient thermal impedance and the distance of the paralleled modules. In order to derive the *RC* network parameters, the transient temperature drop between the center of the block and the middle point of the paralleled devices on

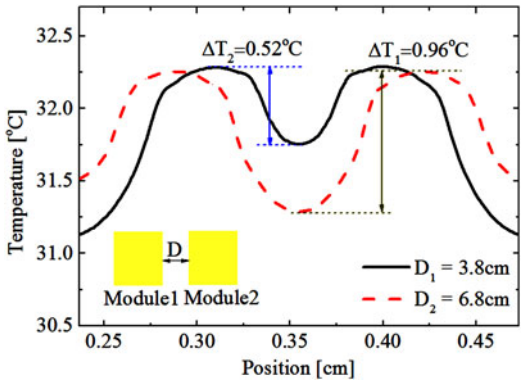


Fig. 16. Temperature distribution on the intersect line of the cut plane and the surface of heat sink with different mounting distance at the moment of 500 s.

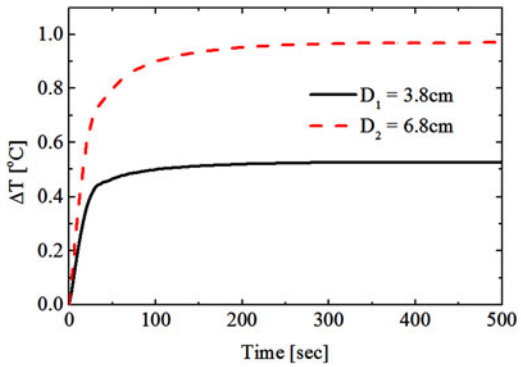


Fig. 17. Temperature distribution on the intersect line of the cut plane and the surface of heat sink with different mounting distance at the moment of 500 s.

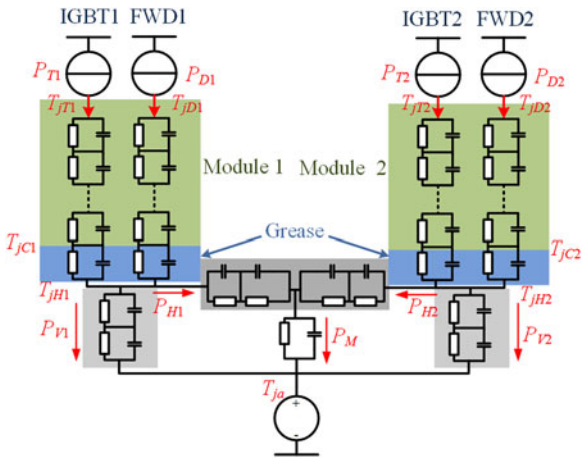


Fig. 18. Network of thermal impedance for paralleled IGBT modules based on Fig. 12.

the surface is calculated and depicted in Fig. 17. With fitting tools, the parameters are derived and shown in Table IV.

According to the structure model of the paralleled system as shown in Fig. 12, the network of thermal impedance for the internal structure and cooling system can be drawn as shown in Fig. 18. The interaction effect of the paralleled modules can be described by the *RC* cells in horizontal direction.

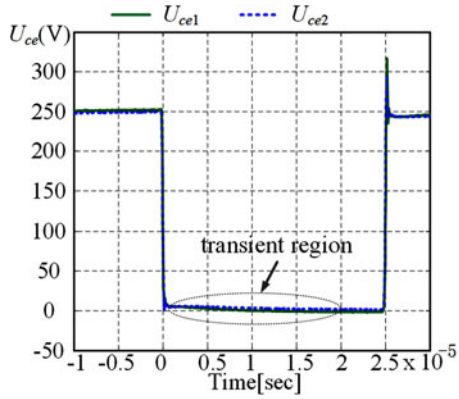


Fig. 19. Typical transient waveforms of $U_{\rm ce}$ during switching under unbalanced parasitic inductance.

V. Electrothermal Models and Experimental Validations

It is necessary to combine the analytical loss model and thermal impedance to build a complete simulation electrothermal model. In addition, experiment should be carried out to verify the proposed model. Since there are parameters varying with junction temperatures in the loss model, the junction temperature should be acquired first. Then, an integrated electrothermal model was established in MATLAB/Simulink environment to calculate the transient junction temperatures and losses in this paper.

A. Derivation of Junction Temperatures

With the aim of investigating the influence on the temperature distributions by different parasitic parameters, the junction temperature should be obtained first with good precision, meanwhile with low cost. Practically, there are several methods that can be employed, including optical methods, physical contacting methods, and electrical methods [37]. It is worth noting that there are few accesses to probe the silicon chips in the module package. Thus, physical contacting methods are not suitable in this application. Besides, by infrared radiation thermometers after disposing of the shell of the modules, the infrared reflectivity of chip surface and silicon gel above the chips will have an inestimable impact on the temperature measurement. Therefore, by surveying some thermosensitive electrical parameters during the operating process of devices, electrical methods are indicated as indirect but low-cost and precise means to obtain junction temperature. The parameter of the on-state collector–emitter voltage $U_{\rm ce}$ is common utilized to estimate the variation of averaging temperature in space with proper calibrations [38], [39]. However, a transient region after the voltage $U_{\rm ce}$ turns to conduction state from blocking state lasts some time, which will emerge especially in high-frequency applications and paralleled systems as observed in Fig. 19. In this study, with the frequency increasing, the on-state duration becomes shorter, which results in the difficulty to measure precise values of the voltage $U_{\rm ce}$. It is worth underlining that the study in [35] provides an alternative and relatively accurate way to determine the junction

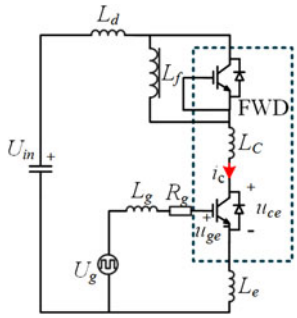


Fig. 20. Equivalent circuit for testing IGBT transient characteristic (dashed area stands for the half-bridge IGBT module).

TABLE V
SPECIFICATIONS OF THE SYSTEM IN FIG. 21

Stray inductance in emitter L_e	14.7 nH
Stray inductance in collector L_c	3.57 nH
Stray inductance in gate driving circuit L_g	51.5 nH
Total stray inductance in other wires L_d	123.5 nH

temperature because $du_{\rm ce}/dt$ at turn-off phase is sensitive to the variation of T_j with a relatively linear relation. Therefore, the temperature-sensitive parameter $du_{\rm ce}/dt$ is derived to determine the junction temperature, which is shown in the next part.

B. Electrothermal Models

First of all, it is necessary to certify that the electrical model is suitable for single device and can be used to estimate the switching losses. So, a chopper cell circuit as shown in Fig. 20 is established to test the switching waveforms and measure the transient power losses. By FEM software ANSOFT, the parasitic inductance can be calculated precisely, and the results are shown in Table V. The input voltage $U_{\rm in}$ is 300 V and the conduction current is 90 A. First, the switching waveforms of the IGBT module (FF300R12KT4) with different driving resistors are tested and compared with calculated results as shown in Fig. 21. Although there are some knee points in the calculated waveforms since we used different equations to model every stage in Section III, the results match well. Then, the module is measured in different junction temperature by utilizing a heating system. The loss calculation results deriving from this analytical model are compared with measurement data in Fig. 22. As seen in the figure, the difference between the measured and calculated switching loss is within 5%, which indicates good agreement. It should be noted that the turn-on duration can be shorten by reducing the driving resistor, and the turn-on losses are decreased accordingly as can be seen in Fig. 22. In additional, test results of $du_{\rm ce}/dt$ versus temperature and collector current in inductive loads is exhibited in Fig. 23. The quantitative relations are fitted in linear by test results.

Generally, the electrothermal model should combine the electrical model and thermal model to make up a feedback network as mentioned in Fig. 1. Thereby, a circuit simulation diagram

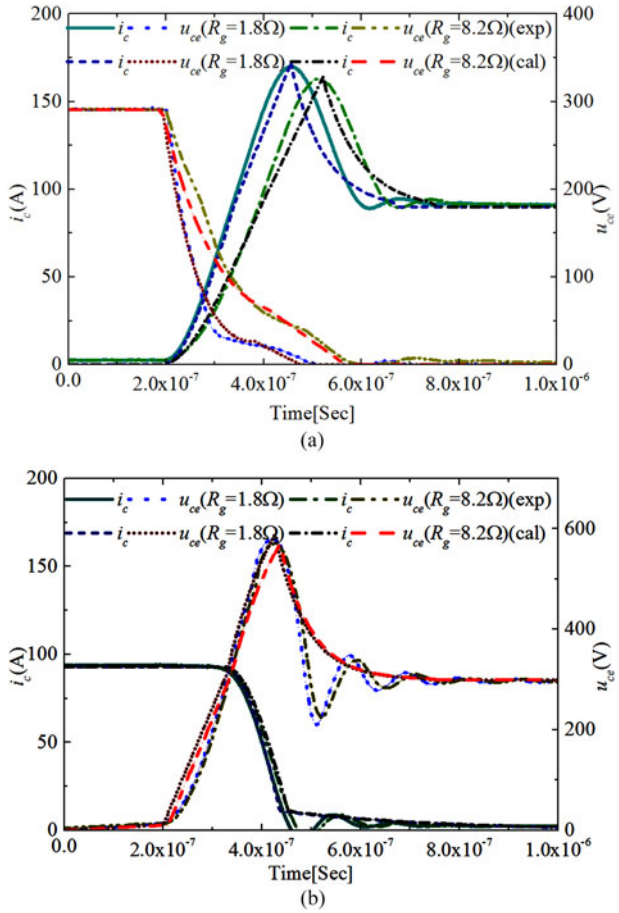


Fig. 21. Comparisons of measured and calculated (a) turn-on and (b) turn-off waveforms of single IGBT module with different driving resistors (test condition: conduction current is 90 A, input voltage is 300 V, junction temperature is 20 °C).

including the *RC* networks was built in MATLAB/Simulink environment to verify the proposed paralleled models as depicted in Fig. 24. There are three main parts in this model. First is the initial conditions including the input voltage $U_{\rm in}$ output filter current I_o and unbalance stray inductance L_{c1}, L_{c2}. The second part is the loss models for the paralleled devices under the initial conditions. Besides, the junction temperatures of both devices, which are calculated by thermal models, are the extra inputs since the temperature-sensitive parameters in loss models are determined by the derived temperatures. The derived equations in Section III are realized by program files, which can be embedded in Simulink environment easily. We calculated turn-on losses, turn-off losses, and conduction losses separately because the current distributions are diverse in different stages. The losses of each part are derived by integrating the product of the collector current and the collector–emitter voltage at different stages. The duration of stage 1 in Fig. 6 is determined by the collector current rising from zero to steady current and the duration of stage 2 is the same as the diode reverse recovery time. Moreover, the duration of stage 4 in Fig. 10 is calculated according to the rising slope of $u_{\rm ce}$ and the duration of stage 5 is identical to the tail time of the collector current. After summing

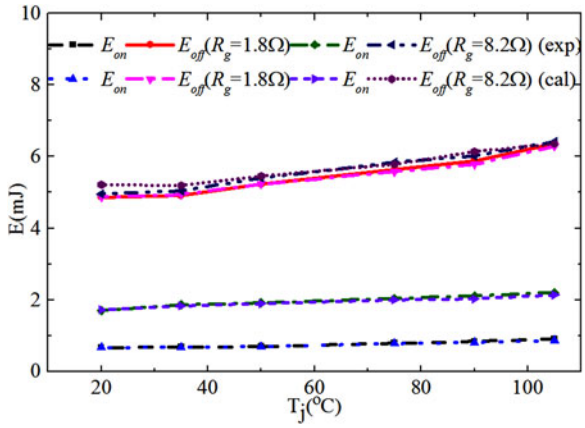


Fig. 22. Comparison of loss models and calculation results with different driving resistors (test condition: conduction current is 90 A, input voltage is 300 V).

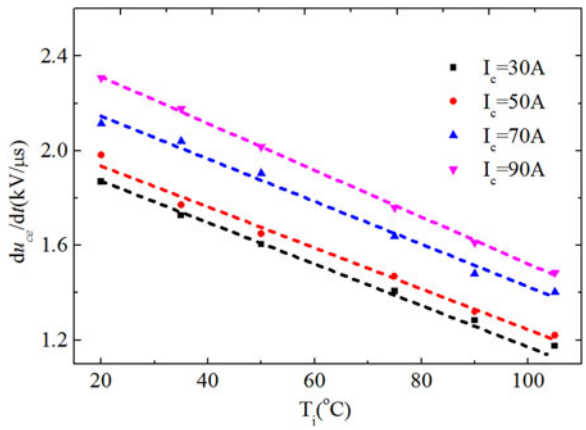


Fig. 23. $du_{\rm ce}/dt$ at turn-off period versus junction temperature at different conduction current.

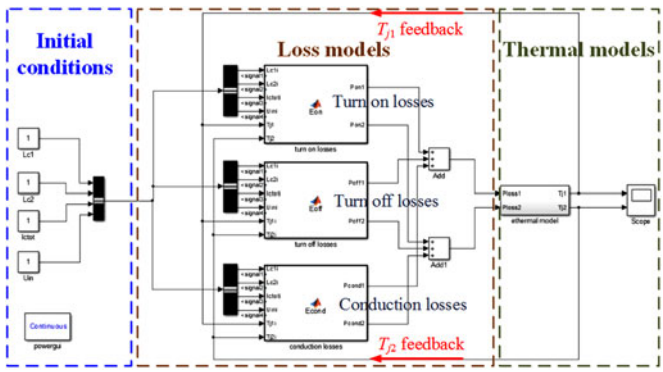


Fig. 24. Electrothermal model of paralleled IGBT modules in MATLAB/Simulink environment.

up each part, the losses of paralleled devices can be obtained. Last part is the thermal model, which is composed of resistors and capacitors as illustrated in Fig. 18. The input of the thermal models is the calculated power dissipations from losses models. At the beginning of the next calculation recursion, the junction

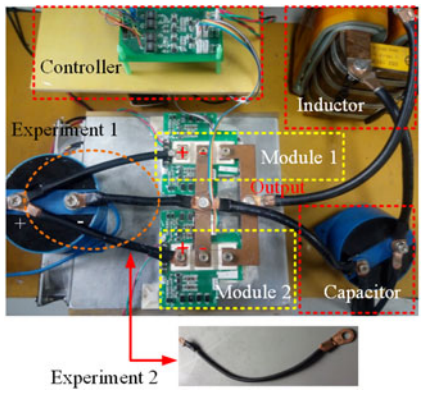


Fig. 25. Buck converter for paralleled modules with equal and unequal stray inductance in collector.

temperatures in losses models are replaced by the output results of the thermal models, as illustrated by the feedback lines in Fig. 24. The recursion is carried on until the junction temperatures tend to be stable. In this study, we set the simulation time 600 s according to the thermal impedance of the heat sink.

C. Experiment Verifications

1) Experiment Setup: In order to validate the proposed transient electrothermal models with different stray inductance as discussed previously, a platform of buck converter with cooling system was established for electrical and thermal measurement as illustrated in Fig. 25. Two cylindrical wires are employed to connect the positive wires of input voltage and the collectors of paralleled modules with the same and different length. The inductance value of wires can be obtained as demonstrated in Section II.

In the first experiment, which is under the same parasitic parameters in collector of modules, the stray inductance of equal-length wires is 58.2 nH. After that, replace one of the wires with a longer one (141 nH), which will lead to unbalanced current sharing. Fig. 26 depicts the comparisons of turn-on and turn-off waveforms of $u_{\rm ce}$ and i_c from measurements and calculations, which are in good agreement. The results show that the paralleled modules share the identical collector current when the collector connecting wires are equal. It is unsurprised to acquire balanced sharing due to that all the structures are symmetrical to ensure all the parasitic elements are as same as possible, plus the same parameters of the driving circuits. The unbalanced stray inductance in collector results in obvious distinctions in current sharing and different voltage mutation as shown in the picture of Fig. 26(c) and (d). The difference can be explained qualitatively by the proposed model as discussed in Section III.

2) Transient Junction Temperature Validations: During the experiment, the transient waveforms of the collector current and the collector–emitter voltage were memorized by the oscilloscope at certain time interval. Subsequently, the junction temperature and power losses at different moment were obtained by analyzing the experimental data. Fig. 27(a) shows the transient temperature in the experiment with equal inductance and

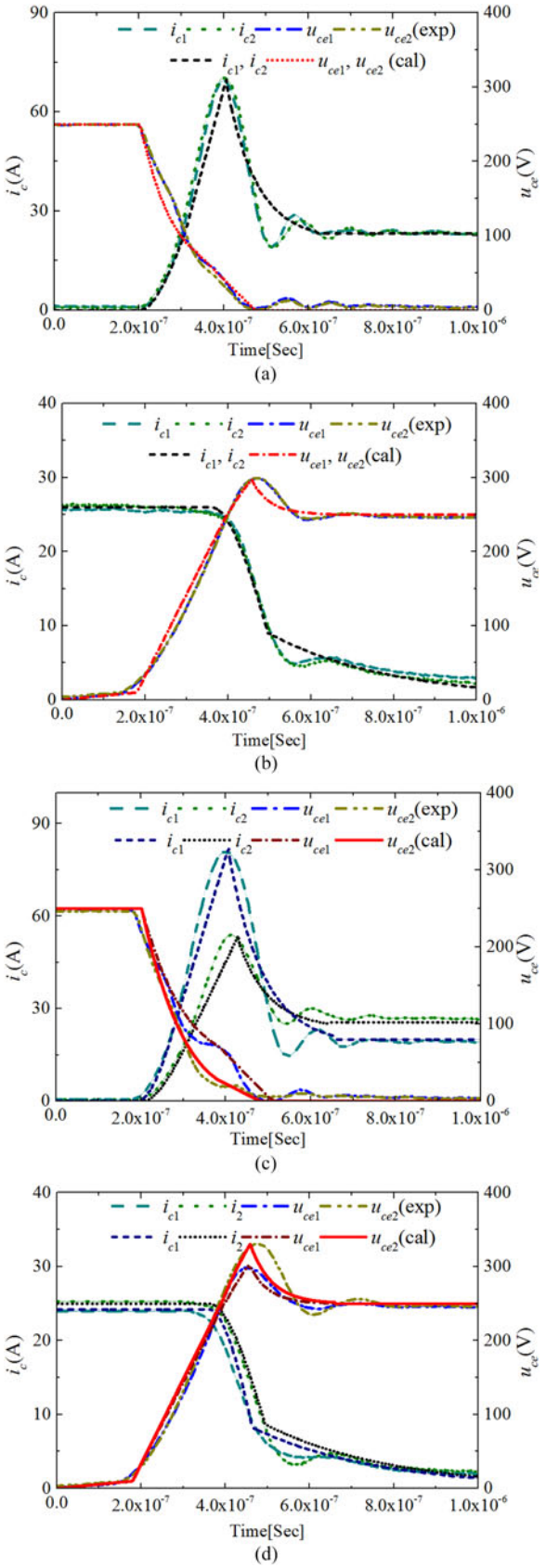


Fig. 26. Comparisons of measured and calculated (a) (c) turn-on and (b), (d) turn-off waveforms of paralleled IGBT modules [(a), (b): identical stray inductance $L_{c1} = L_{c2} = 58.2$ nH, (c), (d): different stray inductance $L_{c1} = 58.2$ nH, $L_{c2} = 141$ nH, junction temperature is 20 °C)].

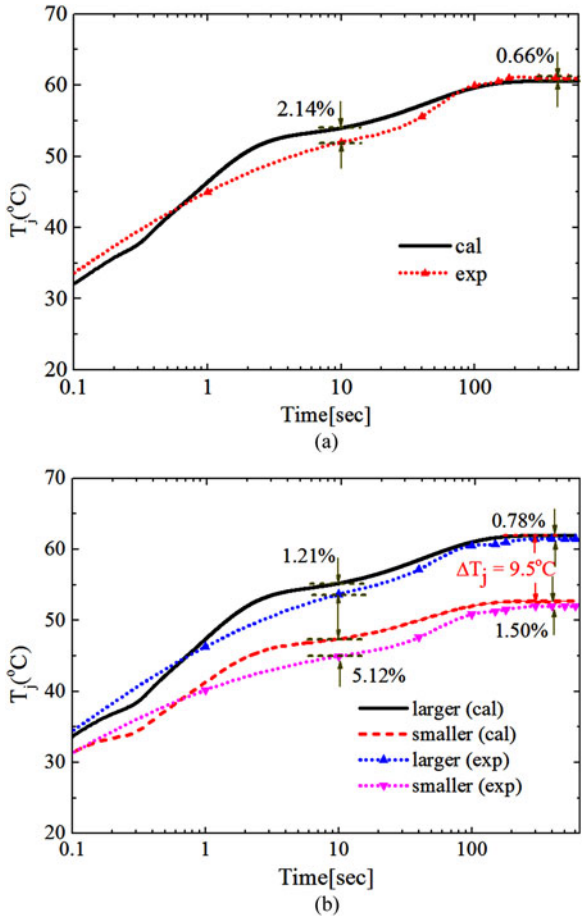


Fig. 27. Transient curves of junction temperature of paralleled modules. (a) Equal stray inductance. (b) Different stray inductance. ($\mathrm{Error}(\%) = \frac{|\mathrm{calculation}-\mathrm{datasheet}|}{\mathrm{datasheet}} \times 100\%$ the same below)

Fig. 27(b) shows the temperature under the test of unequal inductance. The curves show good agreement within 10% error at transient process when compared with the calculation results derived from the proposed models. Some distinctions occurring on the transient process of fast temperature mutations may be due to the imprecise time counting and deviations in the method of temperature measurement. In addition, the manufacturing tolerances result in the modules positions that are not as precisely positioned as in the simulation. The difference in the steady-state junction temperature may come from deviation between the calculated thermal resistors and real ones.

3) Loss Model Validations: It can be drawn that the junction temperature in the paralleled modules is not the same since some distinctions happens on the stray inductance located in the collector. To illustrate the reasons in more details, the transient power losses in different stages are pictured in Fig. 28, including the experimental and calculated results. Fig. 28(a) shows the turn-on, turn-off, and conduction loss energy in one switching cycle in the experiment with equal parasitic parameters. Fig. 28(b) and (c) shows the power loss energy of the modules with larger inductance (141 nH) and smaller inductance (58.2 nH), respectively. It can be observed that the turn-off and conduction losses of the module with larger inductance become

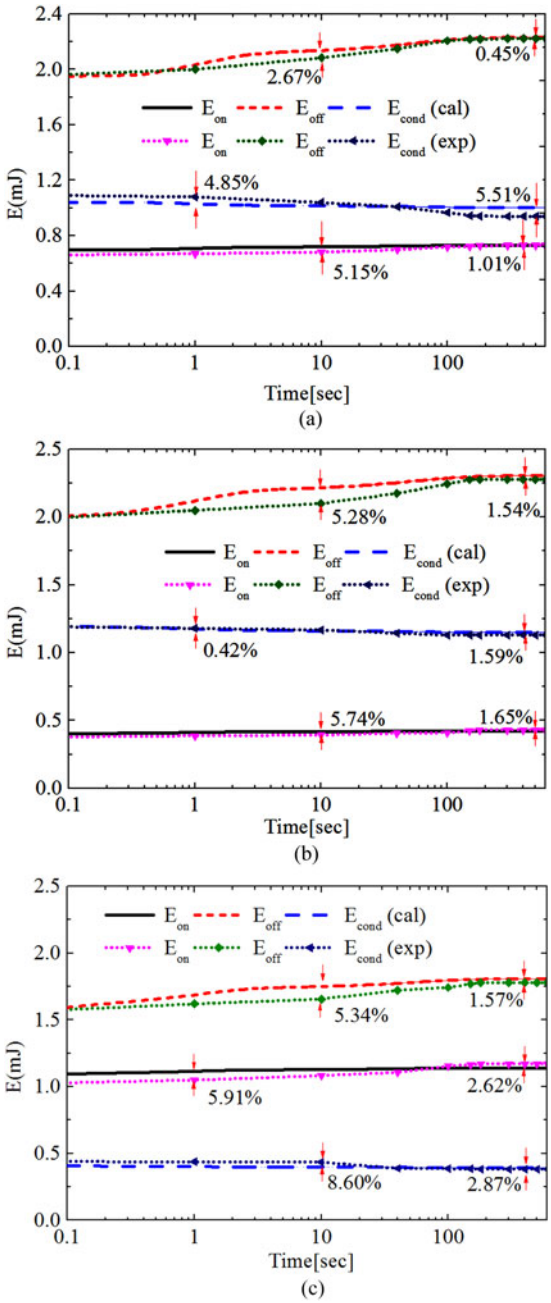


Fig. 28. Transient curves of power losses of paralleled modules. (a) Equal stray inductance, (b) larger inductance, (c) smaller inductance.

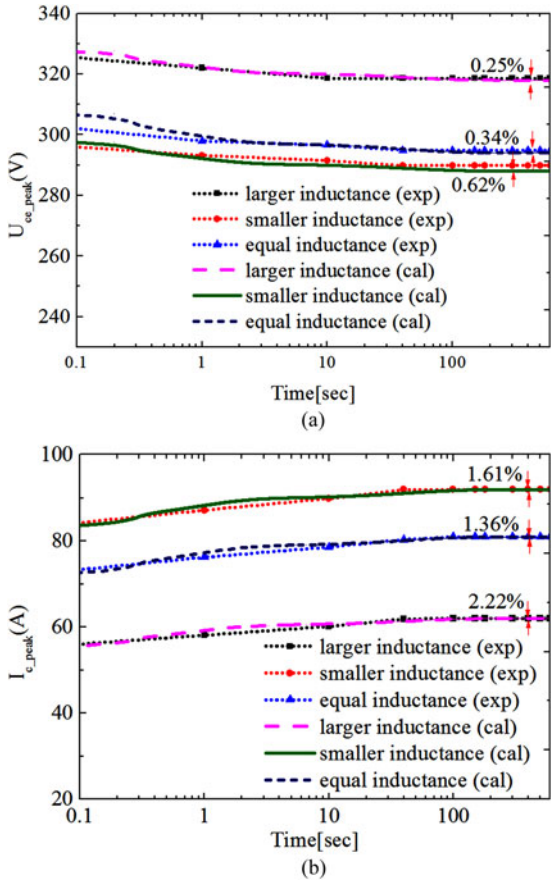


Fig. 29. Transient overshooting of current and voltage of paralleled modules. (a) Collector–emitter voltage during turn OFF, (b) collector current during turn ON.

more, compared with the losses in the experiment with equal inductance, on the contrary, the turn-on losses becomes fewer. The variation tendency of the losses in the other module is in the opposite direction. On the whole, the losses of the branch with larger stray inductance become more, which leads to the junction temperature increasing slight as seen in Fig. 27(b). Meanwhile, the total losses of another paralleled device decreases dramatically, and thus, the junction temperature turns to be lower palpably. In the process of the experiments, the results indicate that as the distinction of stray inductance in the paralleled devices becomes larger, the difference of junction temperature in the devices turns into be larger. An 82.8-nH difference in collector inductance results in about 10 °C distinctions. In the long term of system running, the unbalanced stray inductance will bring about the lifetime of the devices reduced because of the unbalanced temperature distribution in the modules. Compared with electrical models without considering that the losses changes when junction temperature varies, the change of losses in different stages can be predicted precisely, which brings about more accurate temperature results furthermore.

4) Current and Voltage Spike Validations: Another aspect that should be concerned is the overshoot impulse of the collector current in the turn-on period and the collector–emitter voltage in the turn-off period. As shown in Fig. 29(a), in the module with larger inductance, the voltage spike during the turn-off period becomes larger since the voltage is proportional to the stray inductance. However, the spike is weakened as the junction temperature rises. At the same time, the current peak in the turn-on period increases when the junction temperature goes up as illustrated in Fig. 29(b). The reason is that the reverse recovery charge of the FWDs, which determines the current peak during turn ON, is related to the junction temperature directly. According to the impedance of paralleled branch, the modules with larger inductance will share smaller current spike. Therefore, as the power rating of the system increase, the paralleled module with smaller stray inductance takes more risks to get out of order due to higher current spike. Meanwhile,

larger stray inductance may lead to higher voltage spike, which causes the module breakdown more likely. In addition, the proposed method can be expanded to more paralleled devices since impedance analysis in loss models is easily implemented to calculate the current distributions in several paralleled modules.

VI. Conclusion

In applications of parallel modules, junction temperature distributions and overshoot of current and voltage are significant factors that determine lifetime of the devices and reliability of the system. Since some restrictions during the system installation can result in unbalanced stray inductance in the paralleled branch, a dynamic electrothermal model is proposed in this paper. First, the parasitic elements are analyzed and calculated in detail by an FEM tool. By considering the interaction of the paralleled IGBT modules based on impedance analysis, an improved power loss model, which takes into account the influence on the losses by junction temperature, is put forward. Furthermore, a novel thermal model is established to derive the parameters of the *RC* networks. The relative position of the paralleled devices in the same heat sink, which has an impact on the thermal transient behaviors, is also included in the thermal networks. In general, the quantified correlation between stray power losses, thermal impedance, and stray inductance is mathematically built up and validated by experiments. Based on the proposed model, issues such as temperature unbalance and overshoot of current and voltage can be analyzed quantitatively to guide the design more precisely.

References

[1] R. Letor, "Static and dynamic behavior of paralleled IGBT's," *IEEE Trans. Ind. Appl.*, vol. 28, no. 2, pp. 395–402, Mar./Apr. 1992.

[2] J. J. Nelson, G. Venkataramanan, and B. C. Beihoff, "Investigation of parallel operation of IGBTs," in *Proc. 37th IAS Annu. Meet. Conf. Rec. Ind. Appl. Conf.*, 2002, vol. 4, pp. 2585–2591.

[3] U. Schlapbach, "Dynamic paralleling problems in IGBT module construction and application," in *Proc. Int. Conf. Integr. Power Electron. Syst.*, 2010, pp. 1–7.

[4] C. Nan, F. Chimento, M. Nawaz, and L. Wang, "Dynamic characterization of parallel-connected high-power IGBT modules," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 539–546, Jun. 2014.

[5] A. R. Hefner, "A dynamic electro-thermal model for the IGBT," *IEEE Trans. Ind. Appl.*, vol. 30, no. 2, pp. 394–405, Mar./Apr. 1994.

[6] H. Wang, A. M. Khambadkone, and X. Yu, "Control of parallel connected power converters for low voltage microgrid—Part II: Dynamic electrothermal modeling," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2971–2980, Dec. 2010.

[7] A. Castellazzi, "Comprehensive compact models for the circuit simulation of multichip power modules," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1251–1264, May 2010.

[8] B. Du, J. L. Hudhins, E. Santi, A. T. Bryant, P. R. Palmer, and H. A. Mantooth, "Transient electrothermal simulation of power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 237–248, Jan. 2010.

[9] A.Bryant, N. Parker-Allotey, D. Hamilton, I. Swan, P. A. Mawby, T. Ueta, T. Nishijima, and K. Hamada, "A fast loss and temperature simulation method for power converters, Part I: Electrothermal modeling and validation," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 248–257, Jan. 2012.

[10] K. Ma, A. S. Bahman, S. Beczkowski, and F. Blaabjerg, "Complete loss and thermal model of power semiconductors including device rating information," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2556–2569, May 2015.

[11] A. R. Hefner and D. M. Diebolt, "An experimentally verified IGBT model implemented in the Saber circuit simulator," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 532–542, Sep. 1993.

[12] K. Sheng, S. J. Finney, and B. W. Williams, "A new analytical IGBT model with improved electrical characteristics," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 98–107, Jan. 1999.

[13] P. R. Palmer, E. Santi, J. L. Hudgins, X. Kang, J. C. Joyce, and P. Y. Eng, "Circuit simulator models for the diode and IGBT with full temperature dependent features," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1220–1229, Sep. 2003.

[14] J. T. Hsu and K. D. Ngo, "Behavioral modeling of the IGBT using the Hammerstein configuration," *IEEE Trans. Power Electron.*, vol. 11, no. 6, pp. 746–754, Nov. 1996.

[15] A. Monti, "Fuzzy-based black-box approach to IGBT modeling," in *Proc. IEEE Int. Conf. Electron., Circuit, Syst.*, 1996, vol. 2, pp. 1147–1150.

[16] A. D. Rajapakse, A. M. Gole, and P. L. Wilson, "Electromagetic transients simulation models for accurate representation of switching losses and thermal performance in power electronic systems," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 319–327, Jan. 2005.

[17] L. Lu, A. Bryant, J. L. Hudgins, P. R. Palmer, and E. Santi, "Physics-based model of planar-gate IGBT including MOS side two-dimensional effects," *IEEE Trans. Ind. Appl.*, vol. 46, no. 6, pp. 2559–2667, Nov./Dec. 2010.

[18] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[19] P. J. Grbovic, "An IGBT gate drive for feed-forward control of turn-on losses and reverse recovery current," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 643–652, Mar. 2008.

[20] K. Takao and H. Ohashi, "Accurate power circuit loss estimation method for converters with Si-IGBT and SiC-diode hybrid pair," *IEEE Trans. Electron. Devices*, vol. 60, no. 2, pp. 606–612, Feb. 2013.

[21] Y. C. Gerstenmaier, A. Castellazzi, and G. K. M. Wachutka, "Electrothermal simulation of multichip-modules with novel transient thermal model and time-dependent boundary conditions," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 45–55, Jan. 2006.

[22] I. Swan, A. Bryant, P. A. Mawby, T. Ueta, T. Nishijima, and K. Hamada, "A fast loss and temperature simulation method for power converters, Part II: 3-D thermal model of power module," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 258–268, Jan. 2012.

[23] Z. Luo, H. Ahn, and M. A. Nokali, "A thermal model for insulated gate bipolar transistor module," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 902–907, Jul. 2004.

[24] C. Yun, P. Malberti, M. Ciappa, and W. Fichtner, "thermal component model for electrothermal analysis of IGBT module systems," *IEEE Trans. Adv. Packag.*, vol. 24, no. 3, pp. 401–406, Aug. 2001.

[25] M. Iachello, V. D. Luca, G. Petrone, N. Testa, L. Fortuna, G. Cammarata, S. Graziani, and M. Frasca, "Lumped parameter modeling for thermal characterization of high-power modules," *IEEE Trans. Compon. Packag. Technol.*, vol. 4, no. 10, pp. 1613–1623, Oct. 2014.

[26] A. Ammous, S. Ghedira, B. Allard, H. Morel, and D. Renault, "Choosing a thermal model for electrothermal simulation of power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 300–307, Mar. 1999.

[27] L. Popova, R. Juntunen, T.Musikka, M. Lohtander, P. Silventoinen, O. Pyrhonen, and J. Pyrhonen, "Stray inductance estimation with detailed model of the IGBT module," in *Proc. Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–8.

[28] K. Xing, F. C. Lee, and D. Boroyevich, "Extraction of parasitics within wire-bond IGBT modules," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 1998, pp. 497–503.

[29] N. Zhu, M. Chen, and D. Xu, "A simple method to evaluate substrate layout for power modules," in *Proc. Int. Conf. Integr. Power Electron. Syst.*, 2014, pp. 1–6.

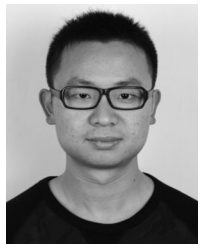
[30] M. Trivedi and K. Shenai, "Parasitic extraction methodology for insulated gate bipolar transistors," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 799–804, Jul. 2000.

[31] D. Xu, H. Lu, L. Huang, S. Azuma, M. Kimata, and R. Uchida, "Power loss and junction temperature analysis of power semiconductor devices," *IEEE Trans. Ind. Appl.*, vol. 38, no. 5, pp. 1426–1431, Sep./Oct. 2002.

[32] S. Linder, *Power Semiconductors.* Milan, Italy: EPFL Press, 2006.

[33] P. O. Lauritzen and C. L. Ma, "A simple diode model with reverse recovery," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 188–191, Apr. 1991.

[34] Y. Tang and H. Ma, "An improved analytical IGBT model for loss calculation including junction temperature and stray inductance," in *Proc. 24th Int. Symp. Ind. Electron.*, 2015, pp. 227–232.
[35] A. Byrant, S. Yang, P. Mawby, D. Xiang, L. Ran, P. Tavner, and P. R. Palmer, "Investigation into IGBT dV/dt during turn-off and its temperature dependence," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 3019–3031, Oct. 2011.
[36] A. R. Hefner, "An improved understanding for the transient operation of the power insulated gate bipolar transistor (IGBT)," *IEEE Trans. Power Electron.*, vol. 5, no. 4, pp. 459–468, Oct. 1990.
[37] D. L. Balackburn, "Temperature measurements of semiconductor devices—A review," in *Proc. 20th Annu. Semicond. Thermal Meas. Manage. Symp.*, 2004, pp. 70–80.
[38] G. Pramod, K. B. Pedersen, A. R. Vega, and B. Rannestad, "A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application," in *Proc. Int. Conf. Integr. Power Electron. Syst.*, 2014, pp. 1–6.
[39] G. Pramod, A. R. Vega, S. Beczkowski, and S. Munk-Nielsen, "A online Vce measurement and temperature estimation method for high power IGBT modules in normal PWM operation," in *Proc. Power Electron. Conf.*, 2014, pp. 2850–2855.



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