An Evolutional Line-Commutated Converter Integrated With Thyristor-Based Full-Bridge Module to Mitigate the Commutation Failure

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***Abstract*—With thyristor-based full-bridge module (TFBM) embedded in the converter valve, an evolutional line-commutated converter (ELCC) is proposed to enhance the commutation failure (CF) immunity. The operating principle of the TFBM and the coordinated control strategy between the TFBM and series-connected valve are presented. The voltage–current stress of the TFBM is analyzed, and the method to select the capacitor parameter is also presented. Then, the ELCC high-voltage direct current (HVDC) under the presented control strategy is developed in PSCAD/EMTDC, and its dynamic responses under ac fault condition are compared with that of capacitor-commutated converter-based HVDC (CCC-HVDC) and conventional line-commutated converter (LCC) HVDC. A dual-infeed HVDC system with TFBM embedded in one HVDC link is also developed to further investigate the merits of TFBM. Finally, the increased capital cost and power loss of the ELCC-HVDC are discussed. The results show that the presented ELCC-HVDC has the ability to reduce the CF risk effectively and also exhibits favorable steady-state and dynamic performances.**

***Index Terms*—Commutation failure, coordinated control strategy, line-commutated converter-based high-voltage direct current, thyristor-based full-bridge module.**

I. Introduction

LINE-COMMUTATED converter-based high-voltage direct current (LCC-HVDC) has been widely used in many areas, such as bulk power long-distance transmission, asynchronous ac grid connection, etc., [1]. However, LCC-HVDC would have poor voltage regulation ability and be susceptible to commutation failure (CF) under weak ac grid or fault condition, which will interrupt the transmitted power, and stress the converter equipment [2]. With the increasing expansion of LCC-HVDC utilization, the ac systems at the terminals of multiinfeed HVDC would become relatively weak, leading to many operational problems. One of the major issues is the cascaded CFs under disturbance. For example, eight LCC-HVDC links, with total dc power capacity of 33 660 MW, located in East-China power grid, where CF is considered as a major concerned issue. The south grid of China also has the similar multiinfeed HVDC situation.

There are many valuable literatures on fault detection, CF recognition, and CF mitigation methods. A calculation method is presented to recognize the CF onset of LCC-HVDC [3]. Wei *et al.* [4] present a direct current predictive control strategy to inhibit the CF in the HVDC converter. Sun *et al.* [5] employ the fuzzy control method to reduce the CF frequency. Hansen and Havemann [6] present a method to calculate the necessity of advancing firing pulses. For three-phase and single-phase faults detection, the abc-$\alpha\beta$ transformation and zero-sequence voltage are used, respectively, which relies on the reliable monitor of the instantaneous ac voltage [7]. Then, an additional angle is deduced from the inverter firing control. Another widely used control is the voltage-dependent dc current order limiter. In [8], a power-component detection method and an improved current order limiter control are proposed, and the CF issues could be mitigated effectively compared with widely used advancing firing angle control. Due to the ac voltage regulation ability, the synchronous condenser, static synchronous compensators or voltage-source converter-based HVDC could be utilized to mitigate the CFs of LCC-HVDC [9]–[11]. However, more extra capital costs are required for additional apparatus.

There are also some enhanced converter topologies for CF mitigation. Lee *et al.* [12] propose a superconducting fault current limiter, which can limit the fault current on the ac side, then to improve the CF immunity. Li *et al.* [13] propose a new filter-commutated inverter, which can greatly increase the commutation margin of the HVDC systems. The well-known concepts of capacitor-commutated converters (CCC) and controlled series capacitor converter (CSCC) show promising results on forced commutation [14], [15], which can offer LCC-HVDC converters an improved power factor and reduced CF probability. However, the CCC could show poor dynamic performance when recovering from unbalanced disturbances such as single-phase fault, and additional voltage limiting arresters are required across the capacitors to protect them against the overcharging during abnormal conditions [16]. Jovcic [17] presents a novel converter configuration that utilizes resonant turn off and forced commutation with auxiliary thyristors to aid commutation in the converter switches, and the CFs issues can be mitigated

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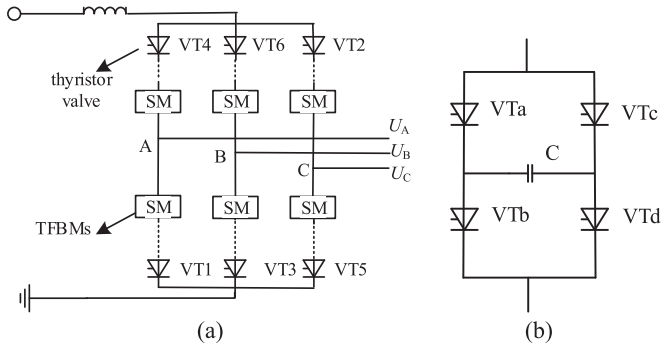

Fig. 1. Topology of ELCC with TFBM. (a) ELCC topology. (b) TFBM.

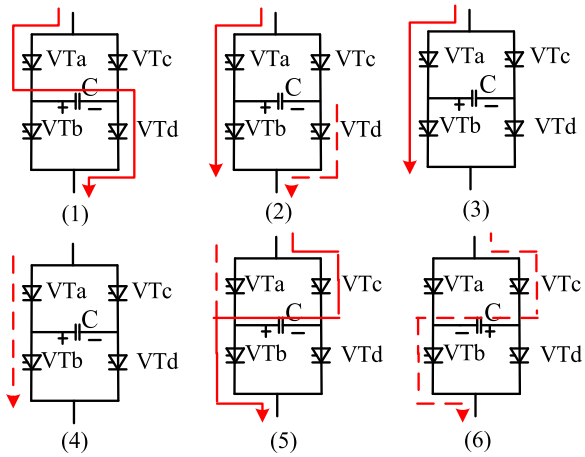

Fig. 2. Current path of TFBM under different stages.

greatly. However, the total harmonic distortion on the ac voltage is somewhat increased and the auxiliary thyristors do increase capital costs. In the motor drive system, the additional six diodes and six static capacitors are also considered to incorporate with the basic six-bridge thyristor-based LCC converter [18], [19], and the additional capacitors also could provide the commutation support for thyristors.

In this paper, an evolutional LCC (ELCC) converter integrating with thyristor-based full-bridge module (TFBM) is proposed to mitigate the CF of LCC-HVDC. The operation principle of TFBM is introduced, and the coordinated control strategy between thyristor valves and series-connected TFBM is presented. Then, the voltage–current stress of TFBM is investigated, and the parameter of capacitor in TFBM is determined. The comparison results among LCC-HVDC, CCC-HVDC, and ELCC-HVDC, based on PSCAD/EMTDC, show that the presented ELCC-HVDC is much less susceptible to CF under both single-phase and three-phase faults, and the voltage–current stress of TFBM can be effectively maintained within its allowable region. Finally, the increased capital cost and power loss of the ELCC-HVDC are discussed.

II. Topology and Coordinated Control Strategy

A. Topology of ELCC

Fig. 1 shows the topology of the presented ELCC converter. Each arm is composed of thyristor valve and certain number of series-connected TFBMs. In each TFBM, four thyristors (VTa–VTd) are arranged as a full-bridge scheme, and the capacitor is utilized to provide the additional volt–time commutation area under abnormal disturbance to reduce the CF risks. VTa (VTb, VTc, or VTd) of TFBM could also be a module with a few thyristors in series, and the number of the switches could be determined according to the dc voltage of the capacitor.

B. Operation Principle of TFBM

The purpose of TFBM is to provide the additional commutation voltage support. However, the series-connected TFBM can also participate in the normal operation state. The operation principle of TFBM is shown in Fig. 2, and the current paths in six different stages are also given below.

Stage 1: Charge the capacitor of TFBM to the set value $U_{C\mathrm{set}}$ by triggering VTa and VTd, when the series-connected arm is conducting.

Stage 2: Trigger VTb, then VTb will conduct with forward bias voltage, and VTd will be turned OFF with reverse bias voltage after state 1 is finished. During this stage, the current of VTb is increasing and the current of VTd is decreasing. Thus, this stage is a transitional stage from stage 1 to 3.

Stage 3: VTa and VTb are fully conductive, and VTd is completely turned OFF after stage 2 is finished.

Stage 4: The current of VTa and VTb is decreasing when series-connected arm is under normal off-going period without experiencing any fault.

Stage 5: When fault occurs and one arm is experiencing off-going period, trigger VTc in TFBM, then VTa will be turned OFF gradually by reverse bias voltage of capacitor. In this stage, the capacitor of TFBM will be charged reversely, and finally, the polarity of capacitor voltage will be reversed in stage 6.

Stage 6: After stage 5, the voltage polarity of capacitor has been reversed. Then, both VTb and VTc will be turned OFF by the reverse bias voltage of capacitor. The reverse bias voltage could also provide the additional volt–time area for the series-connected arm, and the successful commutation process could be much more achievable. It should be noted that the commutation process may experience longer period under a more serious fault condition, and the capacitor will be charged reversely during this stage. Thus, the capacitor may be charged to an unacceptable value. In case of the overvoltage of capacitor, the threshold value, which is regarded as the rated voltage U_{CN} of capacitor, should be carefully considered. If the voltage approaches to the rated value, the capacitor could be bypassed by triggering VTd. Although the commutation support performance from the TFBM is degraded after bypassing the capacitor, the presented ELCC has provided additional volt–time commutation area before bypassing the capacitor, and the capacitor voltage can be maintained in its allowable range. If the fault is not cleared after the capacitor

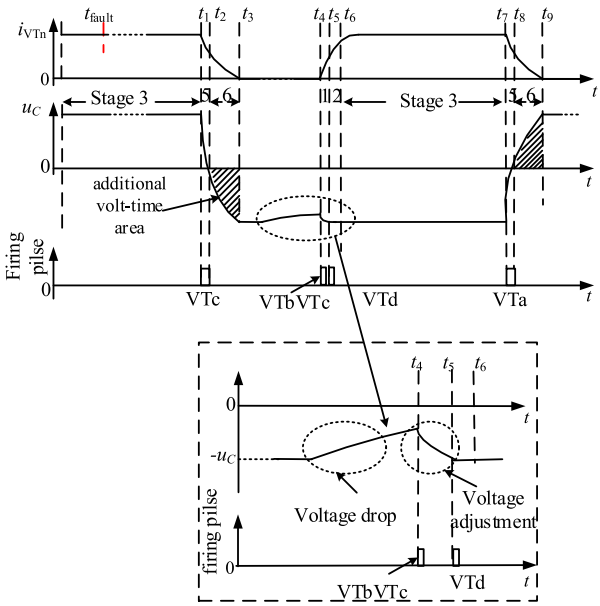

Fig. 3. Schematic diagram of control strategy under fault condition.

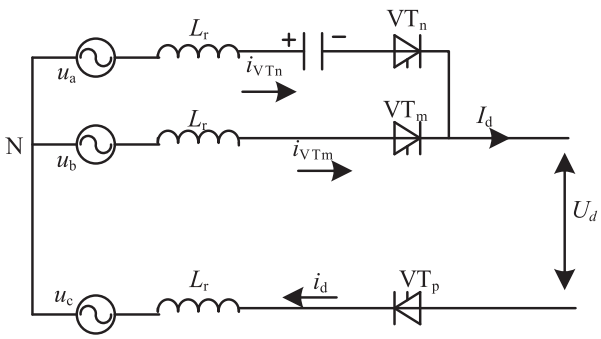

Fig. 4. Equivalent commutation circuit of ELCC.

is bypassed, triggering VTa, turn off VTc gradually. Finally, the capacitor in TFBM will be charged reversely again. Then, both VTa and VTd will be turned OFF. This procedure can be repeatedly conducted to continuously provide the additional volt–time area for the ELCC-HVDC system.

Note that the operation principle of TFBM is illustrated based on the capacitor polarity in Fig. 2. If the capacitor polarity is reversed, the similar operation principle can also be obtained by means of duality. Compared with the conventional LCC-HVDC, the implementation of the control sequence of the presented ELCC-HVDC is more challenging. However, the operation principles and control strategy of ELCC-HVDC are not significantly more demanding. From Fig. 2, the operation modes of TFBM could be simply represented by charging mode, normal operation mode, and fault condition mode. According to different valve conducting state, capacitor voltage state, and fault state, the thyristors in TFBM can be readily controlled by preset logics.

C. Coordinated Control Strategy Between Thyristor Valve and Series-Connected TFBM

Under normal operation state, the TFBM can be controlled according to stages 1–4 of Fig. 2. Under fault condition, the schematic diagram of coordinated control strategy is shown in Fig. 3, and the equivalent commutation circuit of ELCC is given in Fig. 4. u_C is the capacitor voltage of TFBM, and $i_{\mathrm{VT}n}$ and $i_{\mathrm{VT}m}$ are the current of off-going valve and on-going valve, respectively.

As in Figs. 3 and 4, supposed that VT*n* and VT*m* will experience off-going and on-going period, respectively, after the fault occurring time t_{fault}, the detailed control procedures under fault condition are as follows. In Fig. 3, the fault is assumed to be cleared after t_3, and the period from t_3 to t_6 is at the normal operation stage. t_7 is the next fault occurring time instant.

1) *Stage 5 (t_1–t_2):* Trigger VTc in TFBM, VTa will be turned OFF and the capacitor will be charged reversely.
2) *Stage 6 (t_2–t_3):* Due to the reverse voltage of capacitor, both VTb and VTc will be turned OFF. With the additional commutation voltage support provided by TFBM, the successful commutation process from VTn to VTm could be much more achievable, which can also be seen from Fig. 4. When the forced commutation is successfully achieved, the thyristors in TFBM will be turned OFF, and thus, the capacitor voltage will be maintained at a constant value. If fault is not cleared, the similar forced commutation procedures will be carried out repeatedly. In addition, during the on-going process of VT*n*, the additional volt–time area can also be provided by another TFBM in corresponding off-going valve.
3) *Stage 1 (t_4–t_5):* After stage 6, VT*n* is turned OFF and the dc voltage of capacitor will have small drop due to power loss during t_3–t_4 period. At t_4, VT*n* will conduct, VTb and VTc in TFBM are triggered, and the capacitor will be charged to set value at t_5. Note that the capacitor has the opposite polarity compared with that in Fig. 2(1), thus VTb and VTc (not VTa and VTd) are triggered to charge the capacitor during this stage.
4) *Stage 2 (t_5–t_6):* Trigger VTd, then VTd will conduct and VTb will be turned OFF at t_6.
5) *Stage 3 (t_6–t_7):* VTc and VTd are fully conductive, and VTb is completely turned OFF after stage 2 is finished.
6) After t_7: If the fault occurs again, repeat the above procedures.

D. Control Strategy of ELCC-HVDC

If the presented ELCC of Fig. 1 is adopted as the inverter, and the conventional LCC as the rectifier, an ELCC-HVDC system with TFBM embedded in the inverter can be obtained. The most widely used control strategy for conventional LCC-HVDC could also be utilized for the ELCC-HVDC. Thus, constant dc current control and minimized firing angle control are implemented at the rectifier side, and constant extinction angle at the inverter side [20].

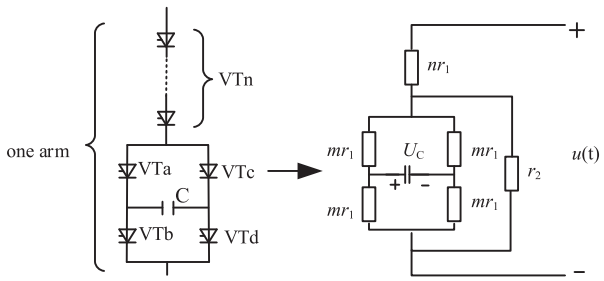

Fig. 5. Equivalent circuit when VT*n* is turned OFF.

III. Investigation of TFBM

A. Voltage–Current Stresses of TFBM

1) Voltage Stress of TFBM: When VT*n* is conductive, it can be easily obtained that the peak voltage of thyristors in TFBM is U_C based on Fig. 2. When VT*n* is turned OFF, an equivalent circuit of Fig. 5 is given to analyze the voltage stress of TFBM where

u(*t*): line-to-line voltage across the valve arm;

m: the number of series-connected thyristors in VT*i* of TFBM (*i* = a, b, c, d);

n: the number of series-connected thyristors in valve VT*n*;

U_C: capacitor voltage;

r_1: voltage balancing resistor for each thyristor in VT*n*;

r_2: voltage balancing resistor for each TFBM.

From Fig. 5, (1) can be deduced based on the superposition theorem as follows:

$$\begin{cases} U_{\mathrm{VTa}} = -\dfrac{1}{2}U_C + \dfrac{r_2'}{2\left(nr_1 + r_2'\right)}u\left(t\right), \\ U_{\mathrm{VTb}} = \dfrac{1}{2}U_C + \dfrac{r_2'}{2\left(nr_1 + r_2'\right)}u\left(t\right), \\ U_{\mathrm{VTc}} = \dfrac{1}{2}U_C + \dfrac{r_2'}{2\left(nr_1 + r_2'\right)}u\left(t\right), \\ U_{\mathrm{VTd}} = -\dfrac{1}{2}U_C + \dfrac{r_2'}{2\left(nr_1 + r_2'\right)}u\left(t\right), \end{cases} \tag{1}$$

where $r_2' = \frac{mr_1r_2}{mr_1+r_2}$ and $U_{\mathrm{VT}i}$ is the voltage of VT*i* in TFBM (*i* = a, b, c, d). According to the analysis above, the peak value U_{VTmax} is given by

$$U_{\mathrm{VTmax}} = \max\left\{U_C, \frac{1}{2}U_C + \frac{r_2'}{2\left(nr_1 + r_2'\right)}u\left(t\right)\right\}. \tag{2}$$

From (2), the peak value U_{VTmax} is affected by resistors r_1, r_2, and the number of series-connected thyristors *n* and *m*. If r_1, r_2, *n*, and *m* are properly selected, the peak value U_{VTmax} could be kept equal or lower than the capacitor voltage U_C. One specified case is given to further investigate the voltage/current stresses of TFBM in Section IV-B1.c.

2) Current Stress of TFBM: As seen from Fig. 1, TFBM is in series with the thyristors in each arm, thus the same arm current will flow over the thyristors in TFBM, and the peak current value will be the instantaneous fault current. Therefore, the current rating of the arm-thyristor could be the guide for that in TFBM.

B. Capacitor Parameter Selection

When the fault occurs, the embedded TFBM operates in stage 5 for a very short time, then transits to stage 6. The equivalent commutation circuit of ELCC in stage 6 is shown in Fig. 4. The variables $i_{\mathrm{VT}n}$ and $i_{\mathrm{VT}m}$ are the current of off-going valve and on-going valve, respectively.

From Fig. 4, the following equation can be deduced:

$$L_r\frac{di_{\mathrm{VT}m}}{dt} - L_r\frac{di_{\mathrm{VT}n}}{dt} = u\left(t\right) + u_C\left(t\right). \tag{3}$$

According to Kirchhoff's current law

$$i_{\mathrm{VT}m}\left(t\right) + i_{\mathrm{VT}n}\left(t\right) = I_d. \tag{4}$$

Assuming I_d is constant, substituting for (3) from (4)

$$-2L_r\frac{di_{\mathrm{VT}n}}{dt} = u\left(t\right) + u_C\left(t\right) \tag{5}$$

where

$$i_{\mathrm{VT}n}\left(t\right) = C\frac{du_C\left(t\right)}{dt}. \tag{6}$$

Assuming *u*(*t*) is the commutation voltage, and initial time instant is at the beginning of the commutation process, then

$$u\left(t\right) = u_b\left(t\right) - u_a\left(t\right) = U\sin\left(\omega t + \alpha\right) \tag{7}$$

where *U* is peak line-to-line voltage, α is the firing delay angle, and ω is angular frequency. Substituting for (5) from (6) and (7)

$$-2L_rC\frac{d^2u_C\left(t\right)}{dt^2} - u_C\left(t\right) = U\sin\left(\omega t + \alpha\right). \tag{8}$$

By employing Laplace transformation, one can deduce

$$\begin{aligned} -2LC\left[s^2U_C\left(s\right) - sU_C\left(0^-\right) - U_C'\left(0^-\right)\right] - U_C\left(s\right) \\ = U\frac{s\sin\alpha + \omega\cos\alpha}{\left(s^2+\omega^2\right)}. \end{aligned} \tag{9}$$

Then

$$U_C\left(s\right) = \frac{U\frac{s\sin\alpha+\omega\cos\alpha}{s^2+\omega^2} - 2LCU_C'\left(0^-\right) - s2LCU_C\left(0^-\right)}{-2LCs^2 - 1}. \tag{10}$$

The initial current value of capacitor can be considered as I_d due to a very short period in stage 5, then

$$CU_C'\left(0^-\right) = I_d. \tag{11}$$

If the initial capacitor voltage happens to be zero after stage 5, the capacitor most probably will be charged to its rated value U_{CN}, which is considered as the most serious scenario to calculate the capacitor size. Thus, the most conservative parameter could be obtained if considering the initial capacitor voltage

$$U_C\left(0^-\right) = 0. \tag{12}$$

Substituting for (10) from (11) and (12)

$$U_C\left(s\right) = \frac{U\frac{s\sin\alpha+\omega\cos\alpha}{s^2+\omega^2} - 2LI_d}{-2LCs^2 - 1}. \tag{13}$$

TABLE I
SYSTEM PARAMETERS

Items	Rectifier side	Inverter side
AC system voltage	345 kV	230 kV
SCR	2.5 at 84°	2.5 at 75°
Transformer ratio	345/213.46	230/209.23
Leakage inductance	0.18 p.u.	0.18 p.u.
DC resistor	5 Ω	
DC inductor	1.1936 H	

Then, the capacitor voltage can be finally obtained as

$$u_C(t) = -\frac{U\sin\alpha}{2L_rC}\left[\frac{2L_rC}{2L_rC\omega^2-1}\cos\frac{1}{\sqrt{2L_rC}}t+\frac{2L_rC}{1-2L_rC\omega^2}\cdot\cos\omega t\right]-\frac{U\cos\alpha}{2L_rC}\cdot\left[\frac{\omega 2L_rC\sqrt{2L_rC}}{2L_rC\omega^2-1}\sin\frac{1}{\sqrt{2L_rC}}t+\frac{2L_rC}{1-2L_rC\omega^2}\sin\omega t\right]+\frac{I_d}{C}\sqrt{2L_rC}\sin\frac{1}{\sqrt{2L_rC}}t. \quad (14)$$

Since at the very beginning of the commutation process is considered as the initial moment of (8), if t is the time interval of overlap angle μ, the corresponding value of $u_c(t)$ would be the additional maximum commutation voltage supported by TFBM. To improve the commutation process of ELCC-HVDC under fault condition, and make it behave like a normal commutation process, the capacitor parameter could be chosen according to the normal operation performances of ELCC-HVDC. An example is given after Table I in Section IV.

IV. SIMULATION STUDY

A. System Parameters

The ELCC-HVDC system is developed based on the CIGRE benchmark model [20]. The rated dc voltage and power are 500 kV and 1000 MW, and the other parameters are shown in Table I.

For the studied case, under the normal operation condition $U = 209.23\sqrt{2}$, $L = 0.18$ per unit(p.u.), $\alpha = 142°$, $\gamma = 15°$, $\mu = 23°$, and the time interval of μ will be 1.278 ms. Considering about 15% of rms value of line-to-line commutation voltage as the additional maximum commutation voltage support, the rated dc voltage $U_{\rm CN}$ of capacitor in each TFBM is chosen as 30 kV, and the set value $U_{C\rm set}$ of capacitor during the charging process is set to 20 kV. It should be noted that two major aspects should be considered for $U_{C\rm set}$ determination. One is $U_{C\rm set}$ should be high enough (not higher than the rated value $U_{\rm CN}$) to make sure VTa turn off quickly after fault occurs; the other one is $U_{C\rm set}$ should not be too high to facilitate the polarity reversal of capacitor, which is helpful for the first forced-commutation procedure. $U_{C\rm set}$ has an important impact on the first forced-commutation procedure after fault occurs, but has relatively small impact on the subsequent forced-commutation procedures during the fault condition. In this case, 50–80% of rated capacitor voltage $U_{\rm CN}$ is recommended as the value of $U_{C\rm set}$, and finally 20 kV of $U_{C\rm set}$ is chosen. If an optimized value of $U_{C\rm set}$ is required, the switching characteristics of thyristor and equivalent circuit of forced commutation process should be considered in the deduction procedures.

Based on (14), the capacitor value can be obtained, i.e., $C \approx 30\ \mu$F. The calculation method is obtained based on one TFBM embedded in each arm, if more than one TFBM inserted into each arm, the same calculation procedure can also be adopted.

As discussed in Section II, VTa (VTb, VTc, or VTd) in TFBM could be a module with a few thyristors in series. Based on the widely used thyristors parameters in practical application and the voltage stress analysis in Section III, each of VTa–VTd in one TFBM is composed of eight thyristors in series if 4 kV is considered as the allowable steady-state dc voltage across each thyristor. The fault detection delay of 1 ms is considered here for the case study.

B. Investigation on CF Mitigation of ELCC-HVDC

To investigate the presented ELCC-HVDC, the dynamics of single-infeed ELCC-HVDC and dual-infeed HVDC are studied under single-phase and three-phase to ground fault conditions.

1) Dynamic Performance of Single-Infeed ELCC-HVDC Under Single-Phase Fault Condition:

a) Dynamic performances comparison of ELCC-HVDC, CCC-HVDC, and LCC-HVDC: In this section, the CF mitigation effects are compared in detail among presented ELCC-HVDC, existing CCC-HVDC, and LCC-HVDC. CCC-HVDC and CSCC-HVDC have similar performances for steady state as well as transient conditions [15]. Thus, only CCC-HVDC is considered here.

The ELCC-HVDC and CCC-HVDC are developed based on the CIGRE Benchmark model, and both systems have the same steady-state operating state compared to the LCC-HVDC benchmark model. In ELCC-HVDC, one TFBM is embedded in each arm of inverter, and the additional maximum commutation voltage support of 30 kV is selected. To make CCC-HVDC own similar commutation voltage support by capacitors between converter and transformer, the maximum capacitor voltage of CCC-HVDC at steady state is selected at 15 kV, due to two capacitors involving in the commutation circuit during every commutation period.

For dynamic performances comparison, an inductive single phase to ground fault, with 0.5 H inductance grounded, is applied at the receiving ac busbar of ELCC-HVDC, CCC-HVDC, and LCC-HVDC, respectively. The faults occur at 1 s and last for 50 ms. The simulation results are shown in Fig. 6.

Fig. 6(a)–(f) are the comparison results of ELCC-HVDC, CCC-HVDC, and LCC-HVDC. When the fault occurs, only LCC-HVDC experiences CF, as seen from Fig. 6(d). Then, the dc voltage of LCC at inverter side drops close to 0.2 p.u., and the dc current increases suddenly as depicted in Fig. 6(a). The maximum power loss in LCC-HVDC is about 0.9 p.u.

As for CCC-HVDC, CF is mitigated and dc current does not show a big increase. However, the dc voltage drops to 0.6 p.u., leading to the maximum power loss of 0.5 p.u. In addition, from Fig. 6(c), CCC-HVDC even requires longer fault recovery time to get back to its prefault power level compared

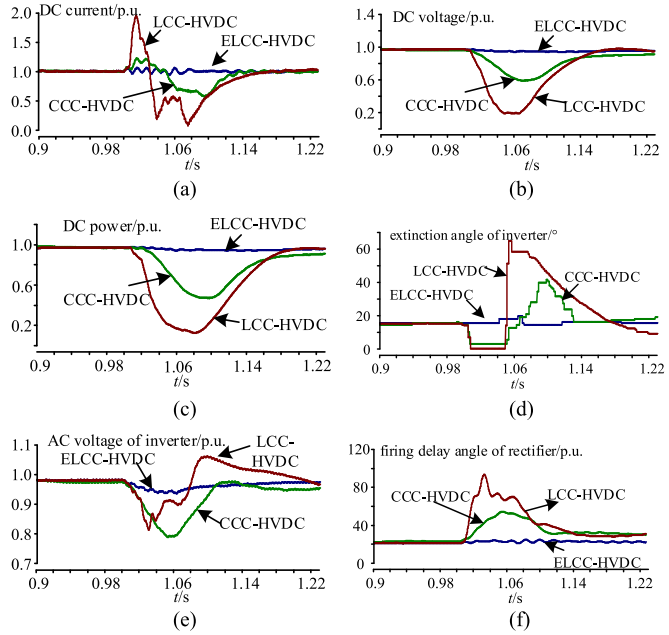

Fig. 6. Dynamic performances comparison of ELCC-HVDC, CCC-HVDC, and LCC-HVDC under single-phase fault. (a) DC current. (b) DC voltage. (c) DC power. (d) Extinction angle. (e) AC voltage of inverter. (f) Firing delay angle of rectifier.

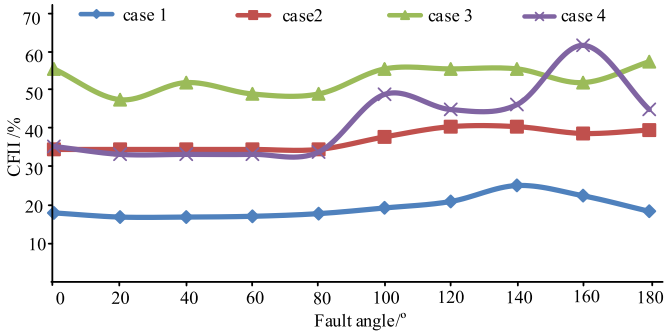

Fig. 7. CFII values comparison under single-phase fault.

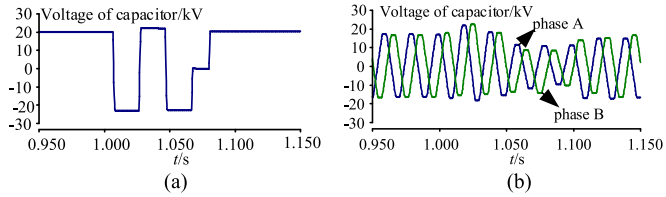

Fig. 8. Capacitor voltages when no CFs happen in both ELCC and CCC. (a) Capacitor voltage of ELCC. (b) Capacitor voltage of CCC.

with LCC-HVDC. The reason is addressed in [16], which states that unbalanced disturbances leave the capacitors incorrectly charged, and to resume normal operation, the capacitors have to exchange the stored energy with the network.

When the same fault occurs at the inverter ac busbar of ELCC-HVDC, the more favorable dynamic performances are shown. Fig. 6(d) shows that no CF occurs. The ac voltage of receiving system, dc voltage, dc current, and active power show slight fluctuations, and can be maintained around the rated values. From the analysis above, with TFBM in series, CFs of ELCC-HVDC are effectively mitigated and the fault recovery performances greatly improved.

b) CF immunity comparison: To evaluate the susceptibility of the presented ELCC converter to CFs, the commutation failure immunity index (CFII) is adopted here, which is defined as [21]

$$\mathrm{CFII} = \frac{V_{\mathrm{ac}}^2}{\omega \cdot L_{\min} \cdot P_{\mathrm{dc}}} \cdot 100 \tag{15}$$

where $L_{\min}$ is the critical inductance which is determined by conducting a sequence of EMT simulations, and P_d is the dc power of the converter. From (15), the larger CFII value represents stronger immunity of the LCC inverter to CF.

To further study the presented ELCC, the CFII values of four cases are compared under single-phase fault:

Case 1: LCC-HVDC (CIGRE Benchmark model)
Case 2: ELCC-HVDC with one TFBM
Case 3: ELCC-HVDC with three TFBMs
Case 4: CCC-HVDC.

Fig. 7 shows the CFII curves of four cases. Here, the fault angle is defined as the angle interval between fault occurring time and the reference point (the zero crossing point from negative to positive of phase A voltage). The fault angle varies from 0° to 180° with a 10° step, and the fault lasts 50 ms.

From Fig. 7, when single phase to ground fault occurs, ELCC-HVDC (case 2 or case 3) and CCC-HVDC can get much larger CFII values than LCC-HVDC (see case 1). Thus, with TFBM embedded in the converter arm, a noticeable higher immunity to CFs is obtained. In addition, due to three TFBMs inserted in case 3, the ELCC-HVDC could provide more volt–time area during the commutation process, and then provide larger CFII values than case 2.

It is also seen from Fig. 7, CCC-HVDC (see case 4) exhibits larger CFII values than ELCC-HVDC with one TFBM (see case 2). The reason is that the larger volt–time area is obtained from capacitors in CCC-HVDC due to uncontrolled capacitor charge under fault conditions, which will lead to unexpected overvoltage on capacitors. Thus, larger CFII values are obtained in CCC-HVDC at the expense of overvoltage risk of capacitor. However, CFs can also be effectively mitigated by embedded TFBM in ELCC-HVDC, and capacitor voltage can still be readily controlled within its allowable range by TFBM under fault condition. To clarify this point, capacitor voltages of ELCC-HVDC and CCC-HVDC under different fault levels are further compared in two scenarios.

Scenario 1: Same fault condition (0.5 H inductive single phase to ground fault) as in Section IV-B1.a, both ELCC-HVDC and CCC-HVDC do not experience CFs. The capacitor voltages are shown in Fig. 8.

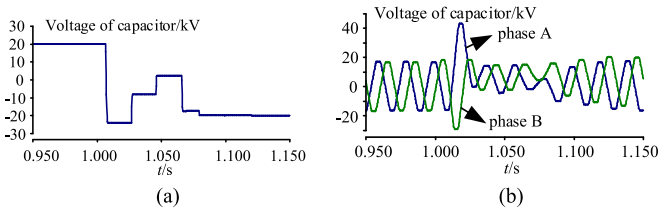

Fig. 9. Capacitor voltages when both ELCC and CCC experience CFs. (a) Capacitor voltage of ELCC. (b) Capacitor voltage of CCC.

Scenario 2: 0.3 H inductive single-phase to ground fault, both ELCC-HVDC and CCC-HVDC experience CFs. The capacitor voltages are shown in Fig. 9.

From Fig. 8, the capacitors in CCC-HVDC continuously provide the commutation support at normal operating condition, and the capacitor voltages are maintained within their allowable value of 15 kV. However, the maximum capacitor voltage reaches to 26.5 kV (176% of rated value) under fault condition, which could be a risk for CCC-HVDC. Due to the uncontrolled capacitor charging, more additional commutation supports are obtained from capacitors in CCC-HVDC under fault condition, which leads to larger CFII values as shown in Fig. 7. However, the capacitor voltage in ELCC-HVDC is always maintained within its rated value of 30 kV under fault conditions in Fig. 8.

From Fig. 9, ELCC-HVDC and CCC-HVDC both experience CFs under serious fault condition. However, the capacitor voltage of ELCC-HVDC still can be maintained within its allowable range, while the maximum capacitor voltage of CCC-HVDC almost reaches to three times of its rated value due to uncontrolled charging process.

c) Voltage–current stress of TFBM: The parameters of ELCC-HVDC are the same as those of Section IV-B1.a, and one TFBM is embedded, and each of VTa–VTd in one TFBM is composed of eight thyristors ($m = 8$) in series, considering 4 kV as the allowable steady-state dc voltage across each thyristor. Here, the value of r_2 is set to mr_1, i.e., $r_2 = mr_1$. Substitute $m = 8$ and $r_2 = mr_1$ into (1) and (2), then the conclusion can be obtained that the maximum voltage across VTi (i = a, b, c, d) will be smaller than the rated capacitor voltage of 30 kV when n (the number of series-connected thyristors in each arm) is larger than 36. In practical ±500-kV LCC-HVDC case, the number of series-connected thyristors is much larger than 36, thus the voltage stress across thyristor in TFBM of ELCC-HVDC could be certainly maintained within allowable operation range.

To further justify the above analysis, the voltage–current stress of TFBM is studied under two scenarios (same scenarios with that in Section IV-B1.b): 1) single-phase fault with 0.5 H grounded, under which no CF happens; 2) single-phase fault with 0.3 H grounded, under which CF happens. Both faults are applied at 1 s, and last 50 ms. The current and voltage stress results of TFBM are shown in Figs. 10 and 11, respectively.

From Fig. 10(a), the ELCC does not experience CF under scenario 1 and the peak current flowing over thyristors in TFBM is close to rated dc current of 2 kA. From Fig. 11(a), the maximum capacitor voltage in TFBM is close to 24 kV, and the maximum voltage across each thyristor in VTa–VTd of TFBM, under fault

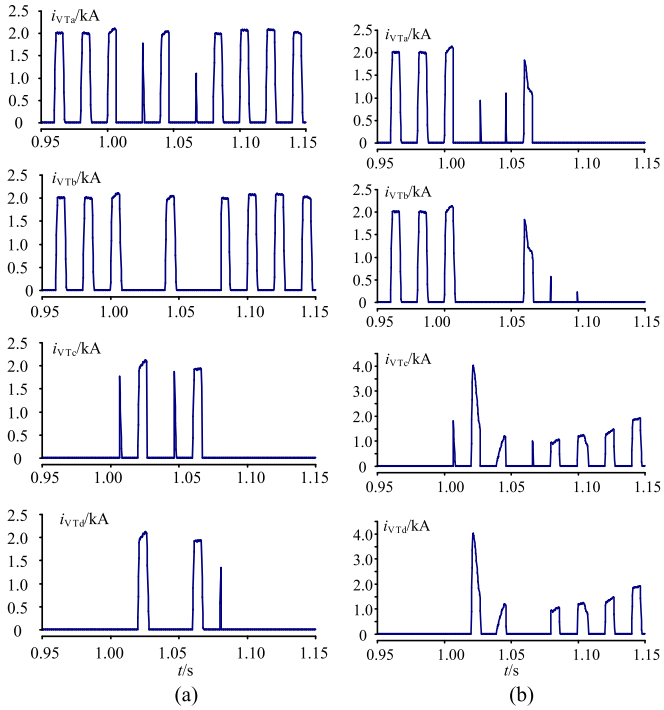

Fig. 10. Current stress of TFBM. (a) 0.5 H inductive single-phase fault. (b) 0.3 H inductive single-phase fault.

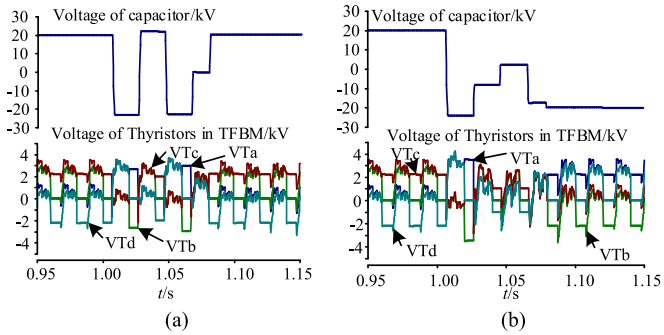

Fig. 11. Voltage stress of TFBM. (a) 0.5 H inductive single-phase fault. (b) 0.3 H inductive single-phase fault.

condition, is about 3.8 kV, which is smaller than its allowable value of 4 kV.

From Fig. 10(b), the ELCC experiences the CF under scenario 2, the maximum overcurrent flowing over thyristors in TFBM is about 4 kA. After fault is cleared, no overcurrent is observed, and with the presented control method, the peak voltage of capacitor is about 25 kV, which is smaller than its rated voltage 30 kV. From Fig. 11(b), even if CF is not effectively mitigated, the peak voltage of each thyristor in TFBM is about 4 kV, which is also within its allowable range.

From Figs. 10, Fig. 11, and the analysis above, the voltage–current stress of TFBM could be maintained within allowable range by proper selection of system parameters. The voltage–current stress of TFBM under three-phase fault condition is also investigated and the similar results could also be

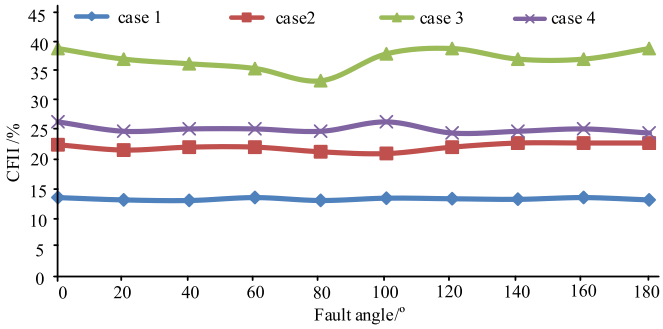

Fig. 12. CFII values comparison under three-phase fault.

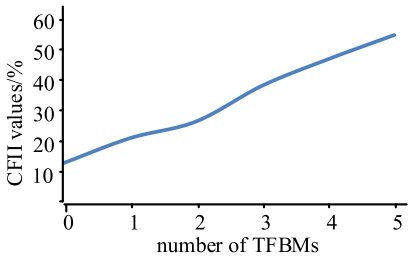

Fig. 13. Relationship between CFII and number of TFBM.

obtained, which will not be shown in this paper due to limited space.

2) CF Immunity of ELCC-HVDC Under Three-Phase Fault:

a) CFII Comparison of ELCC-HVDC, CCC-HVDC, and LCC-HVDC: To further study the presented ELCC, the CFII values of four cases are compared under three-phase fault:

Case 1: LCC-HVDC (CIGRE Benchmark model).
Case 2: ELCC-HVDC with one TFBM.
Case 3: ELCC-HVDC with three TFBMs.
Case 4: CCC-HVDC.

The CFII results are shown in Fig. 12. From Fig. 12, the ELCC-HVDC in case 2 or case 3 and CCC-HVDC are also less susceptible to CFs than that in case 1. With three TFBMs inserted in case 3, much larger CFII values are also obtained. It is also seen from Fig. 12, CCC-HVDC (see case 4) gets larger CFII values than ELCC-HVDC with one TFBM (see case 2). The reason is similar as that under single-phase fault condition.

b) Relationship between CFII values and number of TFBM: From the CFII results above, it can be seen that the presented ELCC-HVDC could get larger CFII values with increasing numbers of embedded TFBMs. For further study, the CFII curve versus number of TFBMs is given in Fig. 13. The results match with that in Figs. 7 and 12. With increasing number of TFBMs, the ELCC-HVDC will provide more support for commutation process, and then get much larger CFII values.

From Sections IV-B1 and IV-B2, under single-phase and three-phase to ground fault, LCC-HVDC may experience CF; however, CCC-HVDC and ELCC-HVDC have the ability to improve the CF immunity resulting in higher CFII values.

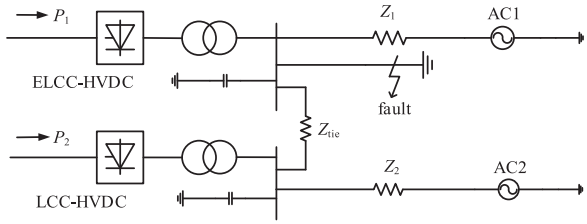

Fig. 14. Dual-infeed HVDC system with one ELCC-HVDC link.

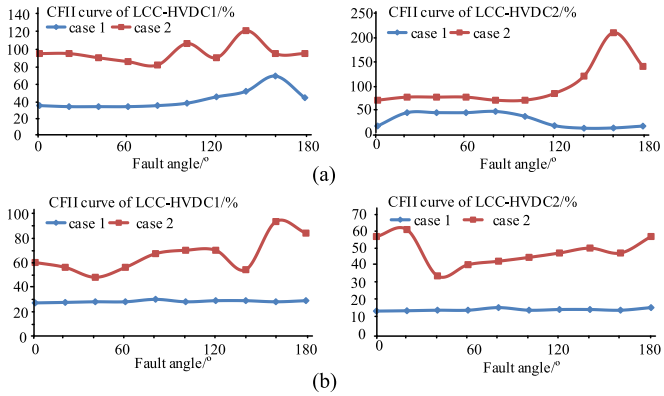

Fig. 15. Comparison of CFII values in dual-infeed HVDC with or without ELCC-HVDC link. (a) Single-phase fault. (b) Three-phase fault.

Although CCC-HVDC can mitigate the CF under fault condition, it may experience bigger power loss and require longer recovery time after fault is cleared, especially under unbalanced fault condition. In addition, the uncontrolled capacitor charge process of CCC-HVDC could lead to the unexpected overvoltage of capacitors. However, ELCC-HVDC has the capability to flexibly control the embedded TFBM, effectively mitigate the CF, and also presents satisfactory transient responses under fault condition.

3) Dynamic Performance of Dual-Infeed HVDC With One ELCC-HVDC Link: To further evaluate the effectiveness of the proposed ELCC, a dual-infeed HVDC system is developed in PSCAD/EMTDC, as shown in Fig. 14. In Fig. 14, the ELCC-HVDC1 with one TFBM embedded in each arm is rated at 500 kV and 1000 MW, and has the same system parameter as the study system in Section IV-A. LCC-HVDC2 is rated at 500 kV and 2000 MW.

In this section, the dynamic performances of two cases are compared:

Case1: Dual-infeed HVDC with two LCC-HVDC links (LCC-HVDC1 is 500 kV/1000 MW and LCC-HVDC2 is 500 kV/2000 M).
Case 2: Dual-infeed HVDC with one ELCC-HVDC link, as shown in Fig. 14.

The CFII curves of dual-infeed HVDC system in two cases, under single-phase and three-phase to ground faults at inverter ac busbar of 1000-MW HVDC link, are obtained, and the results are shown in Fig. 15.

From Fig. 15, the CFII curves marked in red (see case 2) are much larger than that marked in blue (see case 1). Thus, the CFs risks of both local HVDC and remote one are reduced effectively in dual-infeed HVDC with one ELCC-HVDC link. It can be concluded that the ELCC-HVDC with presented control strategy has the ability to improve the commutation process and mitigate the CFs, and it can also potentially strength the CF immunity of adjacent HVDC links.

C. Discussion of the Increased Cost and Power Loss

As described in Section IV-A, one TFBM is embedded, and the additional maximum commutation voltage support is chosen as 30 kV, which is about 15% of rms value or 10.6% of peak value of line-to-line commutation voltage. From the operation principle of TFBM in Section II-B, only two arms (VTa and VTb/VTc and VTd) in TFBM participate in the normal operation, thus the extra cost of ELCC-HVDC is mainly subject to the other two arms and capacitors. Considering that the number of series-connected thyristors is proportional to the peak value of line-to-line commutation voltage, the increased thyristors cost, based on the original valve group cost, is $0.106 * 2 = 0.212$. As for the conventional LCC-HVDC, the valve groups cost accounts for about 25% of the total capital cost [22]. Thus, the valve group cost of ELCC-HVDC increases to $0.25 * (1 + 0.212) = 0.303$. To simplify the cost calculation, the capacitor cost in TFBM can be conservatively estimated as 5% of valve group cost, then the total cost of converter valve group will increase to $0.303 \bullet 1.05 = 0.318$. Finally, the total increased capital cost of ELCC-HVDC can be obtained as $0.318 - 0.25 = 0.068$ (6.8%). Considering the greatly improved CF mitigation ability, and satisfactory steady-state and fault recovery performances, the increased capital cost of 6.8% for ELCC-HVDC is potentially acceptable.

From Section II, under normal operation condition, VTa/VTb and VTc/VTd in TFBM of Fig. 1(b) can be inserted into the series-connected arm in turn. For example, if VTa/VTb is inserted into the series-connected arm at first circle (20 ms for 50 Hz), VTc/VTd will be inserted into the arm at next circle. In addition, the power losses of capacitor unit could be smaller than 0.2 W/kvar [23], which is reasonably negligible compared with thyristor losses. Thus, although the TFBM is embedded, the ELCC-HVDC almost has the similar power loss and efficiency compared to the conventional LCC-HVDC under normal operating state.

V. Conclusion

In this paper, an ELCC-HVDC with TFBM embedded is proposed, and the coordinated control strategy is presented. Then, the voltage–current stress of the TFBM is analyzed, and the method to select the capacitor parameter is given. To validate the CF mitigation effect, ELCC-HVDC, CCC-HVDC, and LCC-HVDC are developed in PSCAD/EMTDC, and the dynamics under single-phase and three-phase to ground faults at the inverter ac busbar among three different HVDC configurations are compared in detail. In addition, the increased capital cost and power loss of the presented ELCC-HVDC is discussed. From the results, the following conclusions can be obtained.

1) Compared with CCC-HVDC and LCC-HVDC, the presented ELCC-HVDC exhibits flexibility in control, favorable CF mitigation effect, and satisfactory steady-state and fault recovery performances. As the number of TFBMs increases, the ELCC-HVDC has much stronger immunity to CF.
2) In dual-infeed HVDC with one ELCC-HVDC link, the CF risks of both local HVDC and remote one are reduced effectively under single-phase or three-phase fault conditions.
3) Considering the greatly improved CF mitigation ability and favorable option in HVDC areas, the increased capital cost for ELCC-HVDC is potentially acceptable.

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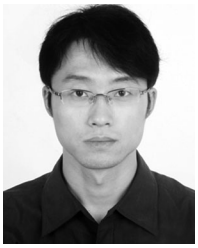

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