A Three-Phase Hybrid Cascaded Modular Multilevel Inverter for Renewable Energy Environment

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***Abstract*—This paper presents a three-phase hybrid cascaded modular multilevel inverter topology which is derived from the proposed modified H-bridge module. This topology results in the reduction of number of power switches, losses, installation area, voltage stress and converter cost. For renewable energy environment such as photovoltaic (PV) connected to the microgrid system, it enables the tranformerless operation and enhances the power quality. This multilevel inverter is an effective and efficient power electronic interface strategy for renewable energy systems. The basic operation of single module and the proposed cascaded hybrid topology is explained. The ability to operate in both symmetrical and asymmetrical modes is analyzed. The comparative analysis is done with classical cascaded H-bridge and flying capacitor multilevel inverters. The nearest level control method is employed to generate the gating signals for the power semiconductor switches. To verify the applicability and performance of the proposed structure in PV renewable energy environment, simulation results are carried out by MATLAB/Simulink under both steady-state and dynamic conditions. Experimental results are presented to validate the simulation results.**

***Index Terms*—Cascaded H-bridge (CHB), multilevel inverters (MLIs), renewable energy systems (RES), total harmonic distortion (THD).**

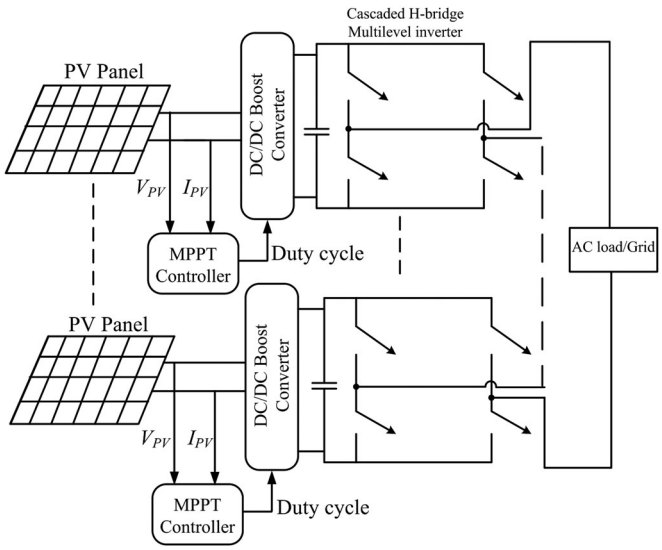

Fig. 1. Transformerless PV system equipped with MLI.

I. Introduction

In the current scenario, due to the environmental issues and limited fossil resources, the demand for renewable energy is increasing. To meet this growing demand, photovoltaic (PV), fuel cell and wind turbine systems have become the important integral part of grid-connected renewable energy systems (RES). Harnessing of electrical energy from the PV systems contributes to clean power generation. This contribution made it widespread in the current global climatic conditions. Long lasting, high efficiency and pollution-free power generation are the advantages of PV systems. The low output voltage PV arrays are connected in series to accomplish high voltage dc, and dc to ac inverter is used to interface with the grid. This approach needs high voltage-rated devices for the inverter. To overcome this issue, the step-up transformer is necessary. This system enables to use the low voltage-rated devices for inverter and then boosting the voltage by transformer. This may lead to increase in losses and cost of the system. Using transformerless concepts are beneficial in reducing cost, size, weight, and complexity of inverter besides enhancing the efficiency. A multilevel converter is the one which uses properly connected power semiconductor devices to several lower dc voltage sources to synthesize a near sinusoidal staircase voltage waveform. The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency. The era of multilevel inverters (MLIs) started with diode clamped MLI, also known as neutral point clamped, in 1981 [1], then capacitor-clamped MLI or flying capacitor (FC) in 1992 [2] and the cascade H-bridge (CHB) MLI in 1995. The different topology presented in the literature as multilevel converters [3], [4] possesses the number of characteristics, giving their clear advantages over bilevel converters. These advantages promote the MLIs as the suitable choice for grid-connected RES in both with and without transformer configurations. The adoption of MLIs results in reduction of cost and size of filtering requirements in transformerless PV system depicted in Fig. 1 [5]–[7]. Various MLI topologies for renewable energy applications are listed in [8]–[10]. The

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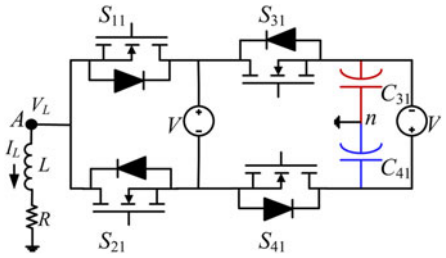

Fig. 2. MHB module of the proposed MLI.

TABLE I
SWITCHING STATES AND OUTPUT VOLTAGES OF MHB

L. No	S_{11}	S_{21}	S_{31}	S_{41}	C_{31}	C_{41}	V_L
1	1	0	0	1	↑	↓	$+3V/2$
2	0	1	0	1	↑	↓	$+V/2$
3	1	0	1	0	↓	↑	$-V/2$
4	0	1	1	0	↓	↑	$-3V/2$

↑-charge; ↓-discharge.

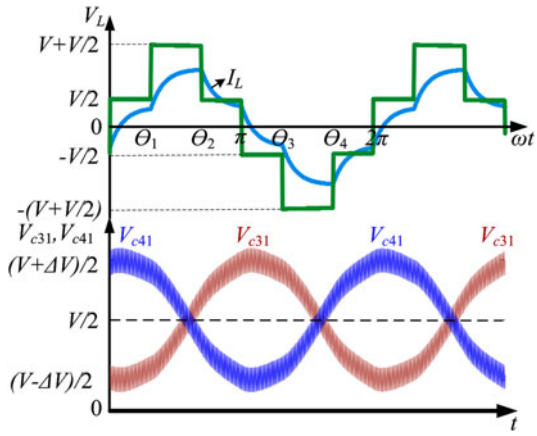

Fig. 3. Voltage, current waveforms of MHB module and self-balanced capacitor voltages.

complexity and requirement of high number of power switches are the main disadvantages associated with the multilevel configurations.

The reduction of semiconductor switches in the MLI topologies has lead to enormous significance in academia and the industry. The reduction in switches further reduces the number of components including gate drives. Eventually, the reduction in switch count improves the efficiency and minimizes the control complexity. Single-phase and three-phase MLI topologies are reported in [11] and [12] focusing on less switch count. Such single-phase topologies are simpler, but extending them to three phase make the configuration and control complex [13]–[17]. Three-phase topologies are developed focusing on reducing the complexity issue [18], [19]. The configuration of less switches and simpler structure for three phase is proposed in [20]. The switching loss is reduced by incorporating the hybrid control strategy [21]. The hybrid three-phase symmetrical [22], [23] and asymmetrical [24]–[26] configurations are developed. Single source hybrid three phase configurations are also reported, but they need complex control in connection with capacitor balancing [27], [28].

In this paper, cascaded hybrid modular structure is presented, keeping with the view aforementioned focal points of simpler in construction, less switch, less source requirement, and no capacitor balancing issues. Each module is constructed from a modified H-bridge (MHB). The proposed structure can be generalized by cascading the modules. The main advantages of this topology are modular in construction, usage of less power electronic switches of the same voltage rating and with less number of gate drive circuit requirement. The proposed MLI is tested by interfacing maximum power point tracking (MPPT) controlled PV RES with low switching frequency nearest level control (NLC) technique.

II. PROPOSED MODEL

The proposed hybrid cascaded modular (HCM) MLI is constructed from a MHB module and T-type three leg inverter structure (TTL).

A. MHB Module

Each module is basically constructed from four unidirectional-blocking-bidirectional-conducting MOSFET power electronic switches S_{11}, S_{21}, S_{31}, and S_{41}. The modification of the CHB is as shown in Fig. 2. The switch pair in both arms (S_{11}, S_{21}) and (S_{31}, S_{41}) is complimentary in nature. It can produce four levels $+3V/2$, $+V/2$, $-V/2$, and $-3V/2$ with proper switching combinations listed in Table I.

Generally, each module requires three sources to produce the aforementioned levels in the output. This is not an effective approach to design each module of MLI to have more sources. In order to reduce one source, two capacitors and one dc source are employed [29]. The voltage balance between two capacitors is guaranteed by a charge balance control method [30]. To employ this control method, the switching states must have a redundancy. To avail the redundancy, the switch count may increase. The proposed MHB module has no redundancy in the switching states in one single module, and by the virtue of its structure, natural balancing of capacitors is enabled. To investigate this feature, consider the MHB module is connected to an inductive load as shown in Fig. 2.

The MHB module output voltage ν_L, current i_L and voltage across capacitors C_{31} and C_{41} waveforms are shown in Fig. 3. The voltage and current waveforms are identical in both the positive and negative half cycles. Therefore, both the current and voltage waveforms in the positive half-cycle interval 0 to θ_1 are a replica of the negative half-cycle interval π to θ_3. Likewise, the current and voltage waveforms in the positive half-cycle interval θ_1 to π are identical with the interval θ_4 to 2π. It can also be concluded that V_{c31} and V_{c41} are tightly balanced despite the small ripple $\Delta V/2$. Accordingly, the average powers in aforementioned intervals in each half cycle are equal and

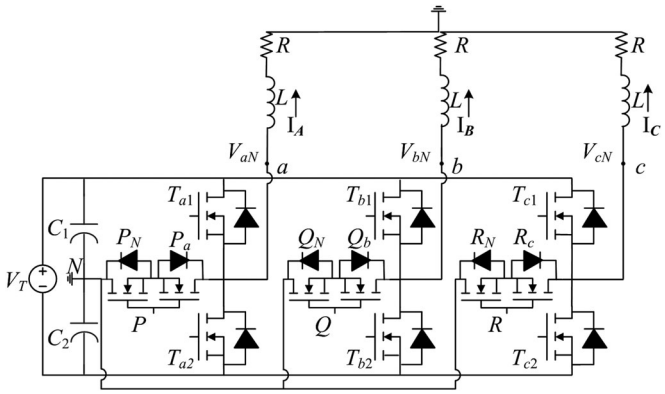

Fig. 4. TTL inverter structure.

TABLE II
SWITCHING STATES AND OUTPUT VOLTAGES OF TTL INVERTER

L. No.	T_{a1}	T_{a2}	P	T_{b1}	T_{b2}	Q	T_{c1}	T_{c2}	R	$V_{a,b,cN}$
1	1	0	0	1	0	0	1	0	0	$+V/2$
2	0	0	1	0	0	1	0	0	1	0
3	0	1	0	0	1	0	0	1	0	$-V/2$

mathematically expressed as

$$\int_0^{\theta_1} [i_L(t)\nu_L(t)]d(\omega t) = \int_{\pi}^{\theta_3} i_L(t)\nu_L(t)d(\omega t)$$
$$\int_{\theta_2}^{\pi} [i_L(t)\nu_L(t)]d(\omega t) = \int_{\theta_4}^{2\pi} i_L(t)\nu_L(t)d(\omega t). \quad (1)$$

B. TTL Inverter Structure

The TTL inverter structure consists of six unidirectional switches $(T_{a1}, T_{a2}), (T_{b1}, Tb_2)$, and (T_{c1}, T_{c2}) in the respective phases *a*, *b*, and *c*. In addition, the structure is incorporated with three bidirectional switches *P, Q*, and *R*, which are formed by back-to-back configuration of two switches $(P_N, P_a), (Q_N, Q_b)$ and (R_N, R_c), with a single gating signal control as shown in Fig. 4. The dc-link voltage is provided by two naturally balanced capacitors C_1 and C_2 connected across one source V_T. This inverter structure in each phase can produce three voltage levels: 0, *V*/2, and $-V/2$ with switching combinations listed in Table II.

C. Proposed Hybrid Modular Inverter Structure

By combining the two structures MHB and TTL inverters, the hybrid modular MLI is developed as shown in Fig. 5. This hybrid modular inverter structure in each phase can produce nine voltage levels: 2*V*, 3*V*/2, *V*, *V*/2, 0, $-V/2$, $-V$, $-3V/2$, $-2V$ in symmetrical mode. The synthesized output voltage and the corresponding state of the switches for phase "*A*" are summarized in Table III. The switching table for the other two phases is the same, but their switching instants are 120° and 240° apart from phase "*A*," respectively. This topology can easily be extended to any desired level "*L*" by just cascading the MHB modules in each phase as illustrated in Fig. 6. This modularity in construction feature facilitates the renewable system planning.

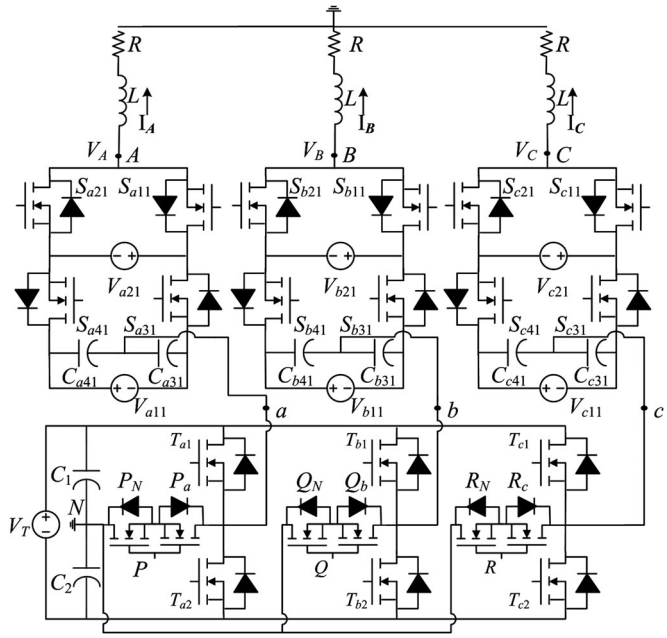

Fig. 5. Proposed three-phase nine-level hybrid modular MLI.

TABLE III
SWITCHING STATES AND OUTPUT VOLTAGES OF THE PROPOSED SYMMETRICAL NINE-LEVEL MLI

L. NO.	S_{a11}	S_{a21}	S_{a31}	S_{a41}	T_{a1}	T_{a2}	P	V_A
1	1	0	0	1	1	0	0	$+2V$
2	1	0	0	1	0	0	1	$+3V/2$
3	1	0	0	1	0	1	0	$+V$
4	0	1	0	1	0	0	1	$+V/2$
5	1	0	1	0	1	0	0	0
6	1	0	1	0	0	0	1	$-V/2$
7	0	1	1	0	1	0	0	$-V$
8	0	1	1	0	0	0	1	$-3V/2$
9	0	1	1	0	0	1	0	$-2V$

III. OPERATING MODES

The feature of this proposed HCM MLI is its ability to operate in both symmetrical and asymmetrical modes. In this section, a mathematical analysis of various parameters is carried out for number of modules "*j*" connected in cascaded. These sets of mathematical expressions are helpful in comparative analysis to make it realizable.

A. Symmetrical Mode

In this mode, the magnitude of the dc voltage sources in each MHB module and that of TTL inverter are set at equal value

$$\left.\begin{aligned} V_{a11} = V_{a12} = \cdots = V_{a1j} \\ V_{a21} = V_{a22} = \cdots = V_{a2j} \end{aligned}\right\} = V \quad (2.a)$$

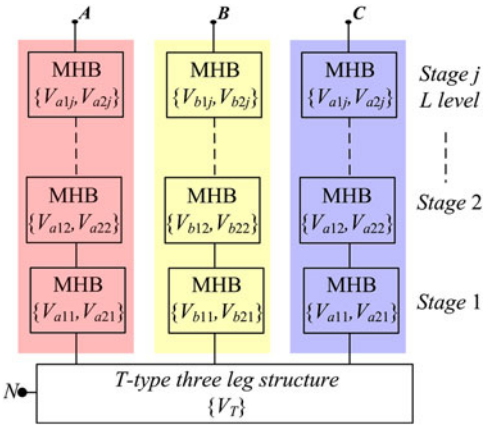

Fig. 6. Proposed three-phase *L*-level HCM MLI structure.

$$\left.\begin{aligned} V_{b11} &= V_{b12} = \cdots = V_{b1j} \\ V_{b21} &= V_{b22} = \cdots = V_{b2j} \end{aligned}\right\} = V \tag{2.b}$$

$$\left.\begin{aligned} V_{c11} &= V_{c12} = \cdots = V_{c1j} \\ V_{c21} &= V_{c22} = \cdots = V_{c2j} \end{aligned}\right\} = V \tag{2.c}$$

$$V_T = V. \tag{2.d}$$

The number of levels "*L*" generated per phase voltage is expressed as

$$L = 6j + 3. \tag{3}$$

The maximum value of phase voltage $V_{A,B,C}$ achieved in this mode is

$$V_{A,B,C,\max} = \frac{(1+3j)V}{2}. \tag{4}$$

The switch requirement (*S*) for the whole three-phase inverter is given as

$$S = 12(1+j). \tag{5}$$

The gate drive requirement (*G*) is expressed as

$$G = S - 3 = 9 + 12j. \tag{6}$$

The voltage blocking capability (*VBC*) is the voltage appears across the switch when the device is in off state, and can be expressed as follows for three-phase symmetrical operation.

For the TTL inverter structure, *VBC* for different switches is expressed as

$$\begin{aligned} T_{a,b,c,1} &= T_{a,b,c,2} = V \\ P &= Q = R = V \end{aligned} \tag{7}$$

$$VBC_{\mathrm{TTL}} = 9V. \tag{8}$$

For the MHB module inverter structure, *VBC* for different switches is expressed as

$$\left.\begin{aligned} S_{a11} &= S_{a12} = \cdots = S_{a1j} \\ S_{a21} &= S_{a22} = \cdots = S_{a2j} \end{aligned}\right\} = V$$

$$\left.\begin{aligned} S_{a31} &= S_{a32} = \cdots = S_{a3j} \\ S_{a41} &= S_{a42} = \cdots = S_{a4j} \end{aligned}\right\} = 2V \tag{9}$$

$$VBC_{\mathrm{MHB}} = 18jV \tag{10}$$

Total voltage blocking capability of inverter (VBC)

$$= VBC_{\mathrm{TTL}} + VBC_{\mathrm{MHB}} = (9 + 18j)V. \tag{11}$$

B. Asymmetrical Mode

Employing different dc voltages with proper ratios can improve the output voltage total harmonic distortion (THD) and hence the power quality. In this mode, the magnitudes of the dc voltage sources in each MHB module and that of TTL inverter are set at distinct values. This increases the level count "*L*" with the same switch "*S*" and gate drive "*G*" count. The three possible cases are analyzed in the following section.

Case 1: In this case, the magnitude of the dc voltage sources in each MHB module is set at equal value and that of TTL inverter is set at twice the value. Equations (2.a)–(2.c), (5), (6), (9), and (10) are the same as that of symmetrical mode. The other expressions (3), (4), (7), (8), and (11) are modified as

$$V_T = 2V \tag{12}$$

$$L = 4j + 1 \tag{13}$$

$$V_{A,B,C,\max} = \frac{(2+3j)V}{2} \tag{14}$$

$$\begin{aligned} T_{a,b,c,1} &= T_{a,b,c,2} = V \\ P &= Q = R = 2V \end{aligned} \tag{15}$$

$$VBC_{\mathrm{TTL}} = 18V \tag{16}$$

$$VBC = 18(1+\mathrm{j})V. \tag{17}$$

Case 2: In this case, the magnitude of the dc voltage sources in TTL inverter is set the same as in case 1 (12) and that of each MHB module is set as follows:

$$\left.\begin{aligned} V_{a11} &= V_{a12} = \cdots = V_{a1j} \\ V_{b11} &= V_{b12} = \cdots = V_{b1j} \\ V_{c11} &= V_{c12} = \cdots = V_{c1j} \end{aligned}\right\} = 2V \tag{18}$$

$$\left.\begin{aligned} V_{a21} &= V_{a22} = \cdots = V_{a2j} \\ V_{b21} &= V_{b22} = \cdots = V_{b2j} \\ V_{c21} &= V_{c22} = \cdots = V_{c2j} \end{aligned}\right\} = V. \tag{19}$$

Equations (5), (6), (15), and (16) are also valid for this case. The other expressions (3), (4), and (7)–(11) are modified as

$$L = 4j + 3 \tag{20}$$

$$V_{A,B,C,\max} = (1+2j)V. \tag{21}$$

For the MHB module inverter structure, *VBC* for different switches is expressed as

$$\left.\begin{aligned} S_{a11} &= S_{a12} = \cdots = S_{a1j} \\ S_{a21} &= S_{a22} = \cdots = S_{a2j} \end{aligned}\right\} = V$$

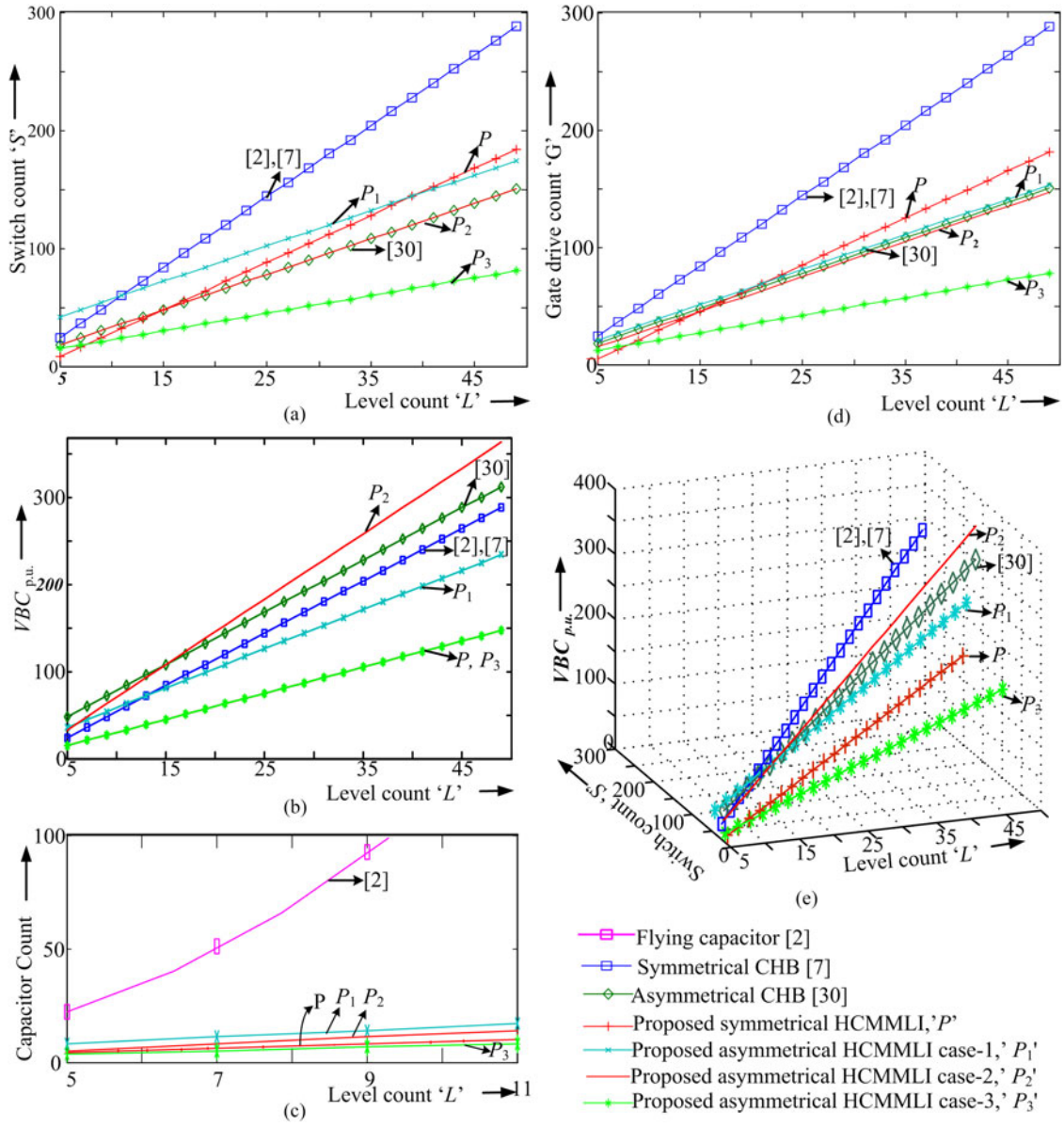

Fig. 7. Comparative analysis with CHB: (a) switch count "*S*," (b) voltage blocking capability "$VBC_{p.u}$", (c) capacitor count, (d) gate drive count "*G*" and (e) voltage blocking capability "$VBC_{p.u}$" and switch count "*S*", with level count "*L*".

$$\left.\begin{aligned} S_{a31} = S_{a32} = \cdots = S_{a3j} \\ S_{a41} = S_{a42} = \cdots = S_{a4j} \end{aligned}\right\} = 3V \tag{22}$$

$$VBC_{\mathrm{MHB}} = 24jV \tag{23}$$

$$VBC = VBC_{\mathrm{TTL}} + VBC_{\mathrm{MHB}} = (18 + 24j)V. \tag{24}$$

Case 3: In this case, the magnitudes of the dc voltage sources in each MHB module are set the same as in case 2 and that of TTL inverter is set the same as in symmetrical. Equations (2.d), (5), (6), (15), (16), (18), (19), (22), and (23) are also valid for this case. The other equations representing level count "*L*," maximum value in per phase voltage, and total *VBC* of inverter are given as follows:

$$L = 8j + 3 \text{ where } j = 2, 4, 6... \tag{25}$$

$$V_{A,B,C,\max} = \frac{(1 + 4j)V}{2} \tag{26}$$

$$VBC = (9 + 24j)V. \tag{27}$$

IV. Comparative Analysis

The comparative analysis of the proposed hybrid cascaded modular MLI (HCMMLI) has been carried out with classical CHB and FC as shown in Fig. 7(a)–(e). Various parameters are summarized in Table IV in terms of level count (*L*).

From Fig. 7(a) and (d), it is evident that the proposed HCMMLI has minimum switch count in asymmetrical mode case 3 "P_3" and also require minimum gate drive count. The capacitor requirement in FC increases more rapidly with *L* resulting in bulky and costly inverter structure, but less number of capacitors are sufficient in the case 3 of proposed asymmet-

TABLE IV
COMPARATIVE ANALYSIS WITH RESPECT TO LEVEL COUNT "*L*"

Parameter	CHB			HCMMLI			
	Symmetrical [7]	Asymmetrical [30]	FC [2]	Symmetrical (*P*)	Asymmetrical		
					P_1	P_2	P_3
Switch count	$6(L-1)$	$3(L+1)$	$6(L-1)$	$4L-12$	$3L+9$	$3(L+1)$	$3\left(\frac{L+5}{2}\right)$
Gate drive count	$6(L-1)$	$3(L+1)$	$6(L-1)$	$4L-15$	$3L+6$	$3L$	$3\left(\frac{L+3}{2}\right)$
VBC p.u.	$6(L-1)$	$3(2L+6)$	$6(L-1)$	$3L$	$9\left(\frac{L+3}{2}\right)$	$6L$	$3L$
Capacitor count	–	–	$(L-1)+3\left\{\sum_{k=1}^{L-1} L-1-k\right\}$	$L-1$	$\frac{3L+1}{2}$	$\frac{3L-5}{2}$	$\frac{3L-1}{4}$

TABLE V
SPECIFICATIONS OF SOLAREX MSX-60 PV MODULE (1 KW/M^2), 25 °C

Parameter	Values
Maximum power ($P_{\max}$)	60 W
Voltage at $P_{\max}$ ($V_{\rm mp}$)	17.1 V
Current at $P_{\max}$ ($I_{\rm mp}$)	3.5 A
Short-circuit current ($I_{\rm sc}$)	3.8 A
Open-circuit voltage ($V_{\rm oc}$)	21.1 V
Temperature coefficient of open-circuit voltage	−80 mV/°C
Temperature coefficient of short circuit current	0.065%/°C
Temperature coefficient of power	−0.5%/°C
No. of series cells	36
No. of parallel cells	1

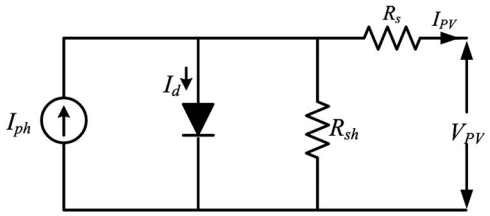

Fig. 8. Single diode model of PV cell.

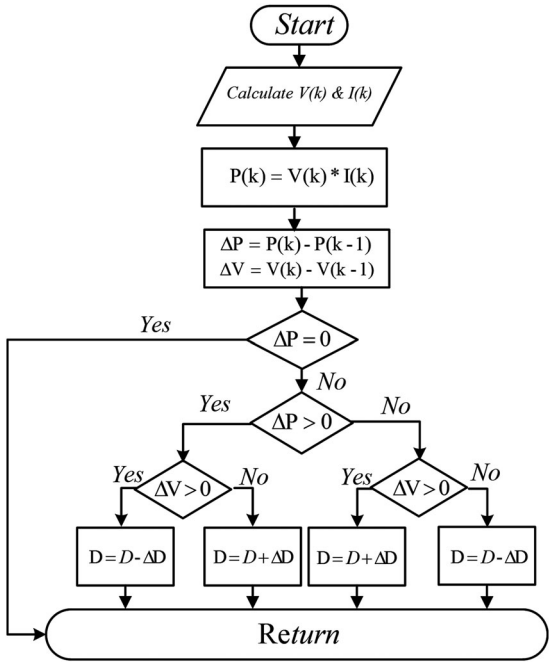

Fig. 9. Conventional perturb & observe MPPT algorithm.

rical mode depicted in Fig. 7(c). Fig. 7(e) shows the variation of $VBC_{p.u}$ and the switch count "*S*" with level count "*L*." It is seen that "P_3" of asymmetrical mode has the minimum $VBC_{p.u}$. and switch count "*S*" for the same level count "*L*." It can be concluded that the proposed HCMMLI has superior features compared to classical CHB. Asymmetrical mode case 3 "P_3" is preferable in view of more level count and less *VBC* and switch requirement. Tradeoff should be made between symmetrical and asymmetrical modes depending on the availability of energy sources of distinct magnitude.

V. MODELING OF PV CELL

PV panel directly converts solar energy into electricity in the form of dc with the help of PN junction. The quality of electricity directly depends on the solar intensity as well as the environmental conditions. It executes two nonlinear characteristics such as *P–V* curve and *I–V* curve. To extract the maximum energy from the PV source, a controller is required to monitor the dynamic behavior, accordingly maximum power point (MPP) is tracked and updated. The output voltage level of a PV panel may not always satisfy the desired value. Therefore, it is a good practice to connect a step-up dc/dc converter to fulfill the load requirement.

A PV panel can be mathematically build and simulated in software to observe the dynamic behavior by changing various parameters such as irradiance, temperature, etc. An algorithm is implemented for the tracking of maximum power by sensing the PV panel voltage $V_{\rm PV}$ and current $I_{\rm PV}$. To simulate the PV panel, the specifications shown in the Table V are taken from the SOLAREX MSX 60 datasheet [31].

The equivalent model of PV panel consists of photocurrent $I_{\rm ph}$, diode, a series resistor R_s, and a parallel resistor $R_{\rm sh}$ shown in Fig. 8 [32]. The key equation for *I–V* characteristic based on the single diode model is given by

$$I_{\rm PV} = I_{\rm ph} - \underbrace{I_o\left[\exp\left(\frac{V_{\rm PV}+I_{\rm PV}R_s}{V_t a}-1\right)\right]}_{I_d}$$

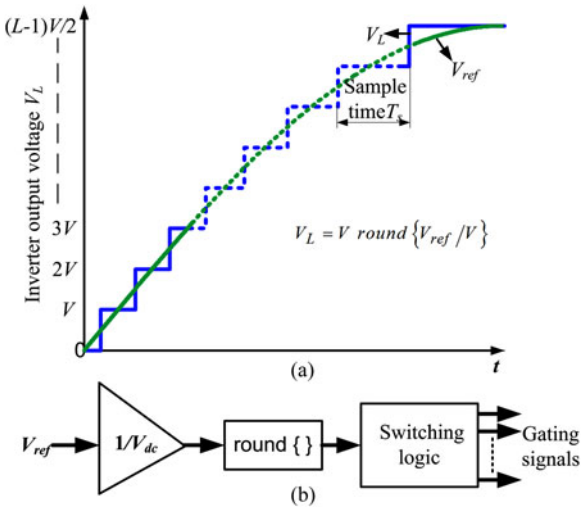

Fig. 10. NLC technique: (a) waveform synthesis of level counts "L" and (b) control method.

TABLE VI
SIMULATION PARAMETERS FOR MLI

Parameter	Values
No. of MHB modules (j)	1 and 2
Capacitors in each module	2200 μF
Switching frequency	50 Hz
Modulation index (m)	1.0
Load (R–L) per phase	126 Ω, 120 mH

$$-\frac{V_{\rm PV}+I_{\rm PV}R_s}{R_{\rm sh}} \tag{28}$$

where I_d is diode current, I_o is the diode saturation current, and V_t is junction thermal voltage which can be defined as

$$V_t = \frac{kATn_s}{q} \tag{29}$$

where

q is an electron charge (1.6×10^{-19} C);
k Boltzmann's constant (1.38×10^{-23} J/K);
A ideal factor of diode;
T working temperature;
n_s number of series connected cells.

Simulation is done using (28) on the basis of SOLAREX MSX-60 PV panel.

VI. CONTROL SCHEMES

The proposed MLI adapted to the PV RES is being controlled using MPPT at the generation side and NLC method at the inverter side. The underlining principles of these two control schemes are discussed in this section.

A. MPPT

To extract the maximum power from PV panel, two main MPPT tracking algorithms are generally employed such as perturbation and observation (P&O) and incremental conductance

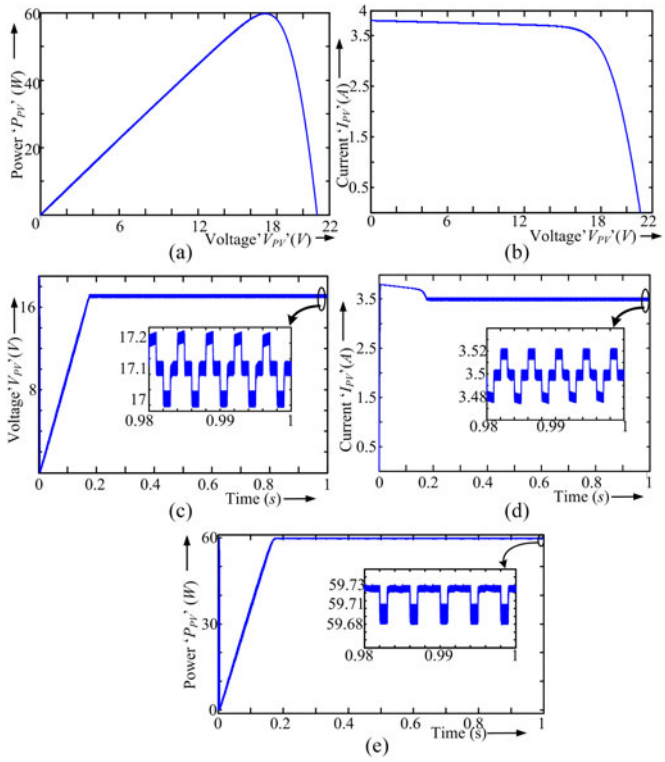

Fig. 11. PV panel characteristics. (a) P–V curve, (b) I–V curve, (c) PV panel output voltage, (d) PV panel output current, and (e) MPPT with P&O MPPT algorithm.

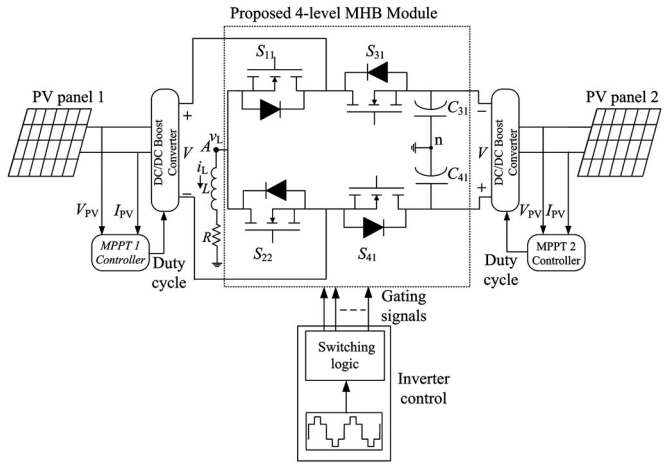

Fig. 12. Proposed four-level MHB module connected with PV RES.

techniques. Because of simplicity and efficient tracking, P&O is implemented [34]–[44]. The major advantages of this technique are PV array independent, provides true MPPT, ease of implementation in digital platform, capable of providing top level efficiency. The flowchart of P&O method is shown in Fig. 9, which provides step by step process to track the MPPT point and maintains the same. The algorithm perturbs the MPP of the PV panel by increasing or decreasing a control parameter by a small step size and measures the PV panel output power before and after the perturbation. If the power increases, the algorithm continues to perturb the system in the same direction; otherwise,

TABLE VII
CONDUCTION ANGLE COMPARISON FOR DIFFERENT CASES

Cases	Conduction angle (deg.)/time (ms) of switches in MHB module								Remarks on capacitor voltages (V_{c31} & V_{c41})
	Positive half-cycle				Negative half-cycle				
	S_{11}	S_{21}	S_{31}	S_{41}	S_{11}	S_{21}	S_{31}	S_{41}	
I	60°/3.3	120°/6.6	–	180°/10	120°/6.6	60°/3.3	180°/10	–	Tightly balanced
II	60°/3.3	120°/6.6	–	180°/10	110°/6.1	70°/3.8	180°/10	–	Marginally balanced
III	40°/2.2	110°/6.1	–	150°/8.3	100°/5.5	110°/6.1	210°/11.6	–	Unbalanced
IV	45°/2.5	105°/5.8	–	150°/8.3	180°/10	30°/1.6	210°/11.6	–	Balanced

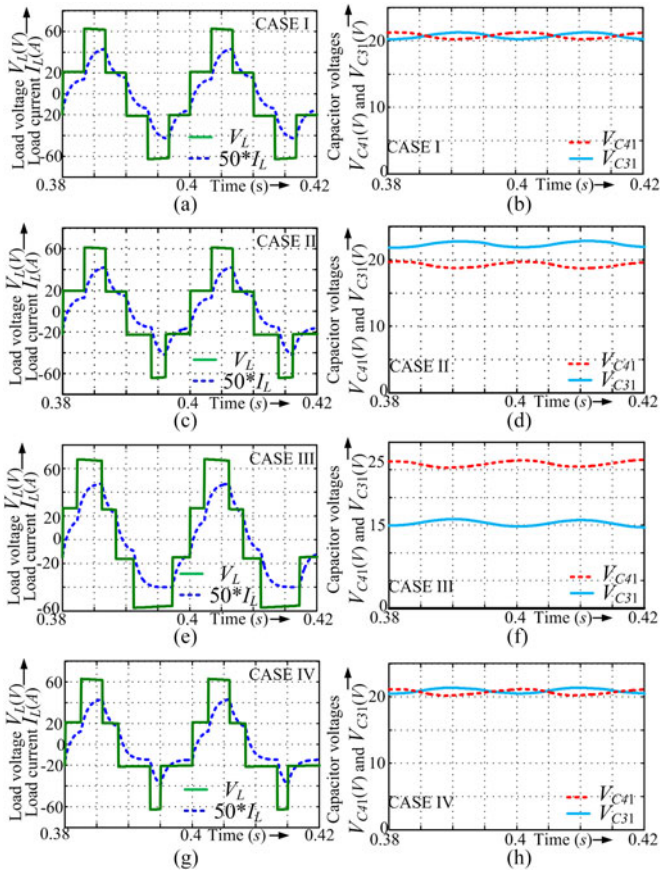

Fig. 13. (a), (c), (e), and (g) Load voltage $\boldsymbol{V}_{\mathrm{L}}$ and load current waveforms $\boldsymbol{I}_{\mathrm{L}}$ for cases I, II, III, and IV, respectively. (b), (d), (f), and (h) voltage across capacitors $\boldsymbol{V}_{\mathrm{c}41}$ and $\boldsymbol{V}_{\mathrm{c}31}$ for cases I, II, III, and IV, respectively.

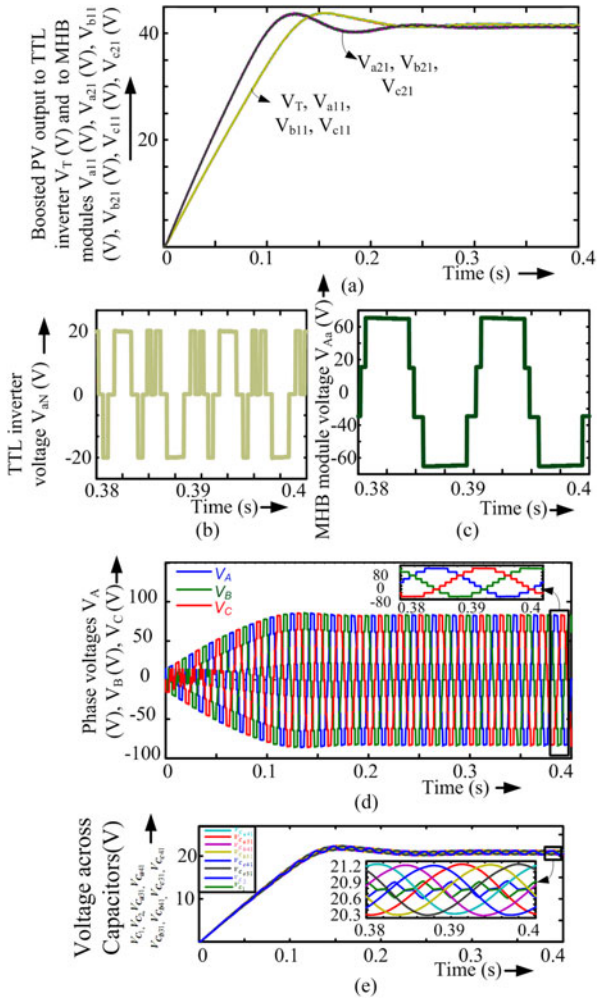

Fig. 14. Symmetrical mode nine-level operation: (a) boosted PV output to TTL inverter V_T and to MHB modules in all phases $V_{a11}, V_{a21}, V_{b11}, V_{b21}, V_{c11}, V_{c21}$, (b) TTL inverter voltage V_{aN}, (c) MHB module voltage V_{Aa}, (d) three-phase voltages $V_A V_B$ and V_c and (e) voltage across capacitors $V_{c_1}, V_{c_2}, V_{c_{a31}}, V_{c_{a41}}, V_{c_{b41}}, V_{c_{b42}}, V_{c_{c41}}, V_{c_{c42}}$.

the system is perturbed in the opposite direction. The principle of P&O algorithm is based on the slope of *P–V* curve. The slope is defined as the ratio of step change in power (ΔP) with step change in voltage (ΔV) on the *P–V* curve, i.e., $\Delta P/\Delta V$, where $\Delta P/\Delta V>0$ indicates the left of MPP, $\Delta P/\Delta V<0$ indicates the right of MPP and $\Delta P/\Delta V = 0$ indicates the MPP. The PV panel is not sufficient to provide the required output. A dc/dc converter is usually preferred to boost up the PV panel voltage to meet the requirement. The output of dc/dc boost converter is dependent on the duty cycle (*D*), so MPPT is used to calculate the duty cycle to obtain the maximum output voltage. The MPPT P&O controlled boost converter is interleaved between proposed MLI module and each PV panel.

B. NLC Method

A wide variety of modulation schemes have been researched and applied to MLIs such as level-shifted PWM (LSPWM), selective harmonic elimination (SHE), space vector modulation (SVM), etc. The application of SVM for MLIs is limited due to its complexity with an increase in the number of levels despite the efforts have been made to reduce it [45], [46]. The realization

TABLE VIII
SWITCHING STATES AND OUTPUT VOLTAGES OF THE PROPOSED 15-LEVEL MLI IN SYMMETRICAL MODE

L.NO.	S_{a11}	S_{a21}	S_{a31}	S_{a41}	S_{a12}	S_{a22}	S_{a32}	S_{a42}	T_{a1}	T_{a2}	P	V_A
1	1	0	0	1	1	0	0	1	1	0	0	$+7V/2$
2	1	0	0	1	1	0	0	1	0	0	1	$+3V$
3	1	0	0	1	1	0	0	1	0	1	0	$+5V/2$
4	1	0	0	1	0	1	0	1	0	0	1	$+2V$
5	1	0	0	1	0	1	0	1	0	1	0	$+3V/2$
6	1	0	0	1	1	0	1	0	0	0	1	$+V$
7	1	0	0	1	1	0	1	0	0	1	0	$+V/2$
8	1	0	0	1	0	1	1	0	0	0	1	0
9	0	1	1	0	0	1	0	1	1	0	0	$-V/2$
10	0	1	1	0	0	1	0	1	0	0	1	$-V$
11	0	1	1	0	1	0	1	0	1	0	0	$-3V/2$
12	0	1	1	0	1	0	1	0	0	0	1	$-2V$
13	0	1	1	0	0	1	1	0	1	0	0	$-5V/2$
14	0	1	1	0	0	1	1	0	0	0	1	$-3V$
15	0	1	1	0	0	1	1	0	0	1	0	$-7V/2$

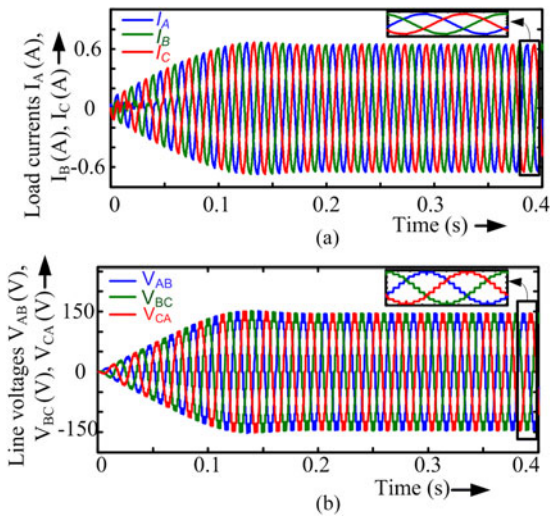

Fig. 15. Symmetrical mode nine-level operation: (a) load currents I_A, I_B, and I_c, (b) line voltages V_{AB}, V_{BC}, and V_{CA}.

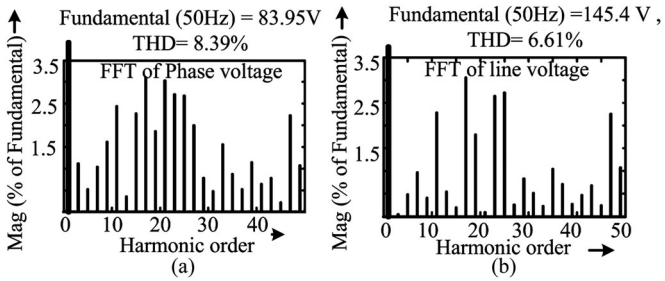

Fig. 16. Symmetrical mode nine-level operation: (a) frequency spectrum of phase voltage and (b) frequency spectrum of line voltage.

of LSPWM is done by three methods by different positions of triangular carrier signals such as phase disposition (PD), phase opposition disposition, and alternative phase opposite disposition [47]. The lowest harmonic distortion is achievable by the PD method at higher modulation indices as compared to other disposition methods. The LSPWM results in higher switching

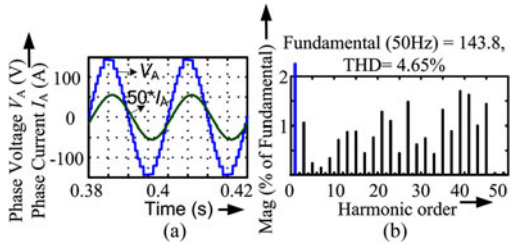

Fig. 17. Symmetrical mode 15-level simulation results for phase "*A*": (a) phase voltage V_A and phase current I_A, and (b) frequency spectrum of phase voltage.

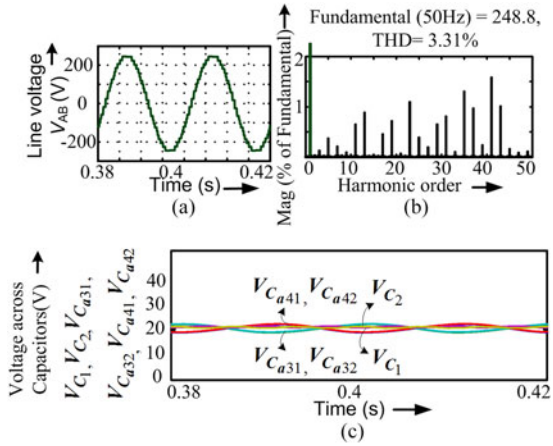

Fig. 18. Symmetrical mode 15-level simulation results for phase *A*: (a) line voltage V_{AB}, (b) frequency spectrum of line voltage, and (c) voltage across capacitors $V_{c_1}, V_{c_2}, V_{c_{a31}}, V_{c_{a32}}, V_{c_{a41}}, V_{c_{a42}}$.

losses due to higher carrier frequency to eliminate the lower order harmonics (LOH). The provision for eliminating LOH is with SHE, which produces less switching losses. But the issue of complexity arises in finding switching angles at higher number of levels.

The NLC or round method is a low switching frequency control technique [48]. This method leads to reduction in switching losses. The proposed topology adopts the NLC algorithm. It uses the nearest voltage level that can be generated by converting to the desired output voltage reference. Sampled waveform can be formed by comparing the reference waveform with the existing output voltage with level count "*L*" as depicted in Fig. 10(a). Its implementation is illustrated in Fig. 10(b). Given a voltage reference V_{ref}, the modulation index "*m*" the nearest output voltage level can be determined as

$$V_{\mathrm{ref}} = m\left(\frac{L-1}{2}\right)V\sin(\omega t) = V_m\sin(\omega t) \tag{30}$$

$$m = \frac{V_m}{\left(\frac{L-1}{2}\right)V} \tag{31}$$

$$V_L = V\,\mathrm{round}(V_{\mathrm{ref}}/V). \tag{32}$$

VII. SIMULATION RESULTS

To validate the theoretical analysis of proposed MLI, simulations are carried out in MATLAB/Simulink software tool

TABLE IX
SWITCHING STATES AND OUTPUT VOLTAGES OF THE PROPOSED 19-LEVEL MLI IN ASYMMETRICAL MODE

L.NO.	S_{a11}	S_{a21}	S_{a31}	S_{a41}	S_{a12}	S_{a22}	S_{a32}	S_{a42}	T_{a1}	T_{a2}	P	V_A
1	1	0	0	1	1	0	0	1	1	0	0	$+9V/2$
2	1	0	0	1	1	0	0	1	0	0	1	$+4V$
3	1	0	0	1	0	0	1	0	0	1	0	$+7V/2$
4	1	0	0	1	0	1	0	1	0	0	1	$+3V$
5	1	0	0	1	0	1	0	1	0	1	0	$+5V/2$
6	0	1	0	1	0	1	0	1	0	0	1	$+2V$
7	0	1	0	1	0	1	0	1	0	1	0	$+3V/2$
8	1	0	0	1	1	0	1	0	0	0	1	$+V$
9	1	0	0	1	0	1	1	0	1	0	0	$+V/2$
10	1	0	0	1	0	1	1	0	0	0	1	0
11	0	1	1	0	1	0	0	1	0	1	0	$-V/2$
12	0	1	1	0	0	1	0	1	0	0	1	$-V$
13	0	1	1	0	0	1	0	1	0	1	0	$-3V/2$
14	1	0	1	0	1	0	1	0	0	0	1	$-2V$
15	0	1	1	0	1	0	1	0	1	0	0	$-5V/2$
16	0	1	1	0	1	0	1	0	0	0	1	$-3V$
17	0	1	1	0	0	1	1	0	1	0	0	$-7V/2$
18	0	1	1	0	0	1	1	0	0	0	1	$-4V$
19	0	1	1	0	0	1	1	0	0	1	0	$-9V/2$

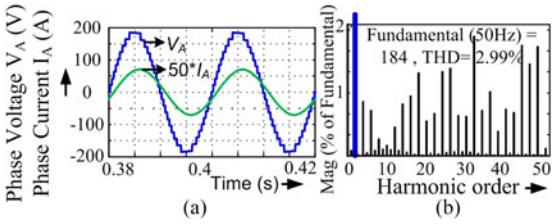

Fig. 19. Asymmetrical mode 19-level simulation results for phase "*A*": (a) phase voltage V_A and phase current I_A, and (b) frequency spectrum of phase voltage.

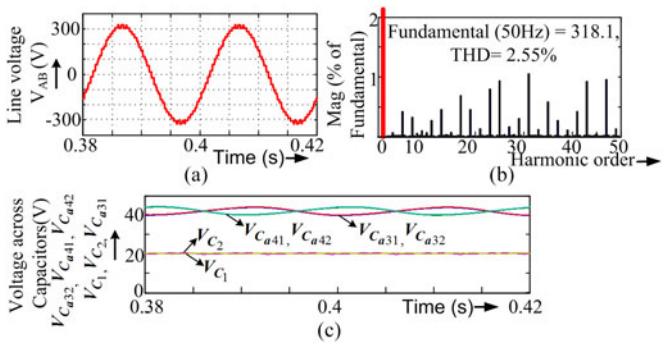

Fig. 20. Asymmetrical mode 19-level simulation results for phase "*A*": (a) line voltage V_{AB}, (b) frequency spectrum of line voltage, and (c) voltage across capacitors $V_{c_1}, V_{c_2}, V_{c_{a31}}, V_{c_{a32}}, V_{c_{a41}}, V_{c_{a42}}$.

incorporating SOLAREX MSX-60 PV panels as renewable energy sources. The proposed MLI parameters for the simulation are given in Table VI.

A. Performance Characteristics of PV Panel

The aforementioned the utilization of the PV panel has been increased by employing the P&O MPPT algorithm. The irradiance is maintained at 1 kW/m^2 and nominal temperature of

TABLE X
SUMMARY OF SIMULATION RESULTS

S. no.	Operating mode	Level count (L)	Phase voltage		Line voltage	
			Fundamental (V)	THD (%)	Fundamental (V)	THD (%)
1	Symmetrical	9	83.95	8.39	145.4	6.61
2	Symmetrical	15	143.8	4.65	248.8	3.31
3	Asymmetrical case 3	19	184	2.99	318.1	2.55

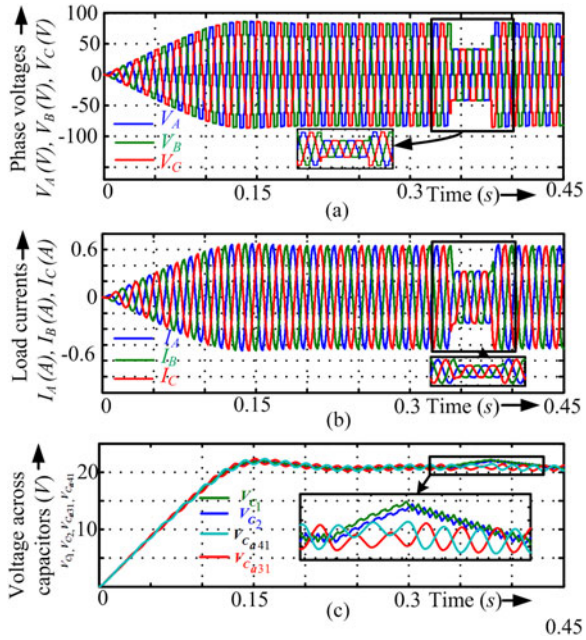

Fig. 21. Dynamic response of proposed MLI for step change in modulation index "*m*" for symmetrical nine-level operation: (a) phase voltages $V_A V_B$ and V_c, (b) phase currents I_A, I_B, and I_c and (c) voltage across capacitors $V_{c_1}, V_{c_2}, V_{c_{a31}}, V_{c_{a41}}$.

25 °C. The simulation results are presented in Fig. 11(a)–(e) by using (28). Fig. 11(a) and (b) represents *P–V* and *I–V* characteristics, respectively. The MPPT provides maximum power $P_{\max}$ of approximately 60 W at voltage V_{mp} of 17.1 V and current I_{mp} of 3.5 A. Fig. 11(c)–(e) shows $V_{\mathrm{PV}}, I_{\mathrm{PV}}$, and P_{PV} curves, respectively. The steady state is achieved approximately at 0.2 s and all three parameters oscillate around the MPP. The step size of MPPT is updated at a frequency of 50 kHz.

B. Effect of Conduction Time on the Performance of MHB Module

In this section, the simulation studies are presented considering the effect of conduction time of all switches in the proposed MHB module depicted in Fig. 12. The self-balancing of capacitors is studied under four cases I–IV. The analysis summarized in Table VII with simulation results presented in Fig. 14(a)–(h) shows that the capacitors are balanced except case III. This unbalance occurs because of different charging and discharging time of the capacitors in positive and negative half cycles, but

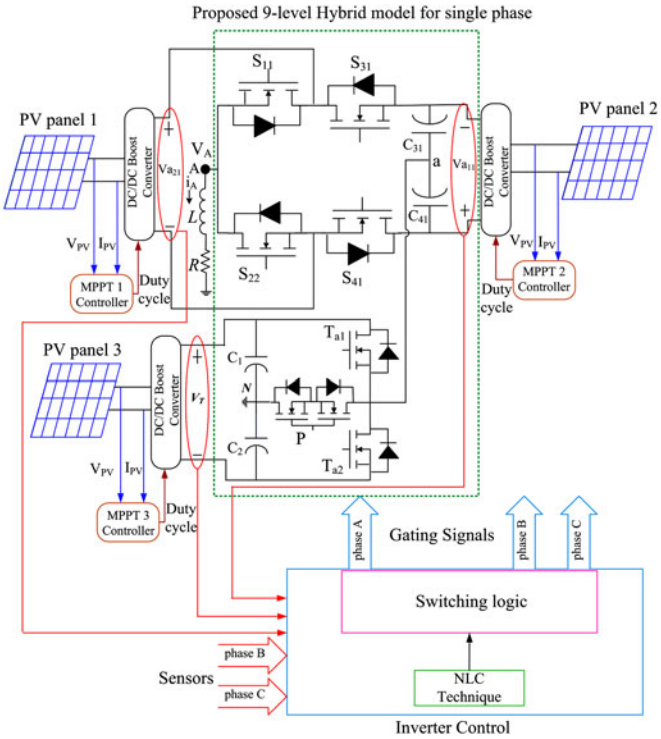

Fig. 22. Proposed nine-level PV RES-connected HCMMLI.

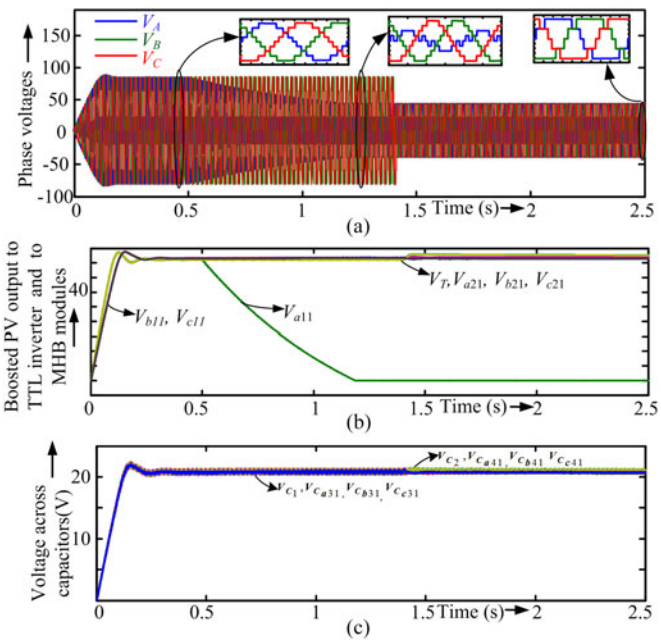

Fig. 23. Dynamics of PV panel 1 failure for symmetrical nine-level HCM MLI operation: (a) phase voltages, (b) boosted PV output to TTL inverter V_T and to MHB modules in three phases and (c) voltage across capacitors.

produces the voltage levels without skipping. The comparative analysis show the proposed MHB module is able to maintain the self-balancing feature with equal conduction times as in case I of Fig. 14(a) and (b) as well as in case IV with unequal conduction times of Fig. 14(g) and (h). The voltage across capacitors

TABLE XI
UPDATED SWITCHING TABLE FOR PHASE A WHEN PV PANEL 1 IS FAILED

S. no.	S_{a11}	S_{a21}	S_{a31}	S_{a41}	T_{a1}	T_{a2}	P	V_A
1	0	1	0	1	1	0	0	$+V$
2	0	1	0	1	1	0	0	$+V$
3	0	1	0	1	0	0	1	$+V/2$
4	0	1	0	1	0	0	1	$+V/2$
5	1	0	1	0	1	0	0	0
6	1	0	1	0	0	0	1	$-V/2$
7	1	0	1	0	0	0	1	$-V/2$
8	1	0	1	0	0	1	0	$-V$
9	1	0	1	0	0	1	0	$-V$

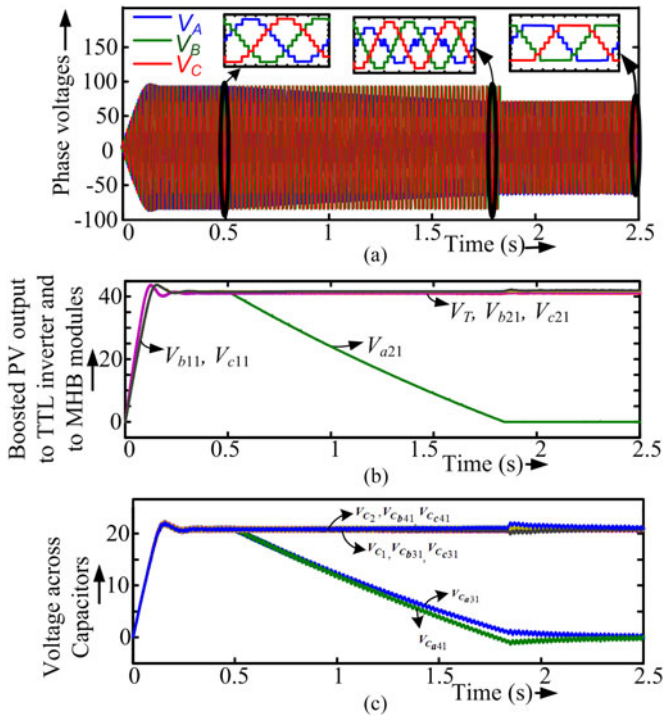

Fig. 24. Dynamics of PV panel 2 failure for symmetrical nine-level HCMMLI operation: (a) phase voltages, (b) boosted PV output to TTL inverter V_T and to MHB modules in three phases and (c) voltage across capacitors.

slightly deviated in case II of Fig. 14(c) and (d), i.e., capacitors are marginally balanced.

C. Three-Phase Symmetrical/Asymmetrical 9/15-Level HCM MLI

In the symmetrical mode operation, all the boosted PV panel output voltages are set to equal. The number of MHB modules "*j*" is chosen 1 and 2 in order to get 9 and 15 levels in the phase voltage, respectively. The switching states for generation of 9-level and 15-level in phase voltage are listed in Tables III and VIII, respectively. Each PV panel output of 17.1 V is boosted up to 41.5 V by a boost converter and is supplied to the proposed MLI as shown in Fig. 14(a). The voltage across the TTL inverter and MHB module in phase "*A*" is shown in Fig. 14(b) and (c). Three-phase voltages, self-balanced voltage across capacitors, currents, and line voltages are shown in Fig. 14(d) and (e) and

TABLE XII
UPDATED SWITCHING TABLE FOR PHASE $[A]$ WHEN PV PANEL 2 IS FAILED

S. no.	S_{a11}	S_{a21}	S_{a31}	S_{a41}	T_{a1}	T_{a2}	P	V_A
1	1	0	0	1	1	0	0	$+3V/2$
2	1	0	0	1	1	0	0	$+3V/2$
3	1	0	0	1	0	0	1	$+V$
4	0	1	0	1	1	0	0	$+V/2$
5	1	0	1	0	0	0	1	0
6	1	0	1	0	0	1	0	$-V/2$
7	0	1	1	0	0	0	1	$-V$
8	0	1	1	0	0	1	0	$-3V/2$
9	0	1	1	0	0	1	0	$-3V/2$

TABLE XIII
UPDATED SWITCHING TABLE FOR PHASES "*B*" AND "*C*" WHEN PV PANEL 2 IS FAILED

S. no.	$S_{b,c11}$	$S_{b,c21}$	$S_{b,c31}$	$S_{b,c41}$	T_{a1}	T_{a2}	P	$V_{B,C}$
1	1	0	0	1	0	0	1	$+3V/2$
2	1	0	0	1	0	0	1	$+3V/2$
3	1	0	0	1	0	1	0	$+V$
4	0	1	0	1	0	0	1	$+V/2$
5	1	0	1	0	1	0	0	0
6	1	0	1	0	0	0	1	$-V/2$
7	0	1	1	0	1	0	0	$-V$
8	0	1	1	0	0	0	1	$-3V/2$
9	0	1	1	0	0	0	1	$-3V/2$

TABLE XIV
EFFECT OF IRRADIANCE ON QUALITY OF LOAD VOLTAGE AND CURRENT

Irradiance (W/m^2)	Voltage (V_A)		Current (I_A)	
	V_{A1} (V)	THD (%)	I_{A1} (A)	THD (%)
1000	83.95	8.39	0.637	1.87
800	83.21	8.45	0.6327	1.93
600	82.29	8.54	0.6257	2.05
400	80.72	8.74	0.6137	2.29
200	74.06	9.92	0.5631	3.42
0	46.93	17.5	0.3567	8.71

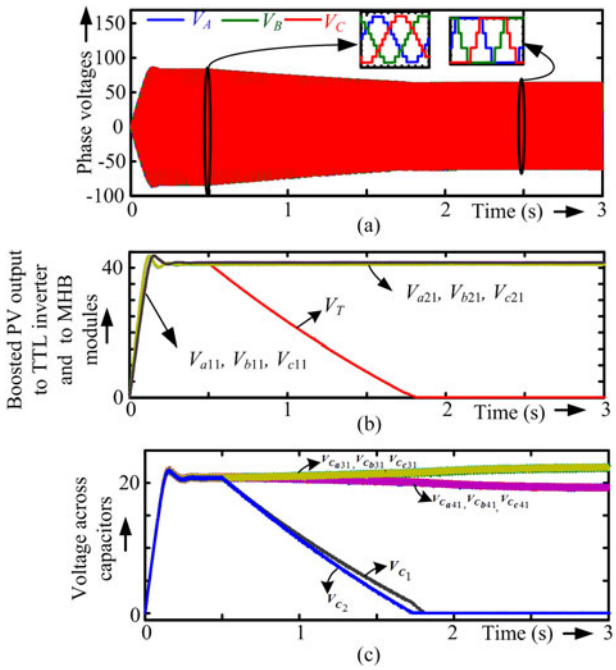

Fig. 25. Dynamics of PV panel 3 failure for symmetrical nine-level HCM MLI operation: (a) phase voltages, (b) boosted PV output to TTL inverter V_T and to MHB modules in three phases and (c) voltage across capacitors.

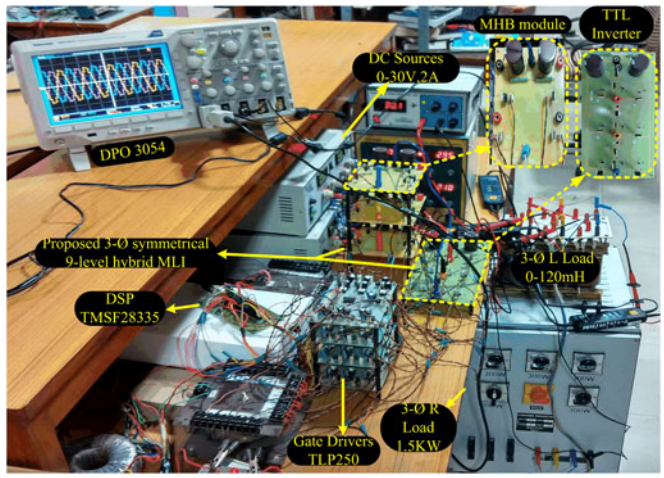

Fig. 26. Prototype setup in the laboratory.

Fig. 15(a) and (b), respectively, for symmetrical nine-level operation. The phase "*A*" voltage and line voltage V_{AB} are presented in Figs. 17(a) and 18(a) for symmetrical 15-level operation.

The frequency spectra of phase voltage are shown in Figs. 16(a) and 17(b) for 9-level and 15-level operation, respectively. Figs. 16(b) and 18(b) show the harmonic analysis of line voltage for 9-level and 15-level operation, respectively. The capacitor voltages of phases for 15-level operation presented in Fig. 18(c) are balanced.

In the asymmetrical mode case 3 operation, all the available voltages are set to V or $2V$ according to (2.d), (18), and (19). The number of MHB modules "*j*" is chosen 2 in order to get 19 levels in the phase voltage. The switching states for generation of 19-level in phase voltage are listed in Table IX. The simulation results for phase "*A*" are presented in Fig. 19(a) and (b) for synthesizing 19-level. The capacitors in the MHB module and TTL inverter are strictly balanced despite of small ripple, which can be visualized from Fig. 20(c). The line voltage and frequency spectrum in Fig. 20(a) and (b) show reduction in % THD with increase in fundamental.

All the simulation studies under steady-state condition in both symmetrical and asymmetrical modes are summarized in Table X. It can be concluded that there is a remarkable reduction in the total harmonic distortion (% THD) both in the phase and line voltages. Consequently, this reduction of % THD leads to improvement in the power quality. It results in bring down size and cost of filtering requirements.

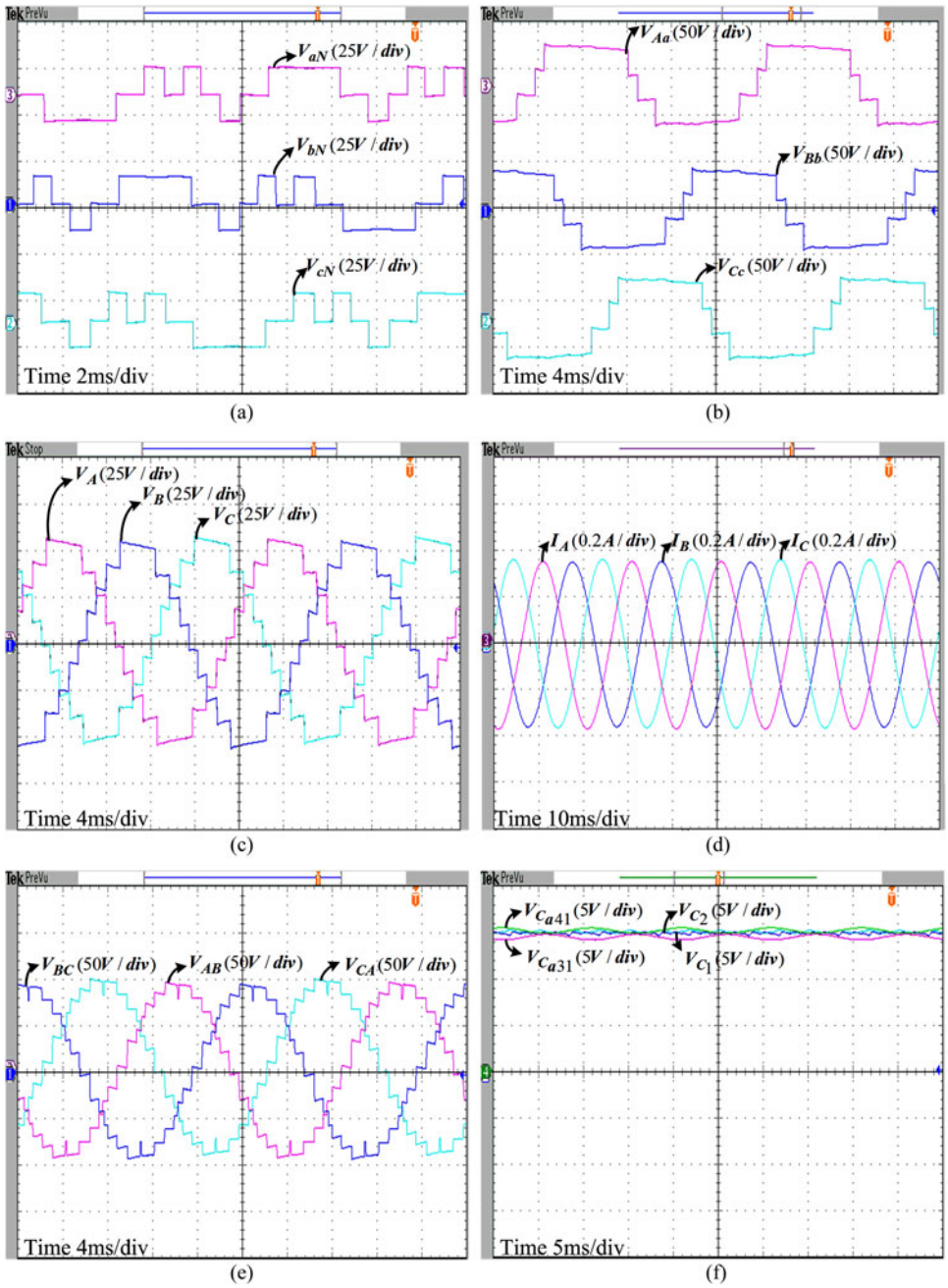

Fig. 27. Symmetrical mode nine-level experimental results: (a) *TTL* inverter voltages, (b) *MHB* module voltages, (c) phase voltages, (d) phase currents, (e) line voltages, and (f) voltage across capacitors.

D. Dynamic Response for Step Changes in Modulation Index "m"

To analyze the dynamic behavior of the proposed MLI, a step change in modulation index "*m*" is considered for symmetrical nine-level operation. A step *change to* $m = 0.6$ for two cycles (i.e., 40 ms) is applied at $t = 0.32$ s as shown in Fig. 21(a)–(c). The level count "*L*" gets reduced to 5 from 9 in the phase voltages as shown in Fig. 21(a). The phase currents variations are presented in Fig. 21(b). From Fig. 21(c), it is evident that the balancing of capacitor voltages unfazed due to variations in modulation index "*m*."

E. Impact of PV Panel Failure/Removal

To discuss the impact of removing a PV panel for the purpose of maintenance or failure due to faults [49] on the behavior of overall inverter, the PV RES connected to the proposed nine-level HCM MLI for single phase is shown in Fig. 22. In each phase of the proposed inverter-connected RES, three PV panels viz., 1, 2, and 3 are employed. The sensors are provided at the boost converter end to detect the voltage and given to inverter control block. The switching logic is updated in the inverter control block to maintain the three phase balanced output voltages under faulty conditions. Three possible failures or

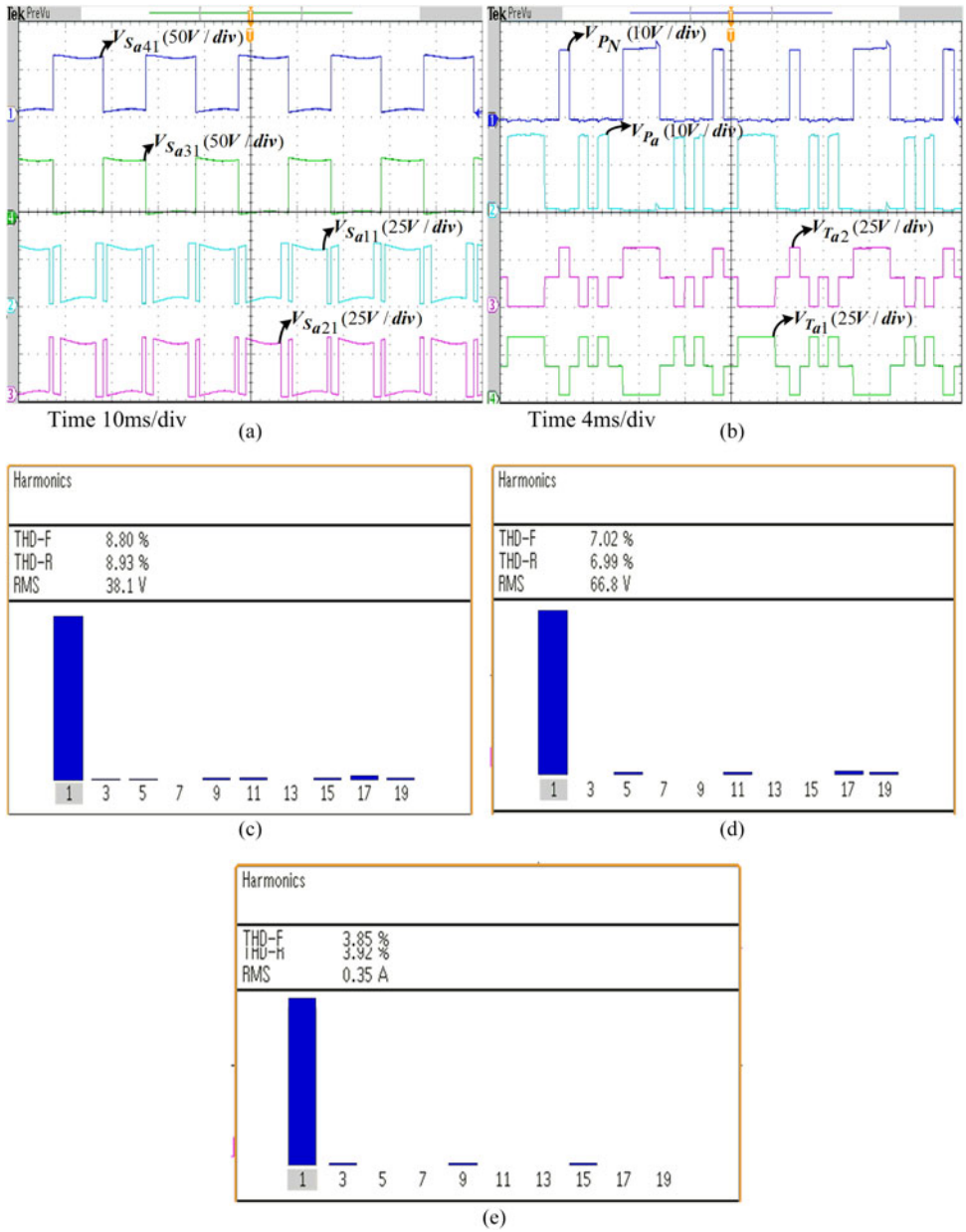

Fig. 28. (a) and (b) Voltages across the switches in MHB module and *TTL* inverter, respectively. (c), (d) and (e) Frequency spectra of phase voltage, line voltage, and load current, respectively.

removal are considered in this section and simulation results are presented.

When PV panel 1 is failed to pump the voltage V_{a11} due to the fault, the phase "*A*" voltage gets distorted and level gets reduced resulting in unbalance in the three-phase system. These dynamics are analyzed with the help of simulation studies presented in Fig. 23(a)–(c). As shown in Fig. 23(a), the system enters into steady state after $t = 0.35$ s and producing balanced three-phase voltages. When a fault is introduced by setting the PV panel 1 irradiance to zero at t = 0.5 s, the corresponding panel 1 voltage V_{a11} gradually reduced to zero at $t = 1.2$ s as seen from Fig. 23(b). The phase "*A*" voltage gets distorted resulting in a reduced fundamental voltage of 35.51 V unlike the fundamental at normal operation of 83.87 V and increased % THD from 8.40% to 41.74%. To balance the system, the switching logic in Table III is updated according to Table XI at $t =$ 1.4 s. The system is well balanced and producing five levels in all three phases with the improvement of % THD to 17.5% and fundamental is increased to 46.93 V. During these changes, the balancing of capacitors is unfazed as shown in Fig. 23(c).

The dynamics for the failure of PV panel 2 at $t = 0.5$ s are shown in Fig. 24(a)–(c). Since the capacitors are connected across the PV panel 2, V_{a21} takes more time to settle down to zero at $t = 1.78$ s as depicted in Fig. 24(b) and correspondingly the capacitor voltages $V_{ca31,}$ V_{ca41} settle down to zero, while the other capacitor voltages are balanced as shown in Fig. 24(c). The unbalance occurs in system due to phase "*A*" and it is rectified by updating the switching sates as per Table XII. The balance

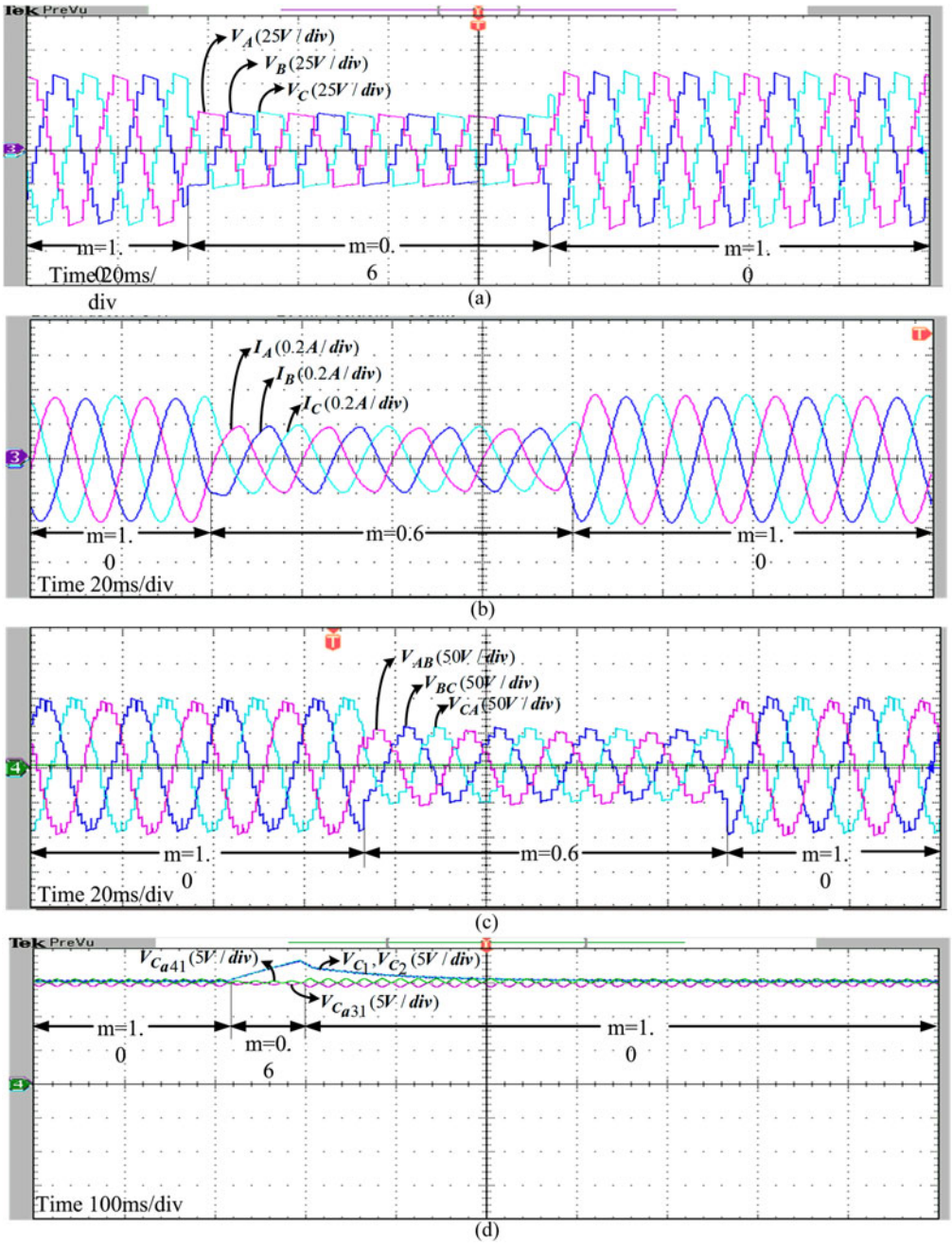

Fig. 29. Dynamic response of the proposed MLI for step change in modulation index "*m*": (a) phase voltages, (b) phase currents, (c) line voltages, and (d) voltage across capacitors.

is achieved by synthesizing seven levels in other phases "*B*" and "*C*" with updating entries of Table XIII. The phase "*A*" is recovered from distortion as shown in Fig. 24(a) and improves the fundamental voltage from 58.04 to 71.43 V and % THD from 24.71% to 14.14%.

When the fault occurs at $t = 0.5$ s in the PV panel 3, the TTL inverter voltage V_T and capacitor voltages V_{c_1}, V_{c_2} gradually reduce to zero as shown in Fig. 25(b), leads to balanced operation with four level in each phase as depicted in Fig. 25(a). During this change, capacitor voltages are marginally balanced as shown in Fig. 25(c) with consistent four levels in all three phases.

F. Impact of Irradiance on Quality of Load Voltage and Current

Environmental conditions are one of the key factors in the operation of PV RES, which can reflect the significant changes in the efficiency of the system. The variations of solar irradiance can affect the quality of load voltage and current being supplied by the PV RES, hence the power quality. The partial shading causes the fluctuations in irradiance [50]–[52]. To analyze this issue, the proposed HCM MLI as depicted in Fig. 22 for one phase "*A*," the variations in the irradiance of PV panel 1 are taken into consideration. When the solar irradiance changes,

eventually the change is reflected in the PV output and hence at the source side of proposed MLI. This results in reduced voltage step size, though it can maintain the same number of nine levels in the phase voltage "A." The simulation results are tabulated in Table XIV by considering the changes in irradiance levels in the range from 1 to 0 kW/m^2. The zero value of irradiance may be a fault or removal of PV panel as discussed under the previous section. The analysis of these results shows that there is reduction in fundamental value of load voltage and current and also increase in the % THD in both.

VIII. Experimental Results

To validate the simulation and theoretical results, a low power three-phase MLI prototype has been built as shown in Fig. 26. The parameters used for experimentation are the same as that of simulation listed in Table VI. Due to laboratory constraints, the prototype is tested with input dc voltage (*V*) 30 V, which is supplied from isolated dc power supplies. The symmetrical nine-level mode is taken as experimental case study.

The NLC algorithm is implemented digitally by using DSP TMS32F28335 with code composer studio 5.3.0. In the converter, IRF640N MOSFETs of rating 200 V, 15 A are used as switching devices. The amplification and the isolation from the power circuit are provided by the gate driver TLP250. A deadband of 500 ns is provided in the DSP programming keeping with the view of complementary switching action for each arm of MHB module. A power scope of TEKTRONIX make, Model No. DPO 3054, was used for recording the harmonic content.

The steady-state experimental results of the proposed MLI under loaded conditions are presented in Fig. 27(a)–(f). The three-level phase voltages of TTL inverter are shown in Fig. 27(a). The four-level MHB module voltages in each phase are shown in Fig. 27(b). The nine-level phase voltages and phase currents of the proposed symmetrical MLI are presented in Fig. 27(c) and (d). The line voltages are shown in Fig. 27(e). Fig. 27(f) shows that the capacitor voltages in TTL inverter across C_1, C_2 and MHB module capacitors C_{a31}, C_{a41} in phase "*A*" are balanced. The capacitor balancing is achieved in other phases also to produce nine levels in all three phase voltages as depicted in Fig. 27(c). The voltage across switches $S_{a11}, S_{a21}, Sa_{31}$, and S_{a41} in MHB module and P_N, P_a, T_{a1}, and T_{a2} in TTL inverter in phase "*A*" are presented in Fig. 28(a) and (b), respectively. The frequency spectra of phase voltage V_A, line voltage $V_{\rm AB}$, and phase current I_A are presented in Fig. 28(c), (d), and (e), respectively. The third-order harmonics are absent in $V_{\rm AB}$. The % THD of $V_A, V_{\rm AB}$, and I_A are 8.80%, 7.02%, and 3.85%, respectively. The higher order harmonics can easily be eliminated with low filtering requirements.

To analyze the dynamic behavior of the proposed MLI with step change in modulation index "*m*" is considered. The "*m*" is reduced to 0.6 from 1 for duration of four cycles (i.e., 80 ms) is applied as shown in Fig. 29. The level count "*L*" gets reduced to 5 from 9 in the phase voltages as shown in Fig. 29(a). The phase currents variations are presented in Fig. 29(b). The levels in the line voltages are changed from 17 to 9 as shown in Fig. 29(c). The voltage across main capacitors in TTL inverters C_1, C_2 and capacitors C_{a31}, C_{a41} in phase "*A*" are shown in Fig. 29(d). These capacitor voltages undergo sudden changes when step change is occurred but soon these transients die and balancing of capacitor voltages is regained. It is evident that proposed MLI responds dynamically to the changes in "*m*." These dynamic analyses are quite similar to those obtained in simulation studies in Fig. 21(a)–(c).

IX. Conclusion

In this paper, a three-phase HCMMLI topology developed from a MHB module is proposed. The comparative analysis with classical CHB and FC shows superior features of less switch count, capacitor requirement and less *VBC*. It reduces the switch count by 50%, gate drive requirement by 43.75% and energy source requirement by 58.33% compared with a three-phase nine-level CHB inverter. The MPPT algorithm and NLC method have been discussed and evaluated for proposed topology interfaced with PV RES. The simulation results are validated by conducting experiment on proposed inverter. The experimental results show the ability of a proposed inverter to generate all the levels in both symmetrical and asymmetrical modes while maintaining the natural balancing of all the capacitors voltages in each module. Due to its modular structure, it can be easily interfaced with PV-connected microgrid.

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