Parameter Design of a Novel Series-Parallel-Resonant *LCL* Filter for Single-Phase Half-Bridge Active Power Filters

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***Abstract*—This paper proposes a novel high-order passive filter, i.e., series-parallel-resonant *LCL* (SPRLCL) filter, for single-phase half-bridge active power filters. The proposed SPRLCL filter consists of a series resonance introduced by adding a small inductor to the capacitor branch loop and a parallel resonance by paralleling a small capacitor with the gird-side inductor. Three design methods are proposed to fine tune the parameters of the SPRLCL filter. Design method I and method II enable the SPRLCL filter to attenuate more switching-frequency and double switching-frequency current harmonics than *LCL* or *LLCL* filters, while with design method III, the SPRLCL filter can be more robust against filter parameter variations. In order to achieve a better damping performance and facilitate the design of active damping control, the dominant resonance frequency of the proposed filter is set at one-third of the system sampling frequency. Based on this, a comprehensive parameter design process of the SPRLCL filter is presented, where the variation of source inductance is also considered. A proportional plus repetitive current-loop controller is designed to ensure system control stability and satisfactory harmonic compensation. Simulation and experimental results are finally presented to validate the feasibility of the theoretical analysis.**

***Index Terms*—Active damping, active power filter (APF), *LCL* filter, series-parallel-resonant *LCL* filter.**

I. Introduction

GRID-CONNECTED converters (GCCs) have been widely used in modern power systems due to large-scale deployment of renewable energy generation and energy storage systems [1]–[23]. In addition to simply converting active power, GCCs with properly designed controllers can also function as power quality conditioning equipment, such as active power filters (APF) [24], [25] or unified power quality conditioners (UPQC) [26] to resolve the ever-challenging power quality issues introduced by nonlinear electronic loads. The main objective of such equipment is to eliminate system current and/or voltage harmonics and ensure the reliable and secure operation of power grids.

For power conditioning equipment, the voltage source converters (VSC) controlled by pulse width modulation (PWM) may cause high-frequency current harmonics to the power grid, especially those at the switching frequency and its multiples [1]–[4]. In order to comply with grid codes, a passive filter is required to interface the VSC to the power grid and provide sufficient attenuation to the current harmonics injected into the point of common coupling (PCC). For selection of passive filters, an *LCL* filter is more preferred than a simple *L* filter as it can achieve better high-frequency harmonics attenuation, smaller size, and lower cost and power losses. To further attenuate the switching-frequency harmonics and reduce the grid-side inductance, an *LLCL* filter was proposed in [3], where a small inductor is inserted into the capacitor branch loop to create a series resonant tank at the switching frequency. This additional *LC* branch loop can bypass most of the current harmonics around the switching frequency, and, thus, allow further reduction of passive filter inductance. Nonetheless, the insertion of this series *LC* resonance reshapes the system frequency characteristic and makes its roll-off rate to be -20 dB/decade [3]. Therefore, the passive filter essentially becomes a simple *L* filter in the high-frequency range and more current harmonics would appear at the double switching frequency. In order to maintain the same high-frequency roll-off rate as that of an *LCL* filter, another independent filter capacitor can be added in parallel with the series *LC* resonance to form a so called *LCL-LC* filter [5]. This type of filters exhibits better harmonic attenuation than the *LLCL* filter in the high-frequency domain, but its attenuation at the double switching frequency could be even worse due to the presence of a new resonance. To tackle this problem, more series *LC* resonant tanks can be introduced to remove the harmonics at the switching frequency and its multiples, and this concept was presented in [4] and named as *LTCL* filters. Although being effective in high-frequency harmonic attenuation, the parameter design process of *LTCL* filters involves complicated iterative steps even with only two *LC* resonant tanks, and each resonant tank should be formed by one extra capacitor and one extra inductor, leading to an increased number of discrete passive components. Moreover, both *LLCL* filters and *LTCL* filters are sensitive to parameter variations [3]–[5], and the attenuation of

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switching-frequency harmonics will be much deteriorated under such circumstances.

Despite their improved ability of switching-frequency harmonic attenuation, high-order passive filters may introduce low impedances at certain frequencies and cause the well-known resonance issue, and this complication not only exists in *LCL* filters but also in *LLCL* and *LTCL* filters. Since such a low impedance resonance can induce system instability issues, it is necessary to implement some proper resonance damping techniques to stabilize the system. State-of-the-art resonance damping techniques can be categorized into two types. One way is to add extra resistors and other passive elements to the filter network, namely passive damping [6]–[9], which is simple and reliable. However, extra resistors result in increased power losses and filter cost as well as reduced high-frequency harmonic attenuation. The other way is realized by control algorithms, namely active damping. In contrast, active damping requires no extra resistor, making it more attractive than its counterpart in terms of power losses and cost. Therefore, this damping control technique has recently gained a lot of research attentions and been extensively studied in the literature [10]–[22]. Among all methods of active damping, the capacitor-current-feedback active damping is widely used due to its easy realization and clear physical meaning [10]–[18], [34]. For *LCL* filters, the capacitor-current-feedback active damping can be modeled as a frequency-dependent virtual resistor in parallel with a frequency-dependent virtual inductor [11]. By properly setting the parameters of passive components and feedback gains, this paralleled virtual resistor can well damp the *LCL* resonance and guarantee the stability of closed-loop current control. Unfortunately, for *LTCL* filters, a new resonant peak above 0 dB may appear between the switching frequency and double switching frequency even with the consideration of source resistance. Since this new resonance frequency is higher than the switching frequency, it can only be passively damped. In addition, the new resonant frequency approaches the switching frequency, and it may deteriorate the harmonic attenuation ability of *LTCL* filters at the switching frequency [4].

In order to simplify the topology of high-order trap filters and meanwhile facilitate the design of resonance damping, this paper proposes a novel high-order passive filter, named as series-parallel-resonance LCL (SPRLCL), for high-frequency switched-mode power converters. Being similar as the *LTCL* filter with two resonant tanks, the proposed SPRLCL filter can also provide strong attenuation to the first and second dominant switching harmonics. Since the grid-side inductor is utilized to form one resonant tank in the proposed filter topology, one series resonant inductor can be saved to reduce the size and cost of passive filters. Moreover, the new resonant peak is now shifted to a higher frequency range, i.e., above the double switching frequency, and it can be much more easily damped by the source resistance as compared to that of the *LTCL* filter. In this case, only the low-frequency *LCL* resonance needs to be considered, and all existing damping methods can be adopted for the proposed SPRLCL filter, which may greatly facilitate the system controller design.

The remaining parts of this paper are organized as follows. In Section II, the principle and three design methods of the SPRLCL filter are given. In Section III, based on the average switch model (ASM) of the SPRLCL filter, analysis of the capacitor-current-feedback actively damped SPRLCL filter is presented. It is identified that the proportional feedback of the capacitor branch loop current is equivalent to a pure virtual resistor paralleled with the capacitor branch loop when the resonance frequency f_r of the SPRLCL filter is set at one-third of the switching frequency, i.e., $f_s/3$. In Section IV, a comprehensive parameter design process of the SPRLCL filter is given. When applied to a half-bridge APF, an enlarged bandwidth of the controller is quite necessary as the output current contains a lot of high-order harmonics [24]. Furthermore, the grid inductance variation is also considered in the design process to make the control system more robust [2]. In Section V, a proportional plus repetitive current-loop controller is designed based on the derived filter parameters to achieve better harmonic elimination. Simulation and experimental results are provided in Section VI to validate the theoretical analysis. Section VII finally concludes the main contributions of this paper.

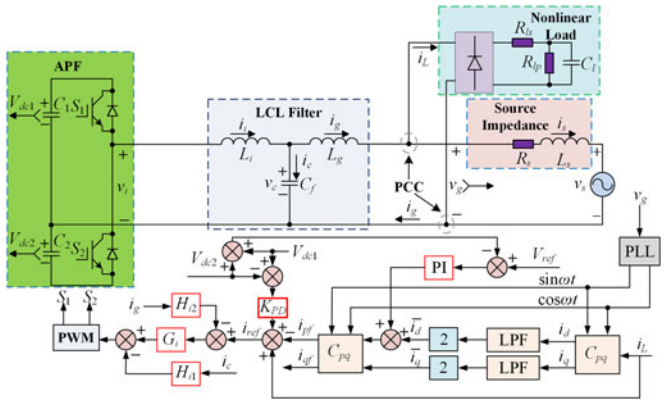


Fig. 1. Topology and control diagram of an *LCL* filtered half-bridge APF.

II. Principle of Proposed SPRLCL Filter

The topology and the control diagram of an *LCL* filtered half-bridge APF is shown in Fig. 1. The *LCL* filter is composed of an inverter-side inductor L_i, a grid-side inductor L_g, and a filter capacitor C_f. The equivalent-series resistances (ESRs) of the passive components are relatively small, and, hence, ignored here. The output voltage and current of the APF in the inverter side are denoted as v_i and i_i, respectively, and the filter capacitor current and voltage are represented as i_c and v_c, respectively. The voltage at the PCC and the grid-side current are expressed as v_g and i_g, respectively, and the grid voltage and the source current are denoted as v_s and i_s, respectively. The source impedance is modeled to be an ESR R_s connected in series with an inductor L_s. An uncontrolled diode rectifier with a resistive–capacitive load serves as a nonlinear load connected to the PCC, and the nonlinear load current is denoted as i_L. A phase-locked loop is adopted to synchronize the phase of v_g for *dq* transformation. The fundamental current of i_L is extracted first by multiplying $\sin\omega t$ and $\cos\omega t$ with i_L and then filtered through low-pass filters (LPF) with a gain of 2. $V_{\rm ref}$

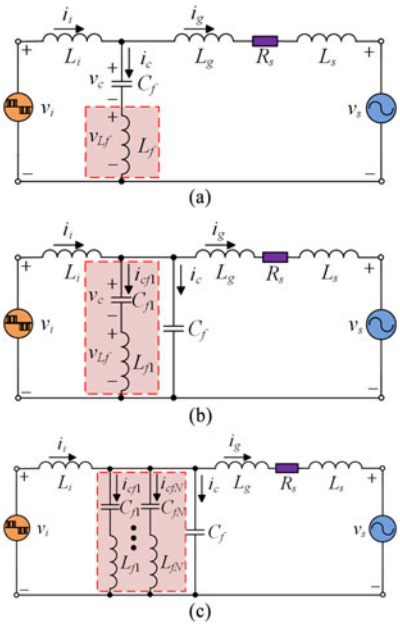


Fig. 2. Simplified circuits of (a) *LLCL* filter, (b) *LCL-LC* filter, and (c) *LTCL* filter.

denotes the reference dc voltage used for the dc-link capacitors C_1 and C_2, and their voltages are, respectively, denoted as $V_{\mathrm{dc}1}, V_{\mathrm{dc}2}$. Through a proportional-integral (PI) controller, the total dc bus voltage can be always regulated at the commanded value by controlling the active current. A proportional controller with a gain K_{PD} is required to balance the two capacitors' voltages in the dc link. H_{i2} denotes the feedback coefficient of i_g and G_i stands for the current controller. H_{i1} is a proportional gain and used as the feedback coefficient of i_c to achieve capacitor-current-feedback active damping. S_1 and S_2 are the insulated-gate bipolar-transistors (IGBTs) modulated at the switching-frequency f_s. Detailed filter and controller designs will be given in the following sections.

For switched-mode power electronic converters, the ability to attenuate high-frequency switching harmonics is an important performance index according to IEEE standard 1547.2-2008 [27] and IEEE standard 519-1992 [28]. In order to provide sufficient attenuation to the most dominant switching harmonics, the *LCL* filter shown in Fig. 1 can also be replaced by other advanced filters, e.g., *LLCL* filters, *LCL-LC* filters, or *LTCL* filters, and their simplified circuits are shown in Fig. 2.

The transfer function $i_g(s)/v_i(s)$ of the *LLCL* filter can be described as

$$G_{L1}(s) = \frac{i_g(s)}{v_i(s)} = \frac{a_2 s^2 + 1}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{1}$$

where

$$\begin{cases} a_2 = L_f C_f \\ b_3 = L_g L_i C_f + L_s L_i C_f + L_f C_f L_i + L_f C_f L_g + L_f C_f L_s \\ b_2 = L_i C_f R_s + L_f C_f R_s \\ b_1 = L_i + L_g + L_s \\ b_0 = R_s. \end{cases}$$

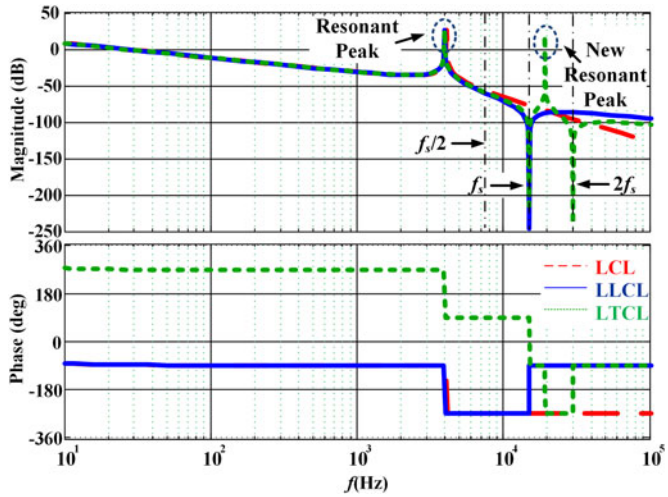


Fig. 3. Bode plots $i_g(s)/v_i(s)$ of *LCL* filter, *LLCL* filter, and *LTCL* filter.

The transfer function $i_g(s)/v_i(s)$ of the *LTCL* filter with two *LC* resonant tanks can be derived as

$$\begin{aligned} G_{L2}(s) &= \frac{i_g(s)}{v_i(s)} \\ &= \frac{a_4 s^4 + a_2 s^2 + 1}{b_7 s^7 + b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}, \end{aligned} \tag{2}$$

where the parameters can be derived as

$$\begin{cases} a_4 = L_{f1} C_{f1} L_{f2} C_{f2} \\ a_2 = L_{f1} C_{f1} + L_{f2} C_{f2} \\ b_7 = (L_g + L_s) L_i C_f L_{f1} C_{f1} L_{f2} C_{f2} \\ b_6 = R_s L_i C_f L_{f1} C_{f1} L_{f2} C_{f2} \\ b_5 = L_i (L_g + L_s)[(L_{f1} + L_{f2}) C_{f1} C_{f2} \\ \quad + (L_{f1} C_{f1} + L_{f2} C_{f2}) C_f] \\ \quad + (L_i + L_g + L_s) L_{f1} C_{f1} L_{f2} C_{f2} \\ b_4 = L_i R_s [(L_{f1} + L_{f2}) C_{f1} C_{f2} + (L_{f1} C_{f1} + L_{f2} C_{f2}) C_f] \\ \quad + R_s (L_i + L_g + L_s) L_{f1} C_{f1} L_{f2} C_{f2} \\ b_3 = (L_g + L_s)(C_{f1} + C_{f2} + C_f) L_i \\ \quad + (L_i + L_g + L_s)(L_{f1} C_{f1} + L_{f2} C_{f2}) \\ b_2 = R_s (C_{f1} + C_{f2} + C_f) L_f + R_s (L_{f1} C_{f1} + L_{f2} C_{f2}) \\ b_1 = L_f + L_g + L_s \\ b_0 = R_s. \end{cases}$$

The Bode plots $i_g(s)/v_i(s)$ of *LCL* filters, *LLCL* filters, and *LTCL* filters with two *LC* tanks are presented in Fig. 3, where the total capacitance in each filter is the same. As can be observed from Fig. 3 and also discussed in Section I, the *LTCL* filter may stand out among these three types of filters in terms of switching harmonic attenuation and requirement of filter inductance. However, the number of discrete passive components is inevitably increased due to the introduction of multiple resonant tanks. Moreover, the system is noted to have a new resonant peak whose magnitude response may exceed 0 dB even with a source resistance of $R_s = 0.5\ \Omega$ considered, and this resonant peak may bring in difficulties for damping controller design.

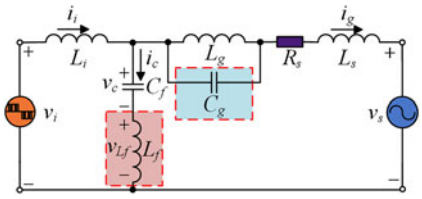


Fig. 4. Simplified circuit of SPRLCL filter.

In order to tackle these issues, this paper proposes a novel SPRLCL filter, and its topology is presented in Fig. 4. As shown, the grid-side inductor L_g is utilized in the SPRLCL filter to form a resonant tank together with C_g for switching harmonic attenuation. In this case, one of the series resonant inductors shown in Fig. 2(c) can be saved to reduce the size and cost of passive filters.

The transfer function $i_g(s)/v_i(s)$ of the SPRLCL filter can be derived as

$$G_L(s) = \frac{i_g(s)}{v_i(s)} = \frac{a_4 s^4 + a_2 s^2 + 1}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{3}$$

where the parameters can be derived as

$$\begin{cases} a_4 = L_f C_f L_g C_g \\ a_2 = L_f C_f + L_g C_g \\ b_5 = L_f C_f L_i L_g C_g + L_i C_g L_g C_g L_s + L_f C_f L_g C_g L_s \\ b_4 = L_i C_f L_g C_g R_s + L_f C_f L_g C_g R_s \\ b_3 = L_i C_f L_s + L_f C_f L_s + L_s L_g C_g + L_i C_f L_g \\ \qquad + L_f C_f L_g + L_i L_g C_g + L_f C_f L_i \\ b_2 = L_i C_f R_s + L_f C_f R_s + L_g C_g R_s \\ b_1 = L_i + L_g + L_s \\ b_0 = R_s. \end{cases}$$

This paper proposes three methods to design the SPRLCL filter. Design method I is to set the series resonance frequency at f_s and the parallel resonance frequency at $2f_s$, while for design method II, the two resonance frequencies are simply swapped.

The Bode plots $i_g(s)/v_i(s)$ of the *LCL* filter and the SPRLCL filters designed with method I and method II are illustrated in Fig. 5(a) and (b), respectively. As can be seen, the SPRLCL filter can inherit the advantages of the *LTCL* filter and provide very sharp harmonic attenuation at f_s and $2f_s$. Moreover, it is also noted that the new resonant peak is now shifted to a higher frequency range as compared to that of the *LTCL* filter shown in Fig. 3. With the same source resistance considered, the magnitude of this resonant peak can now be damped below 0 dB, indicating no stability issue. In fact, such passive damping effects will be more significant in real applications as the ESR of passive components generally increases at high frequencies.

Design method III is to fix both the series resonance frequency and the parallel resonance frequency at f_s to counteract filter parameter variations. The Bode plots $i_g(s)/v_i(s)$ of the *LCL* filter and the SPRLCL filter designed with method III are depicted in Fig. 5(c). Through design method III, the SPRLCL filter loses its attenuation ability at $2f_s$. However, the SPRLCL

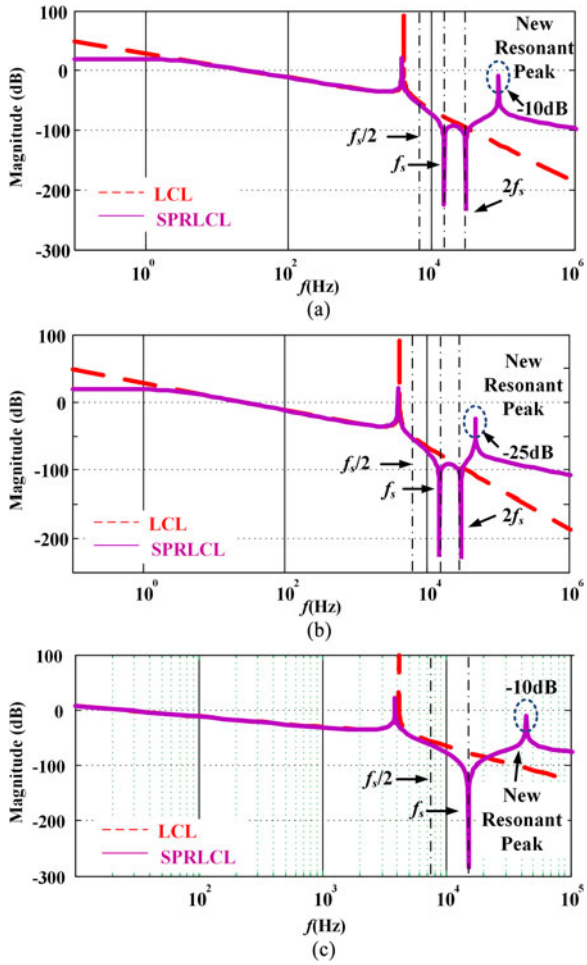


Fig. 5. Bode plots $i_g(s)/v_i(s)$ of *LCL* filter and SPRLCL filter designed with (a) method I, (b) method II, and (c) method III.

filter can maintain the high attenuation at f_s even with parameter deviations as shown in Fig. 6.

For comparison, the Bode plots of the SPRLCL filters designed with method I and method II considering parameter deviations are presented in Fig. 7. It can be seen that the switching-frequency attenuation ability deteriorates without accurate filter parameters.

The filter parameters adopted in this paper are listed in Table I, and the detailed filter parameter design process will be discussed in Section IV.

III. Capacitor-Current-Feedback Active Damping Analysis

A capacitor-current-feedback actively damped *LCL* filter can be modeled as a frequency-dependent virtual resistor in parallel with a frequency-dependent virtual inductor when the effect of computation delay and PWM delay is taken into consideration [11]. Given that the additional capacitor C_g is relatively small, the frequency responses of the SPRLCL filter and the *LCL* filter almost overlap before the Nyquist frequency. Therefore, C_g is ignored here to simplify the analysis. However, the SPRLCL filter contains an additional inductor in the capacitor branch

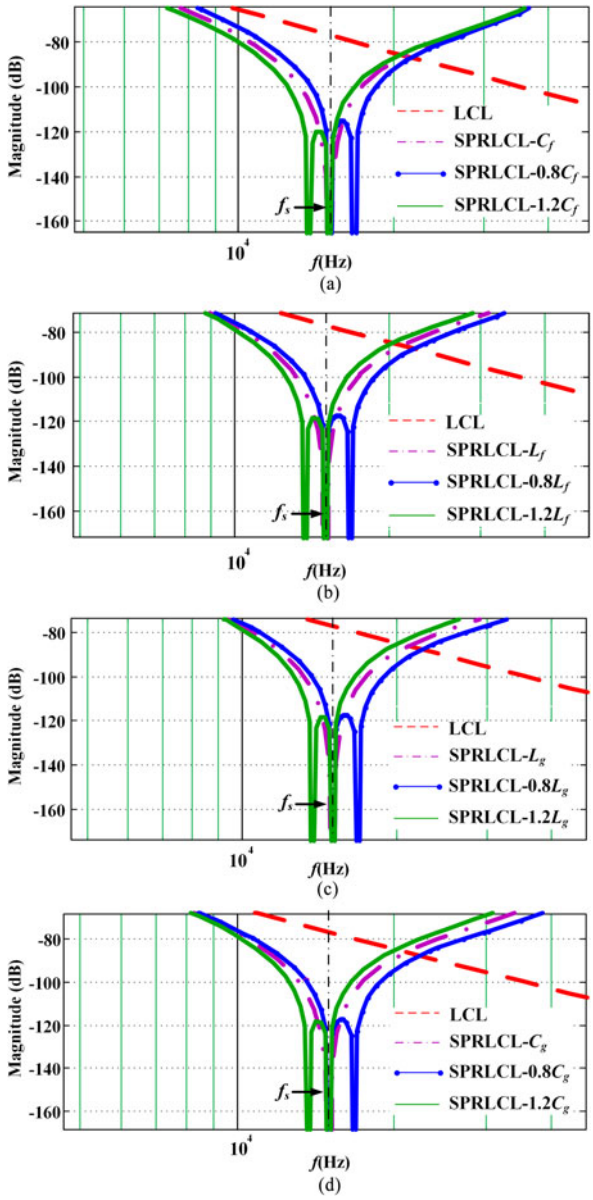


Fig. 6. Bode plots $i_g(s)/v_i(s)$ of *LCL* filter and SPRLCL filter designed with method III with variation of (a) $\pm 20\% C_f$, (b) $\pm 20\% L_f$, (c) $\pm 20\% L_g$, and (d) $\pm 20\% C_g$.

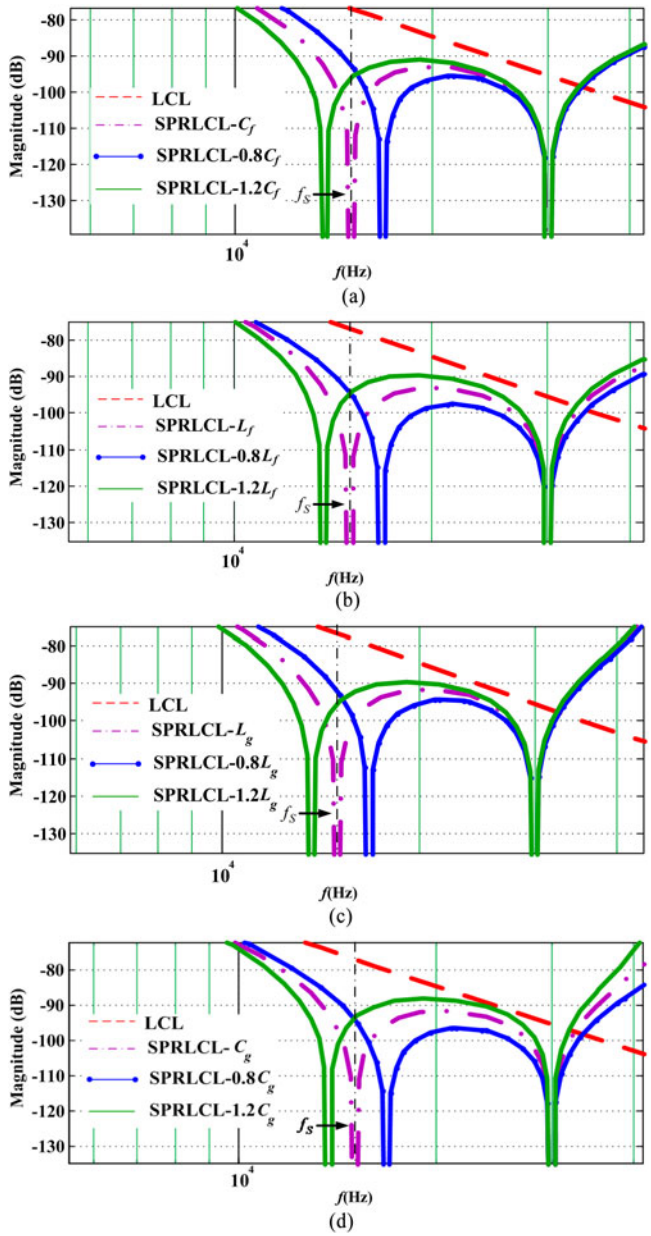


Fig. 7. Bode plots $i_g(s)/v_i(s)$ of SPRLCL filters designed with method I and method II with parameters variation (a) method I: $\pm 20\% C_f$, (b) method I: $\pm 20\% L_f$, (c)method II: $\pm 20\% L_g$, and (d)method II: $\pm 20\% C_g$.

loop, which may influence the active damping performance of the SPRLCL filter and the indices of its controller design. Hence, the capacitor-current-feedback active damping analysis of the SPRLCL filter is derived next.

A. Modeling of SPRLCL Filter

The ASM of the SPRLCL filtered APF current control loop with capacitor-current-feedback active damping and time delay is shown in Fig. 8, where K_{PWM} is the converter gain, T_s denotes the sampling period, and $e^{-1.5Tss}$ denotes the total time delay resulted from digital computation and PWM [12], [33].

In Fig. 8, transferring the feedback branch of H_{i1} to the branch connected between $i_c(s)$ and $v_c(s)+v_{Lf}(s)$, the equivalent virtual impedance $Z_{\mathrm{eq}}(s)$ connected in parallel with the capacitor branch loop can be obtained and derived by substituting $j\omega$ for s as

$$\begin{aligned} Z_{\mathrm{eq}}(j\omega) &= R_{\mathrm{eq}}(\omega)//jX_{\mathrm{eq}}(\omega) \\ &= \frac{L_i(1-L_fC_f\omega^2)}{H_{i1}K_{\mathrm{PWM}}C_f}e^{j\omega 1.5T_s} \\ &= R_d(\omega)e^{j\omega 1.5T_s} \\ &= R_d(\omega)\cos(1.5\omega T_s)+jR_d(\omega)\sin(1.5\omega T_s) \quad (4) \end{aligned}$$

TABLE I
FILTER PARAMETERS

Parameter	*LLCL* value	SPRLCL value (method I)	SPRLCL value (method II)	SPRLCL value (method III)
L_i	1.5 mH	1.0 mH	1.0 mH	1.5 mH
C_f	1.7 μF	3.0 μF	3.0 μF	1.7 μF
L_g	1.0 mH	0.5 mH	0.5 mH	1.0 mH
L_f	66.67 μH	37.04 μH	9.26 μH	66.67 μH
C_g	–	56.29 nF	225.16 nF	112.58 nF

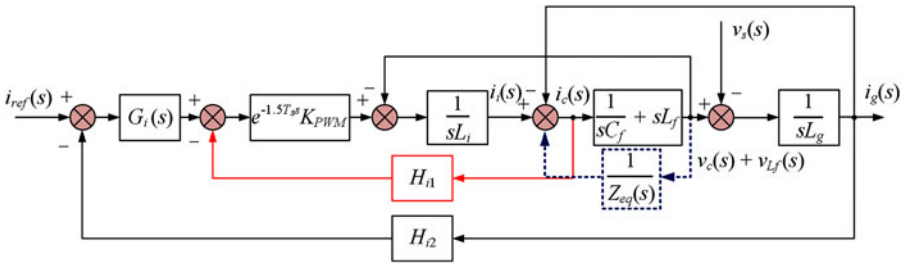


Fig. 8. ASM of SPRLCL filtered APF current control loop with capacitor-current-feedback active damping and time delay.

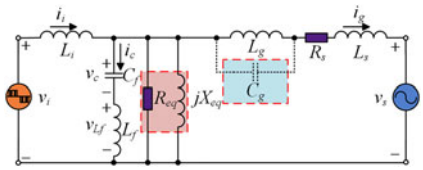


Fig. 9. Equivalent virtual impedance of capacitor-current-feedback actively damped SPRLCL filter.

where

$$R_{\rm eq}(\omega)=\frac{R_d(\omega)}{\cos(1.5\,\omega T_s)},\ X_{\rm eq}(\omega)=\frac{R_d(\omega)}{\sin(1.5\,\omega T_s)}. \tag{5}$$

$R_d(\omega)=L_i(1-L_fC_f\omega^2)/(H_{i1}K_{\rm PWM}C_f)$ represents the equivalent virtual parallel resistor without considering time delay. The virtual impedance of the *LCL* filter can be obtained with $L_f=0$. It can be found that the essence of the capacitor-current-feedback actively damped SPRLCL filter is to parallel a frequency-dependent virtual resistor and a frequency-dependent virtual inductor with the capacitor branch loop, as shown in Fig. 9.

It is also noted that R_d is frequency dependent for SPRLCL filters but not for *LCL* filters [13], [14], and this difference may slightly change the system high-frequency response. The absolute value of $R_{\rm eq}(\omega)$ determines the damping effect, and a smaller value represents a better resonance damping. The absolute value of $X_{\rm eq}(\omega)$ changes the resonance frequency, and a smaller value leads to a larger resonance frequency shift. Fig. 10 shows the values of $R_{\rm eq}(\omega)$ and $X_{\rm eq}(\omega)$ with variable frequencies for the *LCL* filter and the SPRLCL filter designed with method I. As can be seen from Fig. 10(a), the equivalent resistance $R_{\rm eq}$ of the SPRLCL filter remains positive in the frequency band $(0,\ f_s/6)$ and then becomes negative in $(f_s/6, f_s/2)$. $R_{\rm eq}$ reaches the minimum value at $f_s/3$ before the Nyquist frequency, and this implies that designing f_r to be $f_s/3$ will give the best active damping performance. In contrast, designing f_r to be $f_s/6$ should be avoided as $R_{\rm eq}$ becomes infinite, indicating no damping effect. Similarly, the equivalent inductance $X_{\rm eq}$ can also be plotted as a function of frequency shown in Fig. 10(b). At $f_s/3$, $X_{\rm eq}$ is noted to be infinite, and, thus, it can be ignored from the equivalent circuit shown in Fig. 9. This characteristic is actually desired in the design as the SPRLCL resonance frequency will be solely determined by the parameters of the passive components.

If $f_r=f_s/3$ cannot be satisfied, the resonance frequency will be affected by the capacitor-current-feedback loop as shown in Fig. 11(a) and (c). A larger feedback coefficient H_{i1} may give rise a more significant frequency drift as the value of $X_{\rm eq}$ becomes smaller as discussed. Therefore, it can be concluded from these figures that setting $f_r=f_s/3$ can offer the optimal design as the damping effect of capacitor-current feedback can be maximized and the resonance frequency will always be fixed at $f_s/3$. These two features may greatly facilitate the current controller design as well as its performance evaluation.

B. Performance Indices of SPRLCL Filter

The loop gain in Fig. 8 can be derived as

$$T(s)=\frac{H_{i2}K_{\rm PWM}e^{-1.5T_s s}G_i(s)(L_fC_fs^2+1)}{L_gC_fs^2(L_is+K_{\rm PWM}e^{-1.5T_s s}H_{i1})+(L_i+L_g)(L_fC_fs^2+1)s}. \tag{6}$$

Below or at the crossover frequency f_c, the *LC* tank has a relatively large impedance and the SPRLCL filter can be simplified to be an inductor L_i+L_g. Suppose that the controller $G_i(s)$ is a simple proportional controller with a gain K_P, $|T(s)|$

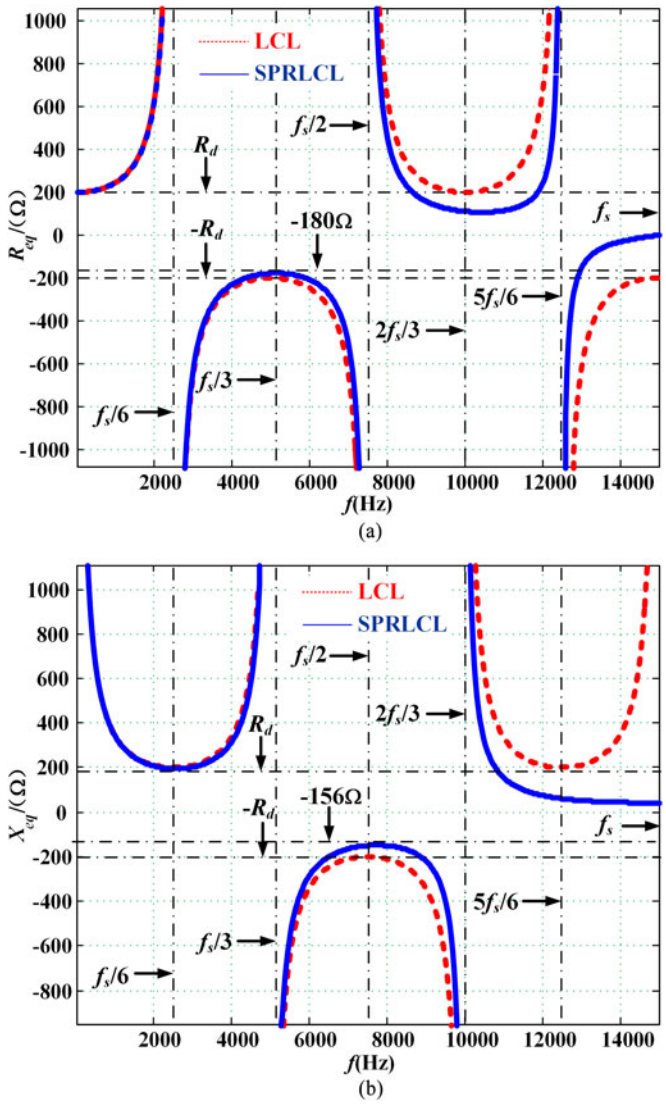


Fig. 10. Values of (a) $R_{\mathrm{eq}}(\omega)$ and (b) $X_{eq}(\omega)$ with variable frequency.

can be simplified at f_c as

$$|T(j2\pi f_c)| \approx \frac{H_{i2}K_{\mathrm{PWM}}K_P}{(L_i+L_g)2\pi f_c}. \tag{7}$$

K_P can be expressed as

$$K_P \approx \frac{(L_i+L_g)2\pi f_c}{H_{i2}K_{\mathrm{PWM}}} \tag{8}$$

In z-domain, the loop gain can be derived as (9) shown at the bottom of the page. In (9)

$$\omega_r = 2\pi f_r = \sqrt{\frac{L_g+L_i}{L_gC_f(L_i+L_f)}}. \tag{10}$$

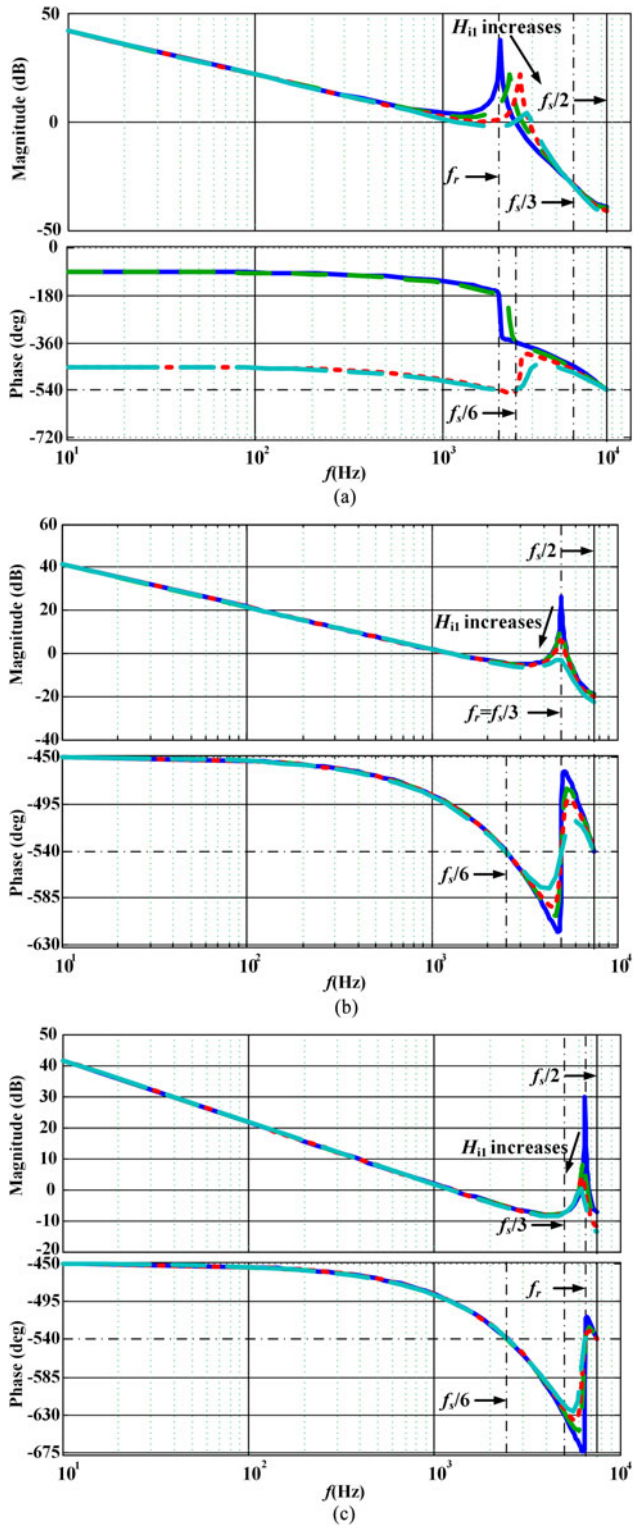


Fig. 11. Bode plots of loop gain T(z) with variable H_{i1} when (a) $f_r < f_s/3$, (b) $f_r = f_s/3$, (c) $f_r > f_s/3$.

$$T(z) = \frac{G_i(z)H_{i2}K_{\mathrm{PWM}}}{(L_g+L_i)\omega_r} \frac{[z^2-2z\cos(\omega_rT_s)+1]T_s\omega_r + (L_fC_f\omega_r^2-1)(z-1)^2\sin(\omega_rT_s)}{(z-1)\left\{z[z^2-2z\cos(\omega_rT_s)+1] + H_{i1}K_{\mathrm{PWM}}\frac{(z-1)\sin(\omega_rT_s)}{\omega_r(L_i+L_f)}\right\}} \tag{9}$$

According to the controller design process in [17], several performance indices are necessary to derive. Let GM_1 denote the gain margin of the SPRLCL filter at the resonance frequency f_r, GM_1 is expressed as

$$\mathrm{GM}_1 = -20\lg\left|T(j2\pi f_r)\right|. \tag{11}$$

The relationship of the capacitor-current-feedback coefficient H_{i1} and GM_1 can be derived as

$$H_{i1} = 10^{\mathrm{GM}_1/20}\frac{[1-L_fC_f(2\pi f_r)^2]2\pi f_c(L_i+L_f)}{K_{\mathrm{PWM}}}. \tag{12}$$

Let GM_2 represents the gain margin of the SPRLCL filter at $f_s/6$, GM_2 is defined as

$$\mathrm{GM}_2 = -20\lg\left|T(j2\pi f_s/6)\right|. \tag{13}$$

The expression of H_{i1} represented by GM_2 can be derived as

$$\begin{aligned} H_{i1} = {} & 10^{\mathrm{GM}_2/20}\frac{(L_i+L_g)(1-L_fC_f\left(2\pi\frac{f_s}{6}\right)^2)f_c}{2\pi L_gC_fK_{\mathrm{PWM}}}\left(\frac{6}{f_s}\right)^2 \\ & + \left(\frac{f_s}{6}\right)\frac{2\pi L_i}{K_{\mathrm{PWM}}} + \left(\frac{f_s}{6}\right)\frac{L_ff_c(L_i+L_g)}{K_{\mathrm{PWM}}} - \left(\frac{6}{f_s}\right) \\ & \times \left(\frac{1}{2\pi}\right)\frac{(L_i+L_g)}{L_gC_fK_{\mathrm{PWM}}} \end{aligned} \tag{14}$$

Note that $\mathrm{GM}_1 < 0$ dB and $\mathrm{GM}_2 > 0$ dB must be satisfied when $f_r > f_s/6$ [17]. The phase margin PM can be derived by calculating the phase of $T(j\omega_c)$ shown in (15) at the bottom of the page, where $\omega_c = 2\pi f_c$.

Let T_{fo} denote

$$T_{fo} = 20\lg\left|T(j2\pi f_o)\right| \tag{16}$$

where f_o stands for the fundamental frequency. The expression of H_{i1} represented by PM and T_{fo} can be derived as (17) shown at the bottom of the page.

The above performance indices are necessary for the current-loop controller design.

IV. SPRLCL Filter Parameter Design

In this section, the parameter design procedure of the SPRLCL filter is presented and applied to a half-bridge APF with sine-triangle symmetrical-regular-sampled PWM. It should be noted that the converter output harmonics may be changed with circuit topologies and modulation techniques [29], [30]. However, the same design approach is still applicable.

A. Requirements for Filter Design

When designing passive filters for APF applications, several limitations must be considered [3], [6], [11], [19], [24], [25]. The following requirements can be used to determine the values of L_i, C_f, and L_g.

1) Requirement of Resonance Frequency f_r: As discussed in the previous section, $f_r = f_s/3$ is preferred as the resonance frequency can be fixed and the equivalent parallel damping resistance can be minimized. In addition to this, some other limitations should be considered to judge whether setting $f_r = f_s/3$ is a proper design. First, the bandwidth of the current controller f_c must be wide enough to compensate the dominant current harmonics produced by the nonlinear load [24], [25], described as

$$f_c \geq k_a f_o \tag{18}$$

where k_a stands for the highest order of harmonics to be compensated. Second, the ratio of f_r to f_c must be large enough. This requirement guarantees that the phase margin of the current controller is sufficient [11], [24], described as

$$f_r \geq f_c/0.3. \tag{19}$$

Third, f_r must be designed to be away from the critical frequency $f_s/6$. Furthermore, the resonance frequency f_r should be large enough in order to save filter elements [11], [19]. Hence, the following equation should be satisfied:

$$f_r > f_s/6. \tag{20}$$

Fourth, to ensure the controllability of the digital current controller, f_r should be designed below the Nyquist frequency $f_s/2$ [6], [19]

$$f_r < f_s/2. \tag{21}$$

With $f_r = f_s/3$, (20) and (21) can be satisfied. In most cases, $f_r = f_s/3$ provides a wide enough bandwidth f_c [24], [25]. Thus, $f_r = f_s/3$ is chosen as a design requirement.

2) Requirement of Harmonic Attenuation: As required by IEEE standard 1547.2-2008 and IEEE standard 519-1992, the switching-frequency and multiple switching-frequency harmonics should be limited to be less than 0.3% of the fundamental current [28], [29], represented as

$$\begin{aligned} & \left|G_L(j2\pi f)\right|_{f=Nf_s(N=1,2,3\ldots)} \\ & = \left|\frac{i_g(j2\pi f)}{v_i(j2\pi f)}\right|_{f=Nf_s(N=1,2,3\ldots)} \leq \frac{0.3\%I_{\mathrm{ref}}}{V_{\mathrm{inv}}(2\pi f)} \end{aligned} \tag{22}$$

$$PM = \frac{\pi}{2} - 3\pi f_cT_s - \arctan\frac{2\pi f_cL_gC_fK_{\mathrm{PWM}}H_{i1}\cos(3\pi f_cT_s)}{-(2\pi f_c)^2[L_iL_gC_f+(L_i+L_g)L_fC_f]+2\pi f_cL_gC_fK_{\mathrm{PWM}}H_{i1}\sin(3\pi f_cT_s)+(L_i+L_g)} \tag{15}$$

$$H_{i1} = \frac{\{-(2\pi)f_c^2[L_i+(L_i/L_g+1)L_f]+(L_i+L_g)/(2\pi L_gC)\}\{f_c^2 - f_o\sqrt{(10^{T_{fo}/20}f_o)^2-f_c^2}\tan(3\pi f_cT_s+PM)\}/(f_cG_{\mathrm{inv}})}{f_c^2[\cos(3\pi f_cT_s)\tan(3\pi f_cT_s+PM)-\sin(3\pi f_cT_s)]+f_o\sqrt{(10^{T_{fo}/20}f_o)^2-f_c^2}[\cos(3\pi f_cT_s)+\sin(3\pi f_cT_s)\tan(3\pi f_cT_s+PM)]} \tag{17}$$

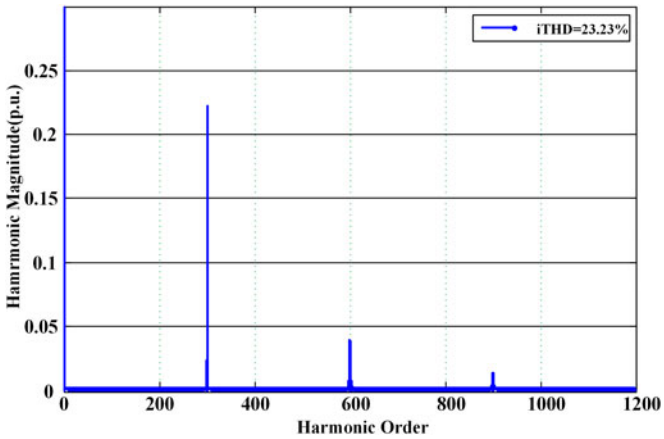


Fig. 12. Harmonic current spectrum of a single inductor L_i filtered APF.

where $I_{\rm ref}$ denotes the root-mean-square (RMS) value of the fundamental reference current. $V_{\rm inv}(2\pi f)$ represents the RMS value of the output voltage in the inverter side. G_L can also be replaced by G_{L1} if the *LLCL* filter is designed. When the filter inductors L_i and L_g are fixed, this requirement determines the minimum value of C_f [25]. It should be noted that circuit topologies (e.g., half-bridge, full-bridge), modulation methods (e.g., symmetrical-regular-sampled PWM, asymmetrical-regular-sampled PWM), dc-link voltage $V_{\rm dc}$, and modulation index can change the RMS value of the inverter output voltage $V_{\rm inv}(2\pi f)$. For a half-bridge APF, the inverter output voltage $v_i(t)$ in the time domain can be derived as [29]

$$v_i(t) = \frac{4V_{\rm dc}}{\pi}\sum_{\substack{m=0\\ m>0}}^{\infty}\sum_{\substack{n=1\\ n=-\infty}}^{\infty}\frac{1}{q}J_n\left(q\frac{\pi}{2}M\right)\sin \times\left([q+n]\frac{\pi}{2}\right)\cos(m\omega_s t+n\omega_o t) \quad (23)$$

where M is the modulation index, m represents the order of multiple switching frequency, n represents the order of multiple fundamental-frequency sideband, and $q = m + n(\omega_o/\omega_s)$, $J_n(x)$ is referred as the integrals of the Bessel function, expressed as

$$J_n(x) = \frac{1}{2\pi}\int_0^{2\pi}\cos(nt - x\sin t)dt. \quad (24)$$

Fig. 12 shows the current harmonic spectrum of a single inductor filtered APF under the condition of $V_{\rm dc} = 400$ V, $M = 220/400 = 0.55$, $f_s = 15$ kHz, $L_i = 2$ mH, and $P = 2$ kW. It can be noted that the switching-frequency sideband and double switching-frequency sideband current harmonics may exceed the IEEE limit, and this is the main motivation of designing more advanced high-order passive filters.

3) Requirement of Capacitor C_f: Reactive power consumed by C_f should be less than 5% of the rated power capacity of APF [6]:

$$C_f \le \frac{5\%P}{v_c^2\omega_o} \approx \frac{5\%P}{v_s^2 2\pi f_o} \quad (25)$$

TABLE II
SYSTEM PARAMETERS

Parameter	Symbol	Value
Fundamental frequency	f_o	50 Hz
Switching/Sampling frequency	f_s	15 kHz
Grid voltage (RMS)	V_s	220 V
Source resistance	R_s	0.05 Ω
Source inductance	L_s	0.1–3 mH
IGBT	S_1/S_2	1200 V, 50 A
DC-link voltage	$V_{\rm dc}$	400 V
DC-link capacitance	C_1/C_2	4700 μF
Resonance frequency	f_r	5000 Hz
Rated power	P	2 kW
Load resistance	R_{ls}/R_{lp}	10/20 Ω
Load capacitance	C_l	4700 μF

where P denotes the rated power capacity of APF. Considering the variation of source impedance, the design requirement is that the actual resonant frequency $f_r{}'$ should be always higher than the critical frequency $f_s/6$. This requirement is a prerequisite for the stability of the current controller, which is often ignored in the previous literatures. It can be derived as

$$f_{r\_\infty} = \frac{1}{2\pi}\sqrt{\frac{1}{L_i C_f}} \ge f_s/6, C_f \le \frac{9}{L_i f_s^2 \pi^2} \quad (26)$$

where f_{r_∞} represents the resonance frequency under the worst-case scenario where the source inductance is infinite. In real applications, the source inductance can only vary in a certain range [2]. Therefore, this requirement guarantees that the resonance frequency would not approach the critical frequency $f_s/6$. This requirement (i.e., (25) and (26)) sets the maximum value of C_f when the inductances are fixed.

4) Requirement of Inductors L_i and L_g: The fundamental voltage drop on the inductors should be lower than 10% RMS value of v_s [3], [6]. This requirement gives the upper limit of $L_i + L_g$

$$L_i + L_g \le \frac{0.1V_s}{\omega_o I_{\rm ref}} \quad (27)$$

where V_s denotes the RMS value of the grid voltage. The output current of APF should be able to track the reference current, and in steady state, the following equation should be satisfied:

$$L_i + L_g \le \frac{V_{\rm dc} - V_{s\_\rm peak}}{\omega_o I_{\rm ref\_peak}} \quad (28)$$

where $V_{s\_\rm peak}$ denotes the peak value of the grid voltage. $I_{\rm ref\_peak}$ denotes the peak value of the fundamental reference current, and $V_{\rm dc}$ is the dc-link voltage. For dynamic reference current tracking [25]

$$L_i + L_g \le \frac{V_{\rm dc} - V_{s\_\rm peak}}{2k_a\omega_o\left|i_c^*\right|_{\max}} \quad (29)$$

where $|i_c^*|_{\max}$ denotes the maximum value of harmonic currents.

5) Requirement of Inductor L_i: In order to protect the IGBTs and prevent the inverter-side inductor from saturation, the value of the inverter-side inductor should be designed based on the

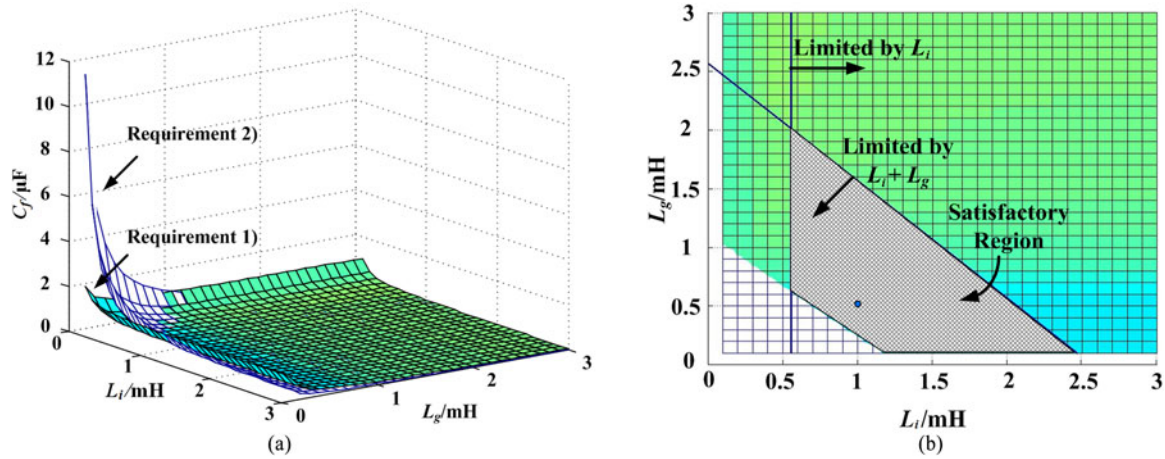


Fig. 13. Satisfactory region of SPRLCL filter designed with method I or method II: (a) 3-D plot and (b) *xy* view.

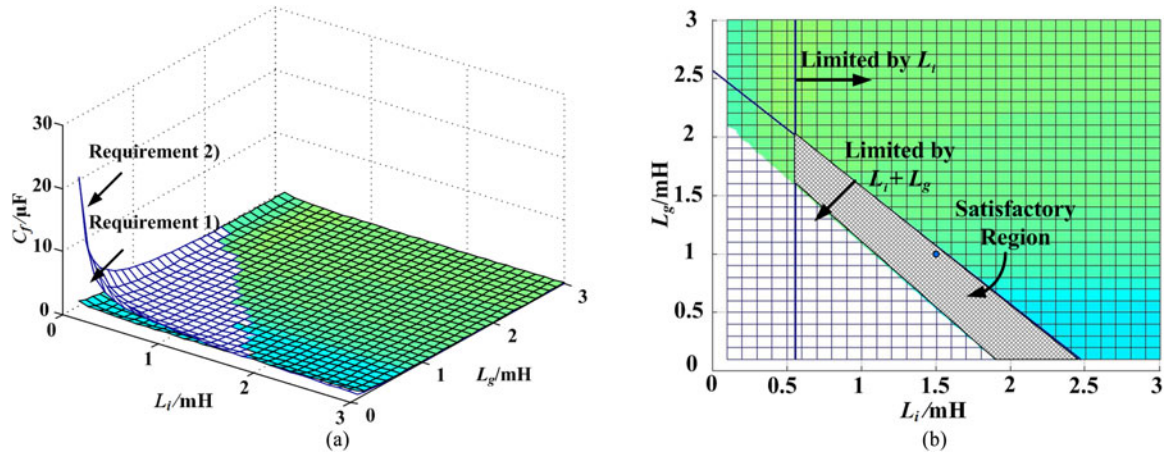


Fig. 14. Satisfactory region of SPRLCL filter designed with method III (a) 3-D plot and (b) *xy* view.

following equation:

$$\frac{\Delta I}{I_{\rm ref}} = \frac{V_{\rm dc}}{4L_i f_s I_{\rm ref}} \leq 60\% \tag{30}$$

where ΔI represents the peak value of the current ripple in the inverter side, and the ratio of ΔI to $I_{\rm ref}$ is less than 60% in this case [4].

Given that the aforementioned requirements are all satisfied, smaller inductance and capacitance should be selected to minimize the cost and size of passive filters.

B. Design Procedure of SPRLCL Filter

In this section, the SPRLCL filter will be designed based on the parameters listed in Table II, but the same design approach can be applied to other systems without the loss of generality. Several additional parameters can be derived from Table II: fundamental angular frequency $\omega_o = 2\pi f_o = 314$ rad/s; switching-angular frequency $\omega_s = 2\pi f_s = 94248$ rad/s; highest order compensated current harmonics $k_a = 25$; base impedance $Z_b = V_s^2/P = 24.2\ \ \Omega$; base inductance $L_b = Z_b/\omega_o = 77.07$ mH; base capacitance $C_b = 1/(Z_b\omega_o) = 131.60\ \mu$F; RMS value of the fundamental reference current $I_{\rm ref} = P/V_s = 9.09$ A; bandwidth of the current controller $f_c = kf_o = 1250$ Hz; critical frequency $f_s/6 = 2500$ Hz; resonance frequency $f_r = f_s/3 = 5000\,{\rm Hz} > f_c/0.3$. Then, a step-by-step design procedure of the SPRLCL filter is given as follows.

1) Draw a 3-D plot with a curved-surface based on requirement 1 $f_r = f_s/3 = 5000\,{\rm Hz}$, shown as the shaded curved surface in Fig. 13(a). *x*-axis and *y*-axis represent the values of inverter-side inductor L_i and grid-side inductor L_g, respectively. z-axis shows the value of capacitor C_f. With a fixed resonance frequency, C_f increases with the decrease of L_i and L_g.
2) According to requirement 2, the minimum necessary value of C_f under certain L_i and L_g can be derived, shown as the uncolored curved surface in Fig. 13(a). Note that for the SPRLCL filter designed with method I or method II, the main objective of requirement 2 is to attenuate the triple switching-frequency current harmonics down to 0.3% of the fundamental reference current. As for the SPRLCL filter designed with method III, requirement 2 is to attenuate double switching-frequency

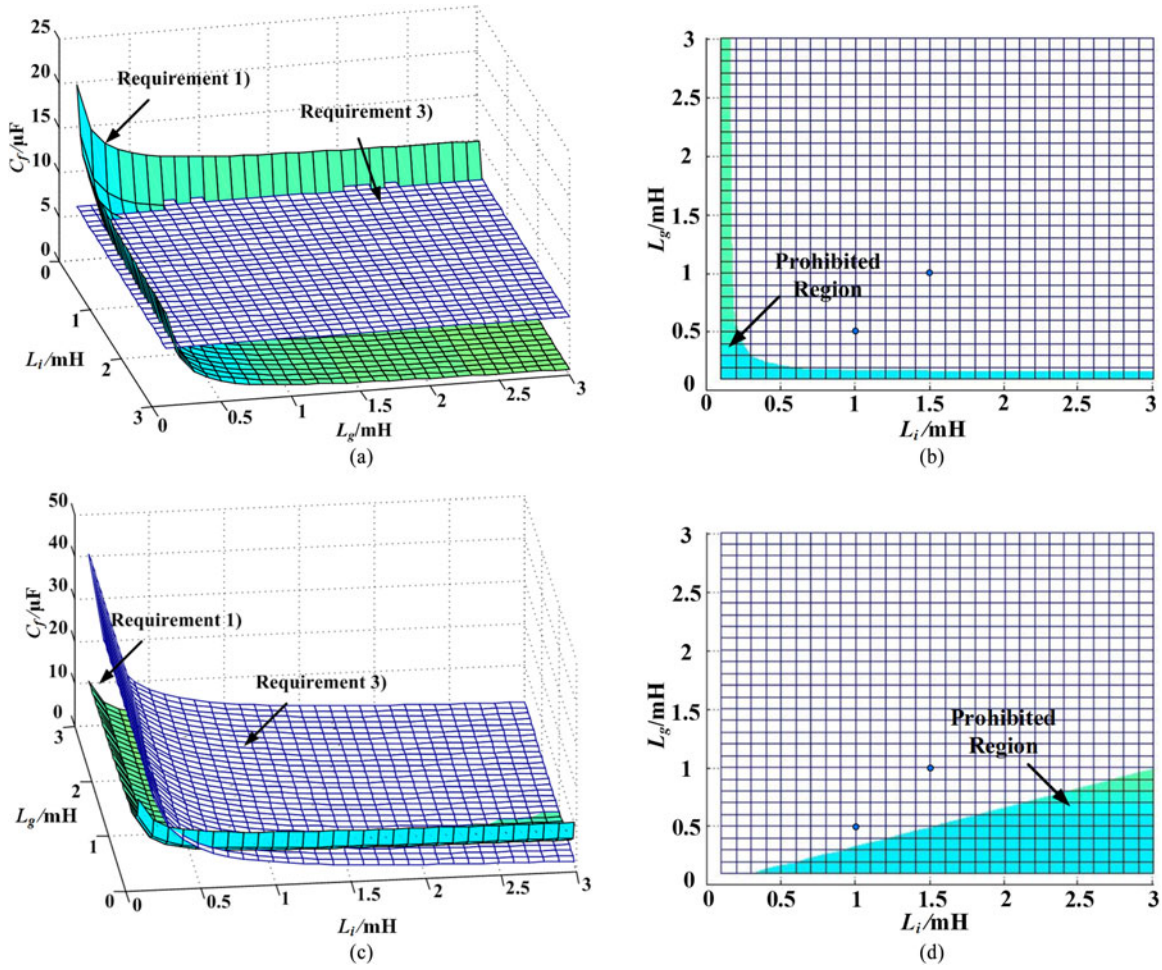


Fig. 15. Prohibited region of SPRLCL filter. (a) 3-D plot of (25), (b) *xy* view of (25), (c) 3-D plot of (26), and (d) *xy* view of (26).

current harmonics down to 0.3% of the fundamental reference current. When the uncolored curved surface is above the shaded curved surface, the filter parameters may fail to meet this requirement. Fig. 13(b) shows the *xy* view of Fig. 13(a). Thus, the satisfactory region is inscribed in the shaded region drawn in Fig. 13(b).

3) According to requirements 4 and 5, the maximum value of $L_i + L_g$ and the minimum value of L_i also limit the satisfactory region. These requirements can be added into the *xy* planes as shown in Fig. 13(b). Then, the satisfactory region can be obtained as the meshed area in Fig. 13(b). Similarly, the satisfactory region of the SPRLCL filter designed with method III is illustrated in Fig. 14.
4) According to requirements 3, the maximum value of C_f can be derived from (25) and (26). Fig. 15(a) and (b) shows the prohibited region based on (25). As can be seen, the additional requirement constructs a new constant value C_f plane. The value of C_f above this plane is not permmitted according to requirements 3, the maximum value of C_f can be derived from (25) and (26).

Fig. 15(a) and (b) shows the prohibited region based on (25). As can be seen, the additional requirement constructs a new constant value C_f plane. The value of C_f above this plane is not permitted, as shown in the prohibited region in Fig. 15(b). Fig. 15(c) and (d) depicts the prohibited region based on (26). This additional requirement creates another uncolored curved surface. The value of C_f above the shaded one is not allowed, as shown in the prohibited region in Fig. 15(d).

5) With the above plots, the values of L_i and L_g can be chosen based on Figs. 13 or 14. If these values are located in the prohibited region shown in Fig. 15, another pair of L_i and L_g should be designed. Then, C_f can be calculated using $f_r = f_s/3$ and the following equation:

$$C_f = \frac{L_g + L_i}{L_g L_i (2\pi f_r)^2}. \tag{31}$$

The additional inductor L_f in the *LLCL* filter can be derived from

$$\omega_s = 2\pi f_s = \sqrt{\frac{1}{L_f C_f}}. \tag{32}$$

The additional inductor L_f and the additional capacitor C_g in the SPRLCL filter are determined by the following equations:

TABLE III
CONTROLLER PARAMETERS

Parameter	Value	Parameter	Value
K_P	18.85	H_{i1}	2
N_s	300	$Q(z)$	0.95
K_r	2	k_s	4
H_{i2}	1	K_{PD}	0.1
K_{PU}	2	K_{IU}	0.2

Method I

$$\omega_s = 2\pi f_s = \sqrt{\frac{1}{L_f C_f}}, \quad 2\omega_s = 4\pi f_s = \sqrt{\frac{1}{L_g C_g}}. \tag{33}$$

Method II

$$2\omega_s = 4\pi f_s = \sqrt{\frac{1}{L_f C_f}}, \quad \omega_s = 2\pi f_s = \sqrt{\frac{1}{L_g C_g}}. \tag{34}$$

Method III

$$\omega_s = 2\pi f_s = \sqrt{\frac{1}{L_f C_f}}, \quad \omega_s = 2\pi f_s = \sqrt{\frac{1}{L_g C_g}}. \tag{35}$$

6) Finally, the filter parameters should be checked and satisfy all of the requirements. The design procedure involves six steps, and every step is clear and straightforward.

Following these design steps, all the parameters of the *LLCL* filter and the SPRLCL filters with three different design methods can be obtained as listed in Table I. It should be noted that $f_r' > 1/6 f_s$ can be always guaranteed for the designed four sets of passive filters thanks to the consideration of source inductance variation in (26).

V. CONTROLLER DESIGN OF SPRLCL FILTER

A. Current-Loop Proportional Controller Design

Based on the filter parameters in Table I, a proportional controller is designed using the performance indices derived from Section III-B. The controller is designed based on the SPRLCL filter with method III, but the idea can be equally applicable to the SPRLCL filters with design method I and method II. In order to yield a satisfactory steady-state performance and a fair transient-state performance, the indices are set to be: phase margin PM $= 45°$, crossover frequency $f_c = 1250$ Hz, magnitude at the fundamental frequency $T_{fo} = 30$ dB, gain margin $GM_1 < -3$ dB, gain margin $GM_2 > 3$ dB. From (8), K_P can be calculated as $K_P = 18.85$. According to (12) to (17), the satisfactory region of H_{i1} can be derived as $(-11.968, 7.357)$, H_{i1} is chosen to be 2 in this paper. The controller parameters are listed in Table III.

When an *LCL* filter is designed with the same filter parameters and performance indices (the relevant formulas are given in [17]), the corresponding satisfactory region of H_{i1} is $(-10.535, 8.007)$. The satisfactory regions of H_{i1} with variable f_c for the SPRLCL filter designed with method III and the *LCL* filter are illustrated in Fig. 16.

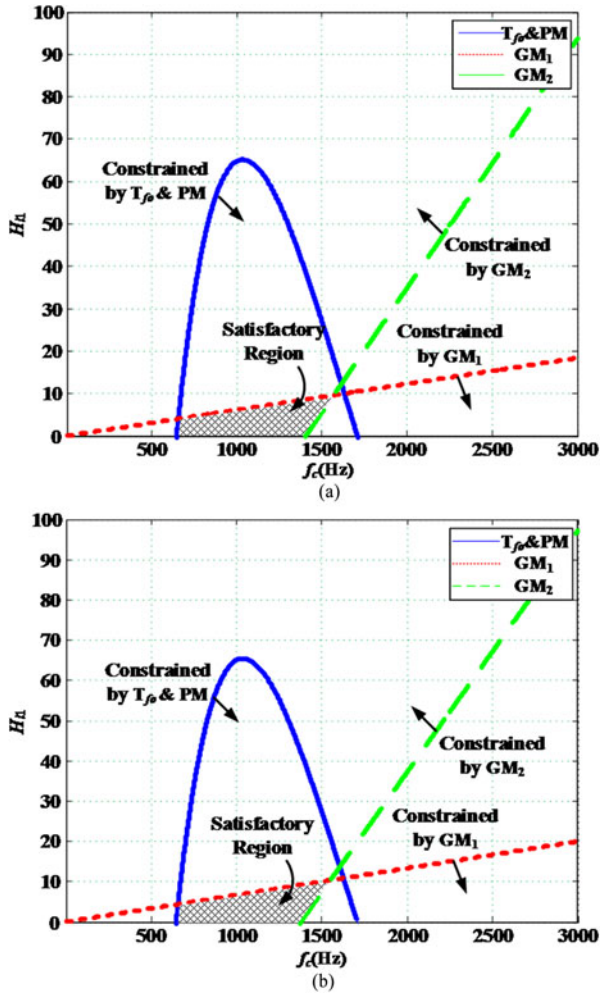


Fig. 16. Satisfactory regions of H_{i1} with variable f_c for (a) SPRLCL filter and (b) *LCL* filter.

With $K_P = 18.85$ and $H_{i1} = 2$, the Bode plots of the proportional-controller-based current-loop gain of the SPRLCL filter and the *LCL* filter are depicted in Fig. 17. As can be seen, PM $= 45°$, $f_c = 1260$ Hz, $T_{fo} = 30$ dB, $GM_1 < -3$ dB, $GM_2 > 3$ dB can be obtained as expected.

Compared with the *LCL* filter, the absolute value of GM_1 of the SPRLCL filter is smaller and the absolute value of GM_2 of the SPRLCL filter is larger. Thus, GM_1 requirement of the SPRLCL filter is more difficult to achieve, whereas GM_2 requirement of the SPRLCL filter is easier to satisfy as compared with the *LCL* filter. However, the difference is relatively small. Therefore, the additional series inductor in the capacitor branch loop poses negligible control difficulties when the series resonance frequency is designed at f_s.

B. Current-Loop Proportional Plus Repetitive Controller Design

As seen in Fig. 17, the current-loop gains at the fundamental frequency and low-order harmonic frequencies, e.g., 100, 150 Hz, etc., are still low, which leads to a large steady-state

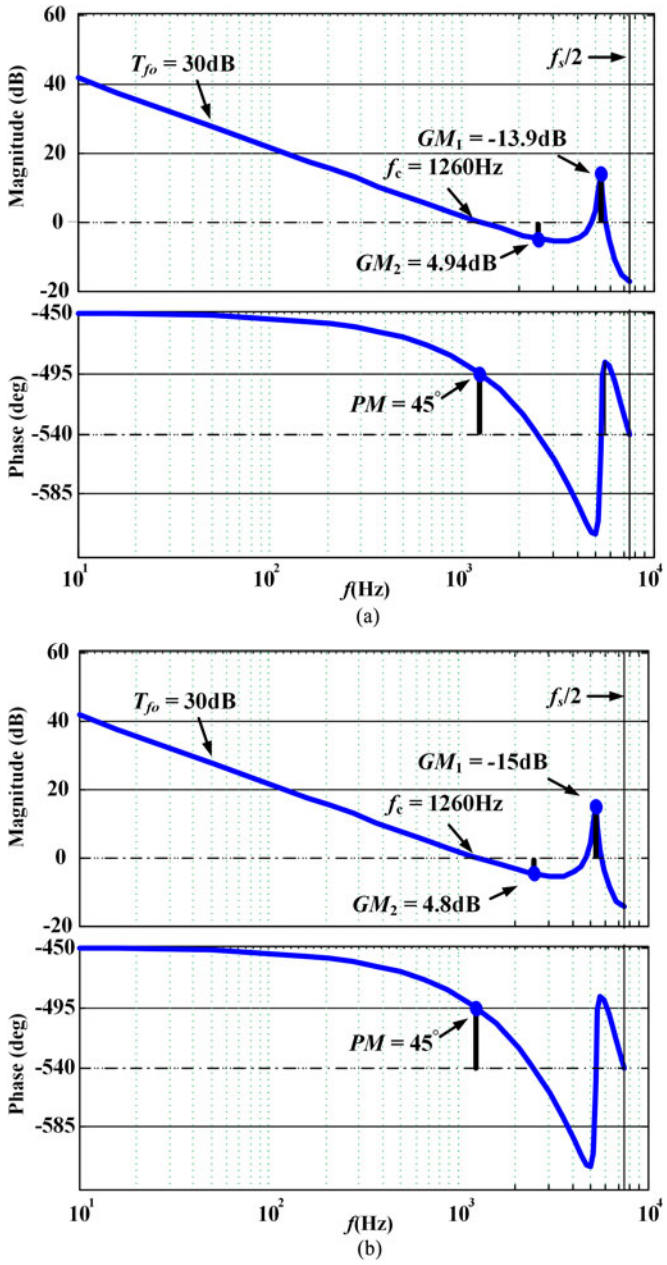


Fig. 17. Bode plots of proportional controller-based current-loop gain of (a) SPRLCL filter and (b) *LCL* filter.

tracking error. Thus, a repetitive controller is paralleled with the proportional controller to enhance the steady-state performance of the current-loop controller. Fig. 18 shows the block diagram of the current-loop proportional plus repetitive controller, where N_s stands for the number of switching-period delay to achieve one fundamental-period delay. Q(z) is a constant or a LPF to stabilize the system. K_r represents the gain coefficient, and k_s denotes the number of the leading switching period to compensate the phase lag. S(z) is selected to be a LPF [31] or a notch filter [32] to suppress high-frequency noises and is designed to be a second-order Butterworth LPF with a cut-off frequency of 1000 Hz. The Bode plot of the proportional plus repetitive-controller-based current-loop gain of the SPRLCL filter is

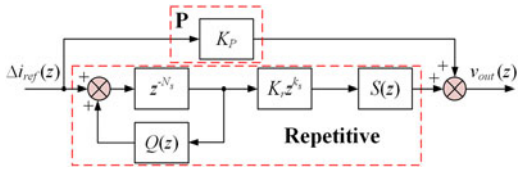


Fig. 18. Block diagram of $G_i(z)$ with proportional plus repetitive controller.

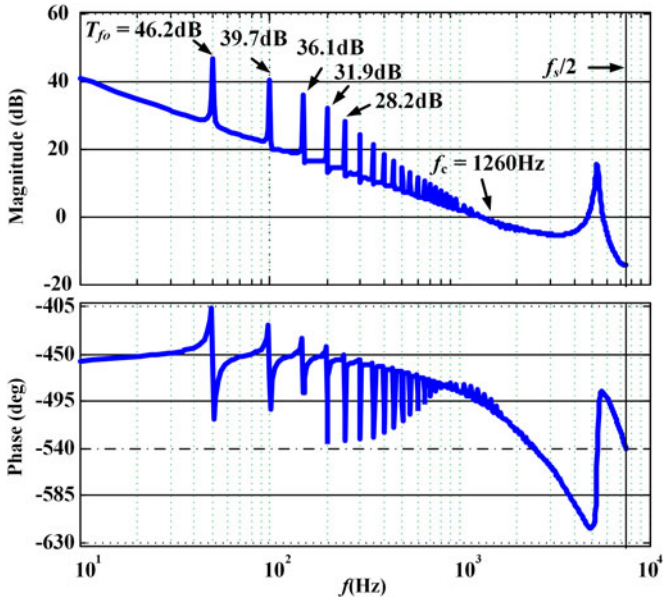


Fig. 19. Bode plot of proportional plus repetitive controller-based current-loop gain.

depicted in Fig. 19. As can be noted, the fundamental frequency and low-order harmonics-frequency-loop gain increases, and, thus, results in smaller current-loop tracking error.

VI. Simulation and Experimental Results

A. Simulation Results

With the parameters listed in Table I–Table III, a simulation model was constructed in MATLAB/Simulink based on the system configuration shown in Fig. 1. The objectives are to examine the effectiveness of the proposed SPRLCL filter design methods and to compare the performance of SPRLCL filters with that of *LLCL* and *LCL* filters.

The simulated steady-state waveforms of the grid voltage v_s, the source current i_s, the grid-side current i_g, the load current i_L, and the dc-link voltages $V_{\rm dc1}$ and $V_{\rm dc2}$ using the *LCL* filter are shown in Fig. 20(a). As can be seen, the sum of the dc-link voltage $V_{\rm dc1}$ and $V_{\rm dc2}$ approximates 800 V, and the error is less than 1 V (0.125%) due to the voltage-loop PI controller. The voltage difference between $V_{\rm dc1}$ and $V_{\rm dc2}$ is less than 2 V (0.5%) because of the voltage-loop proportional controller. The total harmonic distortion (THD) of the load current is 30.49%. Fig. 20(b) shows the spectrum of the compensated source current. As can be seen, although the low-order harmonics can be attenuated to meet IEEE standard 519-1992, the

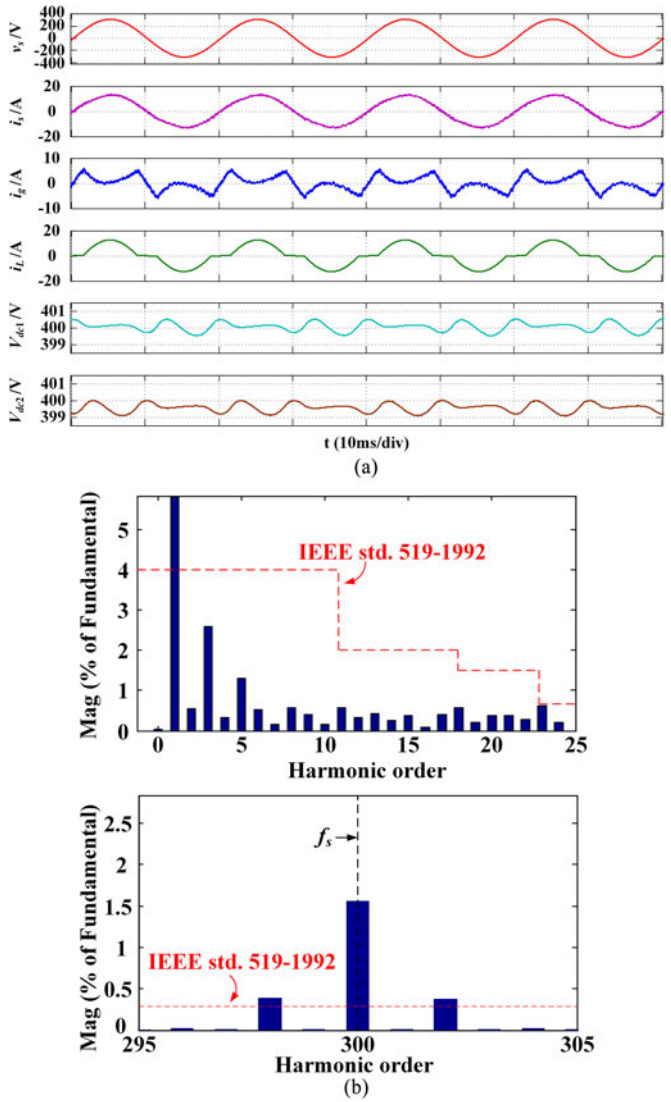


Fig. 20. (a) Simulated waveforms and (b) source current spectrum of APF using the *LCL* filter.

switching-frequency sideband harmonics exceed the 0.3% fundamental current standard requirement, and the source current THD can be up to 5.16%.

Fig. 21(a) shows the simulated waveforms of APF using the SPRLCL filter designed with method II. Since these waveforms are very similar to those obtained from the SPRLCL filter designed with method I, only the performance of the SPRLCL filter designed with method II is given here. As seen, when the *LCL* filter is replaced by the SPRLCL filter, the source current waveform is still sinusoidal, indicating the low-order harmonic compensation is not affected. Moreover as shown in Fig. 21(b), both the switching-frequency and double switching-frequency harmonics of the source current are eliminated. The triple switching-frequency harmonics are increased to 0.12% of the fundamental current but still under the limit. With a source current THD value of 4.33%, the designed SPRLCL filter can satisfy the IEEE requirements with smaller filter elements. It is also noted that the grid current is mainly distorted by low-order

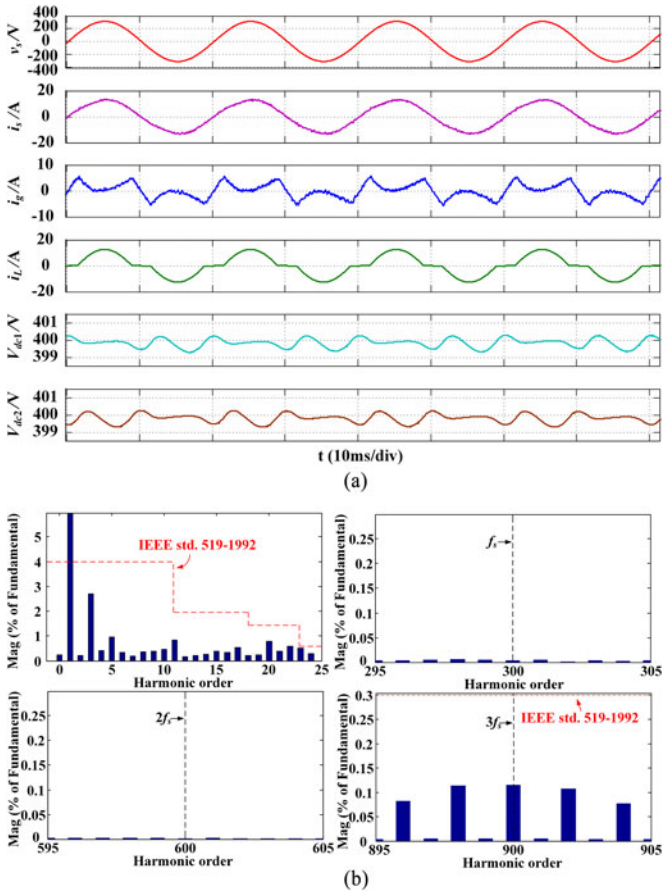


Fig. 21. (a) Simulated waveforms and (b) source current spectrum of APF using method II designed SPRLCL filter.

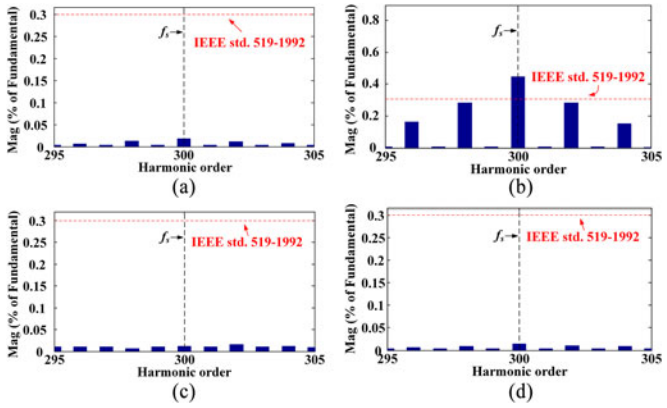


Fig. 22. Simulated source current spectra with parameters deviation of (a) *LLCL* filter ($100\%L_f$), (b) *LLCL* filter ($50\%L_f$), (c) method III designed SPRLCL filter ($50\%L_f$), and (d) method III designed SPRLCL filter ($50\%C_g$).

harmonics due to the nonoptimized design of the harmonic extraction and repetitive current controller. The THD of grid current can be further reduced by fine tuning these two control blocks. Moreover, the background harmonics in the grid voltage may impose another challenge to the control system and worsen the THD. Such disturbances can be compensated by introducing grid voltage feedforward or more resonant controllers

TABLE IV
SIMULATED SOURCE CURRENT THD

Filter	Harmonics around f_s /(% I_{ref})	Harmonics around $2f_s$ /(% I_{ref})	Harmonics around $3f_s$ /(% I_{ref})	THD/%
LCL	1.61	0.06	0.00	5.16
LLCL ($100\%L_f$)	0.01	0.13	0.03	4.40
LLCL ($50\%L_f$)	0.44	0.09	0.03	4.77
LLCL (3 mH L_s)	0.01	0.01	0.01	4.33
SPRLCL (method I)	0.01	0.00	0.05	4.62
SPRLCL (method II)	0.01	0.00	0.11	4.33
SPRLCL (method III)	0.01	0.12	0.02	4.43
SPRLCL($50\%L_f$) (method III)	0.01	0.08	0.02	4.40
SPRLCL($50\%C_g$) (method III)	0.01	0.09	0.06	4.45
SPRLCL (3 mH L_s)	0.01	0.01	0.02	4.35

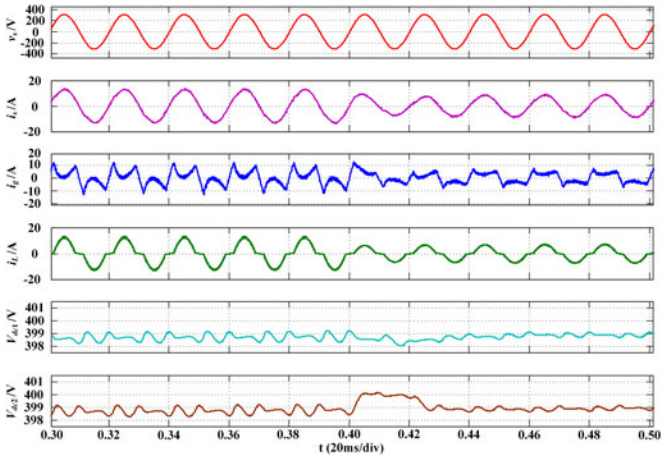


Fig. 23. Simulated dynamic waveforms of APF using SPRLCL filter designed with method II.

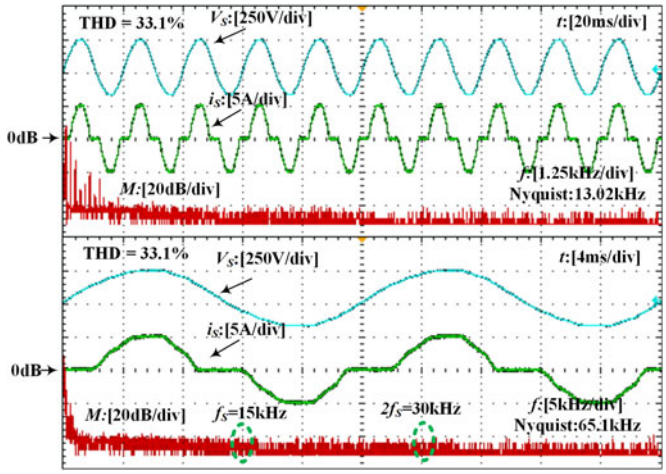


Fig. 24. Experimental waveforms of grid voltage and nonlinear load current with its FFT spectrum.

particularly designed at these harmonic frequencies. It should be pointed out that the system high-frequency responses, e.g., control stability and switching harmonic attenuation will not be affected by these low-order harmonics.

When the filter parameters deviate from the nominal values, the simulated source current spectra of APF using the *LLCL* filter and the SPRLCL filter designed with method III is shown in Fig. 22. As shown in Fig. 22(a) and (b), although the *LLCL* filter can offer a satisfactory damping performance at the switching frequency with nominal filter parameters, it is unable to satisfy the IEEE standard when the additional inductor L_f deviates 50% from its nominal value, which has also been proved in [3], [4], [9]. As can be seen in Fig. 22(c) and (d), the SPRLCL filter designed with method III can keep its harmonic attenuation ability even with parameter deviations, which is in consistence with the theoretical analysis.

The APF is also stable when the source inductance varies from 0.1 to 3.0 mH thanks to the robustness design of these filters. The THD of the source current under different design scenarios with rated power of 2 kW is listed in Table IV.

The SPRLCL filter designed with method II is taken as an example to validate the controller dynamic performance, and the relevant simulated waveforms are shown in Fig. 23. The nonlinear load is stepped down to 50% of its nominal value at $t = 0.40$ s. As seen, the dc-link voltage overshoot is less than 2 V and the dynamic time duration is 0.03 s, which indicates well designed voltage-loop and current-loop controllers.

B. Experimental Results

A prototype based on a digital signal processor (TMS320F28335) controller was built and tested. The parameters are listed in Table I–Table III except for the grid voltage $V_s = 150$ V/50 Hz. All the voltages were measured with voltage halls LV25-P and all the currents were measured with current halls LA55-P. The converter was implemented using an IGBT module, driven by M57962. A 100-V metallized polypropylene film capacitor was used as C_g and it can handle high ripple currents. The rated current of L_f is designed to be 15 A, which is higher than the nominal grid current. The switching frequency of IGBTs is 15 kHz, which is reasonable as the power rating of the system is relatively low. If a lower frequency is considered, the bandwidth of the control system will be limited and the recommended filter may not be suitable for APF applications. This is a common problem for all power converters with linear regulators.

The waveforms of the nonlinear load current and its FFT spectrum are shown in Fig. 24. As can be seen, the load current is distorted with its THD value as high as 33.1%. Without

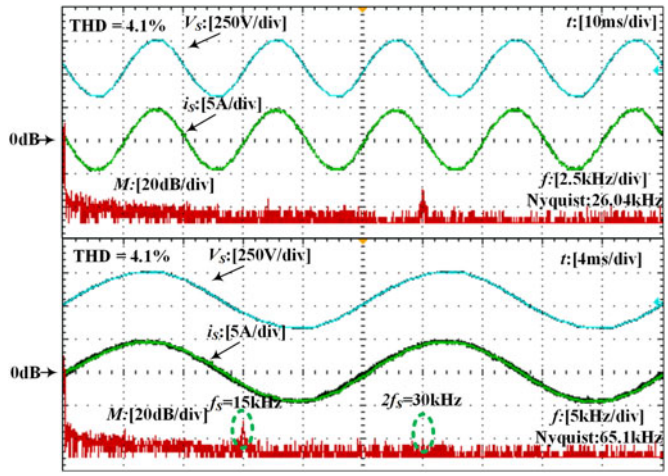


Fig. 25. Experimental waveforms of grid voltage, grid current, and its FFT spectrum with *LCL*-filtered APF.

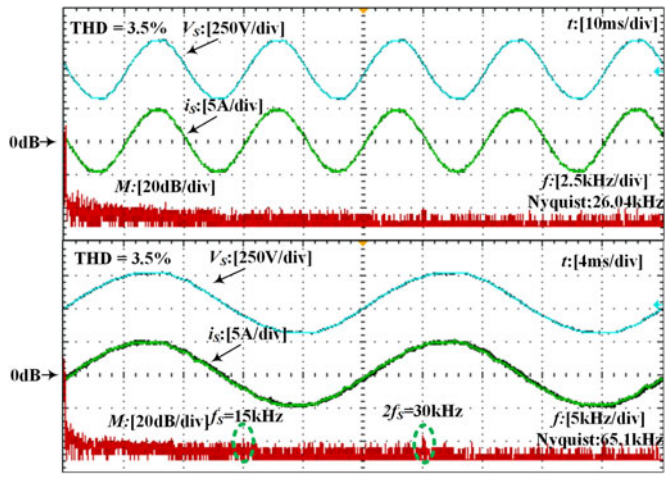


Fig. 26. Experimental waveforms of grid voltage, grid current, and its FFT spectrum with *LLCL*-filtered APF.

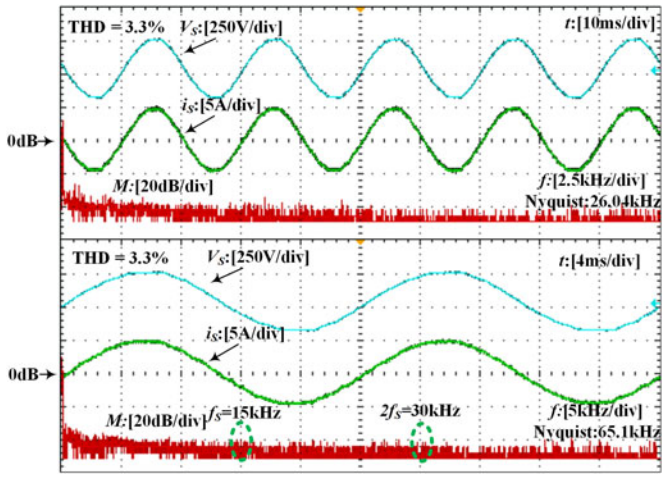


Fig. 27. Experimental waveforms of grid voltage, grid current, and its FFT spectrum with SPRLCL-filtered APF (design method II).

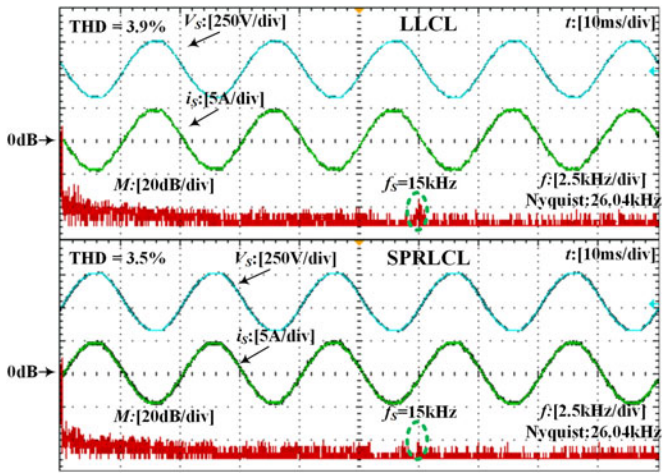


Fig. 28. Experimental waveforms of grid voltage, grid current, and its FFT spectrum with *LLCL*-filtered APF and SPRLCL-filtered APF (design method III) considering 50% deviation of L_f.

operating the APF, the current harmonics around f_s and $2f_s$ are basically negligible. Fig. 25 shows the experimental results when the nonlinear load is compensated by the *LCL*-filtered half-bridge APF. The current harmonic spike at f_s is obvious and may fail to comply with IEEE standard 1547.2-2008 and IEEE standard 519-1992. After compensation, the grid current becomes more sinusoidal with its THD reduced to 4.1%. Fig. 26 illustrates the experimental compensation results of the *LLCL* filter-based APF. The THD of the grid current is reduced to 3.5% thanks to the elimination of the current harmonics at f_s. However, the current harmonics at $2f_s$ are noted to be increased as the roll-off rate of *LLCL* filters is only 20 dB/decade at high frequencies.

In order to simultaneously suppress switching-frequency and double switching-frequency harmonics, the *LLCL* filter is replaced by the SPRLCL filter designed with method II, and the experimental results are given in Fig. 27. It is clear that these two dominant switching current harmonics can be successfully eliminated, and the grid current THD is further reduced to 3.3%, which is the lowest among all the cases.

As discussed, the SPRLCL filter designed with method III can be immune to parameter deviations. Its experimental result under 50% deviation of L_f is presented in Fig. 28 and compared to that of the *LLCL* filter subjected to the same parameter deviation.

As seen from Fig. 28, the switching-frequency current harmonics can be well attenuated by the SPRLCL filter designed with method III and the grid current THD is 3.5%, whereas for the *LLCL* filter may lose the harmonic attenuation ability at f_s, leading to an increased THD value of 3.9%. These experimental results match well with the theoretical analysis. It should be noted that the reduction of switching-frequency harmonics in experiments is not so significant as compared to that of the simulated ones shown in Fig. 22. This is mainly due to the presence of measurement noises and other system noises in experiments, and such noises cannot be removed by the proposed SPRLCL

filter. Moreover, the ESRs of passive components may also limit the harmonic attenuation while these ESRs (except for R_s) are all ignored in simulations.

VII. Conclusion

This paper has proposed a novel high-order passive filter, named SPRLCL filter, to suppress the dominant switching harmonic currents of a single-phase half-bridge APF. The proposed SPRLCL filter features a reduced number of discrete passive components and an easy implementation of active damping control. Three design methods are also proposed to realize different objectives. Design method I and method II enable the SPRLCL filter to simultaneously remove the switching-frequency and double switching-frequency harmonics, while with design method III, the proposed SPRLCL filter will be more robust against parameter variations. Through analyzing the capacitor-current active damping control, it is identified that setting the resonance frequency at one-third of the sampling frequency may give rise to a minimized virtual damping resistance, and, thus, offer the best damping effect to the *LCL* resonance. Moreover, the resonance frequency under this design is always fixed at one-third of the sampling frequency irrespective of the value of the capacitor-current-feedback coefficient. A comprehensive step-by-step design process has been given to guide the parameter selections of the proposed SPRLCL filter, and the designed filters can also be robust to source impedance variations. With the derived filter parameters, a proportional plus repetitive current controller is designed. Simulation and experimental results are finally presented to verify the effectiveness of the designed filters.

References

[1] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[2] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 263–272, Jan. 2006.

[3] W. Wu, Y. He, and F. Blaabjerg, "An *LLCL* power filter for single-phase grid-tied inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 782–789, Feb. 2012.

[4] J. Xu, J. Yang, J. Ye, Z. Zhang, and A. Shen, "An LTCL filter for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4322–4338, Aug. 2014.

[5] Z. Xing, Z. Hong, L. Fei, L. Fang, L. Chun, and L. Benxuan, "An LCL-LC power filter for grid-tied inverter," in *Proc. IEEE TENCON Region 10 Conf.*, 2013, pp. 1–4.

[6] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an *LCL* filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sep./Oct. 2005.

[7] R. P. Alzola, M. Liserre, F. Blaabjerg, R. Sebastian, J. Dannehl, and F. W. Fuchs, "Analysis of the passive damping losses in LCL-filter-based grid converters," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2642–2646, Jun. 2013.

[8] W. Wu, Y. He, T. Tang, and F. Blaabjerg, "A new design method for the passive damped LCL and LLCL filter-based single-phase grid-tied inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4339–4350, Oct. 2013.

[9] W. M. Wu, Y. J. Sun, M. Huang, X. F. Wang, H. Wang, F. Blaabjerg, M. Liserre, and H.S-H. Chung, "A robust passive damping method for LLCL-filter-based grid-tied inverters to minimize the effect of grid harmonic voltages," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3279–3289, Jul. 2014.

[10] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Step-by-step controller design for *LCL*-type grid-connected inverter with capacitor-current-feedback active-damping," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1239–1253, Mar. 2014.

[11] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-current-feedback active damping with reduced computation delay for improving robustness of *LCL*-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3414–3427, Jul. 2014.

[12] S. G. Parker, B. P. McGrath, and D. G. Holmes, "Regions of active damping control for *LCL* filters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 424–432, Jan./Feb. 2014.

[13] M. Huang, X. Wang, P. C. Loh, and F. Blaabjerg, "LLCL-filtered grid converters with improved stability and robustness," *IEEE Trans. Power Electron*, vol. 31, no. 5, pp. 3958–3967, May 2016.

[14] M. Huang, X. Wang, P. C. Loh, and F. Blaabjerg, "Active damping of LLCL-filter resonance based on LC-trap voltage and capacitor current feedback," *IEEE Trans. Power Electron*, vol. 31, no. 3, pp. 2337–2346, May 2016.

[15] J. He and Y. W. Li, "Generalized closed-loop control schemes with embedded virtual impedances for voltage source converters with *LC* or *LCL* filters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1850–1861, Apr. 2012.

[16] W. Li, X. Ruan, D. Pan, and X. Wang, "Full-feedforward schemes of grid voltages for a three-phase *LCL*-type grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2237–2250, Jun. 2013.

[17] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Design of injected grid current regulator and capacitor-current-feedback active- damping for *LCL*-type grid-connected inverter," in *Proc. IEEE Energy Conver. Congr. Expo.*, Sep. 2012, pp. 579–586.

[18] J. Dannehl, F. W. Fuchs, S. Hansen, and P. B. Thogersen, "Investigation of active damping approaches for PI-based current control of grid-connected pulse width modulation converters with LCL filters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1509–1517, Jul./Aug. 2010.

[19] K. Jalili and S. Bernet, "Design of LCL filters of active-front-end two level voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1674–1689, May 2009.

[20] F. Liu, Y. Zhou, S. Duan, J. Yin, B. Liu, and F. Liu, "Parameter design of a two-current-loop controller used in a grid-connected inverter system with LCL filter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4483–4491, Nov. 2009.

[21] E. Wu and P. W. Lehn, "Digital current control of a voltage source converter with active damping of LCL resonance," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1364–1373, Sep. 2006.

[22] J. R. Massing, M. Stefanello, H. A. Grundling, and H. Pinheiro, "Adaptive current control for grid-connected converters with LCL filter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4681–4693, Dec. 2012.

[23] G. Shen, D. Xu, L. Cao, and X. Zhu, "An improved control strategy for grid-connected voltage source inverters with an LCL filter," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1899–1906, Jul. 2008.

[24] Y. Tang, P. C. Loh, P. Wang, F. H. Choo, F. Gao, and F. Blaabjerg, "Generalized design of high performance shunt active power filter with output *LCL* filter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1443–1452, Mar. 2012.

[25] Q. Liu, L. Peng, Y. Kang, S. Y. Tang, D. L. Wu, and Y. Qi, "A novel design and optimization method of an LCL filter for a shunt active power filter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 4000–4010, Aug. 2014.

[26] V. Khadkikar, "Enhancing electric power quality using UPQC: A comprehensive overview," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2284–2297, May 2012.

[27] *IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, IEEE Standard 1547.2-2008, 2008.

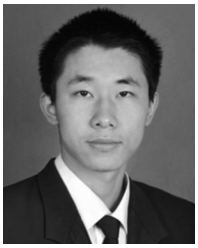
[28] *IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems*, IEEE Standard 519-1992, 1992.

[29] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*, New York, NY, USA: Wiley-IEEE Press, 2003.

[30] X. Wang, M. Huang, H. Bai, P. C. Loh, and F. Blaabjerg, "Influence of modulation method on using *LC*-tarps with single-phase voltage source inverters," in *Proc. Power Electron. Appl. Conf.*, Sep. 2015, pp. 1–9.

[31] A. Garcia-Cerrada, O. Pinzon-Ardila, and V. Feliu-Batlle, "Application of a repetitive controller for a three-phase active power filter," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 237–246, Jan. 2007.

[32] K. Zhang, Y. Kang, J. Xiong, and J. Chen, "Direct repetitive control of SPWM inverter for UPS purpose," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 784– 792, May 2003.
[33] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Design of LCL-filters with LCL resonance frequencies beyond the Nyquist frequency for grid-connected converters," *J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 3–14, Mar. 2016.
[34] X. Wang, F. Blaabjerg, and P. C. Loh, "Virtual *RC* damping of *LCL*-filtered voltage source converters with extended selective harmonic compensation," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4726–4737, Sep. 2015.



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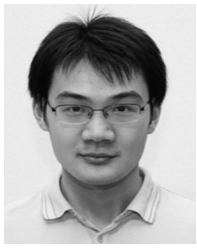

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