Multitrack Power Conversion Architecture

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***Abstract*—This paper introduces a *MultiTrack* power conversion architecture that represents a new way of combining switched-capacitor circuits and magnetics. The MultiTrack architecture takes advantages of the distributed power processing concept and a hybrid switched-capacitor/magnetics circuit structure. It reduces the voltage ratings on devices, reduces the voltage regulation stress of the system, improves the component utilization, and reduces the sizes of passive components. This architecture is suitable to dc–dc and grid-interface applications that require both isolation and wide voltage conversion range. An 18–80 V input, 5 V, 15 A output, 800 kHz, 0.93 in^2 (1/16 brick equivalent) isolated dc–dc converter has been built and tested to verify the effectiveness of this architecture. By employing the MultiTrack architecture, utilizing GaN switches, and operating at higher frequencies, the prototype converter achieves a power density of 457.3 W/in^3 and a peak efficiency of 91.3%. Its power density is 3$\times$ higher than the state-of-the-art commercial converters with comparable efficiency across the wide operation range.**

***Index Terms*—DC–DC power conversion, magnetic circuits, passive circuits, resonant power conversion, switched-capacitor circuits.**

I. Introduction

POWER electronic designs have generally been cost driven. Simple circuit topologies with low complexity, low component count, and simple controls have traditionally been preferred in practical designs. However, with increasing electronic content in industrial and consumer applications, and wider deployment of renewable energy systems, power electronics are required to have much higher performance. At the same time, the relative cost of power devices and control circuitry has fallen (following the general trend in the semiconductor industry). Hence, enhancing system performance through more sophisticated circuit architectures is an attractive option and presents many emerging design opportunities [1].

Power conversion systems can generally be grouped into single-stage architectures and multistage architectures. In a single-stage architecture, multiple tasks (e.g., output voltage modulation, input current shaping) are realized in a single power stage. They have low circuit complexity and simple control, but cannot achieve high performance while meeting requirements such as wide operating ranges and high power density. Multistage architectures have multiple power conversion stages with each stage performing one or more functions. Each stage can be optimally designed to only address a portion of the system requirements. As a result, the overall system performance is often better, while the total component count and complexity is usually higher. In many cases, a multistage architecture may process the full system energy multiple times, imposing a penalty on efficiency. *Merged multistage power conversion*—in which portions of a multistage system are partly merged together, reducing component count and redundancy of power processing while preserving flexibility—can, thus, be a desirable middle ground between true single-stage and multistage conversion.

There has been significant recent work in hybridizing switched-capacitor and magnetic conversion, with consequent advantages. Building or merging multistage systems incorporating switched-capacitor circuits, switched-inductor circuits, and magnetically coupled circuits (e.g., "dc transformers") has been one fruitful approach [2]–[23]. These three groups of circuits are often used as the basic building blocks of multistage systems. They have complementary advantages and limitations. Switched-inductor circuits are popular for their voltage regulation capability. However, basic switched-inductor circuits suffer in terms of size and performance at high voltage conversion ratios, and their power density is typically limited by the bulky power stage magnetics. Switched-capacitor circuits, by contrast, can provide balanced efficiency and power density tradeoffs for fixed voltage conversion ratios, but cannot efficiently regulate voltage and have limited voltage conversion ratio options with reasonable component count. Magnetic isolation circuits, i.e., isolated converters with fixed voltage conversion ratio ("dc transformers") can provide high voltage conversion ratio, galvanic isolation, and soft switching. However, they often do not maintain high performance across wide operation range.

Leveraging of these different kinds of stages in multistage architectures has often proved beneficial. For example, a switched-capacitor voltage divider and a multiphase buck converter were cascaded to implement a high performance laptop power supply in [12]. The wide input range converter presented in [13] likewise incorporated a switched-capacitor circuit with a switched-inductor circuit in a manner to best leverage their benefits in low-voltage CMOS. Clever usage of switched-capacitor and magnetic stages likewise has been demonstrated in multioutput converters [14]. Integrated techniques were applied with switched-capacitor converters at higher voltages: an on-chip switched-capacitor converter was combined with capacitive isolation circuits and magnetics as the dc–dc portion of an LED driver in [15]. Innovative structures combining

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switched-capacitor circuits and multiwinding coupled magnetics in ac–dc and dc–dc applications were proposed in [16] and [17].

More highly coupled use of switched-capacitor/magnetic conversion has also been exploited to advantage. For example, in [18] and [19], it was shown that significant system benefits can be obtained by merging the operation of the magnetic and switched-capacitor stages through "soft charging" of the capacitor elements, enabling one or both of higher efficiency and smaller capacitor size. A few high-performance high-frequency grid-interfaced LED drivers using merged circuit architectures were presented in [20]–[22]. Resonant switched-capacitor circuits and other "merged" switched-capacitor/magnetics techniques have also proven advantageous [24]–[26]. By adding one or more inductive components into the switched-capacitor circuit structure, enhanced performance with reasonable regulation capability and/or minimization of passive component size can be achieved.

This paper introduces a MultiTrack power conversion architecture that represents a new way of utilizing switched-capacitor and magnetic circuit elements. It incorporates a *hybrid switched-capacitor/magnetics* circuit structure that splits the wide voltage conversion range into multiple smaller ranges, delivers power in multiple tracks, and functionally merges the regulation stage and the isolation stage. The system operates in multiple modes across the wide operation range, with its performance optimized for each operation mode. Compared to conventional two-stage designs, it gains advantages through distributed parallel power processing, rather than multiple full power processing, and facilitates reduced device ratings, reduced magnetics size, improved component utilization, and reduced drive of parasitic transformer capacitances. It also enables zero-voltage switching (ZVS or near ZVS) of the transistors used in charge transfer among voltage domains without additional elements, which is not available in a traditional switched-capacitor circuit. The proposed approach embraces trends in the development of semiconductor devices, and is suitable for power converter designs operating at high frequencies (close to megahertz or higher). This paper is developed from our earlier conference publication [27] and presents extended theoretical analysis and experimental results.

The remainder of this paper is organized as follows: Section II provides an overview of the MultiTrack power conversion architecture. A basic 2-Track implementation and its operation is introduced in Section III, and is extended to a generalized MultiTrack architecture. Analysis and discussion about the advantages of the MultiTrack architecture are provided in Section IV. Section V presents several practical design considerations. Experimental and benchmark results are provided in Section VI, and Section VII concludes this paper. Extended theoretical analysis about the MultiTrack architecture is provided in Appendix.

II. Architecture Concept and Overview

Fig. 1 shows the block diagram of the proposed MultiTrack power conversion architecture. It comprises two merged conversion stages that provide the functional benefits of a switched-inductor circuit (for regulation), a switched-capacitor circuit (for distributing voltage stress among different levels and providing voltage balancing), and a magnetic isolation circuit (for transformation and galvanic isolation). While the circuit subsystems are actually merged, one can understand its operation considering the multiple circuit functions as if they were performed independently: the switched-inductor portion of the circuit is principally responsible for voltage regulation; the magnetic isolation portion of the circuit offers isolation and voltage scaling (and, if needed, a secondary means of voltage regulation); and the switched-capacitor circuit creates multiple related voltage levels (V_1, V_2, V_3, etc.) and many stacked current tracks that bridge the other two subsystems.

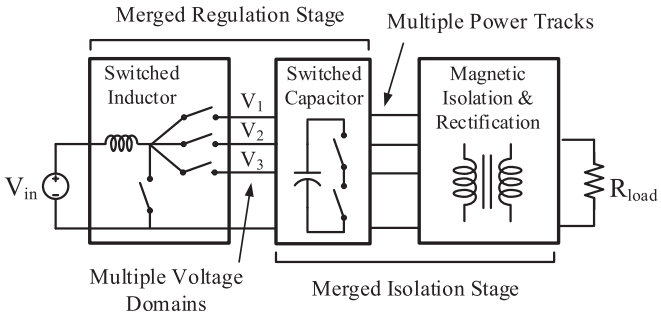

Fig. 1. Proposed MultiTrack power conversion architecture comprising multiple voltage domains and multiple power tracks. Its regulation and isolation stages are merged, hence reducing the amount of power that is "reprocessed" by the two-stages.

One advantage of the MultiTrack converter is that components of the subsystems are shared, and their functions are partially merged. The switched-inductor circuit block couples into the multiple levels of the switched-capacitor circuit block to form a *merged regulation stage*. Likewise, by using a single set of switches to perform charge transfer and voltage balancing among different levels of the capacitor stack, and to drive the parallel-track magnetic isolation device, we obtain a *merged isolation stage*.

Merging the stages in this manner yields a circuit having improved performance as compared to what could be achieved with separate stages. In conventional wide input voltage dc–dc converter designs, there is usually a regulation stage (typically a buck or boost converter) that compresses the variable input voltage to a fixed intermediate bus voltage. This intermediate bus voltage is then processed by a separate isolation stage. Since the regulation stage has to be designed for the worst case (peak input voltage and peak input current), the voltage or current ratings of these components are usually not well utilized: when the voltage is high, the current is usually low; when the voltage is low, the current is usually high.

The proposed MultiTrack architecture improves the component utilization through a hybrid switched-capacitor/magnetics circuit structure. Multiple voltage domains with multiple ratiometrically related intermediate bus voltages (V_1, V_2, V_3, etc.) are synthesized using a switched-capacitor circuit structure which also simultaneously acts to drive the isolation stage magnetics. This reduces the number of switches required and provides ZVS opportunities for the switches (which is not available in a true switched-capacitor structure). Depending on the input voltage,

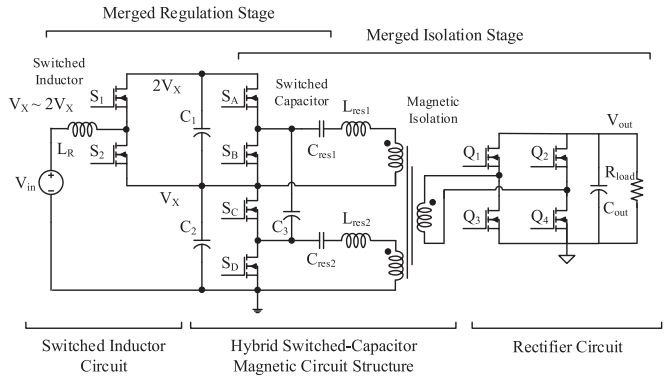

Fig. 2. Schematic of an example 2-to-1 input voltage range 2-Track converter comprising a switched-inductor circuit, a switched-capacitor circuit, and a magnetic isolation circuit. The regulation stage and the isolation stage are merged by a *hybrid switched-capacitor magnetic* circuit structure.

the switched inductor circuit redistributes the regulation stage inductor current into the closest intermediate bus voltages, thus effectively reduces the voltage drop across the inductor, and reduces the stress on switches (as will be discussed in Section V).

A 2-to-1 input voltage range 2-track converter as shown in Fig. 2 is a simple embodiment of the MultiTrack architecture. This 2-track converter has two related intermediate bus voltages (V_X and $2V_X$) and has a 2-to-1 input voltage range between V_X and $2V_X$. The relative values of bus voltages V_X and $2V_X$ are synthesized by a 2:1 ladder switched-capacitor circuit structure, whose switches are also used as the inverter switches in the isolation stage.

We first introduce the merged isolation stage. The merged isolation stage includes a pair of half bridges (S_A/S_B and S_C/S_D) that operate synchronously to drive a pair of identical resonant tanks (C_{res1}–L_{res1} and C_{res2}–L_{res2}). These are coupled to a *multiple-input single-output* (MISO) transformer (whose leakage inductances form L_{res1}, L_{res2}) with the output tied to a synchronous full-bridge rectifier (Q_1–Q_4). The isolation stage can be interpreted as two ac power tracks distributed in two stacked voltage domains ([0, V_X] and [V_X, $2V_X$]), each processing a half of the total output power. The cross-sectional area of the magnetic core is determined by the volt–seconds of the secondary winding. The window area of the magnetic core is determined by the output current. Thus, the power conversion stress of the merged isolation stage in this 2-Track converter is the same as a conventional series-resonant-converter-based dc transformer, indicating equivalent magnetics volume and efficiency. This MultiTrack configuration distributes the concentrated device voltage ratings on the high-voltage side into multiple devices, which can take advantage of the distributed power processing concept [29]–[32]. Moreover, as will be shown shortly, the current driven through the common-mode capacitances of the transformer is much smaller than that in a single primary-winding design. This effect is beneficial in high frequency or high turns-ratio designs. It is in some respects similar to a series-primary parallel-secondary configuration [28] with similar advantages, whereas only a single magnetic core and a single rectifier is needed.

S_A–S_D are reused to create a capacitive energy transfer mechanism that can balance the two stacked bus voltages (V_X and $2V_X$) formed by the two capacitors (C_1 and C_2). Charge is transferred through an additional capacitor C_3, which ties the two switch nodes together. The capacitive energy transfer mechanism ensures $V_{C1} \approx V_{C2}$. It is also possible to envision variants in which balancing currents are delivered through the transformer windings. This combination of capacitive energy transfer and inverter drive of a multiple-winding transformer may be described as a *hybrid switched-capacitor/magnetics* circuit structure. This structure performs key functions in the MultiTrack architecture—the switching of this structure drives the MISO transformer, and at the same time smoothly rebalances the power processed by different tracks with low loss. The hybrid structure also enables ZVS of the switches. Resonant switched-capacitor and zero-current-switching mechanisms can be included by adding inductive impedances in the C_3 branch and utilize the transformer appropriately.

The merged regulation stage in this 2-Track converter comprises inductor L_R and switches S_1 and S_2. By controlling the duty ratio of S_1 and S_2, the voltage of C_1 is regulated, and the voltage of C_2 is effectively regulated through the capacitive energy transfer mechanism. In this embodiment, voltage regulation and dynamic control are achieved by the modulation of S_1 and S_2. For an input voltage $v_{\rm in}$ between V_X and $2V_X$, S_1 and S_2 are controlled such that the voltages across C_1 and C_2 are always V_X. If $v_{\rm in}$ is closer to V_X, S_2 has a higher duty ratio and more charge is delivered to V_X; if $v_{\rm in}$ is closer to $2V_X$, S_1 has a higher duty ratio and more charge is delivered to $2V_X$. If S_1 and S_2 are switched in complimentary pulse width modulation mode, the duty ratio of S_1 that can regulate the voltage across C_1 and C_2 to be V_X, d_1, is

$$d_1 = \frac{v_{\rm in} - V_X}{V_X} \tag{1}$$

and the duty ratio of S_2, d_2, is

$$d_2 = 1 - d_1 = 2 - \frac{v_{\rm in}}{V_X}. \tag{2}$$

This is somewhat similar to regulating the output voltage of a boost converter, but with V_X instead of ground as the second potential. Other similar control approaches (e.g., DCM control, constant on-time control, current-mode control) can also be used.

III. Extended MultiTrack Architecture With Wide Input Voltage Range

The basic 2-Track converter shown in Fig. 2 is suitable for applications in which $v_{\rm in} \in [V_X, 2V_X]$ with a restricted nominal 2-to-1 input voltage range. Moreover, by adding two additional switches (S_3 and S_4) in the regulation stage as shown in Fig. 3, the converter can handle any desired input voltage range in the $[0, 2V_X]$ region (i.e., $[V_{\min}, V_{\max}] \in [0, 2V_X]$), so long as the components are sized appropriately.

The voltage ratings of C_1 and C_2 are both V_X. The operation of this enhanced design can be split into two regions determined by the input voltage $v_{\rm in}$. When $v_{\rm in} \in [0, V_X]$, S_3 and S_4

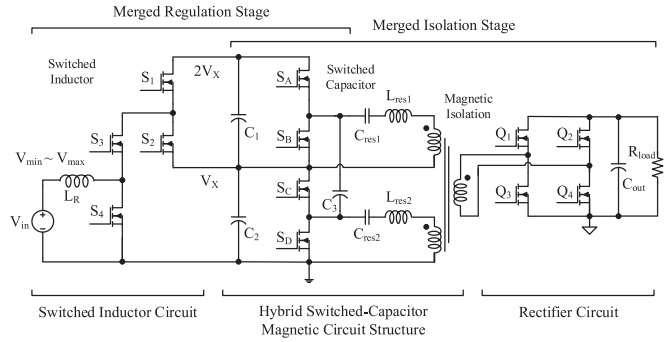

Fig. 3. Example 2-Track power converter that can handle wide input voltage range. For this converter, the maximum input voltage $V_{\max}$ must be smaller than $2V_X$.

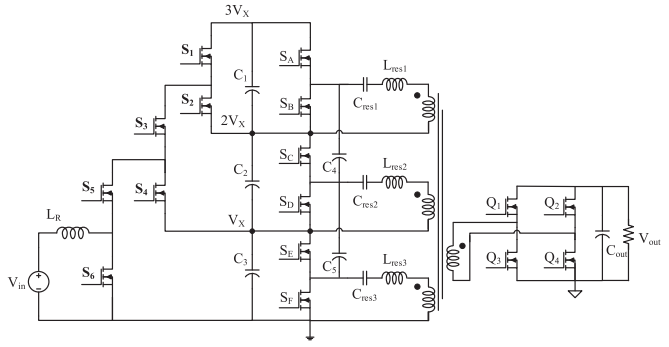

Fig. 5. Example 3-Track power converter that can handle arbitrary input voltage range.

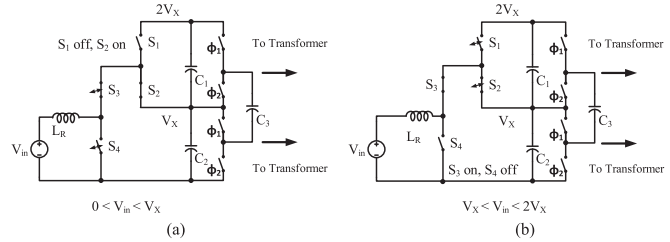

Fig. 4. Two operation modes of the two pairs of half-bridges in the regulation stage of a 2-Track converter: (a) when $0 < v_{\rm in} < V_X$, S_3 and S_4 are switching, S_1 is kept OFF, and S_2 is kept ON; (b) when $V_X < v_{\rm in} < 2V_X$, S_3 is kept ON, S_4 is kept OFF, and S_1 and S_2 are switching.

are switching, S_1 is kept OFF, and S_2 is kept ON. The inductor L_R, switches S_3 and S_4 formulates a ground-referenced boost converter that feeds current into the V_X node. The switched capacitor circuit balances the voltages of C_1 and C_2. When $v_{\rm in} \in [V_X, 2V_X]$, S_3 is kept ON, S_4 is kept OFF, and S_1 and S_2 are switching. The L_R, S_1, and S_2 formulates a boost-type converter structure that feeds power from the input into both the V_X and the $2V_X$ node. Fig. 4 illustrates the operation of the switches in these two operation modes. Within each subsection of the voltage domain, conventional feedback control for boost converters (e.g., a classic PWM control) can be directly utilized in the proposed MultiTrack architecture. When the input voltage fluctuates between two regions, a hysteresis control can be utilized to stabilize the mode transition.

Fig. 4 shows the two different operating modes of the merged regulation stage. Depending upon the operating mode, the switched capacitor charge transfer is used differently to maintain voltage balance between the two stacked capacitors. When the input voltage is low ($v_{\rm in} < V_X$), S_3 and S_4 operate as a boost converter and the input power is injected into the V_X node only [see Fig. 4(a)]. When the input voltage is between V_X and $2V_X$, S_1 and S_2 operate as a boost converter and the input power (from the input inductor) is injected into both the V_X and $2V_X$ nodes [see Fig. 4(b)], and the total voltage of the two stacked capacitors serve to counter the input voltage (in providing volt–seconds balance on the inductor). The switched-capacitor energy transfer operates to redistribute charge such that the different windings of the isolation stage magnetics can be utilized equally.

Benefiting from the 2-Track architecture, the magnitude of the voltage applied across the inductor L_R never exceeds V_X, even if the maximum input voltage is $2V_X$. The charge coming from the input source is always delivered to the closest dc voltages to the input. For example, if $v_{\rm in} \in [0, V_X]$, power coming from $v_{\rm in}$ is always delivered to the V_X node; if $v_{\rm in} \in [V_X, 2V_X]$, power coming from $v_{\rm in}$ is always delivered to the V_X node and the $2V_X$ node. As will be analyzed, the smaller resulting voltage imposed on the inductor and the largely compressed voltage conversion ratio of the regulation stage can significantly reduce the inductor size, the current ripple, and/or the regulation loss.

One can even use a higher order capacitor stack to create more intermediate voltages and power delivery tracks if a wider input voltage range is desired. Fig. 5 shows an example 3-Track converter. Implementations with more tracks can be created following a similar pattern. By creating n power tracks, the power conversion stress is further distributed, the voltage across the inductor is further reduced, and the effective voltage conversion ratio is further compressed, at the expense of higher component count and control complexity. As analyzed in Appendix, these advantages do not scale up linearly with the number of tracks, but will gradually saturate in a manner that may be likened to the gradually saturated advantages of multiphase interleaving techniques [29]–[32].

Note that the voltage ratings of S_4 and S_6 in Fig. 5 are $2V_X$ and $3V_X$, respectively. All other switches on the primary side have a voltage rating of V_X. The wide input voltage range is divided into three sections [0–V_X], [V_X–$2V_X$], and [$2V_X$–$3V_X$]. The control of the 3-Track converter is an extended version of the 2-Track converter—the input voltage is tapped to the switch node of a half-bridge that has the closest voltage level to minimize the voltage conversion stress. S_A–S_F are operated as a 3:1 ladder switched-capacitor circuit with 50% duty ratio. S_A, S_C, and S_E are synchronized as one phase, and S_B, S_D, and S_F are synchronized as the other phase. Energy is transferred between adjacent voltage domains by C_4 and C_5. Detailed operation of 2:1 and 3:1 switched-capacitor circuits and corresponding loss analysis can be found in [10] and[11]. The difference between the *hybrid switched-capacitor/-magnetics structure* and conventional switched-capacitor circuits is that the switches in the prior

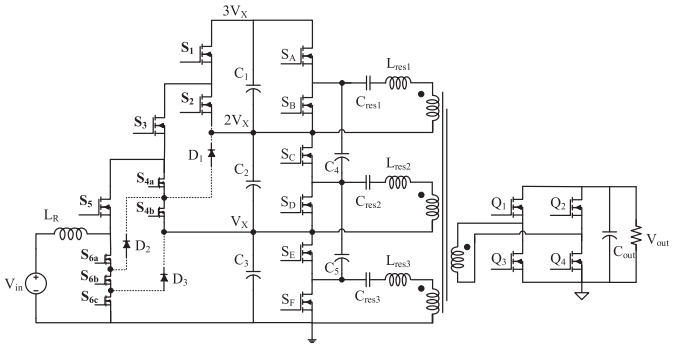

Fig. 6. Modified 3-track converter with uniform switch voltage ratings, which facilitates potential IC implementation. By replacing S_4 and S_6 with low-voltage rating cascaded switches (S_{4a}, S_{4b}, S_{6a}, S_{6b}, S_{6c}), all primary-side devices in this schematic have a voltage rating of V_X. One can add a few protection diodes (e.g., D_1–D_3) with small footprints and low current rating to help ensure voltage sharing of the cascaded switches.

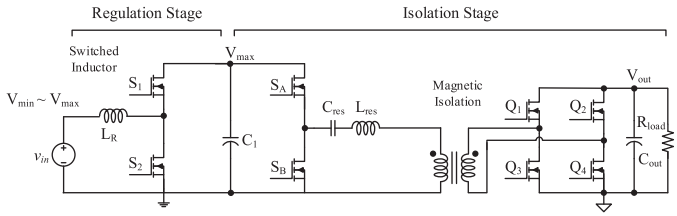

Fig. 7. Schematic of a conventional BTS converter having a boost converter as the regulation stage, and a series-resonant converter as the isolation stage.

circuit are reused as inverters that drive the transformer windings, and can benefit from soft switching owing to the additional magnetic loading.

If S_4 and S_6 are implemented as multiple cascaded devices, such as shown in Fig. 6, all switches on the primary side can be implemented with a voltage rating of V_X. Additional protection can be provided by using the intermediate bus voltage(s) to provide voltage clamping for the devices (e.g., one can add a few small protection diodes, e.g., D_1–D_3, to ensure voltage sharing of the stacked low-voltage-rating devices). This modification is beneficial in discrete designs as considered here, and would also be desirable in an integrated circuit (IC) implementation [10], [15] if the peak device voltage rating is constrained by the fabrication process.

The MISO transformer in the isolation stage has multiple primary windings and a single secondary winding. One can synthesize different tank structures to realize the isolation stage for different purposes, e.g., *LLC* converters, series-resonant converters, and dual-active-bridge converters. If planar transformers are utilized, a systematic magnetics modeling technique [33] that can rapidly estimate the impedances and current distribution can be utilized to advantage, as is done in the design of Section V.

Many known rectifier structures (e.g., center-tapped rectifier, current-doubler rectifier, full-bridge rectifier, switched-capacitor step-down rectifier [34], etc.,) are compatible with the MultiTrack architecture. A full-bridge rectifier with high transformer winding usage and high experimental flexibility is selected as the example in this paper. One can also envision an implementation with multiple secondary transformer windings, separate rectifiers, and separate outputs, which benefits the distribution of power processing at the expense of higher component count.

IV. Comparative Analysis

The boost-type two-stage (BTS) power conversion architecture as shown Fig. 7 is widely used in wide input voltage range applications, e.g., grid-interface power factor correction circuits [35]–[38]. In the BTS architecture, the input voltage is at first boosted to an relatively fixed intermediate bus voltage that is equal to or higher than the maximum input voltage. This voltage is then converted into the desired output voltage by an isolation stage with a fixed voltage conversion ratio.[1] Interestingly, the BTS converter could be thought of as a 1-Track embodiment of the MultiTrack architecture: there is only one power track and one intermediate voltage level. Alternatively, the n-Track circuit could be thought of as related to a "distributed" embodiment of a BTS circuit, with n equal voltage levels stacked on top of each other. Each domain has $\frac{1}{n}$ of the rated input voltage, and processes $\frac{1}{n}$ of the full rated power. The capacitive energy transferring mechanism ensures the power balancing of all distributed voltage domains.

To quantify the advantage of the MultiTrack architecture, we compare the 2-Track converter to a BTS converter for an input voltage range of $[V_{\min}, V_{\max}]$. The intermediate bus voltage of the conventional BTS converter is assumed to be $V_{\max}$. The two intermediate bus voltages of the 2-Track converter are $\frac{1}{2}V_{\max}$ and $V_{\max}$. A generalized comparative analysis considering n-Track converters is provided in Appendix to investigate how the advantage scales as the number of tracks increase.

A. Reduced Regulation Inductor Size

Both the BTS converter and the 2-Track converter have a voltage regulation inductor (L_R) in the regulation stage. The size of L_R is related to the maximum amount of energy that it needs to buffer in each switching cycle, which is related to the voltage conversion ratio of the regulation stage [39]. We define Γ_E as the ratio between the energy buffered in the inductor in each switching cycle and the total energy that the converter delivers in each switching cycle. For a fixed output power, a higher Γ_E ratio indicates a higher inductive energy buffering requirement, yielding a larger inductor size. As derived in Appendix, the Γ_E

[1] A buck-type two-stage architecture with a buck converter as the regulation stage is also widely used, especially in telecom power converters. In a buck-type implementation, the wide input voltage range is first regulated to a voltage that is lower than or equal to the minimum input voltage. The analysis results for such a converter would be quite similar in terms of device stresses and energy storage requirements. Since the Buck converter is a topological dual of the Boost converter, many of their theoretical characteristics are similar or even identical. The MultiTrack design we have implemented is more related to the BTS architecture because its regulation stage is more similar to a boost converter. As a result, we use the BTS architecture as a benchmark in this paper. We note that MultiTrack converters utilizing buck or buck/boost combination front-end topologies are likewise possible.

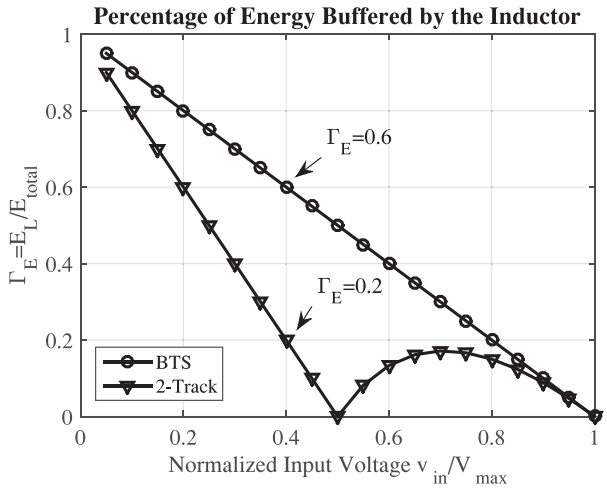

Fig. 8. Fraction of energy buffered by the regulation inductor in each switching cycle ($\Gamma_E = E_L/E_{\rm total}$). E_L is the energy buffered by the inductor. $E_{\rm total}$ is the total energy processed by the full system.

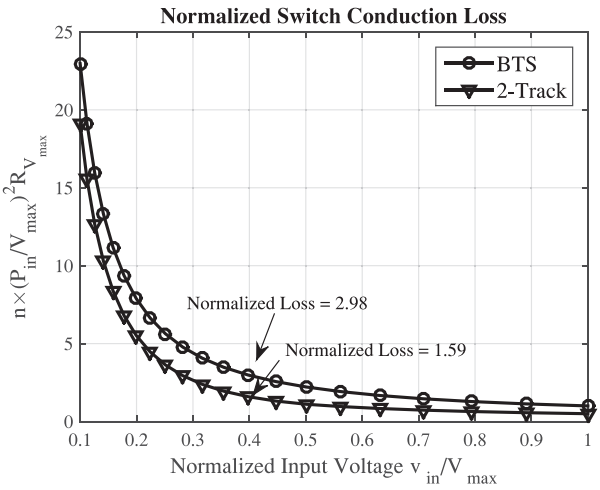

Fig. 9. Normalized switch conduction loss as a function of the normalized input voltage range. The 2-Track converter has a lower conduction loss than the boost converter (1-Track) converter across the full input voltage range.

of the BTS converter when $v_{\rm in} \in [V_{\rm min}, V_{\rm max}]$ is

$$\Gamma_{\rm E,BTS}|_{v_{\rm in}\in[V_{\rm min},V_{\rm max}]} = 1 - \frac{v_{\rm in}}{V_{\rm max}}. \tag{3}$$

Γ_E increases monotonically as the input voltage reduces. This is because the boost converter in the BTS architecture has a higher voltage conversion ratio if the input voltage is lower. The inductor needs to be sized for the worst case—when the input voltage equals to $V_{\rm min}$. The Γ_E of a 2-Track converter is a piecewise function of $v_{\rm in}$. As derived in Appendix, the Γ_E when $v_{\rm in} \in [0, \frac{1}{2}V_{\rm max}]$ is

$$\Gamma_{E,\text{2-Track}}|_{v_{\rm in}\in[0,\frac{1}{2}V_{\rm max}]} = 1 - \frac{v_{\rm in}}{\frac{1}{2}V_{\rm max}}. \tag{4}$$

The Γ_E when $v_{\rm in} \in [\frac{1}{2}V_{\rm max}, V_{\rm max}]$ is

$$\Gamma_{E,\text{2-Track}}|_{v_{\rm in}\in[\frac{1}{2}V_{\rm max},V_{\rm max}]} = \frac{(V_{\rm max}-v_{\rm in})\left(v_{\rm in}-\frac{1}{2}V_{\rm max}\right)}{\frac{1}{2}V_{\rm max}v_{\rm in}}. \tag{5}$$

Equations (3)–(5) are plotted and compared in Fig. 8. The Γ_E of the 2-Track converter is lower than that of the BTS converter across the full input voltage range. As labeled in Fig. 8, if the input voltage range is $[0.4V_{\rm max}, V_{\rm max}]$, the peak maximum Γ_E of the 2-Track converter is one-third lower than that of the BTS converter, indicating significant (approximately 3×) reduction in inductor size. This advantage is similar to the reduced inductor size in a three-level or multilevel boost [36] or buck [40] converters.

B. Reduced Switch Conduction Loss and Switch Stress

The switches in the regulation stage of the BTS converter (S_1 and S_2) have to block the peak input voltage ($V_{\rm max}$). In the 2-Track converter shown in Fig. 3, S_1, S_2, and S_3 only need to block $\frac{1}{2}V_{\rm max}$. S_4 still needs to block $V_{\rm max}$, but it only conducts for a portion of the input voltage range. This mechanism reduces the conduction loss of the switches. Consider a simple model that gives an approximate estimate of the loss reductions that are ideally available, it is derived in [41] that for an ideal Schottky junction device, the on-resistance (per die area) of the drift region is a quadratic function of its rated voltage V_B

$$R_{\rm dson-1} = \frac{4V_B^2}{\epsilon_S \mu_n E_C^3} \tag{6}$$

where $\epsilon_S \mu_n E_C^3$ is a constant that is related to the material characteristics ("Baliga figure-of-merit").

In a BTS converter, S_A and S_B must reach blocks $V_{\rm max}$. Assuming that both of them have the same drain-to-source resistance $R_{V_{\rm max}}$, and the regulation inductor has small current ripple, the total conduction loss in the two switches can be calculated as a function of the input voltage ($v_{\rm in}$) and input power ($P_{\rm in}$)

$$\text{Loss}_{\rm BTS} = \left(\frac{P_{\rm in}}{v_{\rm in}}\right)^2 R_{V_{\rm max}}. \tag{7}$$

In a 2-Track converter, S_1, S_2, and S_3 need to block $\frac{V_{\rm max}}{2}$. According to (B-1), with the device resistance as a quadratic function of the rated voltage, their resistance can be approximated as $\frac{R_{V_{\rm max}}}{4}$. S_4 needs to block $V_{\rm max}$, and its resistance is $R_{V_{\rm max}}$. As derived in Appendix, when $v_{\rm in} \in [0, \frac{1}{2}V_{\rm max}]$, the total conduction loss in the devices of the switched-inductor circuit can be estimated as

$$\text{Loss}_{\text{2-Track}} = \frac{P_{\rm in}^2}{2v_{\rm in}^2} R_{V_{\rm max}}. \tag{8}$$

When $v_{\rm in} \in [\frac{1}{2}V_{\rm max}, V_{\rm max}]$

$$\text{Loss}_{\text{2-Track}} = \frac{P_{\rm in}^2}{v_{\rm in}^2} R_{V_{\rm max}} \left(1 - \frac{v_{\rm in}}{V_{\rm max}}\right). \tag{9}$$

Equations (7)–(9) are plotted and compared in Fig. 9. As labeled in Fig. 9, if $v_{\rm in} \in [0.4V_{\rm max}, V_{\rm max}]$, the estimated conduction loss of the 2-Track converter is ideally approximately half of the BTS converter.

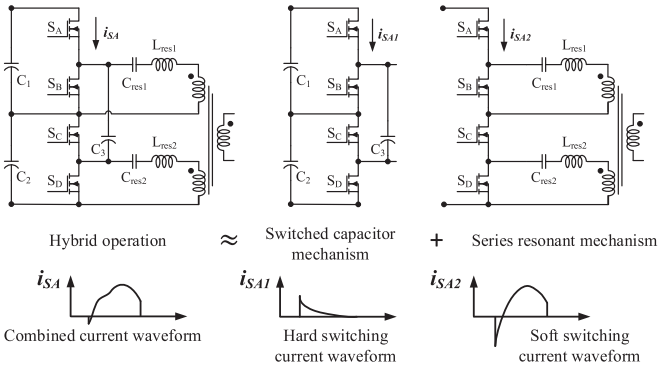

Fig. 10. *Hybrid switched-capacitor/magnetics* circuit structure can be approximated as the superposition of a hard-switched hard-charged ladder switched-capacitor circuit, and multiple stacked ZVS resonant circuits.

TABLE I
BOM OF THE PROTOTYPE CONVERTER

Device Symbol	Component Description
S_1–S_4, S_A–S_D	EPC2016c
L_R	Coilcraft EPL6024-522ME: 5.2 μH, 44 mΩ, height (measured): 2 mm
C_{in}	X5R Ceramic, 100 V, 2 μF, 1206
C_1, C_2	X7R Ceramic, 50 V, 10 μF, 1206
C_3	X7R Ceramic, 50 V, 15 μF, 1206
C_{out}	X5R Ceramic, 10 V, 188 μF, 0805
C_{res1}, C_{res2}	Each consists two paralleled capacitors: One C0G ceramic, 50 V, 0.1 μF, 1206; One X7R ceramic, 50 V, 0.2 μF, 1206;
MISO Transformer	Ferroxcube EQ13, Core material 3F45, turns ratio 4:4:1, 8-layer PCB layers and 2 external 2 oz foil layers.
Q_1–Q_4	EPC2023c

In this idealized estimation, the difference between the die area of the boost/buck converter and the die area of the n-track converter is not rigorously controlled. The MultiTrack architecture reduces the voltage and current ratings of its devices by having higher component counts (with divided voltage/current ratings). A precise theoretical comparison considering these effects is beyond the scope of this paper. For a specific die area and a specific n-track converter, the optimal die-area allocation on each device also depends on the input voltage range and the rms current carried by each devices in the worst condition. All these factors may impact the tradeoff analysis in a specific design.

C. Soft Switching and Reduced Switching Loss

In the regulation stage, conventionally, the high-side switch of a boost converter (S_1 in Fig. 7) can operate as a diode, with zero voltage turn on. Under PWM operation with small inductor current ripple (continuous conduction mode, CCM), the low-side switch (S_2) is usually hard-switched at both turn on and turn off. The rated voltage of S_2 is $V_{\max}$, and S_2 always switched with its drain-to-source voltage equals $V_{\max}$ regardless of v_{in}. In a 2-Track converter, the low-side switches (S_2 and S_4) may also be hard-switched with the CCM operation. The voltage ratings of these switches are $\frac{1}{2}V_{\max}$ and $V_{\max}$, respectively. Although their voltage ratings are different, when they are switching, their off-state drain-to-source voltages are always $\frac{1}{2}V_{\max}$, which is half of the switching voltage of the devices in the BTS converter ($V_{\max}$), yielding reduced total switching loss. Moreover, given the reduced ranges over which an individual switch set must be operated, it can be easier to realize soft switching of the boost stage, with consequent performance or size benefits.

In the merged isolation stage, the combination of the switched capacitor circuits and the MISO transformer (the *hybrid switched-capacitor/magnetics* circuit structure) creates both soft-switching and soft-charging opportunities for the switched-capacitor switches [13], [18], [24]–[26]. In the 2-track converter shown in Fig. 10, the operation of S_A–S_D can be interpreted as the superposition of a switched-capacitor circuit and two series-resonant circuits. As shown in Fig. 10, the switched-capacitor circuit consists S_A–S_D, C_1, C_2, and C_3. Here S_A and S_B are one pair of half-bridge switches. S_C and S_D are another pair of half-bridge switches. S_A and S_C are synchronously switched as one phase, and S_B and S_D are synchronously switched as the other phase. Energy is transferred by C_3 across the two voltage domains.

At the same time, S_A, S_B, C_{res1}, and L_{res1} formulate one series-resonant circuit, and S_C, S_D, C_{res2}, and L_{res2} formulate another series-resonant circuit. The two series-resonant circuits are coupled by the transformer, adding one additional path for energy transfer that can operate together with the switched capacitor energy transfer. When the input voltage is low, significant power is processed by the switched-capacitor mechanism—the switches consequently see a net capacitive load and are hard-switched; when the input voltage is high, the power is processed by the series-resonant mechanism (and delivered to the output) is sufficient for switches to have a net inductive load, enabling ZVS of the switches, which is beneficial for high-frequency designs.

V. PROTOTYPE DESIGN

To demonstrate the advantages of the MultiTrack power conversion architecture, an 18–80 V input, 5 V output, 15 A output, 75 W, 800 kHz 2-Track converter has been built and tested. The prototype is designed based on the schematic shown in Fig. 3. The two intermediate voltage levels are regulated at 40 and 80 V, respectively. A simplified bill-of-materials (BOM) of the prototype is listed in Table I.

Figs. 11 and 12 show the gate drive implementation of the eight primary-side switches (S_1–S_4 and S_A–S_D), and four secondary-side switches (Q_1–Q_4). On the primary side, two identical gate drive modules are utilized. S_1, S_2, S_A, and S_B are driven by one gate drive module referred to the $\frac{1}{2}V_{\max}$ node. S_3, S_4, S_C, and S_D are driven by another gate drive module referred to the ground. Each gate drive module contains one linear regulator, four level shifters, and two half-bridge gate drivers (TI LM5113). The ground referenced gate drive module can be powered by V_X or by V_{in}. The $\frac{1}{2}V_{\max}$ referenced gate drive module is powered by C_1. This gate drive configuration is well suited to the MultiTrack architecture—the additional cost of the driving switches in the floating voltage domains is minimized.

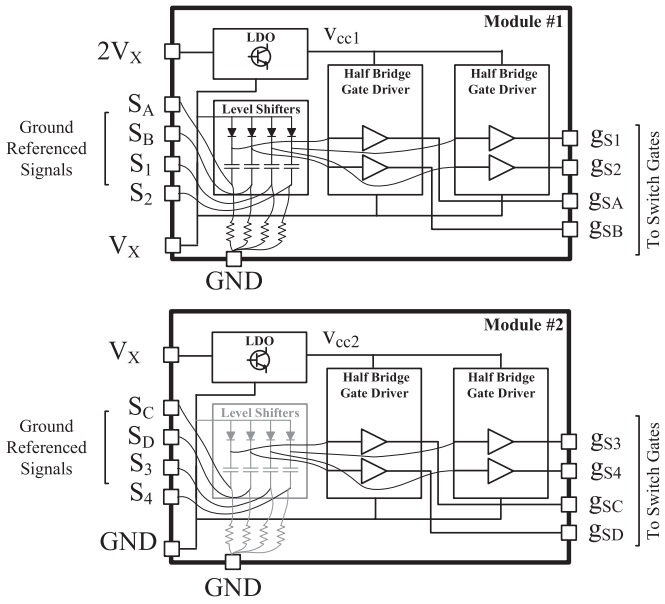

Fig. 11. Gate drive implementation of the primary-side switches. Two identical gate drive module are stacked in two voltage domains. This gate drive implementation can be easily extended and utilized in an n-track implementation. Note the level shifters for the ground-referenced switches (S_3, S_4, S_C, and S_D) are not necessary, and are not implemented in the prototype.

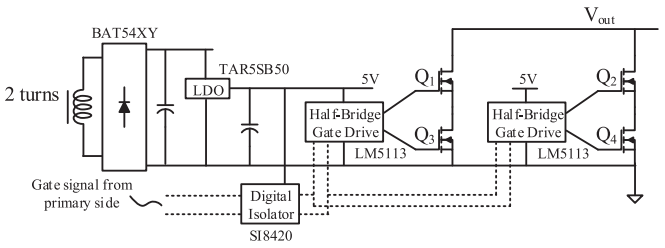

Fig. 12. Secondary-side gate drive circuitry consisting of two auxiliary turns on the transformer (generating +/−10 V), one full-bridge rectifier (BAT54XY), one LDO (TAR5SB50), one digital isolator (SI8420), and two half-bridge gate drivers (LM5113). This gate drive implementation can be modularized and utilized in designs with multiple output ports.

It can be easily integrated and extended to drive the switches in an n-track implementation. An auxiliary power source comprising an additional transformer winding (4-turns) with full-bridge diode arrays and linear regulators is utilized to power the two secondary-side half-bridge gate drivers.

A Texas Instruments TMS320F28069 microcontroller with four PWM channels is utilized to control the prototype. As explained in Fig. 4, there are two operating modes for the regulation switches (S_1–S_4): 1) when the input voltage is between 18 and 40 V, S_2 is kept ON, S_1 is kept OFF, and S_3 and S_4 switch; 2) when the input voltage is between 40 and 80 V, S_3 is kept ON, S_4 is kept OFF, and S_1 and S_2 switch. In actual operation, neither of S_2 and S_3 can be kept ON continuously—an interval is needed to enable the boot-strap and level-shifter capacitors to be refilled periodically. Also, when the input voltage is very close to 40 V, it is a challenge to modulate the duty ratio of S_2 and S_3 because their duty ratios are either very close to unity

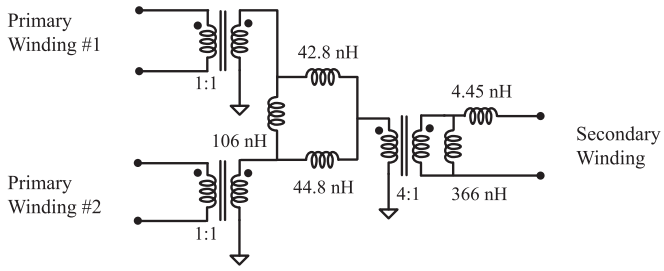

Fig. 14. Experimentally extracted cantilever model of the prototype MISO transformer.

or zero. To address these practical issues, we implemented a "dual modulation mode" operation in the experimental setup, in which both the two half-bridge pairs are modulated:

1) *Low Input Voltage Mode:* When the input voltage is below 40 V, S_1 is mostly kept OFF, and S_2 is mostly kept ON. S_2 may be switched OFF for a short period of time (minimum transistor on-time) every few switching cycles (10–20 cycles) to reset the level-shifter capacitor of S_2. S_3 and S_4 are switched at the PWM frequency.
2) *Dual Modulation Mode:* When the input voltage is close to 40 V, S_1 and S_4 are kept OFF, and S_2 and S_3 are kept ON. S_2 and S_3 may be switched OFFfor a short time every long period to reset their level-shifting capacitors. Modulating the difference between the on-time of S_2 and S_3 would provides the desired voltage regulation capability when the input voltage fluctuates around 40 V.
3) *High Input Voltage Mode:* When the input voltage is above 40 V, S_3 is mostly kept ON, and S_4 is mostly kept OFF. S_4 may be switched ON for a short period of time every few switching cycles to reset the boost-strap capacitor of S_3, and S_1 and S_2 are switched at the PWM frequency.

Measured waveforms illustrating these three operating modes are shown in Fig. 13.

The regulation inductor should be designed such that it can work efficiently across the wide input voltage range and power range. Low profile is also a critical requirement in this prototype as the inductor tends to be the tallest component on the board. We choose to size the inductor such that it has 50% current ripple when the input voltage is at 30 V, the output power is 75 W, with 800-kHz switching frequency. The average inductor current is 2.5 A, and the calculated inductance value is 3.75 μH. A low-profile Coilcraft inductor (EPL6024-522) with 2 mm measured thickness is utilized to implement this inductor. Its loss across the overall input voltage range is within the loss budget. It is the tallest component on the board. It also becomes a major loss component when the input voltage is close to the minimum of the full-voltage range (e.g., 18 V$< v_{\rm in} <$25 V). A custom-designed inductor with larger area and lower thickness could further improve the power density and efficiency of the prototype (for example, reducing the inductor height from 2 to 1.5 mm could raise the overall converter box power density from 453.7 to higher than 500 W/in^3.).

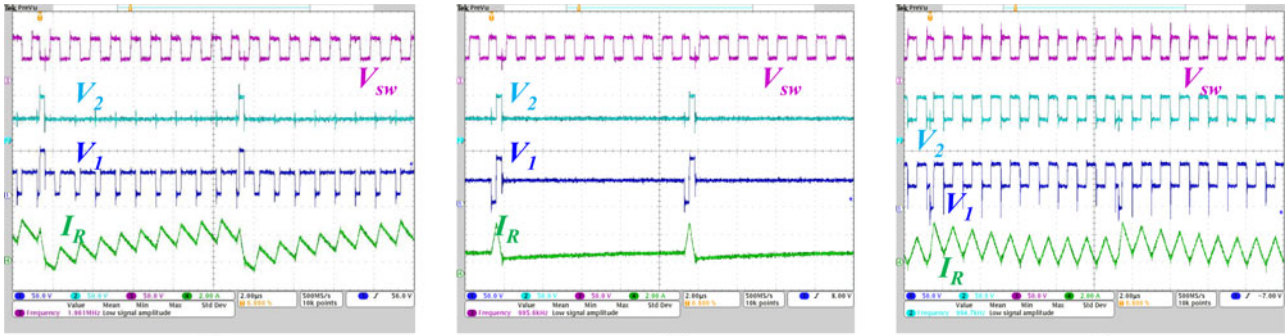

Fig. 13. Example operation waveforms of the prototype converter working in three different operation modes. $V_{\rm sw}$ is the voltage of the switch node between $\rm S_A$ and $\rm S_B$. V_1 is the voltage of the switch node between $\rm S_3$ and $\rm S_4$. V_2 is the voltage of the switch node between $\rm S_1$ and $\rm S_2$. $I_{\rm R}$ is the current of the regulation inductor. (a) Low input voltage mode: $v_{\rm in} = 20$ V, $I_{\rm out} = 7$ A, with $\rm S_1$ and $\rm S_2$ switched at 80 kHz, and $\rm S_3$ and $\rm S_4$ switched at 800 kHz; (b) dual modulation mode: $v_{\rm in} = 40$ V, $I_{\rm out} = 9.5$ A, with two half-bridges both switched at 80 kHz; (c) high input voltage mode: $v_{\rm in} = 60$ V, $I_{\rm out} = 10$ A, with $\rm S_1$ and $\rm S_2$ switched at 800 kHz, and $\rm S_3$ and $\rm S_4$ switched at 80 kHz. The dual-modulation frequency was selected as 80 kHz in this demonstration. This low-frequency fluctuation only exist in the inductor current, and has negligible impact on the system efficiency.

The multiple ac tracks in the isolation stage are implemented as low Q series-resonant converters. The resonant inductance of each low Q tank is created using the leakage inductance of the transformer, together with the PCB trace inductances. Since the resonant tank has low Q (when loaded with the equivalent rectifier resistance of 0.33 Ω at full power), close matching between the two primary windings is not necessary. The ac resistance of the secondary winding of the MISO transformer needs to be minimized because it has to carry the full output current (up to 15 A).

A Ferroxcube EQ13 core with 3F45 material was selected based on the core loss and winding loss analysis for the isolation transformer. It was selected also because it has suitable window-area/core-area/height combinations. The printed circuit board (PCB) winding was designed based on the planar magnetics modeling approach presented in [33]. The windings were fabricated on an eight-layer PCB with 2 oz copper on each layer. The finished PCB thickness is 52 mil (1.32 mm). Layers 1, 2, 7, 8 each have two series-connected turns. Layers 1 and 2 are connected in series through blind vias to implement a 4-turn primary winding. Layers 7 and 8 are also connected in series through blind vias to implement another 4-turn primary winding. Layers 3–6 are utilized to implement the single-turn secondary winding with the four layers connected in parallel. Two additional 2 oz foil layers were attached on top and bottom of the PCB. They are connected as added parallel secondary windings to enable a "symmetric-interleaving" configuration [33] to reduce the ac resistance and provide the design flexibility.

The loop inductance between the two legs of the secondary winding also contributes to the series-resonant tank. Utilizing the method provided in [42], the loop inductance is estimated to be about 3 nH. The trace inductances added by the switches are estimated to be about 0.5 nH. Fig. 14 shows the cantilever circuit model of the transformer extracted by doing open- and short-circuit measurements.

We seek to simplify the cantilever model to facilitate convenient design of the series-resonant tank of the MultiTrack converter. Fig. 15 illustrates a suggested four-step approach. This

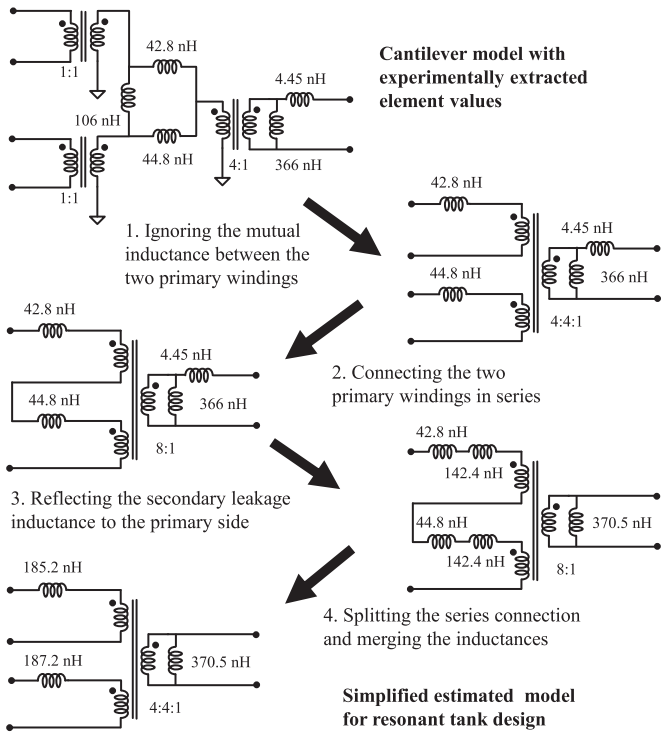

Fig. 15. Simplification of the cantilever model for the transformer to facilitate the resonant tank design.

approach is generally applicable to multiwinding transformers whose windings are driven by multiple identical voltage sources (e.g., by a switched-capacitor circuit).

1) Step 1: The mutual inductance between the two primary windings (the 106 nH inductance in Fig. 14) can be neglected because the two primary windings are driven by two identical voltage sources.
2) Step 2: The two 4-turn primary windings can be connected in series to formulate a single primary winding having eight turns (assuming good current sharing between the two primary windings).

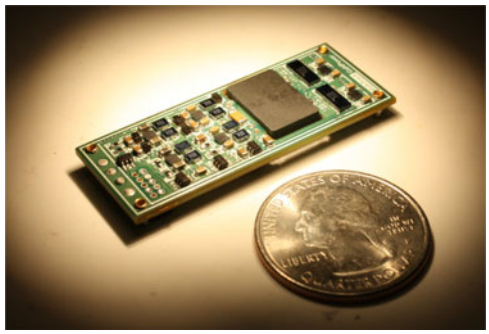

Fig. 16. MultiTrack 18–80 V input, 5 V output, 75 W isolated dc–dc converter, and a US quarter.

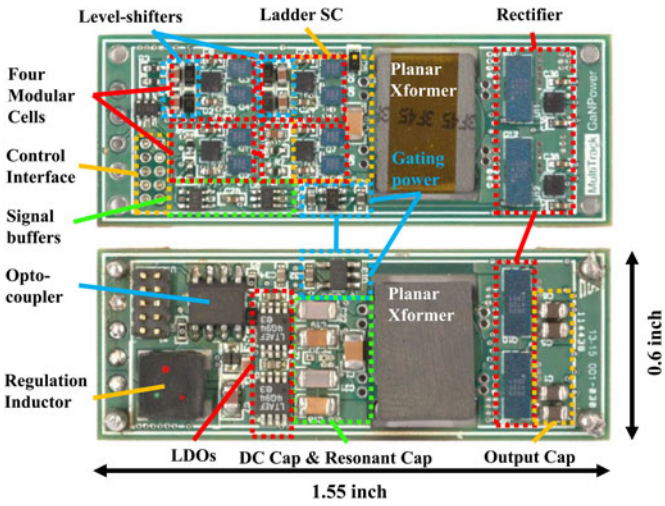

Fig. 17. Component placement on the top and bottom side of the PCB. The four modular half-bridge cells contain level shifters, LDOs, gate drivers, and switches.

3) Step 3: The secondary-side leakage inductance is reflected to the primary side and combined with the primary-side leakage inductances.
4) Step 4: The 8-turn primary winding is split into two 4-turn primary windings. Each winding has a half of the total primary-side leakage inductance.

Based on the estimated primary-side-lumped leakage inductance, the resonant capacitance is tuned to be 300 nF to set the *L–C* resonant frequency to be around 700–750 kHz.

Fig. 16 shows a picture of the prototype 18–80 V input, 5 V output, 75 W isolated dc–dc converter, and a US quarter. Fig. 17 shows component placement on the top and bottom sides of the PCB. There are four modular switch and gate drive circuits on the primary side. Each modular switch and gate drive circuits consists of two switches (EPC2016c) formulating a half-bridge, one LM5113 half-bridge gate drive, and the corresponding signal paths. They are placed on the top side of the PCB. The full-bridge rectifier consists four switches: two of them are on the top side of the board, and two of them are on the bottom side of the board. The optocoupler, linear regulator, capacitors, and other auxiliary circuits and chips are placed on

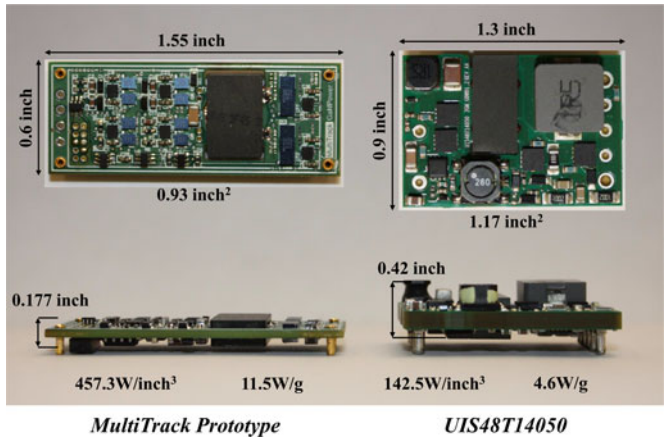

Fig. 18. Form factors of the prototype MultiTrack converter (left) and a comparable commercial converter (PowerOne UIS48T14050, right). The MultiTrack prototype has similar area but is three times thinner with much smaller inductor. Note that the (oversized) microcontroller (TMS320F28069) of the MultiTrack converter is off-board in the experimental prototype.

the bottom side of the board. The regulation inductor (L_R) is placed on the left-bottom corner of the PCB. The microcontroller, Texas Instruments TMS320F28069, interfaces with the prototype through a 10-pin interface. If a custom control IC was implemented, the 10-pin interface and many discrete logic components could be removed to further reduce the board area. An example MultiTrack IC controller implementation would include a controller for voltage regulation (e.g., a PI controller which observes the output voltage and adjusts the duty ratio), a mode selection circuit which determines the operation mode based on the input voltage, associated drivers and miscellaneous logics, and monitoring circuits.

VI. Experimental Results

A state-of-the-art commercial 1/16 brick 18–75 V input, 5 V output, 75 W isolated dc–dc converter (PowerOne UIS48T14050 [43]) was utilized to benchmark this MultiTrack prototype. This converter has the highest power density among commercial converters with similar input voltage range and the same output voltage that the authors were able to find. It is speculated to be a forward converter and has two major magnetic components with similar size—one inductor and one transformer. The PCB is relatively thick, suggesting high current and heat transfer capability.

Fig. 18 compares the form factors of the two converters. Both converters have two magnetic devices—one transformer and one inductor. Benefiting from the MultiTrack architecture and the higher switching frequency, the inductor of the MultiTrack converter is about six times smaller than the inductor utilized in the commercial converter (80 mm^3 versus 480 mm^3) and is much thinner. The distributed power devices in the MultiTrack architecture also facilitate the use of a much thinner PCB because heat generation is naturally distributed across the board. The box power density of the MultiTrack prototype is 457.3 W/in^3, which is 3.2 times higher than the 143.5 W/in^3 of the commercial product (the rated power is defined under 200 LFM 25 °C

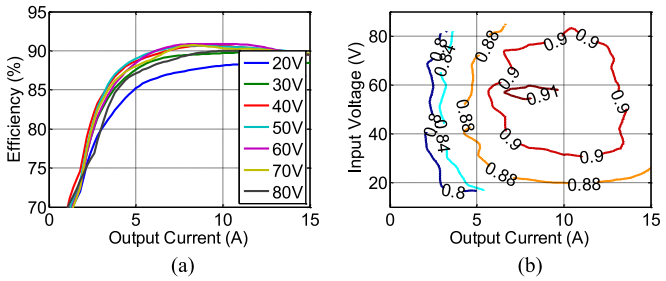

Fig. 19. Measured efficiency of the MultiTrack converter over the 18–80 V input, 0–15 A output range (200 LFM, 25 °C air flow).

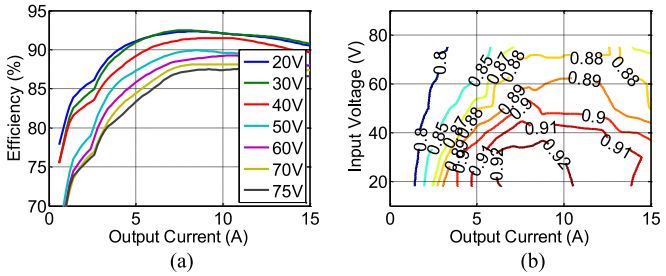

Fig. 20. Measured efficiency of the PowerOne converter over the 18–80 V input, 0–15 A output range (200 LFM, 25 °C air flow).

air flow and 125 °C peak device temperature). The prototype weights 6.53 g, which is 42.7% of the 15.3 g of the commercial product, and has a somewhat smaller overall surface area. As will be shown, the MultiTrack prototype has lower maximum board temperature, even though it dissipates a similar amount of heat, and has higher power density.

Fig. 19 shows the measured efficiency of the MultiTrack prototype with an ambient temperature of 25 °C at 200 LFM air flow (measured using a Pyle PMA90 digital anemometer with a 2.4 W fan providing the air flow). The prototype converter achieves a peak efficiency of 91.3% when the input voltage is 58 V and when the output current is 8 A. Its efficiency is comparable to the commercial product but shows a beneficial profile: when the input voltage is high, the MultiTrack converter is more efficient; when the input voltage is low, the commercial converter is more efficient. The efficiency of the MultiTrack prototype is relatively fixed across the 18–80 V input voltage range because operation across wide input voltage range is split into multiple voltage domains. The converter operates similarly in each voltage domain, although the input voltage is different. In contrast, the efficiency of the PowerOne UIS48T14050 spans across a wide range (as shown in Fig. 20). Its efficiency when $v_{\rm in} = 18$ V is about 5% higher than its efficiency when $v_{\rm in} = 75$ V).

With similar efficiency performance, the MultiTrack prototype dissipates a similar amount of total heat power through a roughly similar surface area (but with a thinner circuit board), while the overall temperature rise is lower. In the MultiTrack converter, heat is generated by multiple distributed devices, across a thinner PCB, providing a more uniform thermal distribution. Fig. 21 shows the thermal images of the MultiTrack

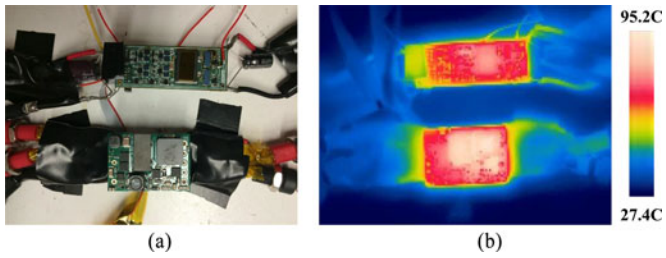

Fig. 21. Thermal image of the MultiTrack converter and the comparable commercial converter when they are working with 42 V input voltage and 7 A output current (0 LFM, 25 °C air flow).

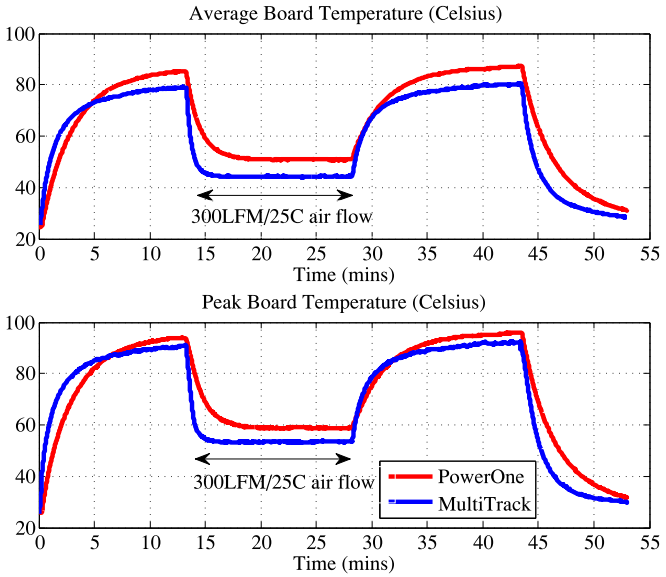

Fig. 22. Measured (a) average board temperature and (b) peak board temperature of the MultiTrack converter and the commercial converter. Both converters are delivering 7 A with 42 V input voltage.

converter and the commercial converter when they are operating in the same steady-state condition (41 V input, 5 V output, 7 A output, 0 LFM 25 °C air flow, measured using an FLIR SC300 thermal camera). Fig. 22 shows the recorded peak and average temperature curves of the two converters working under this condition, with and without the 300 LFM air flow. As a result of the thinner board and the reduced weight, the temperature of the MultiTrack prototype rises and falls faster than the commercial product, but its peak temperature was actually lower than that of the commercial product. Applying 300 LFM 25 °C air flow significantly reduces the temperature of both converters. It can be concluded that either with or without air flow, the MultiTrack converter enjoys a better thermal profile than the commercial converter, benefiting from the distributed power processing concept.

In this prototype design, a simple feedforward control based on a lookup table was implemented in the microcontroller. The duty ratio of the regulation stage is predetermined based on the desired input voltage and output power. Fig. 23(a) shows the startup transient waveforms of the converter when the input voltage ramps up from 0 to 30 V. The voltages of the switched

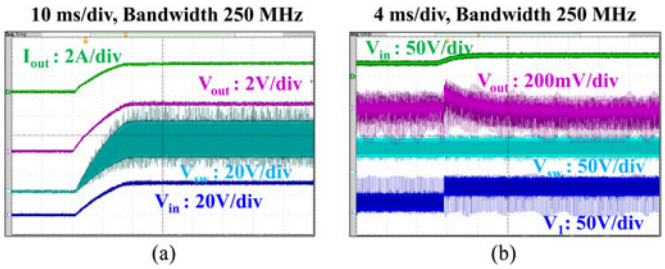

Fig. 23. (a) Input voltage startup transient waveforms when the input voltage ramps up from 0 to 30 V with 3.6 A load. (b) Input voltage step-up transient waveforms when the input voltage ramps up from 35 to 55 V with 3.6 A load. Probe bandwidth: 250 MHz; $I_{\rm out}$: output current; $V_{\rm out}$: output voltage; $V_{\rm sw}$: voltage of the switch node between $\rm S_A$ and $\rm S_B$; V_1: voltage of the switch node between $\rm S_3$ and $\rm S_4$.

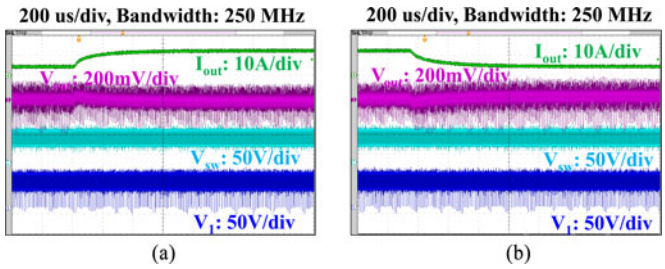

Fig. 24. Transient waveforms when the load current steps between 4 to 12 A and the input voltage is 60 V: (a) step up; (b) step down. Feedforward control; probe bandwidth: 250 MHz; $I_{\rm out}$: output current; $V_{\rm out}$: output voltage; $V_{\rm sw}$: voltage at the switch node between $\rm S_A$ and $\rm S_B$; V_1: voltage at the switch node between $\rm S_3$ and $\rm S_4$.

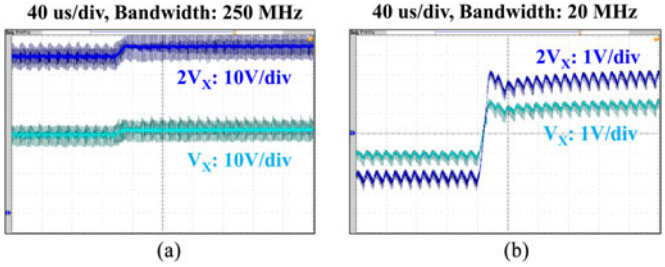

Fig. 25. Measured V_X transient waveforms when the load steps from 4 to 12 A and the input voltage is 60 V: (a) dc coupling; (b) ac coupling. In both ac and dc, the voltage of the V_X node follows closely in half with the voltage of the $2V_X$ node, indicating rapid and smooth switched-capacitor voltage balancing.

capacitors and the output voltage follow closely with the startup input voltage. Fig. 23(b) shows the input transient waveforms of the converter when the input voltage steps from 35 to 55 V (across the operation boundary). Since the operation of the regulation stage jumps directly from one state to another, a transient spike of 200 mV was observed in $V_{\rm out}$. Closed-loop control and external filters can be utilized to improve the transients.

Fig. 24 shows the transient waveforms of the converter when the load current steps between 4 and 12 A. Fig. 25 shows the transient waveforms of the voltages of the node V_X and $2V_X$ in both ac coupling and dc coupling when the load steps from 4 to 12 A. Due to the increased voltage drop in the isolation

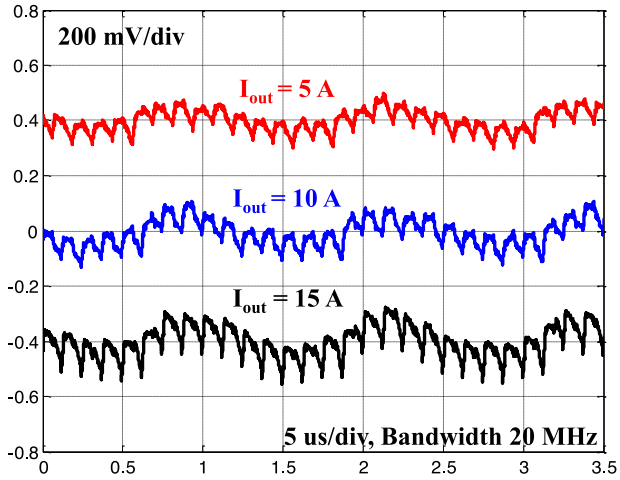

Fig. 26. Steady-state output voltage ripple when the output current is 5, 10, and 15 A, respectively (bandwidth: 20 MHz, input voltage 60 V). A low-frequency ripple (80 kHz) is observed due to the operation mechanism introduced in Fig. 13.

stage as a result of the higher load, the duty ratio of $\rm S_1$ needs to be slightly increased to maintain the output voltage, yielding step-up transients in V_X and $2V_X$. In this experimental setup, V_X steps from 40 to 42.5 V, and $2V_X$ steps from 80 to 85 V. In both ac and dc coupling measurements, the voltage of the V_X node follows closely in half with the voltage of the $2V_X$ node, indicating rapid and smooth voltage balancing of the switched capacitor circuit. Fig. 26 shows the output voltage ripple when the converter delivers 5, 10, and 15 A, respectively. The peak-to-peak output voltage ripple is maintained within 300 mV. A low-frequency ripple (about 80 kHz) with a period of ten switching cycles is observed, due to the low-frequency operation of the switched-inductor circuit described in Fig. 13.

Fig. 27 plots the efficiency and power density of the Multi-Track prototype and many state-of-the-art commercial products (with the power density defined under 200 LFM 25 °C air flow with 125 °C allowable device temperature). All of these commercial products have 18–75 V input ranges and 5 V output. They utilizes Silicon devices and switch at frequencies in the range of 200–300 kHz. By employing the proposed MultiTrack power conversion architecture with the reduced inductor size and PCB thickness, switching at higher frequency, and taking advantage of miniaturized GaN switches, the MultiTrack converter achieves 3× higher power density while maintaining comparable efficiency.

VII. Conclusion

A MultiTrack power conversion architecture that is suitable for designing isolated dc–dc converters with wide input voltage range is presented in this paper. This power conversion architecture represents a new way of combining switched-capacitor circuits and magnetics. It leverages the complementary strengths of switched-inductor, switched-capacitor, and magnetic isolation circuits, and gains mutual benefits from the way they are merged together. As demonstrated in the prototype, by process-

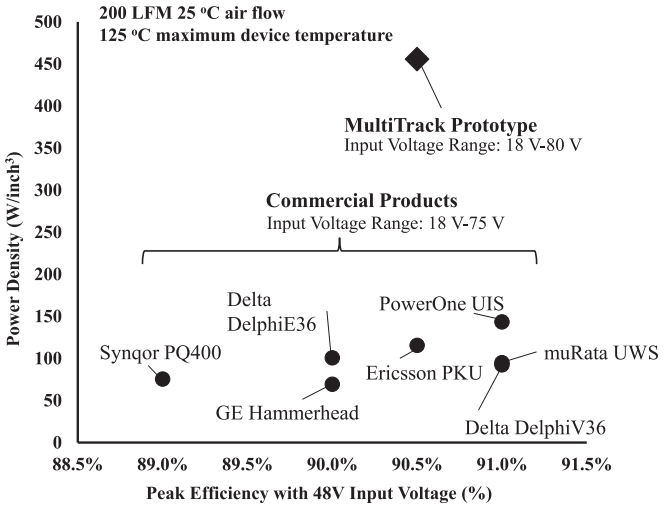

Fig. 27. Comparison of MultiTrack converter with many state-of-the-art commercial products. The MultiTrack converter achieves 3× higher power density while maintaining comparable efficiency performance. Note that the prototype MultiTrack converter does not include the microcontroller on board, though area is provided for a 10-pin connector to the microcontroller (and is included in the density calculation).

ing power in multiple voltage domains and current channels, multiple advantages can be achieved with the MultiTrack architecture to miniaturize wide input voltage range isolated dc–dc converters.

APPENDIX
EXTENDED TOPOLOGY ANALYSIS

In this appendix, we investigate how the advantages of the MultiTrack architecture scale with the number of tracks increases.

A. Generalized Inductor Energy Storage Analysis

In the MultiTrack architecture, the full input voltage range is split by the n intermediate bus voltages ($V_{\mathrm{Xk}} = \frac{k}{n}V_{\max}$, $k = 1, \ldots, n$) into n voltage domains. The inductor energy buffering ratio Γ_E is a piecewise function of the input voltage v_{in}. When v_{in} is located in the kth voltage subsection ($\frac{k-1}{n}V_{\max} < v_{\mathrm{in}} < \frac{k}{n}V_{\max}$), the regulation circuit can be modeled as a direct converter having v_{in} as the input voltage level, and $\frac{k-1}{n}V_{\max}$ and $\frac{k}{n}V_{\max}$ as the two output voltage levels, as illustrated in Fig. 28(a). Fig. 28(b) shows the inductor current i_R assuming that the converter works in critical CCM. In critical CCM mode, the inductor is fully charged and discharged, yield the highest inductor utilization ratio. The average current of i_R is I_{avg}, and the peak current of i_R is $I_{\mathrm{pk}} = 2I_{\mathrm{avg}}$. The switching period is T_{sw}. The total energy that is processed by this circuit in each switching cycle is

$$E_{\mathrm{total}} = v_{\mathrm{in}} \times I_{\mathrm{avg}} \times T_{\mathrm{sw}} = \frac{1}{2}V_{\mathrm{in}}I_{\mathrm{pk}}T_{\mathrm{sw}}. \tag{A-1}$$

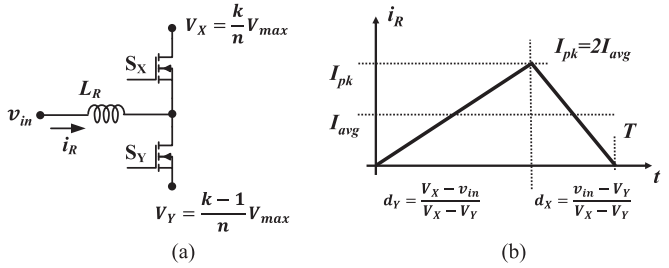

Fig. 28. The regulation circuit can be treated as a direct converter having V_{in}, V_X, and V_Y as the three node voltages.

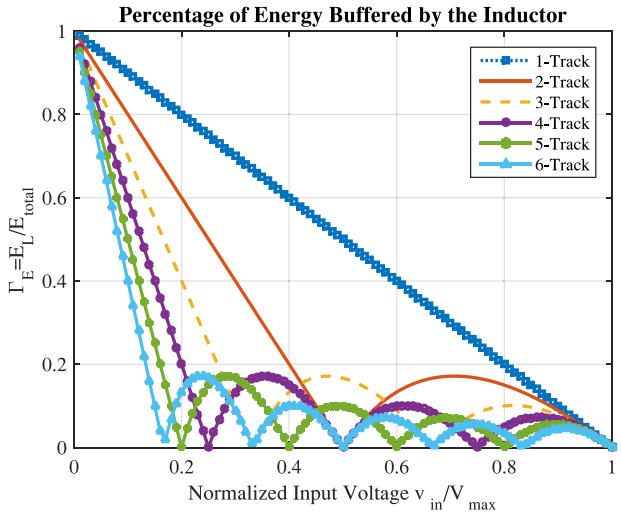

Fig. 29. Fraction of energy buffered by the regulation inductor in each switching cycle ($\Gamma_E = E_L/E_{\mathrm{total}}$). E_L is the energy buffered by the inductor. E_{total} is the energy processed by the full system.

The inductance value that allows critical CCM operation is

$$L_R = \frac{(V_X - v_{\mathrm{in}})d_X T_{\mathrm{sw}}}{I_{\mathrm{pk}}} = \frac{(V_X - v_{\mathrm{in}})(v_{\mathrm{in}} - V_Y)T_{\mathrm{sw}}}{I_{\mathrm{pk}}(V_X - V_Y)}. \tag{A-2}$$

The peak energy that is buffered in the inductor L_R is

$$E_{L_R} = \frac{1}{2}L_R I_{\mathrm{pk}}^2 = \frac{1}{2}\frac{(V_X - v_{\mathrm{in}})(v_{\mathrm{in}} - V_Y)T_{\mathrm{sw}}I_{\mathrm{pk}}}{(V_X - V_Y)}. \tag{A-3}$$

The percentage of energy that is buffered in the inductor when v_{in} belongs to $\frac{k-1}{n}V_{\max} \leftrightarrow \frac{k}{n}V_{\max}$ region Γ_E is

$$\begin{aligned}\Gamma_{\mathrm{E,n-track}}\big|_{\frac{k-1}{n}V_{\max} < v_{\mathrm{in}} < \frac{k}{n}V_{\max}]} &= \frac{E_{L_R}}{E_{\mathrm{total}}} \\ &= \frac{(V_X - v_{\mathrm{in}})(v_{\mathrm{in}} - V_Y)}{(V_X - V_Y)} \\ &= \frac{\left(\frac{k}{n}V_{\max} - v_{\mathrm{in}}\right)\left(v_{\mathrm{in}} - \frac{k-1}{n}V_{\max}\right)}{\frac{1}{n}V_{\max}v_{\mathrm{in}}}.\end{aligned} \tag{A-4}$$

Γ_E is plotted in Fig. 29 as a function of the normalized input voltage ($\frac{v_{\mathrm{in}}}{V_{\max}}$). The Γ_E of a 1-Track converter is identical to the Γ_E of a boost converter, while the Γ_E gradually reduces as the number of tracks increases. Fig. 30 compares the maximum Γ_E of multiple n-track converters as a function of the input

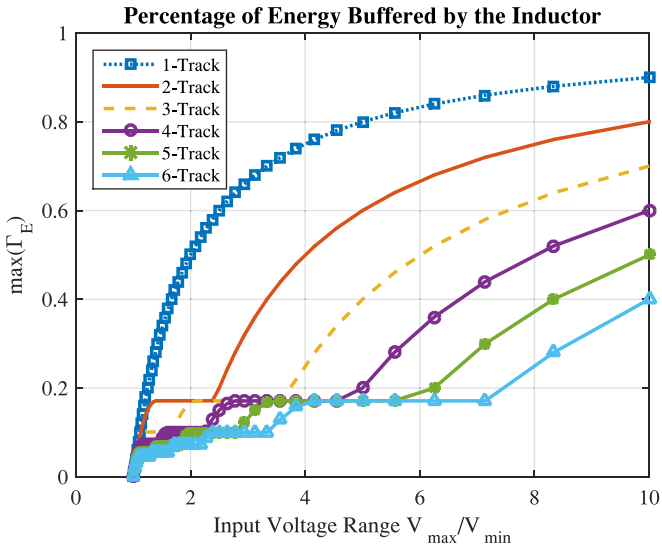

Fig. 30. Maximum fraction of energy buffered by the regulation inductor in each switching cycle ($\Gamma_E = E_L/E_{\text{total}}$). For a fixed overall power, Γ_E is proportional to the inductor size.

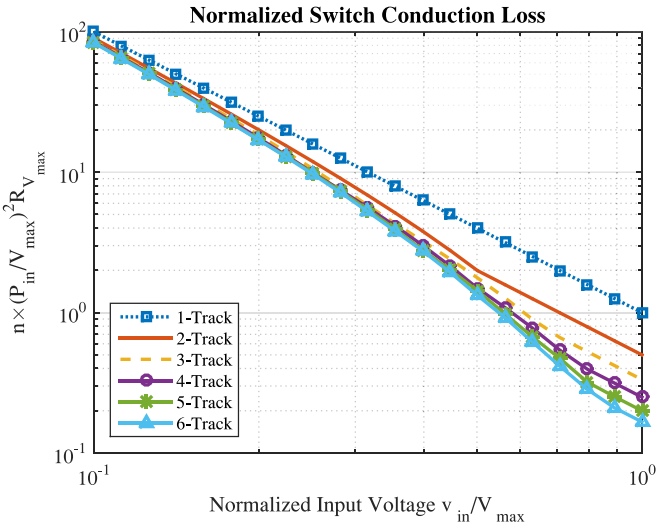

Fig. 31. Normalized total switch conduction loss as a function of the normalized input voltage $v_{\text{in}}/V_{\text{max}}$. The reference value $(P_{\text{in}}/V_{\text{max}})^2 R_{V_{\text{max}}}$ is the conduction loss of a 1-Track converter when $v_{\text{in}} = V_{\text{max}}$.

voltage range ($V_{\text{max}}/V_{\text{min}}$ ratio). For a specified input voltage range ($V_{\text{max}}/V_{\text{min}}$ ratio), increasing the number of tracks can reduce the maximum Γ_E, yield smaller regulation inductor size. As the number of tracks increases, the marginal advantage of adding more tracks gradually saturates. By taking the derivative of Γ_E relative to v_{in}, it can be calculated that in each voltage subsection, Γ_E reaches the local maximum when v_{in} equals the geometrical mean of the two adjacent intermediate voltages

$$v_{\text{in}} = \sqrt{V_X V_Y} = \sqrt{k(k-1)}\frac{V_{\text{max}}}{n}. \tag{A-5}$$

When $k > 1$, the maximum Γ_E when v_{in} is located in the kth voltage domain is

$$\begin{aligned}&\max(\Gamma_{E,n\text{-track}}|_{\frac{k-1}{n}V_{\text{max}} < v_{\text{in}} < \frac{k}{n}V_{\text{max}}]})\\ &= \frac{\sqrt{\frac{k}{n}V_{\text{max}}} - \sqrt{\frac{k-1}{n}V_{\text{max}}}}{\sqrt{\frac{k}{n}V_{\text{max}}} + \sqrt{\frac{k-1}{n}V_{\text{max}}}} = \frac{\sqrt{k}-\sqrt{k-1}}{\sqrt{k}+\sqrt{k-1}}.\end{aligned} \tag{A-6}$$

For a 1-Track converter, the Γ_E as a function of the normalized input voltage $\frac{v_{\text{in}}}{V_{\text{max}}}$ is

$$\Gamma_{E,\text{BTS}}|_{v_{\text{in}} \in [V_{\text{min}}, V_{\text{max}}]} = 1 - \frac{v_{\text{in}}}{V_{\text{max}}} \tag{A-7}$$

which is equal to the Γ_E of a BTS converter.

B. Generalized Switch Conduction Loss Analysis

The conduction loss of a circuit is related to the voltage and current rating of its devices. It is derived in [41] that for an ideal Schottky junction device, the on-resistance (per die area) is a quadratic function of its rated voltage V_B

$$R_{\text{dson}-1} = \frac{4V_B^2}{\epsilon_S \mu_n E_C^3} \tag{B-1}$$

where $\epsilon_S \mu_n E_C^3$ is a constant that is related to the material characteristics ("Baliga figure-of-merit").

In an n-Track converter, all high-side switches in the modular half-bridge pairs ($S_1, S_3, S_5, \ldots, S_{2n-1}$) need to block $\frac{V_{\text{max}}}{n}$. According to (B-1), since the device resistance is a quadratic function of the rated voltage, their resistance can be approximated as $\frac{R_{V_{\text{max}}}}{n^2}$. $R_{V_{\text{max}}}$ is the on-resistance per die area of a switch that need to block a voltage of V_{max}. The low-side switches in the modular half-bridge pairs (S_2, S_4, $S_6, \ldots, S_{2n}$) need to block ($\frac{1}{n}V_{\text{max}}$, $\frac{2}{n}V_{\text{max}}$, $\frac{3}{n}V_{\text{max}}, \ldots, \frac{n}{n}V_{\text{max}}$), respectively, and their resistances would ideally scale as ($\frac{R_{V_{\text{max}}}}{n^2}$, $\frac{2^2 R_{V_{\text{max}}}}{n^2}$, $\frac{3^2 R_{V_{\text{max}}}}{n^2}, \ldots, \frac{n^2 R_{V_{\text{max}}}}{n^2}$).

The total conduction loss is a piecewise function of the input voltage v_{in}. Using our idealized scaling rules, we can approximate the impact of the MultiTrack system on the device conduction loss. When v_{in} is between $\frac{k-1}{n}V_{\text{max}}$ and $\frac{k}{n}V_{\text{max}}$, a total of $(k-1)$ switches (S_{2n-1}, $S_{2n-3}, \ldots, S_{2n-2k+3}$) with their resistances equal to $\frac{R_{V_{\text{max}}}}{n^2}$ are kept ON and are conducting. One $\frac{R_{V_{\text{max}}}}{n^2}$ switch ($S_{2n-2k+1}$) and one $\frac{(n-k)^2}{n^2}R_{V_{\text{max}}}$ switch (S_{2n-2k}) are conducting with a duty ratio of ($\frac{v_{\text{in}}n}{V_{\text{max}}} - k + 1$); and one $\frac{(n-k+1)^2}{n^2}R_{V_{\text{max}}}$ switch ($S_{2n-2k+2}$) is conducting with a duty ratio of ($k - \frac{v_{\text{in}}n}{V_{\text{max}}}$). The input current i_{in} is also a function of v_{in}, $i_{\text{in}} = P_{\text{in}}/v_{\text{in}}$. Assume the inductor current equals the input current and has no ripple. The total conduction loss in the devices of the switched-inductor circuit can be estimated as

$$\begin{aligned}&\text{Loss}_{n\text{-Track}}\\ &= (k-1)\frac{P_{\text{in}}^2}{v_{\text{in}}^2}\frac{1}{n^2}R_{V_{\text{max}}}\\ &\quad + \frac{P_{\text{in}}^2}{v_{\text{in}}^2}\left(\frac{1}{n^2}R_{V_{\text{max}}} + \frac{(n-k)^2}{n^2}R_{V_{\text{max}}}\right)\left(\frac{v_{\text{in}}n}{V_{\text{max}}} - k + 1\right)\\ &\quad + \frac{P_{\text{in}}^2}{v_{\text{in}}^2}\left(\frac{(n-k+1)^2}{n^2}R_{V_{\text{max}}}\right)\left(k - \frac{v_{\text{in}}n}{V_{\text{max}}}\right).\end{aligned} \tag{B-2}$$

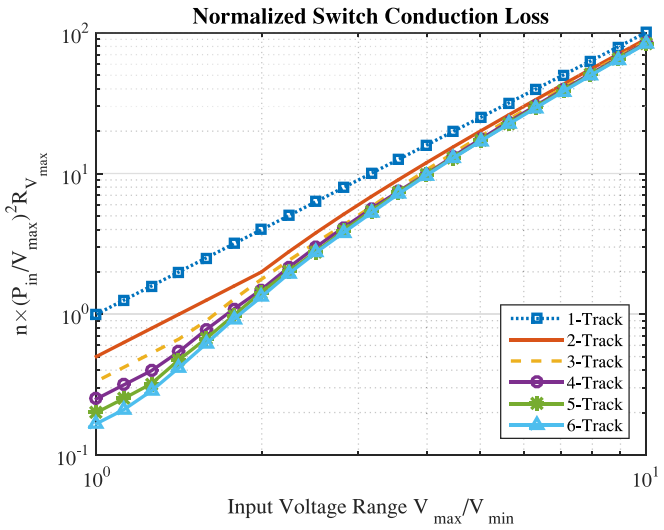

Fig. 32. Normalized total switch conduction loss as a function of the input voltage range $V_{\max}/V_{\min}$. As the input voltage range spans, the total switch conduction loss increases.

For a 1-track (or boost) converter, $k = 1$ and $n = 1$, the total conduction loss is

$$\text{Loss}_{\text{1-Track}} = \left(\frac{P_{\text{in}}}{v_{\text{in}}}\right)^2 R_{V_{\max}}. \tag{B-3}$$

Fig. 31 plots the estimated worst-case conduction loss of a few n-Track converters as a function of the normalized input voltage range ($v_{\text{in}}/V_{\max}$), assuming the device voltage scaling rule described previously in (B-2). Fig. 32 plots the same information as a function of the input voltage range $V_{\max}/V_{\min}$. The conduction loss scales quadratically with the input voltage range (because the conduction loss is a quadratic function of the input current). For an n-Track converter, when $1 < \frac{V_{\max}}{V_{\min}} < \frac{n}{n-1}$, the conduction loss is linearly reduced by a factor of $1/n$. For wider input voltage range, e.g., if $\frac{V_{\max}}{V_{\min}} > \frac{n}{n-1}$, the conduction loss gradually approach the conduction loss of the 1-Track converter.

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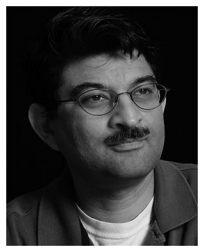

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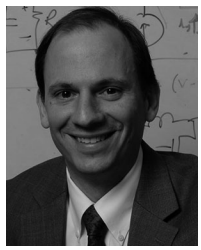

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