Measurement of IGBT High-Frequency Input Impedance in Short Circuit

Carmine Abbate, Giovanni Busatto, Annunziata Sanseverino, Francesco Velardi, Sara Iavarone, and Cesare Ronsisvalle

***Abstract*—Insulated-gate bipolar transistors (IGBTs) operated in short circuit become instable in certain driving and load conditions. The induced oscillations can compromise robustness and reliability of the entire power converter. The stability of the device inserted in a real system can be analyzed using the theory of linear oscillators that requires the knowledge of input or output impedance of the device in real operating conditions. In this paper, we present an experimental procedure for measuring in pulsed mode the small-signal impedance of a power device biased in any test conditions. The small-signal input impedance of a 650-V 20-A IGBT operated in short circuit has been measured as a function of the frequency. This input impedance has been used to extract the stability map of the IGBT in short circuit, which allows us to easily predict the test conditions where the IGBT becomes instable. The validity of this stability map has been confirmed by a large-signal time-domain characterization of the IGBT operated in short circuit. The proposed technique is very useful to design driving circuit able to avoid instable operations.**

***Index Terms*—High-frequency oscillation, IGBT short circuit, IGBT stability, input impedance measurement.**

I. Introduction

INSULATED-GATE bipolar transistors (IGBTs) are extensively used in motor drives and switching converters thanks to the easy controllability of the ON–OFF status and the good switching performances. However, in normal operation and/or in overload conditions, the device can become instable and can compromise the functionality of the entire system in terms of its reliability and electromagnetic interference. In particular, oscillations can be observed during the short circuit (SC), which is an undesired condition where the device can operate due to abnormal operation of the system where the device is inserted. These oscillations can compromise the device controllability and may induce an overstress on it.

The instabilities in SC have been widely studied. They have been often attributed to a negative gate capacitance, which appears at the input leads of the device. The presence of a negative capacitance serves to explain why at positive variation of the gate voltage corresponds to a negative variation of the gate current [1], [2]. This phenomenon was also attributed to the Miller capacitance of the device, which, in particular frequency ranges, may cause a positive feedback between the output and input terminals causing the circuit oscillation [3]. Both explanations underestimate the coupling between the device, its particular load condition (SC), and driving circuit.

The theory of linear oscillators was used to investigate about the origin of high-frequency oscillations by relating the device behavior with the external circuit parameters [4]. In this case, the device under test (DUT) was schematized as a linear two-port system with its impedance matrix, and it was demonstrated that the external circuit plays a relevant role in the device instability. A procedure based on the knowledge of the input impedance of the device has been also developed with the objective of avoiding dangerous oscillations during circuit operation through an appropriate design of the driver. Due to the difficulty in measuring this input impedance, the theory was validated using FEM simulations [4] and experiments in the time domain.

Actually, the measurement of the capacitance and more generally of the impedance between the terminals of a power device is not a trivial task in particular when it is operated in conduction or SC mode due to power dissipation and device self-heating.

An *LCR* meter was used for measuring the terminal capacitance of IGBTs in different bias conditions including the conduction one [5]. In this paper, the authors did not report the measurement of the real part of the impedance, which plays a relevant role in the instability of a power device as discussed in the following sections. On the other hand, the method used in [5] cannot be employed for measuring the impedance in SC because the time required to perform a measure by an *LCR* meter is several milliseconds, which would cause an unacceptable increase of the junction temperature during the SC tests.

In this paper, we describe an experimental procedure to measure the real and imaginary parts of the impedance between the input terminals of a power device in real bias conditions. It is applied to measure the input impedance of a 650-V field-stop trench-gate IGBT in SC conditions as a function of frequency in the range 1–100 MHz.

II. Theory Review

The conditions for having oscillations can be identified studying the simplified circuit model of Fig. 1, where the blocks related to driver, IGBT, load, and stray emitter impedance Z_e have been schematized [4]. In particular, in the typical applications, both driver and load in SC can be synthesized by resistive inductive (*RL*) network whose values are frequency dependent.

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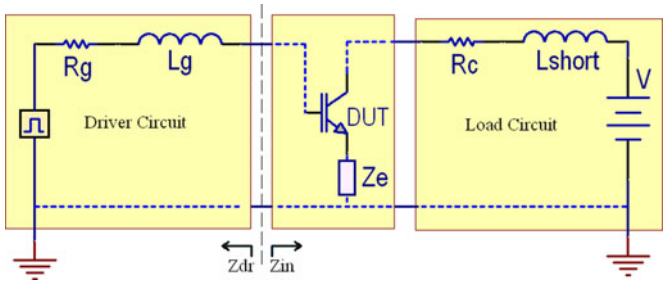

Fig. 1. Equivalent circuit of the system used for the analysis of the IGBT stability in SC.

In general, referring to the circuit of Fig. 1, we can write the condition for having persistent oscillations as

$$Z_{\rm dr} + Z_{\rm in} = 0 \tag{1}$$

where $Z_{\rm dr}$ is the output impedance of the driver circuit and $Z_{\rm in}$ is the equivalent input impedance of the device including the stray inductance Z_e and load effects of the output branch.

Equation (1) can be written in terms of real and imaginary parts as

$$\text{Imag}(Z_{\rm dr}) + \text{Imag}(Z_{\rm in}) = 0 \tag{2}$$

$$\text{Real}\,(Z_{\rm dr}) + \text{Real}(Z_{\rm in}) = 0. \tag{3}$$

Equation (2), which involves the imaginary part of Z, is a necessary condition for the oscillations to take place because it represents the condition for having the resonance between the reactance of the input external circuit (typically inductive) and the reactance of the device (typically capacitive). Moreover, this condition determines the frequency of the oscillations.

Equation (3) supplies the condition to have oscillations with a constant amplitude. If $\text{Real}(Z_{\rm dr}) + \text{Real}(Z_{\rm in}) > 0$, the circuit exhibits damped oscillation, whereas the oscillations become diverging when $\text{Real}(Z_{\rm dr}) + \text{Real}(Z_{\rm in}) < 0$.

III. Experimental Methodology

For measuring the input impedance of the DUT in real bias and load conditions, we have extended the voltamperometric method to the high-frequency range. The circuit used for the measurements is sketched in Fig. 2. It includes a precision high-frequency resistance, R_m, a radio frequency signal generator, RF, and a computer-controlled wideband oscilloscope. The method provides that R_m is inserted in series with the unknown impedance, Z_x, in order to convert the input current, I_x, in a voltage drops across it. This transformation allows us to measure only voltages with the oscilloscope avoiding the use of a current sensor, not easily available in the radio frequency range. The RF generator supplies the signal injected in the measurement box. Three decoupling dc capacitors of 1 μF each, namely $C_{\rm in}$, C_1, and C_2, have been added in order to decouple the static voltage applied on the DUT to bias it in the desired conditions. The voltages $V_{\rm in}$ and $V_{\rm out}$ are measured by the oscilloscope through two 50-Ω coaxial cables terminated with 50-Ω

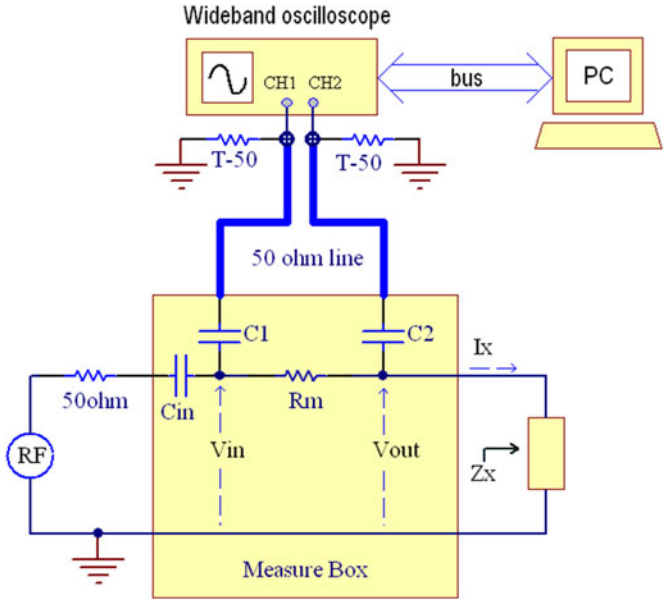

Fig. 2. Schematic of the circuit used for measuring input impedance of IGBT in SC.

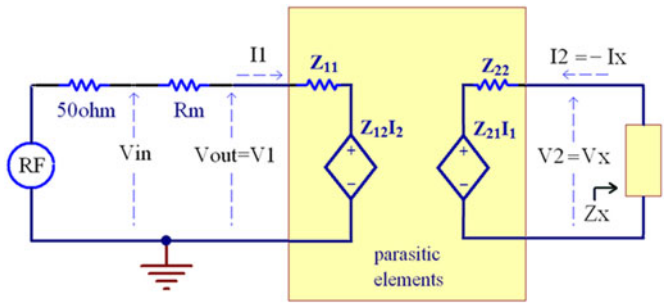

Fig. 3. Small-signal equivalent circuit of the measurement circuit.

resistances (T-50) placed as near as possible to the input channel, in order to minimize the reflected waves.

If we could neglect all the parasitic elements of the circuit, Z_x could be easily computed as

$$Z_x = \frac{V_{\rm out}}{I_X} = R_m \frac{V_{\rm out}}{V_{\rm in} - V_{\rm out}} \tag{4}$$

where $V_{\rm in}$ and $V_{\rm out}$ are phasors and can be expressed either as complex numbers or as modulus and phase. Unfortunately, at high frequency, the parasitic elements, like the input capacitance of the oscilloscope, the stray inductance, and the capacitance of the cables etc., become predominant and (4) cannot be used straightforwardly. For this reason, we have introduced the model of Fig. 3, where all the parasitic elements have been included in a two-port network described as a Z-parameter linear double dipole.

From the analysis of this circuit, after simple calculations, the unknown input impedance, defined as the ratio between V_x and I_x, can be calculated as

$$Z_x = \frac{V_X}{I_X} = -Z_{12}^2 \frac{V_{\rm in} - V_{\rm out}}{R_m\, V_{\rm in} - Z_{11}\,(V_{\rm in} - V_{\rm out})} - Z_{22} \tag{5}$$

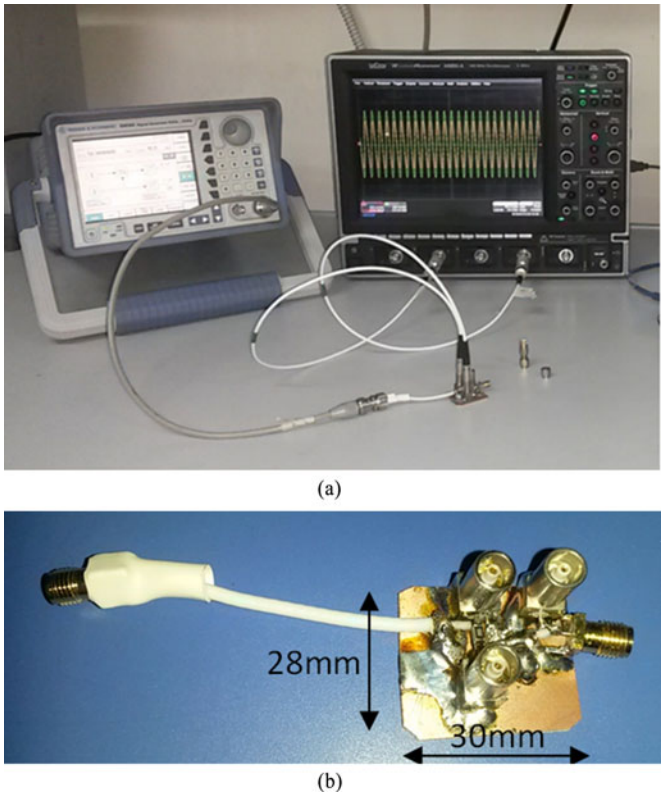

Fig. 4. (a) Experimental setup used for the impedance measurement. (b) Detail of the connection circuit.

where Z_{11}, Z_{12}, Z_{21}, and Z_{22} are the elements of the impedance matrix of the parasitic element network. It is worth to note that the parameters of the radio frequency generator and its connection to the circuit as well as the parasitic elements upstream R_m are not present in the equation, so they have no effect on the precision of the measurement.

Before using (5) for extracting Z_x from the measurement of V_{in} and V_{out}, the parameters of the impedance matrix of the parasitic network must be identified using the procedure depicted in the next section.

IV. Identification of Impedance Parameters of Parasitic Elements

The four parameters of impedance matrix of the experimental setup can be measured using a simple experimental procedure. Only three independent measurements are required because, in our case, $Z_{12} = Z_{21}$ due to the passive nature of our circuit [6]. The three measurements can be performed on the real circuit where we substitute Z_x with three known loads: SC, open circuit, and pure resistive load Z_0.

Let us consider the double dipole describing the parasitic elements in Fig. 3. The mentioned three load conditions result in $I_2 = 0$, $V_2 = 0$, and $Z_x = Z_0$, respectively, from which, after simple transformations, we obtain the following equations:

$$A = \left.\frac{V_1}{I_1}\right|_{\text{open circuit}} = Z_{11} \tag{6}$$

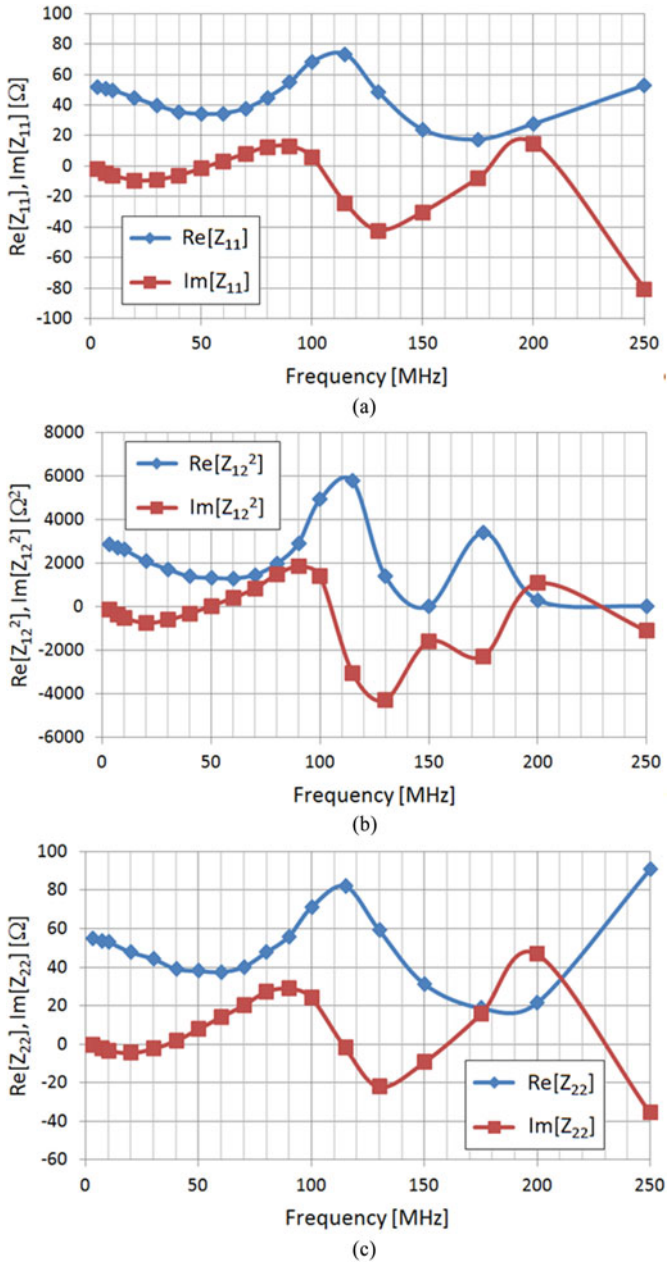

Fig. 5. Parameters of the parasitic impedance matrix of the setup used for the impedance measurement as a function of the frequency. (a) Z_{11}, (b) Z_{12}^2, and (c) Z_{22}.

$$B = \left.\frac{V_1}{I_1}\right|_{\text{short circuit}} = Z_{11} - \frac{Z_{12}^2}{Z_{22}} \tag{7}$$

$$C = \left.\frac{V_1}{I_1}\right|_{Z_o} = Z_{11} - \frac{Z_{12}^2}{Z_{22} + Z_o}. \tag{8}$$

Solving (7) and (8), we obtain

$$Z_{22} = \frac{Z_0\,(Z_{11} - C)}{C - B} \tag{9}$$

$$Z_{12}^2 = Z_{21} = (Z_{11} - B)\,Z_{22}. \tag{10}$$

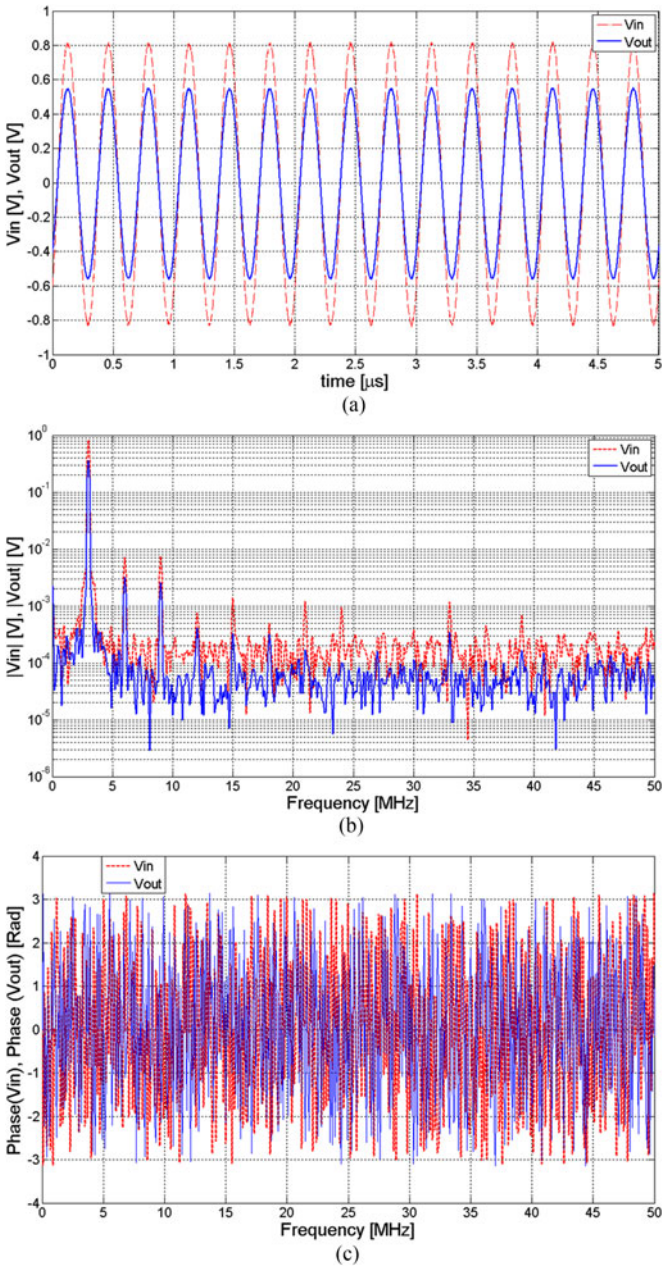

Fig. 6. Example of voltages $V_{\rm out}$ and $V_{\rm in}$ measured in the case of the dummy load Zx = 56 Ω//150 pF at f = 3 MHz. (a) Time-domain waveforms, (b) amplitudes, and (c) phases of their FFT.

Equations (6), (9), and (10) allow us to extract the parameters of the impedance matrix from the measurements of the quantities A, B, and C performed with the oscilloscope.

The measurements must be carried out one-off at different frequencies in the range of interest for obtaining the complete calibration matrix of the parasitic elements of the circuit to be used for the measurement of the unknown impedance.

V. Experimental Verification of the Impedance Measurement Method

As a first step, the proposed procedure was experimentally tested on known loads. A picture of the setup assembled is reported in Fig. 4(a). The circuit board constructed for mounting coupling capacitors and connectors is visible in Fig. 4(b). Standard 50-Ω RG and LEMO cables were used for connecting the circuit with the DUT, RF generator, and oscilloscope.

The procedure presented in the previous section was used for measuring the impedance matrix of the parasitic elements of the circuit. Results are supplied in Fig. 5(a)–(c) for Z_{11}, Z_{12}^2, and Z_{22}, respectively.

These parameters can be used in (5) for extracting the unknown impedance from the measurements of $V_{\rm in}$ and $V_{\rm out}$. It is worth to outline that any changes in the components, cables, or instruments of the setup would require a new identification procedure to be performed.

Several dummy loads, constituted by *RC* parallel circuits, have been assembled and characterized at different frequencies.

By way of example, Fig. 6(a) shows the waveforms of $V_{\rm in}$ and $V_{\rm out}$ measured in the case of a dummy load made of 56 Ω in parallel with 150 pF, indicated as $Z_x = 56\ \Omega//150$ pF in the following. Fig. 6(b) and (c) reports, respectively, the amplitude and the phase of the spectrum obtained as the fast Fourier transform (FFT) of the waveforms. It is possible to recognize the dominant component at 3 MHz that is the frequency of the signal supplied by the RF generator in this experiment.

The phasors of $V_{\rm in}$ and $V_{\rm out}$, required to compute Z_x at the imposed frequency, can be extracted from these spectra.

It is worth to note that this procedure allows us to reduce the measurement errors because the FFT points out the mean values of amplitude and phase of the harmonic component to be measured. Moreover, the application of the windowed FFT on the measured waveforms makes this technique suited to be applied in any pulsed operation as it is required for the measurement of the IGBT impedance in SC.

The measurement of $Z_x = 56\ \Omega//150$ pF has been repeated for several values of the input signal frequency. Fig. 7(a) and (b) shows the real and imaginary parts of this dummy load in the range 3–200 MHz, respectively. Measurements obtained with the proposed procedure (stars) are compared with those ones measured with a vector network analyzer (VNA) used as reference (circles). The agreement between the two sets of measurements is very good.

An extensive experimental characterization, not reported here for brevity, has been executed on several dummy loads in the ranges 1–1000 Ω and 10–1500 pF, which are expected to be the typical values for IGBT input impedance. The maximum error registered between the measurements with the proposed method and those ones with the VNA is less than 2.4% for the real parts and less than 1.5% for the imaginary parts.

VI. Measurement of Input Impedance of a 650-V 20-A IGBT in SC

The proposed technique was used to measure the input impedance of a 650-V 20-A trench-gate field-stop IGBT operated in SC. An experimental setup, which includes both the afore-described circuit and the biasing network able to bias the DUT in SC, was constructed. Its schematic is depicted in Fig. 8.

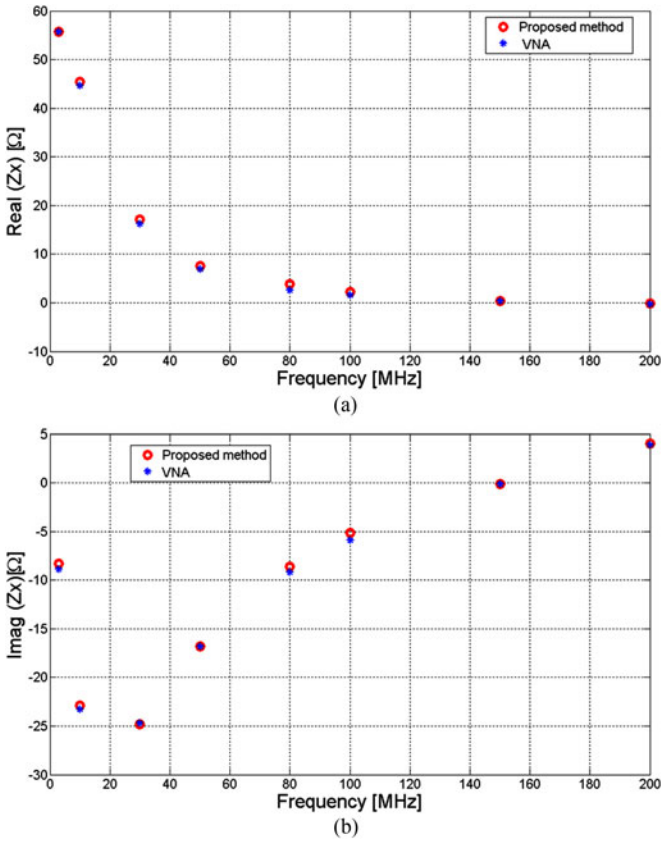

Fig. 7. Comparison between (a) real and (b) imaginary parts of the impedance Zx = 56 Ω//150 pF measured with the proposed method and a VNA.

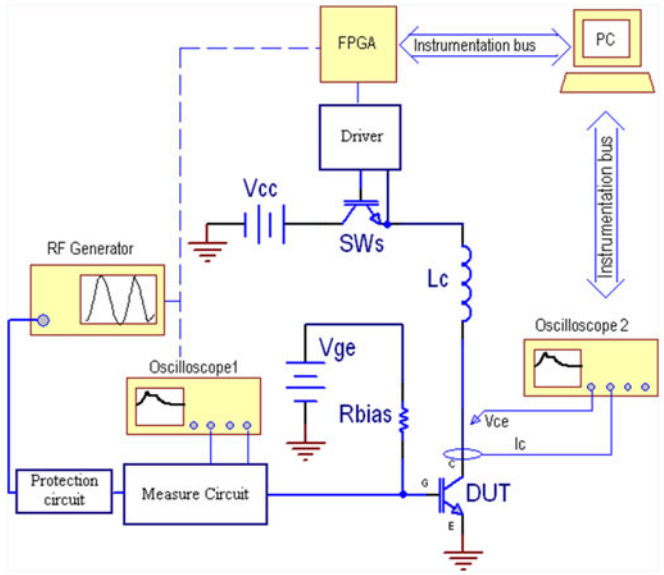

Fig. 8. Schematic of the setup used for the measurement of IGBT input impedance in SC.

A dc power supply is used to bias the gate at $V_{\rm ge}$ through the resistance $R_{\rm bias} = 1$ kΩ. The measurement circuit and the Oscilloscope1 are connected with the gate terminal. A protection circuit is inserted between the RF generator and the measurement circuit to avoid damages to the instrument in case of accidental failures of the DUT.

At the collector side, the inductance $L_{\rm c}$ accounts for the stray inductance of the SC for which a value between 35 and 60 nH in the range 1–300 MHz, with a mean value of about 50 nH, was measured with the VNA. The high-current series switch SWs, made of the parallel of six IGBTs rated at 1700 V 32 A, is used to connect the power supply $V_{\rm cc}$ to the DUT. Oscilloscope2 is used for the acquisition of the collector voltage and current waveforms for which a Rogowsky coil current probe is used. A field-programmable-gate-array-based electronic circuit is employed to generate the logic signals to drive SWs. All the instruments are connected to a PC for data elaboration.

The test procedure provides that before starting the measurement, SWs is left open to block $V_{\rm cc}$, DUT is biased at the required value of $V_{\rm ge}$ and the RF generator is injecting the RF signal. The measurement starts when SWs is turned ON and collector current builds up with a slope limited by L_c. It reaches the SC current determined by the value assigned to $V_{\rm ge}$. In such a way, the DUT experiences an SC similar to the SC1 type [7] from which it differs only in the transient phase required to reach the SC current. In fact, in our test, this transient is associated with the turn-on of SWs and the consequent charge of L_c, whereas in SC1 type, the transient is associated with the buildup of the DUT gate voltage.

It is worth noting that SWs is in the on-state during the SC phase and is not subjected to oscillations, whereas DUT is in the active zone where oscillations can appear. During the test, the waveforms are acquired and afterword analyzed offline.

By way of example, Fig. 9 reports a set of waveforms acquired for the measurement of the IGBT input impedance in SC. The test conditions are $V_{\rm cc} = 400$ V, $V_{\rm ge} = 12$ V, $L_c = 50$ nH, and $f = 10$ MHz, where f is the frequency of the input RF signal. In particular, Fig. 9(a) shows the collector current and voltage waveforms. The duration of the SC was set at about 14 μs resulting in a peak power of about 20 kW and a total energy of about 230 mJ. The waveforms of $V_{\rm in}$ and $V_{\rm out}$ are depicted in Fig. 9(b) with dashed and solid lines, respectively. Their zoom in the interval 6–8 μs is reported in the inset. We can see that at the device turn-on (∼0 μs) and turn-off (≈14.5 μs), the input signals are affected by two voltage transients, which must be excluded from the elaboration. The windowed discrete Fourier transform (DFT) is used for the extraction of amplitude and phase of $V_{\rm in}$ and $V_{\rm out}$ at the frequency of the injected signal. In this case, the FFT algorithm of MATLAB was applied in the time interval from 6 to 8 μs delimited with two segments in Fig. 9(b). The sampling frequency was 500 Msamples/s. A Hamming prefilter window was used.

The above procedure has been applied to obtain the IGBT input impedance as a function of the frequency in the range from 3 to 100 MHz. Results are reported in Fig. 10(a) and (b) for the real and imaginary parts, respectively. The measurements were executed at different collector-to-emitter voltages in the range from 50 to 400 V and at a fixed gate-to-emitter voltage of 12 V. It is worth to outline that we limited the measurement of $Z_{\rm in}$ in the range 3–100 MHz because we have never observed oscillation

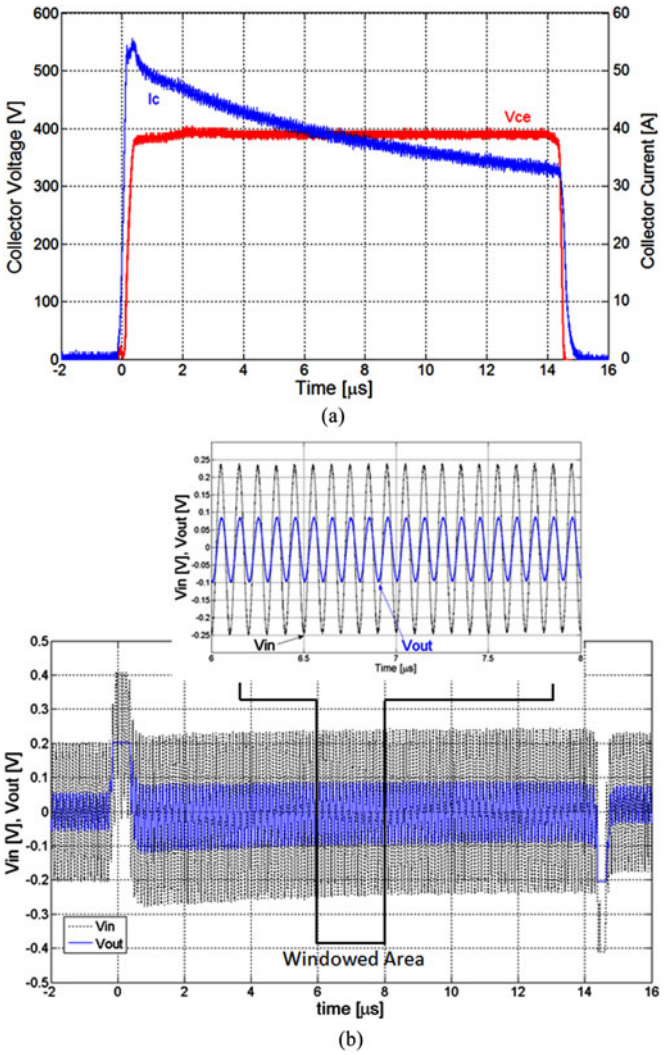

Fig. 9. Waveforms acquired for the measurement of the IGBT input impedance in SC. Test conditions: $V_{\rm cc} = 400$ V, $V_{\rm ge} = 12$ V, $L_c = 50$ nH, and $f = 10$ MHz. (a) Collector current, I_c, and voltage, $V_{\rm ce}$, waveforms (see Fig. 8). (b) Input $V_{\rm in}$ and output $V_{\rm out}$ signals measured (see Fig. 2). The inset is the zoom between 6 and 8 μs. The windowed area used for computing DFT is evidenced.

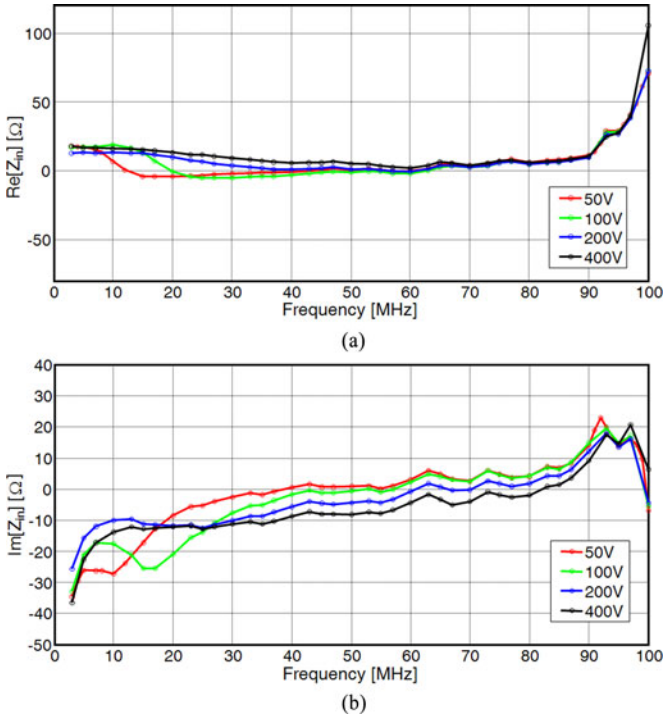

Fig. 10. Input impedance of IGBT in SC as a function of frequency at different collector voltage, $V_{\rm ge} = 12$ V and $L_c = 50$ nH. (a) Real and (b) imaginary parts.

frequencies larger than 70 MHz for the IGBTs analyzed in all the test conditions considered.

From Fig. 10(a), we can see that the real part of the input impedance increases with the collector voltage, whereas the imaginary part [see Fig. 10(b)] decreases at higher collector voltages due to the IGBT stray capacitance decrease. These data are used in the next section to extract the stability map of the IGBT.

VII. Stability Map of IGBT in SC

As reminded in Section II, (2) and (3) represent the conditions for having oscillations with a constant amplitude. But also the case with $\text{Real}(Z_{\rm dr}) + \text{Real}(Z_{\rm in}) < 0$ must be considered as instable. In fact, it corresponds to diverging oscillations which become stable in the real circuit because of its nonlinearity which limits and stabilizes the amplitude of these oscillations. In other words, we can say that (2) and (3) set a boundary between stable and instable operations of the circuit.

Let us consider the driver as inductive and characterized by its equivalent turn-on gate resistance, $R_{g,\rm on} = \text{Real}(Z_{\rm dr})$, and gate stray inductance $L_g = \text{Imag}(Z_{\rm dr})/2\pi f$. Both these quantities are positive so that we have to consider only $Z_{\rm in}$ having real and imaginary parts both negative for satisfying (2) and (3).

From this perspective, results of Fig. 10(a) indicate that the IGBT under test with $L_c = 50$ nH and $V_{\rm ge} = 12$ V is always stable at $V_{\rm cc} = 400$ V. In fact, for this voltage, $\text{Real}(Z_{\rm dr})$ is positive in the whole range from 3 to 100 MHz.

For the other collector voltages, the frequency ranges where the IGBT becomes instable are restricted to those frequencies for which both real and imaginary parts of $Z_{\rm in}$ are negative, namely 12–40, 20–52, and 55–60 MHz for $V_{\rm cc} = 50$, 100, and 200 V, respectively.

For these frequencies, let us plot the curves on the plane $R_{g,\rm on}$–L_g for which (2) and (3) are satisfied. The resulting stability maps at different collector voltages are reported in Fig. 11. For each value of $V_{\rm cc}$, the couples $R_{g,\rm on}$–L_g on the left side of the related curve make the IGBT instable because for them $R_{g,\rm on} + \text{Real}(Z_{\rm in}) < 0$, whereas the device is stable for the points on the right side of the curve being there $R_{g,\rm on} + \text{Real}(Z_{\rm in}) > 0$.

As a comment on the results of Fig. 11, we can say that the IGBT under test becomes more stable at increasing values of the collector voltage. At $V_{\rm cc} = 200$ V, oscillations at about 60 MHz are observed only for very low values of $R_{g,\rm on}$ ($\sim$0.5 Ω) and L_g ($\sim$2 nH).

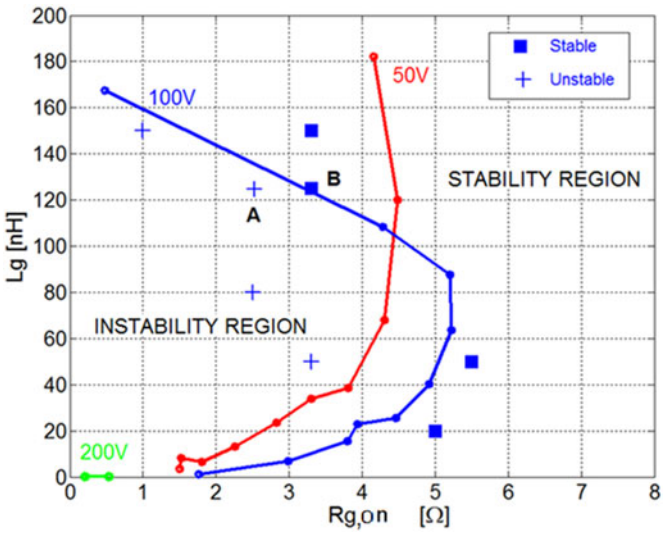

Fig. 11. Stability maps of the IGBT in SC obtained from (2) and (3) assuming a resistive/inductive gate driver with $V_{\rm ge} = 12$ V, for $L_c = 50$ nH and different collector voltages. For verification of the stability regions, time-domain SC tests were executed and reported as points in the figure. In particular, "crosses" and "squares" correspond to instable and stable SCs, respectively.

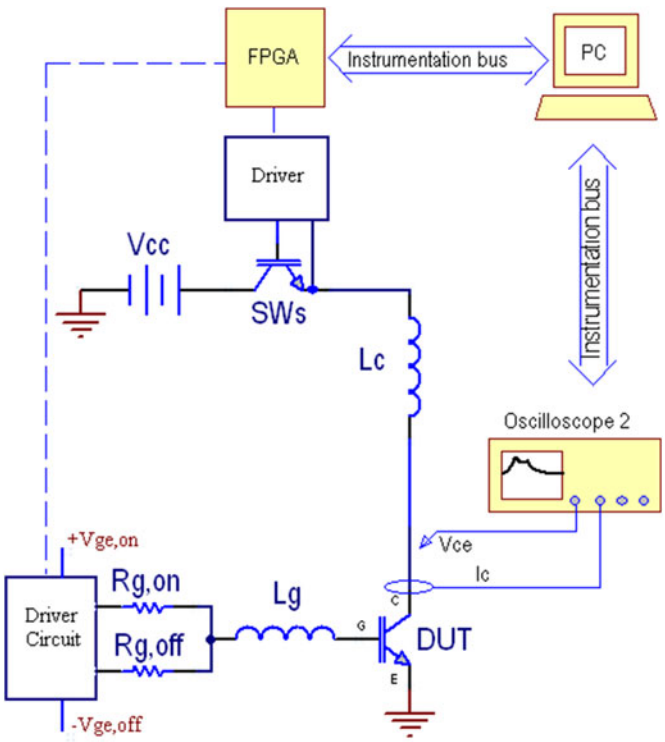

Fig. 12. Schematic of the circuit used for the time-domain short-circuit tests.

To verify the correctness of the results achieved so far, we performed an SC analysis in the time domain by means of the circuit whose schematic is reported in Fig. 12. The main differences between this circuit and the one in Fig. 8 are at the gate side, where a standard IGBT driver replaced the measurement circuit. With this driver, we had the possibility of using two different gate resistors, $R_{g,\rm on}$ and $R_{g,\rm off}$ for the turn-on and the turn-off, respectively. In particular, we used a large value of $R_{g,\rm off} = 200\ \Omega$ to slow down the turn-off of the DUT after the SC thus avoiding dangerous collector overvoltage. Instead, $R_{g,\rm on}$ was changed together with L_g to perform SC tests with or without oscillations and to report them on the stability map of Fig. 11 as instable and stable points, respectively. For permitting normal switching operation, the series switch (SWs) was kept in the on-state for the whole duration of each test.

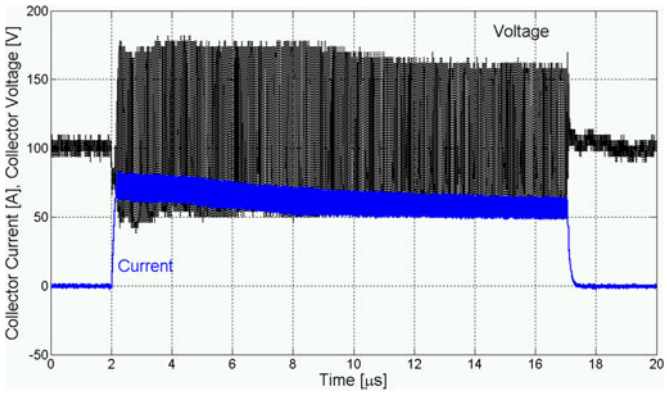

Fig. 13. Collector voltage and current waveforms in the IGBT short-circuit test corresponding to point A in Fig. 11: $V_{\rm CC} = 400$ V, $L_g = 125$ nH, $R_g = 2.5\ \Omega$.

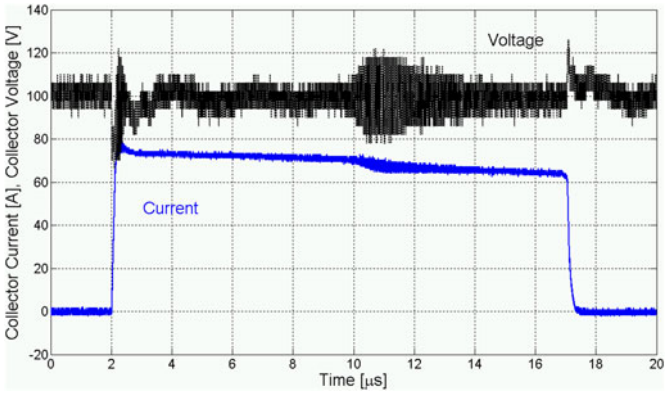

Fig. 14. Collector voltage and current waveforms in the IGBT short-circuit test corresponding to point B in Fig. 11: $V_{\rm ce} = 400$ V, $L_g = 125$ nH, $R_g = 3.3\ \Omega$.

The first analyzed case was at $V_{\rm cc} = 100$ V, $R_g = 2.5\ \Omega$, $L_g = 125$ nH, and $V_{\rm ge} = 12$ V. This corresponds to the instable point indicated with "A" in Fig. 11. The related waveforms supplied in Fig. 13 confirm that the circuit oscillates at about 25 MHz in these test conditions. A second test was executed for $R_g = 3.3\ \Omega$ and $L_g = 125$ nH corresponding to the point "B" in Fig. 11. The related waveforms are shown in Fig. 14, where small-amplitude damped oscillations are evidenced starting at about 10 μs. This indicates that the circuit is at the edge of the instability as expected being the point "B" practically on the boundary between the stability and instability regions of the map.

Other tests were performed at $V_{\rm cc} = 100$ V with several values of R_g and L_g. The points for which the circuit oscillates with $V_{\rm cc} = 100$ V and $L_{\rm C} = 50$ nH are marked with crosses in

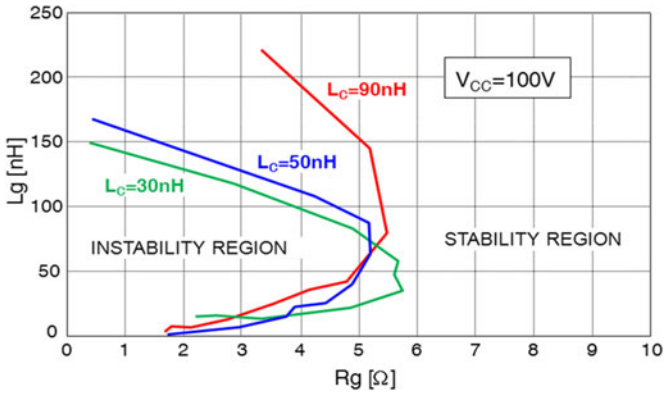

Fig. 15. Stability maps obtained for resistive/inductive gate drivers at $V_{\rm ge} = 12$ V, $V_{\rm cc} = 100$ V and different values of L_c.

Fig. 11, whereas the points corresponding to not oscillating SC tests are marked there with a solid square. Results confirm that the behavior predicted by the stability map, obtained by using the small-signal measurement of the IGBT input impedance, is really observed in the corresponding large-signal time-domain SC experiments.

A wide characterization of the input impedance of the IGBT operated in SC has been executed in several biasing conditions and with different values of L_C. Results indicate that the IGBT under test becomes stable for collector voltage larger than 200 V.

By way of example, the stability maps estimated with the proposed procedure at $V_{\rm cc} = 100$ V for three values of L_C, namely 30, 50, and 90 nH, are depicted in Fig. 15. It shows that the area of the instability region decreases with L_C. Moreover, the maximum values of R_g for which the circuit is instable, namely 5.8, 5.2, and 5.4 Ω for $L_C = 30$, 50, and 90 nH, respectively, are practically independent of L_C. This is an important indication for the application designer who can use a value of R_g larger than 6 Ω for guarantying the SC stability in any test conditions.

VIII. Conclusion

A method for the pulsed measurement of the input impedance of a power device in any biasing condition has been presented. The technique is the extension to the high-frequency range of the voltamperometric method used for measuring impedances at low frequency. A procedure for the extraction of the parasitic elements of the circuits has been also presented. The method has been applied for measuring the input impedance of a 650-V 20-A IGBT in SC. The knowledge of this impedance as a function of the frequency makes it possible to experimentally determine the stability maps of the device, which simplifies the stability assessment of the DUT. Results in the time domain validate the proposed experimental procedure and the stability map predictions. The method is very useful to design appropriate gate drivers able to prevent the IGBT instability in SC.

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