Investigation of Gallium Nitride Devices in High-Frequency LLC Resonant Converters

Weimin Zhang, *Student Member, IEEE*, Fred Wang, *Fellow, IEEE*, Daniel J. Costinett, *Member, IEEE*, Leon M. Tolbert, *Fellow, IEEE*, and Benjamin J. Blalock, *Senior Member, IEEE*

***Abstract*—Newly emerged gallium nitride (GaN) devices feature ultrafast switching speed and low on-state resistance that potentially provide significant improvements for power converters. This paper investigates the benefits of GaN devices in an LLC resonant converter and quantitatively evaluates GaN devices' capabilities to improve converter efficiency. First, the relationship of device and converter design parameters to the device loss is established based on an analytical model of LLC resonant converter operating at the resonance. Due to the low effective output capacitance of GaN devices, the GaN-based design demonstrates about 50% device loss reduction compared with the Si-based design. Second, a new perspective on the extra transformer winding loss due to the asymmetrical primary-side and secondary-side current is proposed. The device and design parameters are tied to the winding loss based on the winding loss model in the finite element analysis (FEA) simulation. Compared with the Si-based design, the winding loss is reduced by 18% in the GaN-based design. Finally, in order to verify the GaN device benefits experimentally, 400- to 12-V, 300-W, 1-MHz GaN-based and Si-based LLC resonant converter prototypes are built and tested. One percent efficiency improvement, which is 24.8% loss reduction, is achieved in the GaN-based converter.**

***Index Terms*—GaN devices, high switching frequency, LLC resonant converter, transformer winding.**

I. Introduction

THE ever-increasing demands in the energy conversion market propel power converters toward high efficiency and high power density. High-performance power semiconductor devices are indispensable to address higher efficiency and density requirements. Newly emerged wide-bandgap (WBG) semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN) devices, provide desirable features of low specific on-state resistance, low junction capacitance, and increased junction temperature. They are promising candidates for the future high-efficiency and high-density power converters [1], [2].

Most recent GaN devices are high electron mobility transistors (HEMT). They are fabricated in a lateral structure with an internal AlGaN–GaN heterojunction that offers high electron mobility and thus low on-state resistance. GaN material has an electrical breakdown field ten times higher than Si, leading to high breakdown voltage capability [3]. The first commercially available enhancement mode GaN FETs (eGaN FETs) had a blocking voltage below 200 V [4]. In addition to low on-state resistance and low junction capacitance, they feature zero reverse recovery charge due to the lateral structure and nonexistent p-n junction [5]. As the blocking voltage of GaN HEMTs increases above 600 V, the cascode structure devices were released to the market [6]. These devices consist of a depletion mode GaN HEMT in series with a low-voltage Si MOSFET, resulting in a rugged gate and stable threshold voltage.

Significant research efforts have been spent on GaN HEMTs and GaN converters in recent years. The static characteristic and switching performance of eGaN FETs and cascode GaN HEMTs were evaluated in [7]–[10], which showed ultrafast switching speed and low switching loss. Hard-switching GaN-based power converter such as synchronous buck converter and boost converter and inverter demonstrated great efficiency improvement over the Si-based counterparts in [11]–[16]. While the GaN HEMTs show significant advantages in hard-switching converters, they also have benefits in soft-switching converters. The eGaN FETs were compared with Si MOSFETs in a dual active-bridge converter in [17]. The combination of the GaN and Si devices achieved the lowest total loss. In [18], eGaN FETs and Si MOSFETs were each applied in 1.2 MHz unregulated isolated resonant converters. The eGaN-based converter improved the efficiency from 95% of the Si-based design to 96%. A 5-MHz soft-switching resonant converter with 89.4% efficiency demonstrated high switching frequency capability of the eGaN FETs in [19].

LLC resonant converter is a typical soft-switching converter, which is widely applied in different applications. The advantages of the LLC resonant converter are that all the devices can achieve zero voltage switching (ZVS) during the entire load range, and the secondary-side synchronous rectification (SR) devices can also achieve zero current switching (ZCS) when the converter operates at or below the resonance [20]–[23]. These benefits make the LLC resonant converter suitable

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W. Zhang was with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996 USA. He is now with Tesla Motors Inc., Palo Alto, CA 94304 USA (e-mail: wzhang29@vols.utk.edu).

F. Wang, D. J. Costinett, and L. M. Tolbert are with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996 USA, and also with the Oak Ridge National Lab, Knoxville, TN 37831 USA (e-mail: fred.wang@utk.edu.; daniel.costinett@utk.edu; tolbert@utk.edu).

B. J. Blalock is with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996 USA (e-mail: bblalock@eecs.utk.edu).

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for high-frequency and high-efficiency applications. An LLC resonant converter design considering the dead time optimization is discussed in [24]. However, there was no analysis on the fundamental relationships between the device parameters and the converter loss, especially the transformer winding loss. The application of cascode GaN HEMTs in an LLC resonant converter was shown in [8], and a system-level consideration of using GaN HEMTs in an LLC resonant converter were qualitatively discussed in [25] and [26]. These papers demonstrated the benefits of GaN HEMTs in LLC resonant converters, but there was no quantified analysis on how the excellent properties of GaN HMETs impact the loss of a high-frequency LLC resonant converter.

This paper establishes an analysis framework to determine the impact of device and converter design parameters on the device and transformer winding loss in an LLC resonant converter operating at the resonance. Using this analysis, the GaN HEMT benefits on reducing the converter loss are quantified. The device loss, which is mainly the conduction loss, is determined by the device on-state resistance and converter rms current. The rms current varies with different magnetizing current and dead-time combinations that need to be properly selected based on the device parameters to guarantee the soft switching. GaN HEMTs, with superior device parameters, are shown to be capable of reducing the device loss.

The transformer loss, especially the winding loss, is another significant loss mechanism in the high-frequency LLC resonant converter. Previous studies have illustrated that the terminal loss, the fringe effect loss, and the intrinsic winding loss are the three dominant contributors to the high-frequency transformer winding loss [27], [28]. In order to reduce the loss, several approaches have been proposed such as discrete secondary-side windings [27], matrix transformer [29], and the hybrid winding structure with Litz wire [30]. However, one particular issue in the LLC transformer winding loss that has not been reported before is the extra winding loss induced by the asymmetrical primary-side and secondary-side current due to the existence of the magnetizing current. The application of the GaN HEMT potentially leads to smaller magnetizing current and reduced asymmetry between both side currents, which is beneficial to the winding loss.

The paper is organized as follows. In Section II, the relationship of device and converter design parameters to the device loss is established. The device loss is compared between GaN HEMTs and Si MOSFETs in a 400- to 12-V, 300-W, 1-MHz LLC resonant converter. In Section III, a new perspective on the extra winding loss due to the asymmetrical primary-side and secondary-side current is proposed. The connection between device parameters and the transformer winding loss is presented. In Section IV, the overall loss breakdown and comparison between the Si-based and GaN-based converters are verified by the prototype experiments. Section V concludes the paper.

II. GaN Device Benefits on Device Loss

The LLC resonant converter operating at the resonance realizes high efficiency at high frequency due to the soft-switching

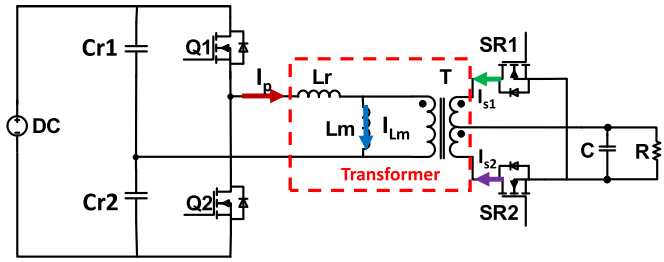


Fig. 1. LLC resonant converter topology.

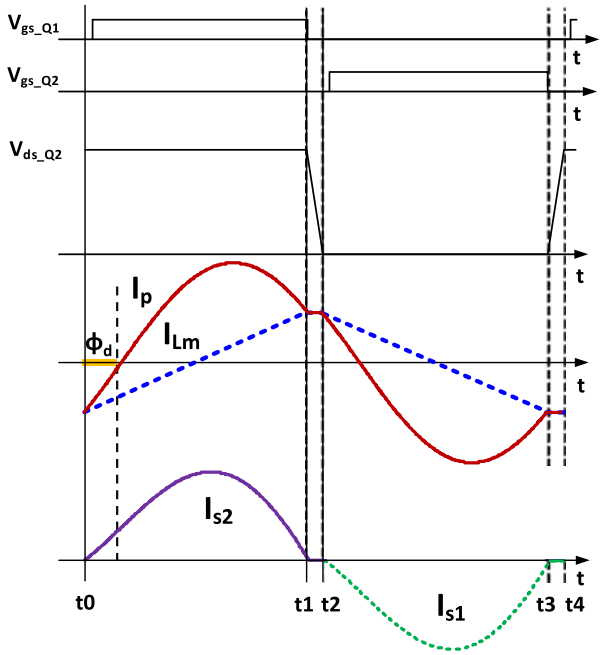


Fig. 2. LLC resonant converter waveforms at the resonance.

of both primary-side and secondary-side devices. Since the voltage gain is close to 1, it is widely applied as a dc–dc transformer (DCX) with voltage ratio determined by the transformer turns ratio. For the high-frequency DCX LLC resonant converter, the primary-side device loss mainly includes conduction loss, driving loss, and turn-off loss, while the secondary side mainly consists of conduction loss and driving loss. Among these loss components, the conduction loss is dominant. This section first establishes the relationships of the device and converter design parameters to the converter rms current in order to evaluate the impact of device parameters on the conduction loss. After that, several GaN and Si device counterparts are compared by using the established relationships. Finally, the specific GaN and Si devices are selected with the minimum loss for both GaN-based and Si-based converter designs. The GaN device loss benefits are quantified.

A. Relationships Between Device Parameters and Loss

The half-bridge LLC resonant converter topology is shown in Fig. 1, and the waveforms at the resonance are shown in Fig. 2. During the dead time (t_1 to t_2), the drain–source voltage of Q_2

drops to zero by the magnetizing current I_{L_m} discharging the device output capacitances. Q_2 then turns on with ZVS.

In order to guarantee ZVS of the devices, sufficient peak magnetizing current and dead time are needed to ensure that all the parasitic capacitances have been discharged, including the output capacitances of the primary-side and secondary-side devices, as well as the transformer winding capacitances. During the dead time (t_1 to t_2), since the magnetizing inductance is large, it can be approximated as a current source. For the primary-side half-bridge topology, the devices ZVS realization can be described by the charge balance equation

$$I_{L_m\_\mathrm{pk}} T_d = 2C_{\mathrm{pri\_oss}} * V_{\mathrm{in}} + C_w * V_{\mathrm{in}} + \frac{1}{N} 2nC_{\mathrm{sec\_oss}} * 2V_o \tag{1}$$

where $I_{L_m\_\mathrm{pk}}$ is the peak magnetizing current, T_d is the dead time, $C_{\mathrm{pri}_{\mathrm{oss}}}$ is the primary-side device charge equivalent output capacitance, $C_{\mathrm{sec}_{\mathrm{oss}}}$ is the secondary-side device charge equivalent output capacitance, C_w is the transformer winding capacitance referring to the primary side, n is the number of secondary-side devices in parallel, N is the transformer turns ratio, V_{in} is the input voltage, and V_o is the output voltage. The transformer turns ratio can be approximately considered as

$$N = \frac{(V_{\mathrm{in}}/2)}{V_o}. \tag{2}$$

According to the LLC topology in Fig. 1, the voltage across the magnetizing inductance is the primary-side voltage of the ideal transformer T, which is equal to NV_o. Considering t_0 to t_1 in Fig. 2, the peak magnetizing current can be expressed as

$$I_{L_m\_\mathrm{pk}} = \frac{NV_o\left((T_s/2) - T_d\right)}{2L_m}. \tag{3}$$

By combining (1), (2), and (3), the magnetizing inductance can be derived in (4). It relates the device output capacitances, the transformer winding capacitance, the dead time, and the switching period

$$L_m = \frac{T_d((T_s/2) - T_d)}{4(2C_{\mathrm{pri\_oss}} + (1/N^2) * 2nC_{\mathrm{sec\_oss}} + C_w)} \tag{4}$$

where L_m is the magnetizing inductance and T_s is the switching time period.

The secondary-side current I_{s1} or I_{s2} in Fig. 2 is equal to the primary-side current I_p minus the magnetizing current I_{L_m}. The average rectified current on the secondary side is the load current. Considering the half switching time period, we have

$$N \cdot \frac{2}{T_s} \int_0^{\frac{T_s}{2} - T_d} (I_p - I_{Lm})dt = \frac{V_o}{R_L} \tag{5}$$

$$I_p = \begin{cases} \sqrt{2} I_{\mathrm{rms\_}P} \sin(\omega_0 t - \Phi_d), & 0 \le t \le \frac{T_s}{2} - T_d \\ I_{L_m\_\mathrm{pk}}, & \frac{T_s}{2} - T_d \le t \le \frac{T_s}{2} \end{cases} \tag{6}$$

$$I_{L_m} = \begin{cases} -I_{L_m\_\mathrm{pk}} + \dfrac{NV_o}{L_m} t, & 0 \le t \le \frac{T_s}{2} - T_d \\ I_{L_m\_\mathrm{pk}}, & \frac{T_s}{2} - T_d \le t \le \frac{T_s}{2} \end{cases}. \tag{7}$$

The primary-side sinusoidal rms current at the resonance can be derived as follows based on the aforementioned equations:

$$I_{\mathrm{rms\_}P} = \sqrt{\frac{V_0^2 T_s^2 \pi^2}{8R_L^2 N^2 (T_s - 2T_d)^2} + \frac{1}{2} I_{L_m\_\mathrm{pk}}^2}. \tag{8}$$

Adding the magnetizing current during the dead time, the total primary-side rms current can be expressed as

$$I_{\mathrm{rms\_}P\_\mathrm{total}} = \sqrt{\frac{V_0^2 T_s^2 \pi^2}{8R_L^2 N^2 (T_s - 2T_d)^2} + \left(\frac{1}{2} + \frac{2T_d}{T_s}\right) I_{L_m\_\mathrm{pk}}^2}. \tag{9}$$

The secondary-side rms current at the resonance can be calculated based on the rms current definition as follows:

$$I_{\mathrm{rms\_}S\_\mathrm{total}} = \sqrt{\frac{1}{T_s} \int_0^{\frac{T_s}{2} - T_d} ((I_p - I_{L_m}) \cdot N)^2 dt}. \tag{10}$$

Solving (10), the secondary-side rms current can be derived as

$$I_{\mathrm{RMS\_}S\_\mathrm{total}} = N\sqrt{\frac{T_s - 2T_d}{2T_s}\left[I_{\mathrm{RMS\_}P}^2 + \left(\frac{1}{3} - \frac{8}{\pi^2}\right) I_{L_m\_\mathrm{pk}}^2\right]}. \tag{11}$$

From (9) and (11), the dead time and the peak magnetizing current impact both primary-side and secondary-side rms current. Under the predetermined converter specifications and switching frequency, one tradeoff in the design of the LLC resonant converter is between the dead time and the peak magnetizing current. As shown in (1), sufficient peak magnetizing current is necessary to achieve device ZVS turn-on during the dead time. However, magnetizing current is the circulating current in the primary-side of converter, which brings additional loss. High peak magnetizing current induces high rms current, leading to high device conduction loss and high transformer winding loss, especially at light-load or no-load condition. Large dead time is not the right choice for the high-frequency LLC resonant converter as well. It results in smaller effective energy transfer

$$I_{\mathrm{rms\_}P\_\mathrm{total}} = \sqrt{\frac{V_0^2 T_s^2 \pi^2}{8R_L^2 N^2 (T_s - 2T_d)^2} + \left(\frac{1}{2} + \frac{2T_d}{T_s}\right)\left(\frac{2C_{\mathrm{pri\_oss}} V_{\mathrm{in}} + C_w V_{\mathrm{in}} + (1/N) 2nC_{\mathrm{sec\_oss}} * 2V_o}{T_d}\right)^2} \tag{12}$$

$$I_{\mathrm{rms\_}S\_\mathrm{total}} = N\sqrt{\frac{T_s - 2T_d}{2T_s}\left[\frac{V_0^2 T_s^2 \pi^2}{8R_L^2 N^2 (T_s - 2T_d)^2} + \left(\frac{5}{6} - \frac{8}{\pi^2}\right)\left(\frac{2C_{\mathrm{pri\_oss}} V_{\mathrm{in}} + C_w V_{\mathrm{in}} + (1/N) 2nC_{\mathrm{sec\_oss}} * 2V_o}{T_d}\right)^2\right]} \tag{13}$$

TABLE I
LLC CONVERTER SPECIFICATIONS

Power rating	300 W
Input voltage	400 VDC
Output voltage	12 VDC
Switching frequency	1 MHz

time from input to load and increases the rms current at full load. Therefore, low peak magnetizing current and small dead time are preferable. That means the overall device capacitance participating in the resonance during the dead time needs to be small. In order to have a quantified relationship directly between the device and rms current, (9) and (11) can be combined with (1), respectively, to obtain (12) and (13), shown at the bottom of the previous page.

where R_L is the load resistance; $I_{\mathrm{rms\_}P\_\mathrm{total}}$ is the primary-side total rms current through L_r, as shown in Fig. 1; $I_{\mathrm{rms\_}P\_\mathrm{total}}$ is the secondary-side total rms current through SR1 (or SR2) shown in Fig. 1. From (12) and (13), the relationship of the device and design parameters to the converter rms current is established. As is expressed that, the primary-side rms current is impacted not only by the primary-side devices but also by the secondary-side devices, which is true for the secondary-side rms current as well.

In the LLC resonant converter, since the conduction loss is dominant in the device total loss due to the soft switching, it is preferable to select devices with low on-state resistance to achieve low conduction loss. However, under the same device structure and blocking voltage, low on-state resistance usually means large die size and high output capacitance. According to (1), (12), and (13), high output capacitance requires high peak magnetizing current and large dead time, which ultimately brings high rms current. Consequently, both the on-state resistance and output capacitance have direct impacts on the device conduction loss. It is different from the hard-switching converter that the on-state resistance and output capacitance compromise between the conduction loss and switching loss. Because of the high figure-of-merit, i.e., demonstrating a lower output capacitance for the similar on-resistance with Si devices, GaN devices have the potential to outperform Si devices in the LLC resonant converter.

B. Device Parameters Impact and GaN Device Benefits in LLC Resonant Converters

Based on the developed relationships, the GaN HEMTs and Si MOSFETs are applied in two LLC resonant converters with the same specifications shown in Table I.

Six-hundred-volt cascode GaN HEMT and Si CoolMOS are selected for the primary-side devices, and 40 V eGaN FET and Si OptiMOS are selected for the secondary-side devices. The device on-state resistances are selected at the same junction temperatures from the datasheet. Since the device output capacitance has a nonlinear characteristic, the charge equivalent capacitance is required be applied in (1). The primary-side charge equivalent output capacitance $C_{\mathrm{pri\_oss}}$ is derived from the total charge divided by 400 V, and the total charge is obtained from the integral of the nonlinear output capacitance curve in the datasheet from 0 to 400 V [31]. The secondary-side charge equivalent output capacitance $C_{\mathrm{sec\_oss}}$ is derived at 24 V using the same approach.

In order to investigate how the device output capacitance impacts device loss, the established relationships in (12) and (13) are utilized. Assuming the selection of secondary-side devices is predetermined, the primary-side and secondary-side rms current versus the dead time based on (12) and (13) are plotted in Fig. 3(a) and (b) with different Si and GaN devices. From Sipri1 to GaNpri2, the charge equivalent output capacitances decrease monotonically while the on-state resistances increase. The minimum rms currents and the corresponding dead times also decrease along with the output capacitances. The conduction loss for the primary-side devices are plotted in Fig. 3(c). Comparing Sipri5 with GaNpri1, which have similar charge equivalent output capacitances, the GaNpri1 demonstrates almost half of the conduction loss of Sipri5. For the devices that have similar on-state resistances, e.g., Sipri4 and GaNpri2, the GaN device still shows lower conduction loss when the dead time is small. As a result, the GaN device conduction loss benefits from the low on-state resistance and low output capacitance. One issue in the analysis using (12) and (13) is that it is not straightforward to determine the optimal dead time since the optimal dead times are different for primary-side and secondary-side rms currents, as shown in Fig. 3(a) and (b). For example, when applying GaNpri2, the converter can achieve minimum primary rms current at 70 ns whereas minimum secondary rms current at 50 ns. Therefore, the optimal dead-time determination requires the consideration of both primary-side and secondary-side devices. The predetermined secondary-side device applied in this analysis is BSC027N04LS. It is selected due to its low on-state resistance without consideration of the output capacitance impact. The combined primary-side and secondary-side device conduction losses are shown in Fig. 3(d). The optimal dead times are close to those in Fig. 3(c). The impact of the dead time is still dominated by the primary-side devices.

In the analysis mentioned earlier, the secondary-side devices are predetermined in order to show the impact of the primary-side devices. In order to achieve the high-efficiency requirement, secondary-side device selection and the number of device in parallel also need to be optimized. The aforementioned analysis utilizes seven different primary-side devices, resulting in seven curves either for the rms current or for the conduction loss. If four different secondary-side devices are considered and the number of devices in parallel is from one to six, there will be more than one hundred cases to study. Therefore, an investigation on how the secondary-side device impacts the converter rms current is necessary to assess if the device selection and loss analysis process can be simplified. In (12) and (13), the equivalent charge $C_{\mathrm{sec\_oss}}2V_o$ is multiplied by the number of devices in parallel n and then divided by the transformer turns ratio N. Since N is large in a 400- to 12-V converter, the impact of secondary-side device output capacitance on rms current is reduced. For example, based on the capacitance versus drain–source voltage curves

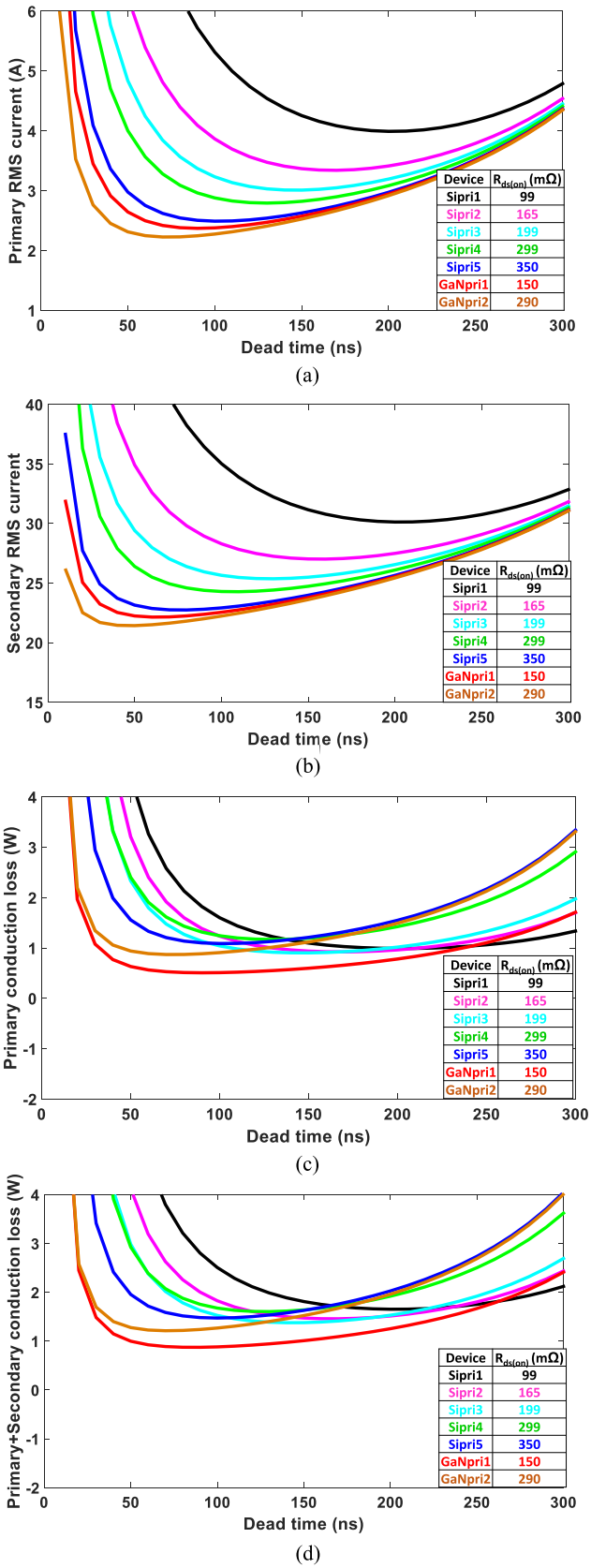


Fig. 3. RMS current and conduction loss versus dead time for different primary-side devices. (a) Primary-side rms current. (b) Secondary-side rms current. (c) Primary-side device conduction loss. (d) Primary-side and secondary-side device conduction loss.

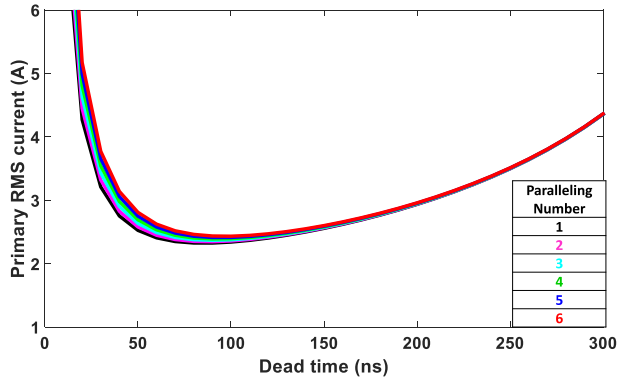
in the datasheet, the equivalent charge of Sipri3 (IPP60R199CP) at 400 V is 131 nC, and for each secondary-side device, it is 44 nC. By having four devices in parallel in each secondary-side leg and considering 16:1 transformer turns ratio, the secondary-side device total equivalent charge referring to the primary side is 22 nC, while the primary-side device total equivalent is 262 nC. Fig. 4(a) and (b) illustrates the variations of the primary-side and secondary-side rms currents along with the number of secondary-side devices in parallel when the primary-side devices are fixed. The current differences are smaller than 0.5 and 2 A, respectively, in each figure. Therefore, due to the high transformer turns ratio, the number of secondary-side devices in parallel has low impact on the converter rms current. Having more secondary side devices in parallel is beneficial to the conduction loss but the main constraint is on the driving loss as shown in Fig. 4(c) and (d). In conclusion, the secondary-side device output capacitances have small impact on the rms current when the transformer turns ratio is high a 400- to 12-V converter. The device selection process can be simplified without considering the impact of the secondary-side devices' output capacitances, while the driving loss is the main constraint.

After the previously presented analysis, it is necessary to quantify the GaN benefits by comparing the specific GaN and Si devices in LLC resonant converters. By applying the analysis, the devices achieving lowest loss are selected, and four devices in parallel are chosen for the secondary side. The device key parameters are shown in Table II and Table III. In the following comparison, device loss, including conduction loss, driving loss, and turn-off loss, will be considered.

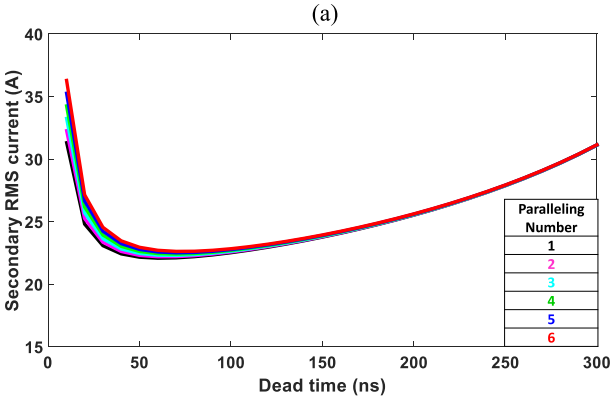
The primary-side and secondary-side rms currents for the selected GaN and Si devices are plotted in Fig. 5. As shown in Fig. 5(a), the minimum primary-side rms current for the Si-based design occurs at 130 ns, while the minimum for the GaN-based design is at 80 ns. Fig. 5(b) shows the secondary-side rms current through each device. For the Si-based design, the minimum rms current is at 130 ns dead time, while the GaN-based design shows 70 ns. Since the rms current in the GaN-based design change between 70 and 80 ns is small in both primary-side and secondary-side devices, 80 ns is selected as the optimal dead time in the GaN-based design.

The device loss breakdowns and comparison are shown in Fig. 6. The primary-side device loss includes conduction loss, turn-off loss, and driving loss. The turn-off loss is derived from the measured turn-off energy of the GaN device in switching test [9] minus the energy stored in the output capacitance from the datasheet. For the secondary-side devices, since the gate driving signal is tuned with the primary-side gate driving signal when the converter operates at the resonance, there is no body diode forward conduction loss and turn-off loss theoretically. The total loss is dominated by conduction loss and driving loss. According to loss breakdown, the GaN device loss demonstrates about 50% reduction compared with the Si devices.

The impact of primary-side devices paralleling will be analyzed as well. Primary-side device paralleling results in the increase of primary-side output capacitance, which has more impact to the rms current than the secondary-side device paralleling.



(a)



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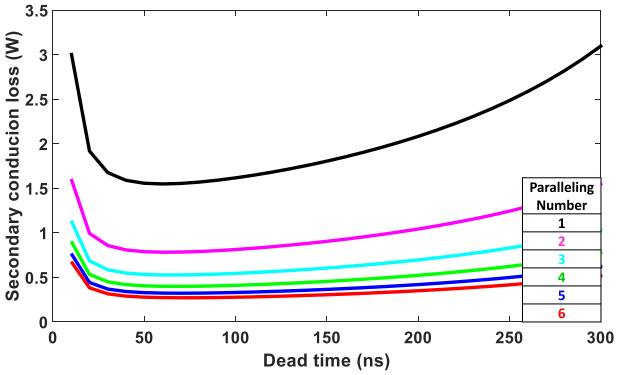

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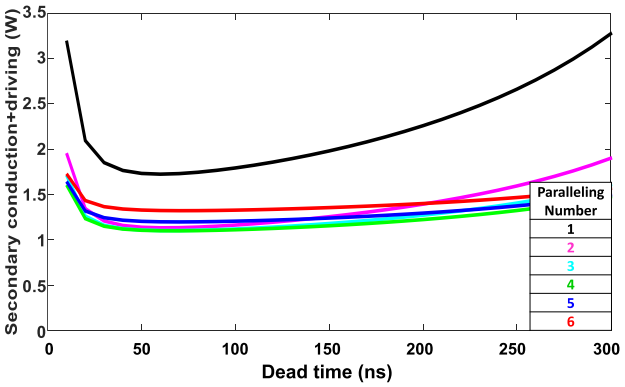
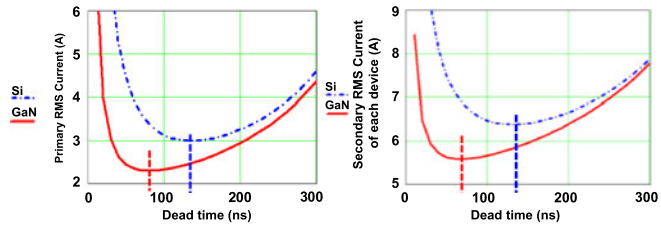


(d)

Fig. 4. RMS current and conduction loss versus dead time for secondary-side devices in parallel. (a) Primary-side rms current. (b) Secondary-side rms current (c) Secondary-side device conduction loss. (d) Secondary-side device conduction loss and driving loss.



(a) (b)

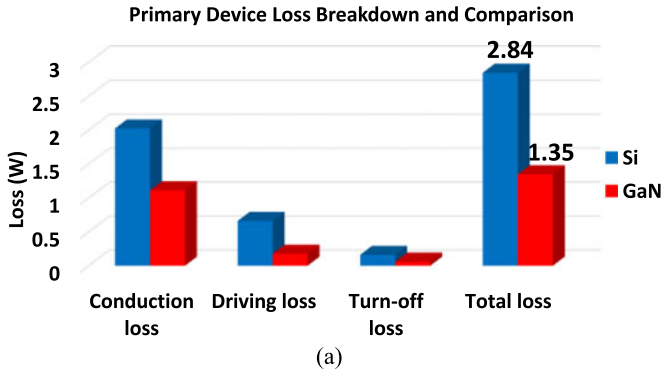
Fig. 5. RMS current comparison. (a) Primary side (b) Secondary side.

TABLE II
PRIMARY-SIDE SI AND GAN DEVICES

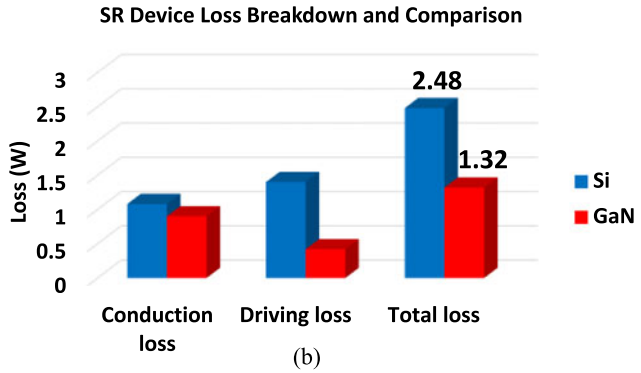
Primary Device	Voltage Rating (V)	$R_{ds(on)}$ (mΩ) @25 °C/50 °C	Charge Equivalent Output Capacitance (pF)	Gate Charge (nC)
IPP60R199CP (Si)	600	180/225 @ 10 V	327 @ 400 V	33 @ 10 V
TPH3006PS (GaN)	600	150/178 @ 8 V	115 @ 400 V	11 @ 8 V

TABLE III
SECONDARY-SIDE SI AND GAN DEVICES

Secondary Device	Voltage Rating (V)	$R_{ds(on)}$ (mΩ) @25 °C/50 °C	Charge Equivalent Output Capacitance (pF)	Gate Charge (nC)
BSC027N04LS (Si)	40	2.9/3.2 @ 5 V	1745 @ 25 V	35 @ 5 V
EPC2015 (GaN)	40	3.2/3.6 @ 5 V	933 @ 25 V	10.5 @ 5 V



(a)



(b)

Fig. 6. Device loss breakdown and comparison. (a) Primary side. (b) Secondary side.

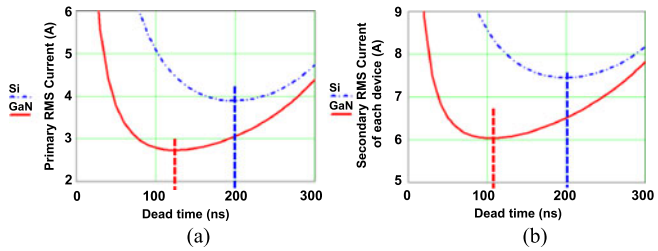


Fig. 7. RMS current comparison with two primary-side devices in parallel. (a) Primary side. (b) Secondary side.

TABLE IV
COMPARISON BETWEEN NONPARALLEL AND PARALLEL CASES

	GaN Pri-RMS/Dead Time	GaN Sec-RMS/Dead Time	Si Pri-RMS/Dead Time	Si Sec-RMS/Dead Time
1 primary, 4 secondary	2.4 A/80 ns	5.6 A/70 ns	3 A/130 ns	6.5 A/130 ns
2 primary, 4 secondary	2.8 A/120 ns	6 A/105 ns	3.9 A/200 ns	7.5 A/200 ns
Current/dead time increment	0.4 A/40 ns	0.4 A/35 ns	0.9 A/70 ns	1 A/70 ns

Fig. 7 illustrates the primary-side and secondary-side rms currents versus the dead time with two primary-side devices in parallel for both GaN and Si designs. The comparison between the parallel and nonparallel cases is shown in Table IV. The results show that the minimum primary rms current of the GaN-based design only increases by 0.4 A, while the Si-based design increases by 0.9 A. The minimum secondary rms current of the GaN-based design increases by 0.4 A as well, while the Si-based design increases by 1 A. Consequently, GaN exhibits a smaller loss increase due to the low output capacitance.

The primary-side and secondary-side loss breakdown and comparison with two primary devices in parallel are shown in Fig. 8. The primary-side device conduction loss reduction of the Si-based design compared with the one in Fig. 6(a) is very small. The reason is that although the equivalent on-state resistance is reduced by half, the rms current increases. For the Si-based design, since the conduction loss reduction is even lower than the increases of driving loss and turn-off loss of the primary-side devices, the total loss with two devices in parallel increases by 0.58 W. For the GaN-based design, the total primary-side devices loss decreases by 0.2 W, which still shows benefits to the Si-based design. However, when more than two GaN devices are paralleled in this example, the total loss increases, as shown in Fig. 9. The reduction of conduction loss is even smaller due to the increase of rms current.

In this section, the relationships of the device and converter design parameters to the converter rms current is established. After that several GaN and Si devices are compared to evaluate the impact of device parameters on device loss. Finally, losses of the selected GaN and Si devices are quantified. The GaN-based design shows about 50% device loss reduction to the Si-based design.

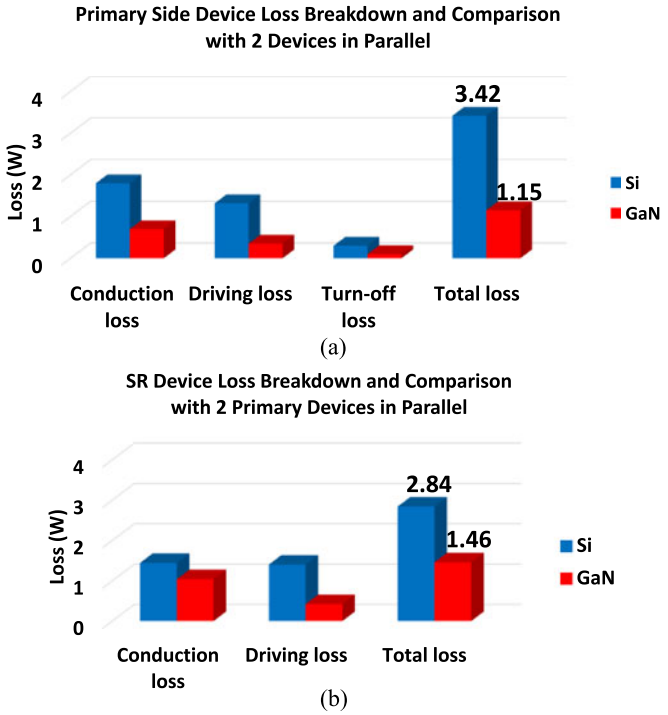


Fig. 8. Device loss breakdown and comparison with two primary-side devices in parallel. (a) Primary side. (b) Secondary side.

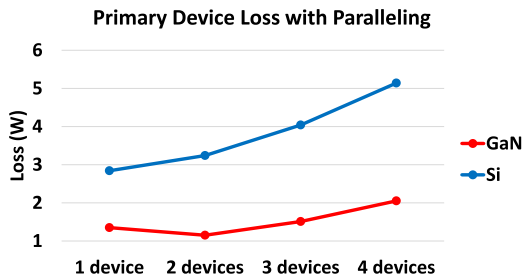


Fig. 9. Primary device loss vs. the number of device in parallel.

III. GaN Device Benefits on Transformer Winding Loss

In the LLC resonant converter, the inductance that builds the current to help ZVS of the devices is usually realized by the transformer magnetizing inductance; therefore, the magnetizing current is part of the transformer primary-side current, and the secondary-side current is equal to the primary-side current minus the magnetizing current. Due to the existence of the magnetizing current, a phase shift exists between the primary-side and secondary-side current. This section first proposes a new perspective on the phase-shift-induced extra winding loss and explains the reason. After that, the transformer winding loss in the GaN-based and Si-based designs are analyzed and compared.

A. Analysis of Phase-Shift-Induced Winding Loss

It is well known that when a transformer winding carries high-frequency current, the eddy current effects become severe,

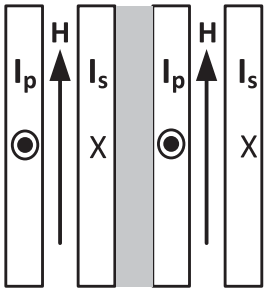


Fig. 10. Interleaving winding structure with H-field cancellation.

leading to unevenly distributed current as well as high winding loss. An interleaved winding structure helps to reduce the winding loss by cancelling the leakage magnetic field (H-field) between the windings where the transformer primary-side and secondary-side currents exist with the same amplitude and in opposite directions. In the LLC resonant converter, the two inductors in the resonant tank are usually integrated in the transformer as shown in Fig. 1. L_r is realized by the transformer leakage inductance; L_m is realized by the transformer magnetizing inductance. As shown in Fig. 2, because of this structure, the transformer primary-side current I_p contains the magnetizing current I_{L_m}. The secondary-side current I_s that delivers the energy to the load is the difference between I_p and I_{L_m}. Due to the existence of I_{L_m}, there is a phase shift Φ_d, which is determined by

$$\Phi_d = \arcsin\left(\frac{-I_{L_m\_\mathrm{pk}}}{\sqrt{2}I_{\mathrm{rms}\_P}}\right) = \arcsin\left(\frac{-Q/T_d}{\sqrt{2}I_{\mathrm{rms}\_P}}\right) \quad (14)$$

where I_{rms_P} is the primary-side rms current, $I_{L_m\_\mathrm{pk}}$ is the peak magnetizing current, Q is the total charge during the soft-switching transient, and T_d is the dead time.

The transformer winding loss is influenced by the H-field distribution between the windings. The mutually cancelled H-field is easily obtained by primary-side and secondary-side winding interleaving. For example, according to the Ampere's law, the H-field in the shaded area in the interleaving winding structure shown in Fig. 10 can be mostly cancelled, if I_p and I_s exist with the same amplitude and in opposite directions. However, in the LLC transformer, I_p and I_s are asymmetrical with the existence of Φ_d. It is difficult to achieve the cancelled H-field between the two windings.

Ansys Maxwell 2-D simulation is applied to investigate the impact of Φ_d on the winding loss. Among all the simulation solvers, the eddy current solver is not suitable for this simulation, because it only works for a sinusoidal current excitation. If there is no center tap for the transformer, the primary-side and secondary-side currents are symmetrical sinusoidal waveforms and the eddy current solver can be applied. Since the LLC transformer is a center-tapped structure, the secondary side takes a half-wave current. Besides, there is also phase shift between the primary-side and secondary-side currents. Therefore, the magnetic transient solver is suitable for this simulation.

A 16:1 transformer winding is modeled in the Maxwell 2-D simulation in Fig. 11. There are 16 turns in series as the

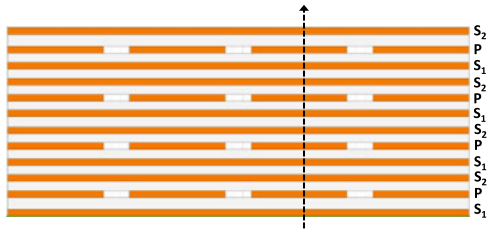


Fig. 11. 2-D transformer winding structure in simulation.

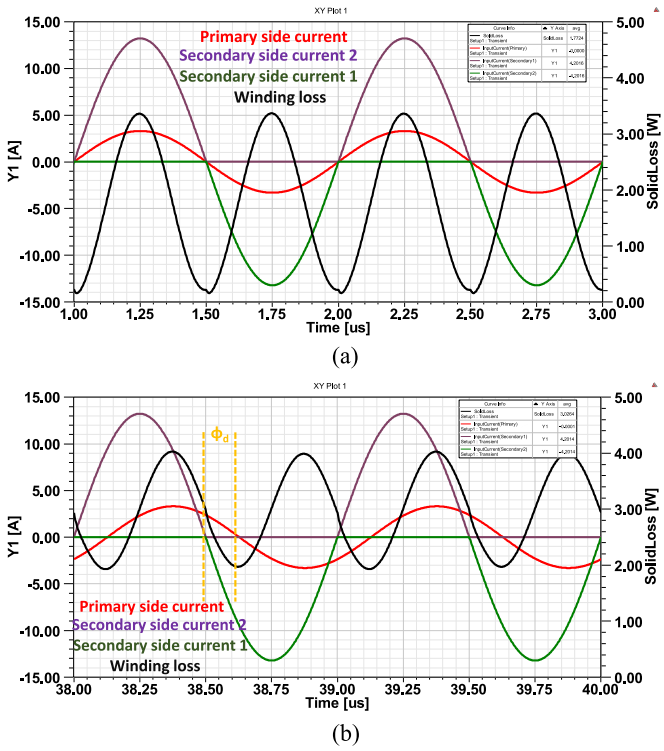


Fig. 12. FEA simulation results at (a) $\Phi_d = 0$ and (b) $\Phi_d = 0.7$.

primary-side winding, and 4 turns in parallel as the secondary-side winding. The geometry model is axisymmetric about Z-axis (or RZ plane). Each PCB winding is 70 μm thick (2 oz copper). The width of the primary-side winding is 1 mm, and the secondary winding is 5 mm. The space between the PCB windings is 0.127 mm. The primary-side excitation is the sinusoidal current excitation that emulates the primary-side resonant current. The secondary-side excitation is half-wave current excitation with 50% duty cycle to emulate the secondary-side current.

In order to have a straightforward understanding on Φ_d impact, the amplitude of the sinusoidal current excitation is assumed to be constant in different phase shift cases. By using the optimal rms current value of the GaN-based design derived from Section II, Φ_d impact on the transformer winding loss is simulated. The simulation results are shown in Fig. 12. As can be seen in Fig. 12(a), the winding loss changes sinusoidally in accordance with the primary-side and secondary-side currents. It reaches the minimum point when the primary-side and secondary-side currents reach zero. In Fig. 12(b), the winding

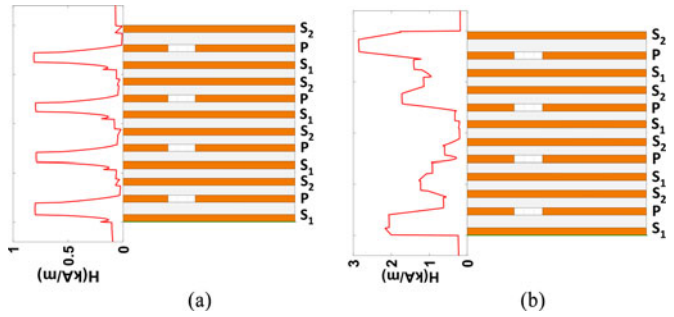


Fig. 13. *H*-field distributions at (a) $\Phi_d = 0$ and (b) $\Phi_d = 0.7$.

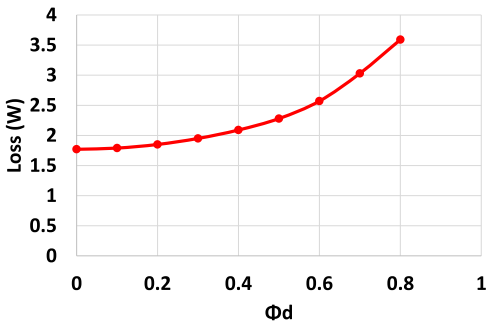


Fig. 14. Winding loss versus Φ_d.

loss exhibits a sinusoidal-shaped waveform as well. The minimum loss happens when the primary-side current reaches zero but still shows about 2 W. In order to have a closer inspection, the *H*-field distributions along with the dashed line in Fig. 11 are plotted in Fig. 13. The current excitation is on *P* winding and S1 winding. The *H*-field in Fig. 13(a) is evenly distributed, and it cancels at each adjacent area of S2. However, in Fig. 13(b), the *H*-field is intensified not only in *P* and S1 windings but also in S2 winding. Therefore, higher current density is induced. According to the simulation results, $\Phi_d = 0$ case shows 1.77 W average winding loss, while $\Phi_d = 0.7$ case shows 3.03 W average winding loss.

The winding loss is simulated from $\Phi_d = 0$ to $\Phi_d = 0.8$. Fig. 14 shows the simulation results of the winding loss versus Φ_d. The winding loss increases when Φ_d is becomes large. The simulation results can be utilized to analyze the impact of GaN devices on transformer winding loss.

B. Transformer Winding Loss in GaN and Si Designs

As shown in Fig. 5, the GaN-based and Si-based designs have the optimal dead time T_d and the primary-side rms current $I_{\mathrm{rms\_}P}$, respectively. If the dead time changes in a small range around the optimal point, the variation of the rms current is small. Fig. 15 plots the transformer primary-side and secondary-side rms currents versus the dead time around the optimal points for both GaN-based and Si-based designs. The rms currents remain almost constant. On the other hand, based on (14), Φ_d is derived by the total device charge Q during the soft-switching transient, the dead time T_d, and the primary-side

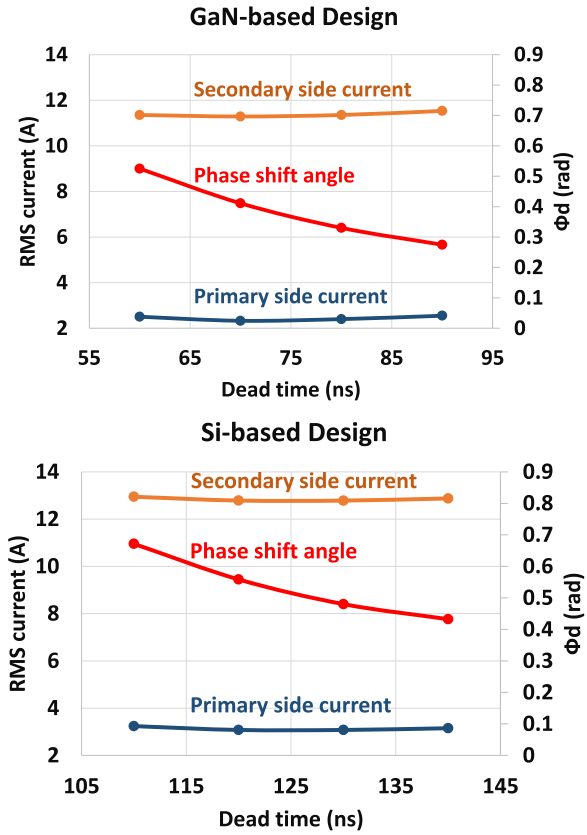


Fig. 15. Winding current and phase shift versus dead time.

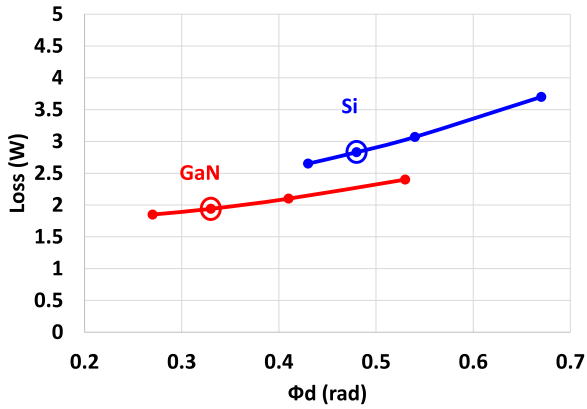


Fig. 16. Winding loss versus Φ_d in the valid range.

rms current $I_{\mathrm{rms\_}P}$. Due to the variation of the dead time, Φ_d changes significantly, shown in Fig. 15. Since the winding loss simulation in finite element analysis (FEA) assumes that the amplitude of sinusoidal current excitation is constant, the simulation results within the Φ_d range in Fig. 15 are considered valid for the GaN-based design. Similarly, the Si-based design also has the valid winding loss results in the Φ_d range. Fig. 16 plots the winding loss versus Φ_d in the valid range. Comparing the two designs, the Si-based design has not only higher primary-side and secondary-side currents but also higher phase shift Φ_d; therefore, the winding loss is higher. For the optimal dead times

presented in Fig. 5, which are 130 ns for the Si-based design and 80 ns for the GaN-based design, the analytical transformer winding loss is about 0.8 W lower in the GaN-based design, shown in Fig. 16.

The aforementioned discussion is based on the preselected devices. However, a more general device selection approach needs to consider the impact of the transformer winding loss and Φ_d as well. A direct relation of Φ_d to the dead time and the device parameters can be established by substituting (1) and (8) into (14), which is expressed as (15), shown at the bottom of the page.

The transformer winding loss versus Φ_d can be derived from the FEA simulation for a certain rms current. The analytical expression between the winding loss and Φ_d can be derived by the curve-fitting method. As an example, Fig. 14 plots the simulated transformer winding loss at the primary-side rms current of 2.4 A. The analytical expression can be obtained as

$$P_{\text{winding}} = 2.593\emptyset_d^4 - 0.387\Phi_d^3 + 1.309\Phi_d^2 + 0.159\Phi_d + 1.767. \tag{16}$$

By substituting (15) into (16), the transformer winding loss is directly connected to the device parameters and the dead time. It is easy to understand that when the dead time is large, the required peak magnetizing current is low, and Φ_d approaches zero. The winding loss also approaches its minimum value. Φ_d behaves as an intermediate variable. It has a direct relation with the winding loss, which is proved by the FEA simulation. Meanwhile, Φ_d is also related to the converter rms current and peak magnetizing current and further to the device parameters and the dead time. As a result, the winding loss can be directly connected to the device parameters and the dead time in the LLC resonant converter, which can be utilized in the device selection process.

IV. Analytical Loss Breakdown and Experimental Verification

Based on the analysis of the GaN device impact on device loss and transformer winding loss, the overall analytical loss breakdown and comparison between the Si-based and GaN-based converters are shown in Fig. 17. Both the primary-side and secondary-side device loss reductions are close to 50%; the transformer loss reduction is 18%; and the capacitor ESR loss reduction is 30%, which is due to the reduced rms current. It should be noted that the transformer loss in Fig. 17 includes the core loss, the fringe effect loss, and the winding loss plotted in Fig 16. The total analytical loss reduction is about 32%.

Both Si-based and GaN-based 400- to 12-V, 300-W, 1-MHz LLC resonant converter prototypes were built, shown in Fig. 18. A 16:1 turns ratio ER23/5/13 N49 ferrite planar transformer was constructed. The PCB winding was designed as the 2-D model in Fig. 11. The control signals were provided by an

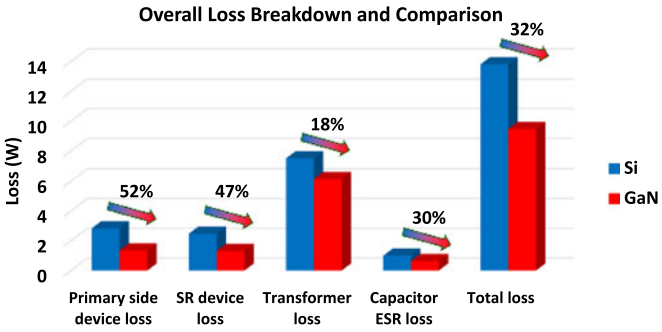


Fig. 17. Overall loss breakdown and comparison.

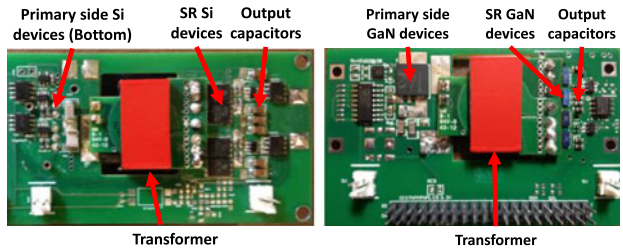


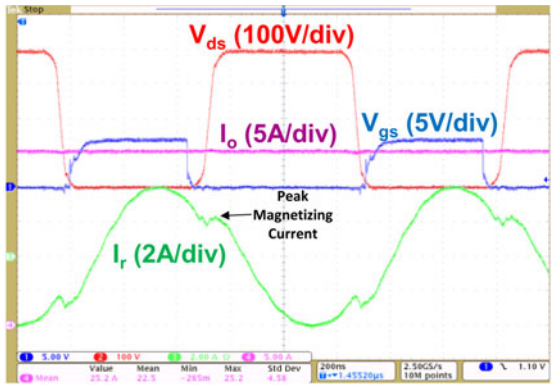
Fig. 18. LLC resonant converter prototypes. (a) Si-based prototype. (b) GaN-based prototype.

FPGA-based digital controller. The dead time was set as 130 ns for the Si-based converter and 80 ns for the GaN-based converter.

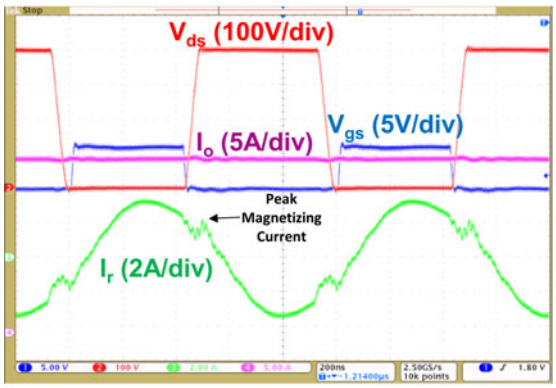
The waveforms of the two converters at full load are shown in Fig. 19 with the peak magnetizing current marked. The GaN-based converter demonstrates shorter drain–source voltage falling time. The peak magnetizing current of the GaN-based converter is also lower than that of the Si-based converter. The measured primary-side rms current is 2.99 A for the Si-based design and 2.35 A for the GaN-based design. The average value of the output current in the Si-based converter is 25.2 A, and for the GaN-based converter, it is 25.3 A. It should be noted that since the layout for the power loops and the values of the passive components are not exactly the same in both prototypes, the resonances are not the same. As the switching frequency needs to track the resonant frequency, the switching frequency was 930 kHz for the Si-based design and 1 MHz for the GaN-based design. By changing the switching period T_s from 1000 to 1075 ns in (9) for the Si-based design, the minimum rms current reduces from 3.01 to 2.94 A. The impact of the rms current and conduction loss is small.

In order to verify the device analytical loss, thermal test was implemented on the GaN-based converter prototype. The device loss versus temperature needs to be established as a reference. First, 8 V dc voltages were applied between the gate and source terminals on both top and bottom cascode GaN devices in Fig. 18(b). After that, by providing the dc current from Agilent E3631A power supply to the device and

$$\Phi_d = \arcsin\left(\frac{-(2C_{\text{pri\_oss}}V_{\text{in}} + C_w * V_{\text{in}} + (1/N)2nC_{\text{sec\_oss}} * 2V_o)/T_d}{\sqrt{(V_0^2 T_S^2 \pi^2/8R_L^2 N^2 (T_s - 2T_d)^2) + (1/2)\cdot((2C_{\text{pri\_oss}}V_{\text{in}} + C_w V_{\text{in}} + (1/N)2nC_{\text{sec\_oss}} * 2V_o)/T_d)^2}}\right) \tag{15}$$

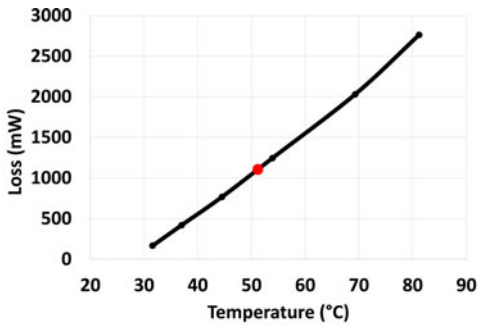


(a)



(b)

Fig. 19. LLC resonant converter waveforms. (a) Si-based LLC resonant converter waveforms. (b) GaN-based LLC resonant converter waveforms.



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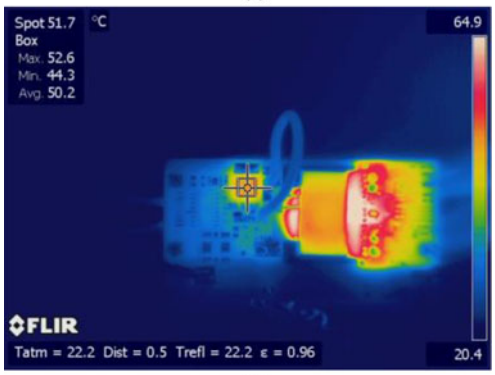

(b)

Fig. 20. Primary-side GaN device thermal test. (a) Device loss versus temperature. (b) Primary-side GaN device thermal image.

TABLE V
COMPARISON BETWEEN ANALYTICAL AND MEASURED DEVICE LOSSES

	Measured Loss (W)	Analytical Loss (W)	Error Percentage Based on Measured Loss
Si primary	1.51	1.42	6%
Si secondary	0.35	0.31	11%
Si total	14.5	13.82	5%
GaN primary	1.14	0.675 (1.075)	41% (6%)
GaN secondary	0.18	0.165	8%
GaN total	10.9	9.46 (10.26)	13% (6%)

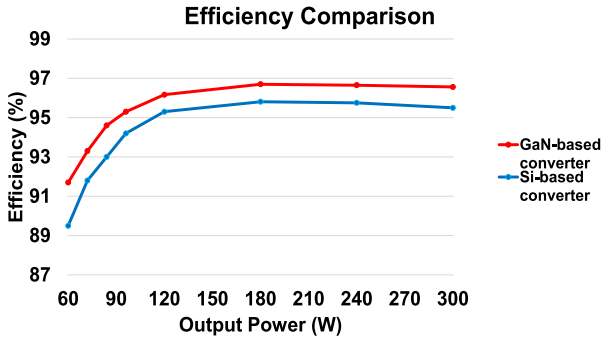

Fig. 21. Efficiencies of Si-based and GaN-based converters.

measuring the drain–source voltage with Agilent 34410A 6 ½ digits high-precision digital multimeter, the device conduction loss was obtained. Meanwhile, the device surface temperature was measured by FLIR SC620 thermal imaging camera. As a result, the primary-side GaN device loss versus temperature was derived in Fig. 20(a). Applying the measured device temperature under the same cooling condition when the converter ran at full load in Fig. 20(b) to the reference, the device loss can be obtained. The losses of the secondary-side devices were obtained by the same approach. Table V compares the measured loss and the analytical loss. One particular issue is that error percentage of the primary-side GaN device is high. Further investigation shows that the cascode GaN device has turn-on loss during the soft-switching transient [32]. By including this additional loss in our analytical model, the error percentage drops to 6%, which is acceptable. The test results verified the analytical results.

Fig. 21 shows the efficiencies of Si-based and GaN-based converters under different load conditions. The GaN-based converter demonstrates 96.8% peak efficiency and 96.6% full-load efficiency, which is about 1% higher than the Si-based converter. The equivalent total loss reduction is 24.8%.

IV. CONCLUSION

In order to understand the GaN device benefits in an LLC resonant converter, this paper first established the relationship of device and design parameters to the device loss and then quantified the loss reduction by comparing GaN-based and Si-based designs. Due to the low effective output capacitance of GaN devices, the GaN-based design demonstrated about 50% device loss reduction. Next, a new perspective on the extra winding loss due to the asymmetrical primary-side and secondary-side currents was presented. The device and design parameters were

tied to the winding loss based on the winding loss results in FEA simulation. The winding loss was reduced by 18% in the GaN-based design. Finally, the overall analytical loss breakdown was summarized, illustrating 32% total loss reduction of the GaN-based LLC resonant converter. Both GaN-based and Si-based converter prototypes were built and tested. A thermal test was applied to verify the analytical device loss. 1% efficiency improvement and 24.8% loss reduction was achieved in the 400- to 12-V, 300-W, GaN-based converter operating at 1 MHz switching frequency.

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Weimin Zhang (S'10) received the B.S. degree from Hefei University of Technology, Hefei, China, in 2007, and the M.S. degree from Xi'an Jiaotong University, Xi'an, China, in 2010, both in electrical engineering, and the Ph.D. degree from the Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT), The University of Tennessee, Knoxville, TN, USA, in Fall 2015.

He is currently a Senior Electronic Design Engineer in Tesla Motors Inc., Palo Alto, CA, USA. His current research interests include wide bandgap power semiconductor devices, dc–dc converters for electric vehicles, and grid-tie dc–ac inverters.

Fred Wang (S'85–M'91–SM'99–F'10) received the Ph.D. degree in electrical engineering from the University of Southern California (USC), Los Angeles, CA, USA.

He was a Research Scientist with the USC Electric Power Lab from 1990 to 1992. He joined the GE Power Systems Engineering Department, Schenectady, NY, USA, as an Application Engineer, in 1992. From 1994 to 2000, he was a Senior Design Engineer with GE Industrial Systems, Salem, VA, USA. During 2000 to 2001, he was the Manager of the Electrical Systems Technologies Lab, GE Global Research Center, Niskayuna, NY, and Shanghai, China. From 2001 to 2009, he was an Associate Professor with the Center for Power Electronics Systems, Virginia Tech. Since 2009, he has been with the University of Tennessee (UTK), Knoxville, TN, USA, and Oak Ridge National Lab, Knoxville, as a Professor and the Condra Chair of Excellence in Power Electronics. He is a Founding Member and the Technical Director of the National Science Foundation/Department of Energy (NSF/DOE) Engineering Research Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT) at UTK.

Daniel J. Costinett (S'10–M'13) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Colorado, Boulder, CO, USA, concluding in 2013.

In 2012, he assisted with Research and Course Development as an Instructor at Utah State University. He is currently an Assistant Professor in the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN, USA. He is the Co-Director of the Education and Diversity for the National Science Foundation/Department of Energy Research Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT). He is also a Joint Faculty with the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory, Knoxville. His current research interests include resonant and soft-switching power converter design, high-efficiency power supplies, mixed-signal integrated circuit design, medical devices, and electric vehicles.

Dr. Costinett is currently an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS.

Leon M. Tolbert (S'88–M'91–SM'98–F'13) received the Bachelor.s, M.S., and Ph.D. degrees in electrical engineering from Georgia Tech, Atlanta, GA, USA, in 1989, 1991, and 1999, respectively.

He joined Oak Ridge National Laboratory (ORNL) in 1991 and worked on several electrical distribution projects at the three U.S. Department of Energy plants in Oak Ridge, TN, USA, from 1991 to 1999. He joined the University of Tennessee, Knoxville, TN, in 1999 and is currently the Min H. Kao Professor and the Head of the Department of Electrical Engineering and Computer Science. He is a Founding Member and the Thrust Leader of CURENT, the NSF/DOE Engineering Research Center established at UT in 2011 to examine the structure and control of future electric grids. He is also a part time Senior Research Engineer at ORNL and conducts joint research in the Power Electronics and Electric Machinery Research Center. His research areas include electric power conversion for renewable energy sources, multilevel converters, utility application of power electronics, microgrids, electric vehicles, and application of wide bandgap (SiC and GaN) power electronics.

Dr. Tolbert is a registered Professional Engineer in the state of Tennessee. He was elected as a Member-At-Large to the IEEE Power Electronics Society Advisory Committee for 2010–2012, and has served as the Chair of the PELS Membership Committee and Education Committee. He was an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2007 to 2012. He has been the Transactions Review Chair for the IEEE TRANSACTIONS ON INDUSTRY APPLICATION for the Industrial Power Converter Committee since 2014. He is the co-author of five IEEE papers that have won prize paper awards.

Benjamin J. Blalock (SM'06) received the B.S. degree in electrical engineering from the University of Tennessee, Knoxville, TN, USA, in 1991, and the M.S. and Ph.D. degrees from the Georgia Institute of Technology, Atlanta, GA, USA, in 1993 and 1996, respectively, both in electrical engineering.

He was an Analog IC Design Consultant for Cypress Semiconductor, Concorde Microsystems, and Global Power Electronics. He is currently a Professor in the Department of Electrical Engineering and Computer Science, University of Tennessee, where he directs the Integrated Circuits and Systems Laboratory. His current research interests include UT includes analog/mixed-signal integrated circuit design for extreme environments (both wide temperature and radiation) across multiple semiconductor technologies, high-temperature/high-voltage gate drive circuits for silicon carbide power electronics, multichannel monolithic instrumentation systems, and mixed-signal/mixed-voltage circuit design for systems-on-a-chip.