Fifth- and Seventh-Order Harmonic Elimination With Multilevel Dodecagonal Voltage Space Vector Structure for IM Drive Using a Single DC Source for the Full Speed Range

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***Abstract*—This paper presents a method for generating a multilevel dodecagonal voltage space vector structure using a single dc source for induction motor drives. Multilevel dodecagonal structure combines the advantages of both multilevel and dodecagonal structures, and hence, generates low d*v*/d*t* phase voltage along with the elimination of fifth- and seventh-order harmonics over the entire modulation range. This eliminates low-order harmonic currents and prevents the generation of sixth-order torque ripple in the motor. The topology used requires only one dc source making four-quadrant operation of the drive system simpler compared to previously proposed multilevel topologies generating dodecagonal space vector structures. The topology used consists of a three-level flying capacitor (FC) inverter cascaded with a capacitor fed H-bridge. The FC inverter operates at a lower switching frequency and the low-order harmonics are eliminated by the switching action of the cascaded H-bridge inverter. The capacitors in the cascaded H-bridge modules are maintained at a substantially smaller voltage compared to the dc-link voltage and are inherently balanced during the pulsewidth modulation operation. This results in low switching loss, in the FC inverter as well as in the cascaded H-bridge inverter. Experimental results are included to validate the operation of the topology and modulation scheme presented in this paper.**

***Index Terms*—Dodecagonal voltage space vector, harmonic elimination, induction motor drive, low order, multilevel, single dc link.**

I. Introduction

HIGH-POWER high-performance variable speed induction motor (IM) drive systems require inverters generating voltage waveforms of low total harmonic distortion (THD) while operating at low switching frequency. Low switching frequency operation reduces the device switching losses and also brings down the device d*v*/d*t* requirement. This results in improved inverter efficiency and lesser electromagnetic interference (EMI) generation from the inverter. Low THD output voltage waveform from the inverter reduces the magnitude of harmonic currents, and hence, reduces the losses in the machine and alleviates the low-order harmonic torque ripple generation [1]. Operating an inverter at low switching frequency generally results in low-order harmonic current generation unless some filtering techniques and or special pulse width modulation (PWM) techniques are used.

Many methods to eliminate or suppress the harmonics are present, which includes passive filters, active methods [2]–[4], and selective harmonic elimination PWM (SHE-PWM) techniques. Passive filtering techniques [5], [6] are not suitable for low-order harmonic suppression because the size of the inductors used becomes large. SHE-PWM [7], [8] techniques have limited linear modulation range and require extensive offline computations. Active harmonic cancellation techniques using series compensators realized using H-bridge cells is mentioned in [9] and [10]. Multilevel inverters [11]–[14] provide low d*v*/d*t* output compared to conventional two-level inverters but at the expense of more number of switching devices. But, conventional multilevel inverters generate space vector structures with hexagonal boundary, and hence, the phase voltages contains $5\text{th}, 7\text{th}, 11\text{th}, 13\text{th}..$ order harmonics when the inverter is operated in the overmodulation range. Inverter topologies generating dodecagonal (12-sided) space vector structures [15][16] eliminate fifth- and seventh-order harmonics, represented as $(6\text{n} \pm 1)\text{th}, \text{n} = \text{odd order harmonics}$, from output voltage over the entire modulation range. At the same time, the linear modulation range also increases compared to a hexagonal space vector structure.

The topologies mentioned previously generates multilevel dodecagonal space vector structure but require two or more energy sources delivering active power. The requirement of more than one dc source makes four-quadrant operation difficult since more than one active front end converters are required. A topology for generating a two-level dodecagonal structure using single dc source is proposed in [17]. In this paper, a method for generating a multilevel dodecagonal voltage space vector structure using a single dc source for a star-connected IM drive is presented.

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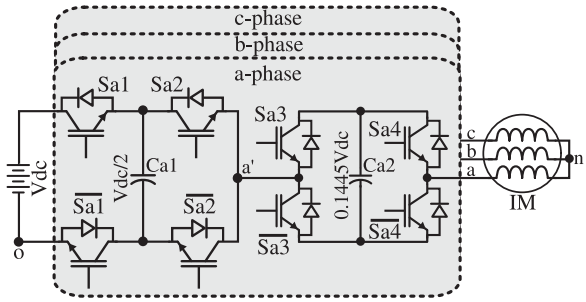

Fig. 1. Inverter circuit topology used (for *a*-phase).

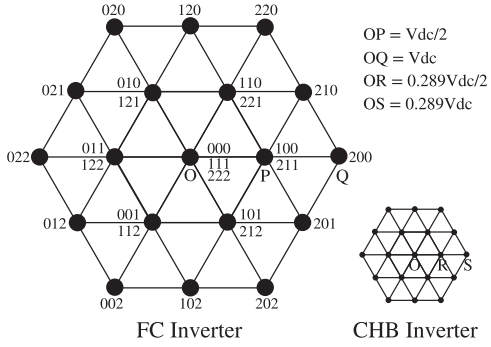

Fig. 2. Space vector diagram for the FC inverter and CHB inverter.

II. Inverter Topology

The inverter circuit used is shown in Fig. 1 (for *a*-phase). The topology consists of two three-level inverter modules cascaded together. The first three-level inverter is realized using a flying capacitor (FC) topology. It is also possible to use other three-level inverter topologies like NPC or ANPC [18] instead of FC topology. The second three-level inverter is realized using a floating capacitor fed cascaded H-Bridge topology (CHB).

For a dc-link voltage of $\mathrm{V_{dc}}$, the FCs Ca1, Cb1, and Cc1 in the FC inverter modules are maintained at $0.5\,\mathrm{V_{dc}}$ and the floating capacitors Ca2, Cb2, and Cc2 in the CHB inverter modules are maintained at $0.1445\,\mathrm{V_{dc}}$. Switches are named as Sxy, where $x = a, b, c$ indicates phase and $y = 1, 2, 3, 4$ indicates switch number for each phase. Complementary switch to Sxy is represented as $\overline{\mathrm{Sxy}}$, i.e, Sxy is ON implies $\overline{\mathrm{Sxy}}$ is OFF. Switches in the FC modules have to be rated for a minimum blocking voltage of $0.5\,\mathrm{V_{dc}}$ and the switches in CHB modules have to be rated for a minimum blocking voltage of $0.1445\,\mathrm{V_{dc}}$. Capacitors are named as Cxy, where $x = a, b, c$ indicates phase and $y = 1, 2$ indicates capacitor number for each phase. In total, there are 24 switching devices and 6 capacitors. Since the FC and CHB inverters are cascaded, the inverter pole voltage is

$$V_{xo} = V_{x'o} + V_{xx'}; x = a, b, c. \tag{1}$$

III. Space Vector Structure

The multilevel dodecagonal space vector structure is obtained by superposing the space vector structures obtained from the two three-level inverters (FC and CHB). Space vector structures for the three-level inverters are shown in Fig. 2.

The space vector structures are identical for both FC and CHB inverters in the topology used, except for the lengths of the vectors. For the FC inverter, the vector lengths are $\mathrm{OP} = \mathrm{V_{dc}}/2$ and $\mathrm{OQ} = \mathrm{V_{dc}}$, whereas for the CHB inverter, the vector lengths are $\mathrm{OR} = 0.1445\,\mathrm{V_{dc}}$ and $\mathrm{OS} = 0.289\,\mathrm{V_{dc}}$. The vector names in Fig. 2 represent the switching states applied to the inverter. For example, vector 210 represents switching state 2 applied to *a*-phase, state 1 applied to *b*-phase, and state 0 applied to *c*-phase. Switching states and corresponding pole voltages generated for the FC and CHB inverters are given in Table I. In Table I, $x = a, b, c$ indicates phase.

Since the FC inverter and CHB inverter are cascaded (see Fig. 1), on each space vector location of the FC inverter, the space vector structure generated by the CHB inverter can be superimposed. Space vector structure generated from the inverter topology is shown in Fig. 3.

TABLE I
Switching States and Pole Voltages

FC Inverter		CHB Inverter	
Switching State	Pole Voltage ($V_{x'o}$)	Switching State	Pole Voltage ($V_{xx'}$)
2	$\mathrm{V_{dc}}$	2	$+0.1445\,\mathrm{V_{dc}}$
1	$\mathrm{V_{dc}}/2$	1	0
0	0	0	$-0.1445\,\mathrm{V_{dc}}$

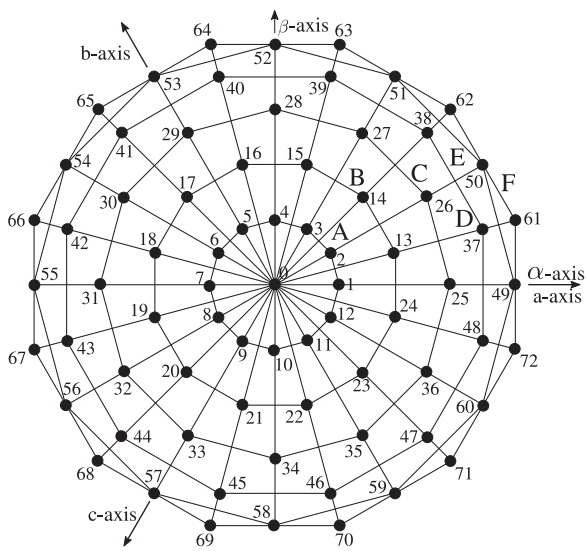

Fig. 3. Space vector diagram generated.

Vectors on the multilevel dodecagonal space vector structure are generated using a vector applied from the FC inverter and a switched averaged vector (pseudovector) generated from the CHB inverter. There are six concentric dodecagons on the space vector structure, resulting in a multilevel structure. Vectors forming the dodecagons are named from 0 to 72. The dodecagons are named from A to F. There are two types of dodecagons, Type1 and Type2, in the space vector structure. In Type1 dodecagons (B, D, and F), the sides are perpendicular to $\alpha\beta$-axis. Type2 dodecagons (A, C, and E) are 15^{o} shifted with respect

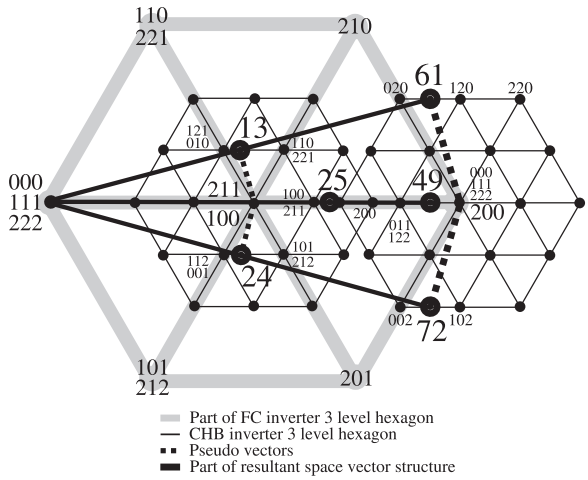

Fig. 4. Generation of vectors 13, 24, 25, and 61.

to Type1 dodecagons. For a given dc-link voltage of V_{dc}, the radius (length of the outermost vectors) of the space vector structure is $0.966\,V_{dc}$. The linear modulation range possible with the aforementioned radius is 48.82 Hz.

IV. Pseudo Vector Generation

Vectors forming the space vector structure (see Fig. 3) are generated from the superposition of the vectors from FC and CHB inverters. The CHB inverter generates a pseudovector by switched averaging of two vectors. Example for generation of vectors $13, 24, 25, 49, 61$, and 72 are given in Fig. 4.

Vector 13 is generated by applying vector 100 (or 211) from an FC inverter and by applying a pseudovector (dotted lines in Fig. 4) from the CHB inverter. The pseudovector is generated by switched averaging of vectors 010 (or 121) and 110 (or 221). Since vector 13 lies on the line joining 010 and 110, zero vector of the CHB need not be switched for generating the pseudovector. Vector 010 of CHB lying closer to vector 13 is called the inner vector (V_{13}^{in}) and vector 110 of CHB lying away from vector 13 is called the outer vector (V_{13}^{out}). The time ratio in which the vectors have to be applied is denoted as k_a. For example, if T_{13} is the duration for which vector 13 has to be generated, then V_{13}^{in} is generated for $k_a T_{13}$ time duration and V_{13}^{out} is generated for $(1-k_a)T_{13}$ time duration. The ratio k_a is used for all vectors in the space vector structure except for all odd numbered vectors on dodecagon E ($49, 51, \ldots, 57$, and 59) and for all vectors on dodecagon F ($61, 62, \ldots, 71$, and 72). To generate vector 61, the FC inverter outputs vector 200 and the CHB inverter switches vectors 020 and 120 (instead of 020 and 220) to generate the pseudovector. If vectors 020 and 220 are used, then the machine phase voltage rating will be exceeded and also the switching dv/dt will be more. Therefore, vectors 020 and 120 are switched at a ratio k_b. Relation between k_a and k_b is derived as follows. Let the pseudovector to be generated in the case of vector 61 is V_p. Writing the volt-second balance for the two ways in which V_p can be generated gives

$$V_p T_s = (020)k_a T_s + (220)(1-k_a)T_s \tag{2}$$

$$V_p T_s = (020)k_b T_s + (120)(1-k_b)T_s. \tag{3}$$

Substituting values for vectors $020, 220$, and 120 and equating the aforementioned two equations gives the relation $k_b = 2k_a - 1$.

V. CHB Floating Capacitor Voltage and Charge Balancing

For obtaining a dodecagonal space vector structure using two two-level inverters (INV1 and INV2) for an open-end winding induction motor using a single dc source as proposed in [17], the INV2 dc-link voltage, which is maintained by a capacitor, is set to $0.289\,V_{dc}$. The inner and outer vectors from the INV2 are switched averaged at a time ratio k = 0.732 to generate a pseudovector of $0.259\,V_{dc} \angle 75^\circ$. This ratio automatically brings charge balance for the capacitor which maintains the dc-link in INV2. A value of $k > 0.732$ can charge the capacitor and $k < 0.732$ can discharge the capacitor. This property is used for balancing the capacitor voltage. This paper extends this idea to obtain a multilevel space vector structure for a star-connected IM drive.

The inverter topology used in this study is derived from the topology in [17] as explained later. The six-concentric dodecagonal structure can be decomposed into superposition of two independent dodecagonal structures. In order to generate one dodecagon, two two-level hexagonal space vector structures are required [17]. Replacing the two-level inverters with three-level inverters (with same dc-links of V_{dc} and $0.289\,V_{dc}$), two independent dodecagons are generated. The two dodecagons generated are superposed to get the six-concentric dodecagonal space vector structure for an open-end winding IM drive scheme. The three-level inverter with dc link of $0.289\,V_{dc}$ is bought to the same side with the other three-level inverter with dc link of V_{dc} using floating capacitor fed CHBs. With a CHB topology, in order to generate a three-level space vector structure of radius $0.289\,V_{dc}$, the floating capacitor voltage needed is $0.1445\,V_{dc}$. Thus, the topology used in this study is obtained. Conceptually the CHB inverter operates similar to the INV2 in [17], and hence, the time ratio $k_a = 0.732$ (or $k_b = 0.464$) are valid for the topology in this study. Using $k_a > 0.732$ charges and $k_a < 0.732$ discharges, the floating capacitors ($Ca2, Cb2, Cc2$) and similarly for k_b.

Since there are three floating capacitors to control, one per phase, the voltage balancing scheme has to independently modify the capacitor voltages. This means that trying to balance the *a*-phase floating capacitor (Ca2) voltage should not unbalance the *b*-phase and *c*-phase capacitor (Cb2 and Cc2) voltages. The same holds for *b*-phase and *c*-phase. For example, consider vector 13 in Fig. 4. The CHB vector pair (inner and outer vectors) used is 010–110. Observe that only the *a*-phase switching state has changed (0 to 1) and the *b*-phase and *c*-phase switching states remain constant over the time duration for which vector 13 is generated. This shows that changing the value of k_a do not have any effect on *b*-phase and *c*-phase floating capacitor voltages. Only such vector pairs of the CHB inverter that affects only one capacitor at a time are used for balancing the capacitors. Therefore, CHB vector pairs corresponding to

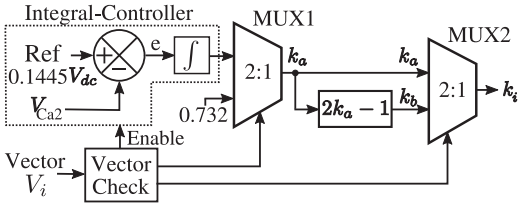

Fig. 5. Controller structure for CHB capacitor balancing (for *a*-phase).

dodecagonal vectors $1, 7, 13, 18, 19, 24, 25, 31, 49, 55, 61, 66, 67$, and 72 (see Fig. 3) are used for balancing a-phase CHB floating capacitor (Ca2). Vectors which are shifted 120° and 240° to above vectors are used to balance Cb2 and Cc2, respectively. Controller scheme used for CHB capacitor balancing (for a-phase) is shown in Fig. 5.

In Fig. 5, when a vector V_i needs to be generated, a vector check logic checks whether the vector can be used for capacitor balancing in a-phase. If the vector cannot be used for balancing the capacitor, then nominal value of 0.732 is selected using a multiplexer (MUX1). If the vector can be used for capacitor balancing, then the integral-controller is enabled. In the integral-controller for a-phase, the capacitor voltage $\mathrm{V_{Ca2}}$ is compared against the nominal value ($0.1445\,\mathrm{V_{dc}}$) to generate the error (e). This error output goes to an integrator which modifies the k_a value. If the error is negative ($\mathrm{V_{Ca2}}$ higher than nominal value), integrator output reduces and hence k_a value reduces, resulting in discharge of Ca2. If error is positive, k_a value increases and capacitor charges. This control action brings the error to zero, and hence, the capacitor voltage to nominal voltage. MUX1 outputs k_a value (0.732 or the integrator output) from which k_b value is derived. Vector check logic again selects between k_a and k_b to generate k_i depending on V_i using MUX2. If V_i is an odd-numbered vector on dodecagon E or any vector on dodecagon F, MUX2 selects k_b, otherwise k_a. Same controller structure is replicated for *b*-phase and *c*-phase.

VI. FC Voltage Balancing

For a dc-link voltage of $\mathrm{V_{dc}}$, in order to generate pole voltage of $0.5\,\mathrm{V_{dc}}$ from the FC inverter (see Fig. 1), it is necessary to maintain the voltages of the FCs (Ca1, Cb1, and Cc1 in Fig. 1) at $0.5\,\mathrm{V_{dc}}$. Then, there are two ways to generate pole voltage of $0.5\,\mathrm{V_{dc}}$ for the FC inverter. One way is to directly use the capacitor voltage ($0.5\,\mathrm{V_{dc}}$) or the second way is to subtract the capacitor voltage ($0.5\,\mathrm{V_{dc}}$) from dc-link voltage ($\mathrm{V_{dc}}$) to get $0.5\,\mathrm{V_{dc}}$. This redundancy along with the current direction is used to initially charge as well as balance the FCs. Whenever a pole voltage of $0.5\,\mathrm{V_{dc}}$ is required at the output of the FC inverter (switching state 1), one of the methods given in Table II is used based on sensed capacitor voltage and current direction. In Table II, $x = a, b, c$ indicates phase and a positive current direction implies current flowing out of the inverter pole, into the motor.

VII. PWM Timing Calculation

From a given sampled reference voltage vector V_s, the timing calculation algorithm finds the nearest vectors $[V_0, V_1, V_2]$ forming the smallest triangle bounding V_s and the time durations $[T_0, T_1, T_2]$ for which the vectors have to be applied within the sampling duration T_s. Vector V_s is generated by time averaging of the vectors $[V_0, V_1, V_2]$ using timing values $[T_0, T_1, T_2]$ over a sampling duration T_s. In vector sense, this time averaging is represented as

$$V_s T_s = V_0 T_0 + V_1 T_1 + V_2 T_2 \tag{4}$$

$$T_s = T_0 + T_1 + T_2. \tag{5}$$

Timing calculation steps are similar to the steps mentioned in [15] and [16] owing to the similarity in space vector structure. Timing calculation involves finding the sector inside which the sampled reference vector lies (sector 3 in Fig. 8). The timing values $[T_0, T_1, T_2]$ for the biggest triangles forming a sector are found next. Timing values obtained are translated and or scaled to smaller triangles. The validity of timing values (all T_i positive, $i = 0, 1, 2$) indicates whether it is possible to synthesize the vector using the triangle checked. Thus, the unique triangle inside which the reference vector lies is obtained. The triangle numbering in the space vector structure for a 45° duration (sectors 24, 1, and 2) is shown in Fig. 6. The vectors $[V_0, V_1, V_2]$ are obtained from a lookup table once the unique triangle is found. A part of this lookup table for 15° duration (sector $= 1$) is given in Table III.

PWM switching scheme generates switching pulses to control the inverter switches according to the vectors $[V_0, V_1, V_2]$ to be applied for time durations $[T_0, T_1, T_2]$ over a sampling period T_s. Any PWM scheme aims at reducing the switching transitions to reduce switching losses without sacrificing the output waveform THD. The PWM schemes implemented for the topology used in this study are explained as follows.

TABLE II
Switching Selection for FC Balancing

Current Direction	Capacitor Voltage	Switches Turned ON	Pole Voltage $\mathrm{V_{x\,o}}$
Positive	$\mathrm{V_{Cx1}} < \mathrm{V_{dc}}/2$	Sx1 and $\overline{\mathrm{Sx2}}$	$\mathrm{V_{dc}} - \mathrm{V_{Cx1}}$
Positive	$\mathrm{V_{Cx1}} > \mathrm{V_{dc}}/2$	Sx2 and $\overline{\mathrm{Sx1}}$	$\mathrm{V_{Cx1}}$
Negative	$\mathrm{V_{Cx1}} < \mathrm{V_{dc}}/2$	Sx1 and $\overline{\mathrm{Sx2}}$	$\mathrm{V_{dc}} - \mathrm{V_{Cx1}}$
Negative	$\mathrm{V_{Cx1}} > \mathrm{V_{dc}}/2$	Sx2 and $\overline{\mathrm{Sx1}}$	$\mathrm{V_{Cx1}}$

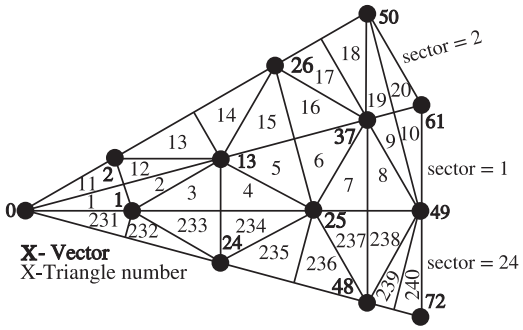

Fig. 6. Triangle numbering for 45° duration.

TABLE III
LOOKUP TABLE FOR 15° DURATION (SECTOR = 1) FOR OBTAINING VECTORS FROM TRIANGLE NUMBER

Triangle#	$[V_0, V_1, V_2]$	Triangle#	$[V_0, V_1, V_2]$
1	$[0, 1, 2]$	6	$[37, 25, 26]$
2	$[13, 1, 2]$	7	$[25, 48, 37]$
3	$[1, 24, 13]$	8	$[49, 48, 37]$
4	$[25, 24, 13]$	9	$[37, 49, 50]$
5	$[13, 25, 26]$	10	$[61, 49, 50]$

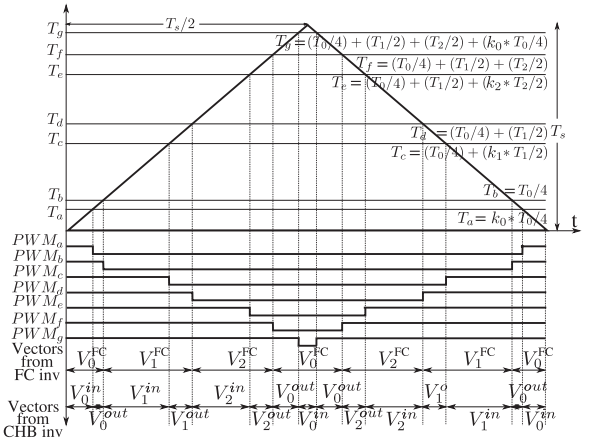

Fig. 7. Vector switching sequence in PWM scheme-1.

A. PWM Switching Scheme-1

In scheme-1, conventional space vector PWM [19] switching sequence $V_0 - V_1 - V_2 - V_0 - V_2 - V_1 - V_0$ for time durations $T_0/4 - T_1/2 - T_2/2 - T_0/2 - T_2/2 - T_1/2 - T_0/4$ in a sampling period T_s is implemented. When a vector $V_i, i = 0, 1, 2$ has to be generated, the FC inverter has to apply the vector (V_i^{FC}) that lies closest to vector V_i. The CHB inverter has to apply switching states corresponding to vector pair V_i^{in} (inner vector) and V_i^{out} (outer vector) in the time ratio set by k_i. Generation of timing signals is shown in Fig. 7. The signals PWM_a to PWM_g are decoded to get time durations for which the switching states from FC and CHB inverters are applied.

B. PWM Switching Scheme-2

PWM scheme-2 is similar to the scheme implemented in [16]. The aim of this PWM scheme is to utilize the higher density of the space vector structure available at higher modulation indices (observe that the dodecagons D, E, and F are closer compared to A, B, and C). The number of switching are reduced in this scheme maintaining the waveform THD. The switching sequence used is $V_1 - V_0 - V_2$ during a sampling period T_s (see Fig. 8). In the next sampling duration $T_s^{'}$, the sequence is $V_1^{'} - V_0^{'} - V_2^{'}$. But note that V_2 is same as $V_1^{'}$, and hence, there is no switching required (see Fig. 8). In this way, switching transitions are reduced.

The number of samples per fundamental cycle is always 12, i.e., once in every 30° duration. Generation of timing signals are

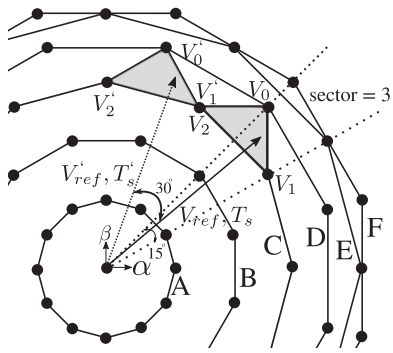

Fig. 8. Vector switching in PWM scheme-2.

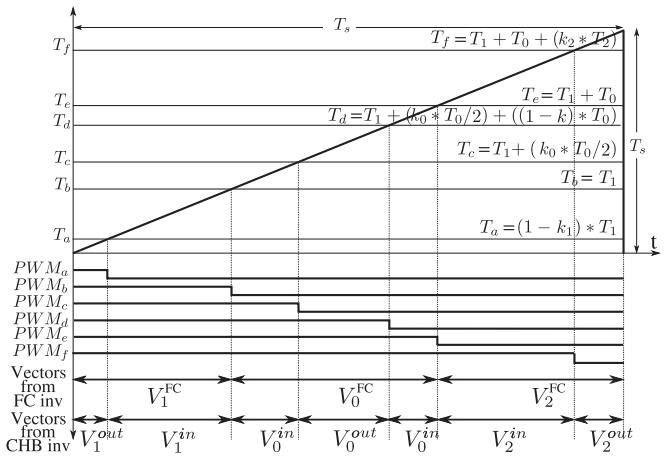

Fig. 9. Vector switching sequence in PWM scheme-2.

shown in Fig. 9. The signals PWM_a to PWM_f are decoded to get time durations for which the switching states from FC and CHB inverters are applied.

VIII. HARDWARE SETUP

The hardware setup used for experiment consists of a DSP platform based on Texas Instruments TMS320F28334 and an FPGA board based on Xilinx Spartan-3E XC3S200. Voltage and current measurements are done using sensor modules LV20-P and LA55-P, respectively. A 1-KW, 400-V, four-pole induction motor is used for testing the topology. The FC and CHB inverter modules are realized using Semikron SKM75GB12T4 (75 A, 1200 V) half-bridge IGBT modules. Block diagram of the hardware set up is shown in Fig. 10.

An open-loop *V/f* scheme is implemented on the DSP chip. The PWM timing calculation algorithm runs on the DSP chip and the PWM signals (PWM_a to PWM_g in Figs. 7 and 9) are send to the FPGA board along with the signals required for FC balancing of the FC inverter. The PWM signals are decoded inside FPGA and gating pulses for the IGBTs are generated. Dead time of about 1.5 μs is inserted at the appropriate edges of the gating pulses before sending to the gate drivers. The dc-link voltage, the phase currents, and all the capacitor voltages are sensed and are used for the FC balancing in an FC inverter and floating capacitor balancing in the CHB inverter.

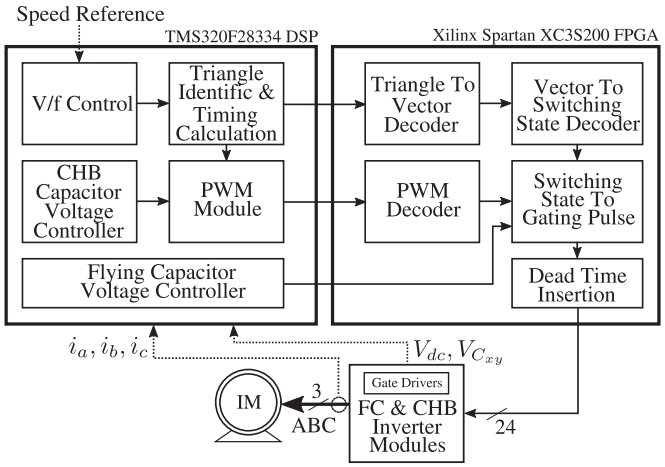

Fig. 10. Hardware block diagram.

IX. Results

A dc-link voltage of $V_{dc} = 200$ V is used for the experiment purpose. The steady-state voltage of FCs in an FC inverter is $0.5\,V_{dc} = 100$ V and the steady-state voltage for floating capacitors in the CHB inverter is $0.1445\,V_{dc} = 28.9$ V. Waveforms are obtained for no load condition to get the worst-case current ripple.

A. Steady-State Results

Synchronous PWM technique is used for all frequencies of operation. Steady-state phase voltage (1), pole voltage of FC inverter (2), pole voltage of CHB inverter (3), and phase current (4) for 10-, 18-, 30-, 40-, 45-, and 48-Hz operation (linear modulation range) for *a*-phase are shown in Fig. 11.

Reference voltage vector lies inside dodecagon A for 10-Hz operation, between dodecagons A and B for 18 Hz, between dodecagons B and C for 30 Hz, between dodecagons C and D for 40 Hz and between dodecagons D and E for 45 Hz. PWM switching scheme-1 is used for 10-, 18-, 30-, and 40-Hz operations and PWM switching scheme-2 is used for 45- and 48-Hz operations. Number of samples taken per fundamental cycle (spc) is 48 spc for 10- and 18-Hz operation, 24 spc for 30- and 40 Hz, and 12 spc for 45 and 48 Hz. Observe that the PWM switching scheme-2 (see Section VII-B) gives quasi-square waveform at FC inverter output, and hence, switching losses are reduced.

Fig. 12 shows 12-step operation generating 50-Hz output in the case of extreme overmodulation. The FC inverter operates in six-step mode generating square wave output. CHB inverter switching cancels the fifth- and seventh-order harmonics present in the square wave generated by an FC inverter.

Fig. 13 shows the pole voltage of the inverter, FC voltage ripple, and floating capacitor voltage ripple for 48-Hz operation.

Frequency spectrum of phase voltages obtained by fast Fourier transform (FFT) for 30 and 48-Hz operations are shown in Fig. 14.

Fig. 14 shows the absence of fifth- and seventh-order harmonics in the phase voltages. For 30-Hz operation, since 24 spc

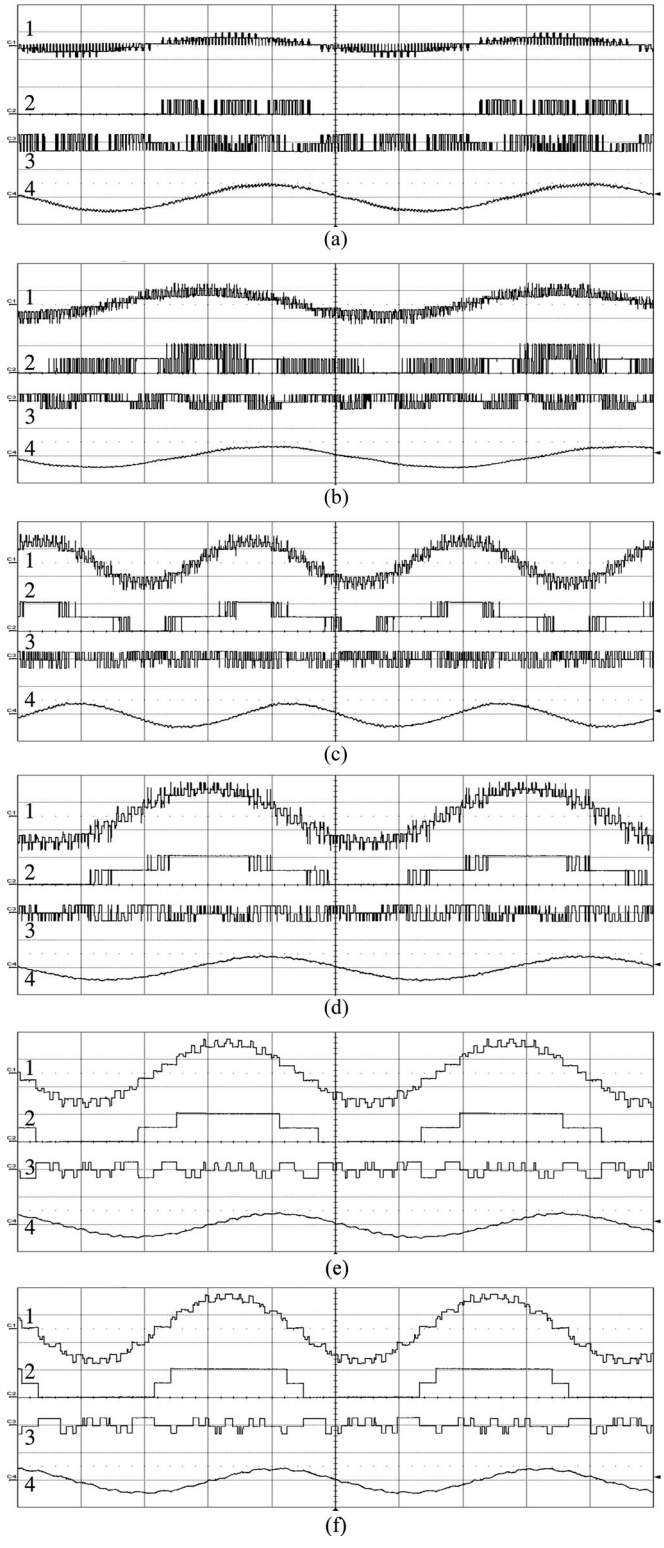

Fig. 11. Steady-state results in linear modulation range for a-phase: (1) phase Voltage, (2) FC inverter pole voltage, (3) CHB inverter pole voltage, (4) phase current. (a) 10 Hz, 48 spc Y: (1) 100 V/div (2) 200 V/div (3) 50 V/div (4) 1 A/div X: 20 mS/div, (b) 18 Hz, 48 spc Y: (1) 100 V/div (2) 200 V/div (3) 50 V/div (4) 1 A/div X: 10 mS/div, (c) 30 Hz, 24 spc Y: (1) 100 V/div (2) 200 V/div (3) 50 V/div (4) 1 A/div X: 10 mS/div, (d) 40 Hz, 24 spc Y: (1) 100 V/div (2) 200 V/div (3) 50 V/div (4) 1 A/div X: 5 mS/div, (e) 45 Hz, 12 spc Y: (1) 100 V/div (2) 200 V/div (3) 50 V/div (4) 1 A/div X: 5 mS/div, (f) 48 Hz, 12 spc Y: (1) 100 V/div (2) 200 V/div (3) 50 V/div (4) 1 A/div X: 5 mS/div.

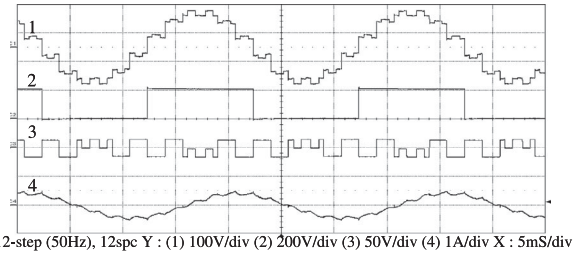

Fig. 12. Steady-state results for extreme overmodulation operation (50 Hz): (1) phase Voltage, (2) FC inverter pole voltage, (3) CHB inverter pole voltage, (4) phase current.

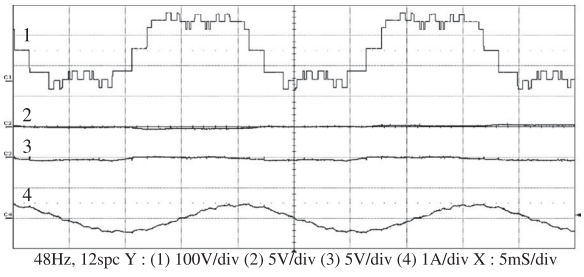

Fig. 13. Steady-state results for 48-Hz operation: (1) pole voltage V_{ao}, (2) FC inverter flying capacitor ($\mathrm{Ca1}$) ripple, (3) CHB inverter floating capacitor ($\mathrm{Ca2}$) ripple, (4) phase current.

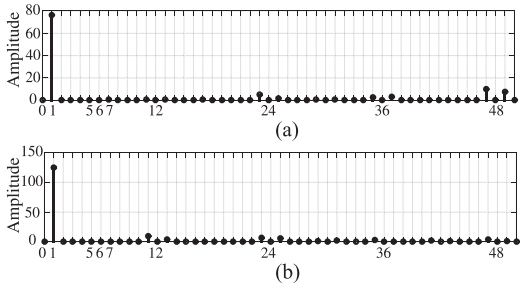

Fig. 14. FFTs of phase voltage for (a) 30-Hz and (b) 48-Hz operation, *Y*-axis: Voltages, *X*-axis: Harmonic number. (a) FFT–Motor Phase Voltage, 30 Hz operation (b) FFT–Motor Phase Voltage, 48 Hz operation.

is used, the switching frequency harmonics and side bands are around 24th-harmonic order. Similarly for 48 Hz, the switching frequency harmonics and side bands are around 12th-harmonic order.

Fig. 15 shows FFTs of the FC inverter pole voltage, CH inverter pole voltage, and motor phase voltage for 12-step operation (50 Hz). FFTs shows that the fifth- and seventh-order harmonics present in the FC inverter pole voltage is canceled by the CHB inverter switching action. The FFTs also show that the fifth- and seventh-order harmonics are absent over the entire modulation range including overmodulation.

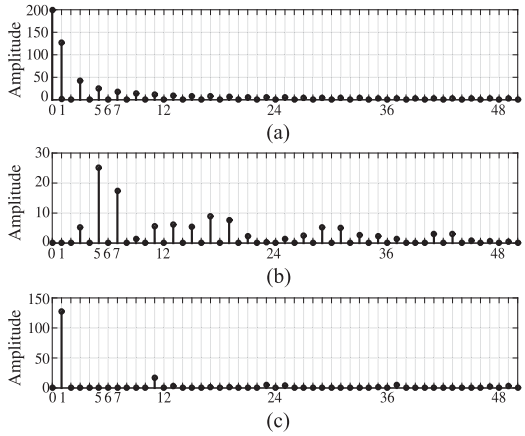

Fig. 15. FFTs of (a) FC inverter pole voltage, (b) CHB inverter pole voltage, and (c) Motor phase voltage for 50 Hz (12-step) operation, *Y*-axis: Voltages, *X*-axis: Harmonic number. (a) FFT–FC Inverter Pole Voltage, 50 Hz operation, (a) FFT–CHB Inverter Pole Voltage, 50 Hz operation, (c) FFT–Motor Phase Voltage, 50 Hz operation.

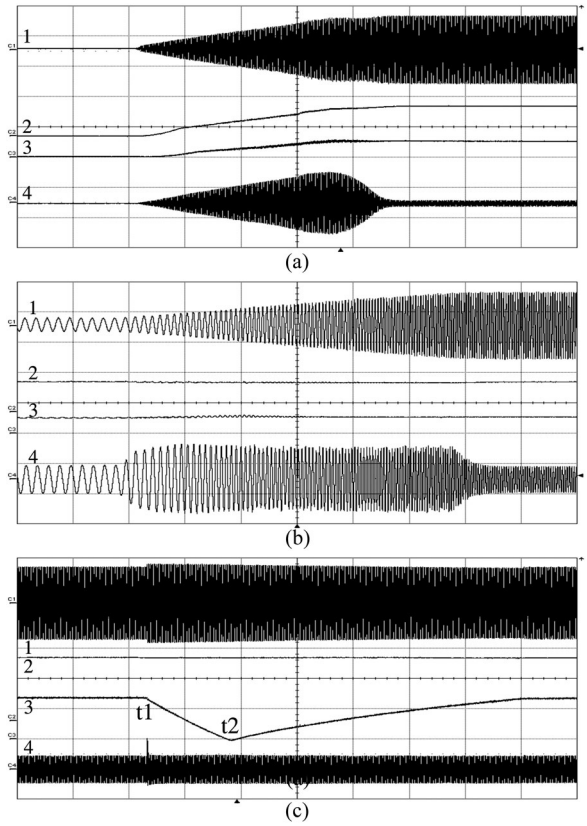

Fig. 16. Transient results, (1) phase Voltage, (2) FC inverter flying capacitor voltage, (3) CHB inverter floating capacitor voltage, (4) phase current. (a) 48 Hz startup, Y: (1) 100 V/div (2) 100 V/div (3) 50 V/div (4) 5 A/div X: 1 S/div, (b) 10–48 Hz acceleration, Y: (1) 100 V/div (2) 100 V/div (3) 50 V/div (4) 1 A/div X: 0.5 S/div, (c) CHB k-control disable, Y: (1) 100 V/div (2) 50 V/div (3) 20 V/div (4) 1 A/div X: 1 S/div.

B. Transient Results

Waveforms during startup at no load for 48-Hz operation is shown in Fig. 16(a). Waveforms show that the voltages of FCs and floating capacitors settle to nominal values at the end of startup without the help of any precharging circuit. This concludes that the capacitor voltage buildup and balancing happens inherently with the PWM operation.

Fig. 16(b) shows waveforms during motor acceleration from 10 to 48 Hz. Waveforms show that the capacitor voltages are tightly controlled during acceleration.

In Fig. 16(c), the CHB floating capacitor controller is disabled at point marked as "t1" and the k_i values are set to zero. This results in discharge of the capacitors. At point marked as "t2," the controllers are reenabled. The floating capacitor voltage builds up and reaches the steady-state value of $0.1445\,V_{dc} = 28.9$ V validating the operation of the controller.

X. Conclusion

An IM drive scheme generating a switched average multilevel six-concentric dodecagonal space vector structure using a single dc source is proposed for the first time. The fifth- and seventh-order harmonic voltages, represented as $(6n \pm 1)$th, n = odd order harmonics, are eliminated from the phase voltage resulting in elimination of sixth-order torque ripple over the full speed range up to the base speed. The FC inverter switches in quasi-square mode at high modulation indices resulting in low switching losses. At extreme overmodulation, the inverter as a whole operates in 12-step mode, while the FC inverter operates in 6-step mode. The CHB inverter switching results in cancellation of the fifth- and seventh-order harmonics generated by the FC inverter. Linear modulation range is extended up to 48.82 Hz compared to 45.29 Hz in the case of a hexagonal space vector structure. Multilevel operation results in low d*v*/d*t* output voltage reducing EMI concerns. The FC inverter switches between pole voltage levels $0, V_{dc}/2$, and V_{dc}, but at a low switching frequency. The CHB inverter switches at a higher frequency but the switching is between smaller voltages of $-0.1445\,V_{dc}, 0$ and $+0.1445\,V_{dc}$. Hence, the switching losses are low, both in the FC and CHB inverters. Since only one dc-link is required, four-quadrant operation of the motor is easy when the dc-link is fed from an active front-end converter. Also, single dc-link requirement brings down the size and cost of the system. None of the capacitors in the topology require any precharging circuit and the voltage buildup and balancing happens automatically with the PWM operation. Proper vector selection for the CHB inverter ensures that the machine phase voltage rating is never exceeded. Steady-state operation of the inverter at different frequencies (10–48 Hz), operation in overmodulation region and operation during transients were validated experimentally. The proposed IM drive scheme is suitable for high-power and high-performance medium-voltage IM drive applications owing to theaforementioned features and advantages.

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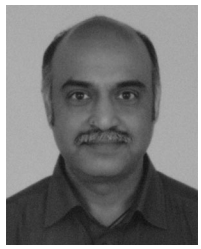

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