# Elimination of Low-Frequency Ripples and Regulation of Neutral-Point Voltage in Stacked Multicell Converters

Amer M. Y. M. Ghias, *Member, IEEE*, Josep Pou, *Senior Member, IEEE*, Pablo Acuna, *Member, IEEE*, Salvador Ceballos, Alireza Heidari, *Member, IEEE*, Vassilios G. Agelidis, *Fellow, IEEE*, and Adel Merabet, *Member, IEEE*

***Abstract*—This paper introduces a modulation method for the stacked multicell converters (SMCs). The proposed method is implemented using phase-disposition pulse width modulation and is capable of balancing and regulating the voltages of all the capacitors in the topology, i.e., the flying capacitors and the dc-link capacitors. The proposed method is also able to eliminate the low-frequency voltage ripples that may appear in the neutral point (NP) of SMCs. In SMCs with two stacks, the NP voltage level can be generated by direct connection of the output to the dc-link NP, but also using two extra states available. This redundancy is used to regulate the NP voltage. Furthermore, since the proposed method can eliminate the low-frequency voltage ripples in the capacitors, the capacitances of all the capacitors of the SMCs can be reduced, while maintaining high quality of the output voltages and currents. This enables the use of film capacitors. Simulation and experimental results are presented from a three-phase five-level $2 \times 2$ SMC to verify the effectiveness of the proposed method.**

***Index Terms*—Converters, HVDC converters, inverters, power electronics, pulse width modulated converters, pulse width modulated inverters, voltage control.**

## I. Introduction

MULTILEVEL converters have become popular for medium- and high-power applications [1]–[9]. Novel hybrid multilevel converters have been introduced in recent years, such as the stacked multicell converter (SMC) [10]. The SMC is based on the flying capacitor (FC) converter [11]; however, the SMC stores less energy and consequently requires fewer capacitors. For example, each phase-leg of a five-level SMC requires two FCs, whereas the five-level FC converter requires three FCs, some of them rated at higher voltages. Although the SMC requires more power switches than the FC converter, the reduction in the total capacitance is more relevant for practical applications. This is why the SMC has potential interest for industry.

As in the FC converter, the FCs of the SMC are naturally balanced [12]–[19], [25]. The balancing process can be speed up with the addition of an $RLC$ booster/filter. However, natural voltage balance depends on the loading conditions. The voltage-balancing dynamic slows down with different types of loads, especially with nonlinear loads. Furthermore, the use of an $RLC$ booster increases the cost and power losses in the converter.

Recently, some active voltage-balancing methods applied to SMCs have been proposed [20]–[24]. These methods address capacitor voltage balance only in the FCs of the SMC, since the dc-link neutral-point (NP) connection is provided by two dc voltage sources. However, the use of a single dc source in the dc link is very common in many applications. In those cases, the NP connection is provided by capacitors, thus requiring capacitor voltage balance to be achieved [25]. However, as with the neutral-point-clamped (NPC) converter [26], [27], a low-frequency voltage ripple appears in the NP of the SMC for some operating conditions when using standard modulation methods such as those in [12]–[24]. If the capacitances of the dc-link capacitors and the FCs are small, the NP voltage ripple becomes large and produces significant voltage ripples in the FCs as well. All these ripples distort the output voltages and currents, besides increasing the maximum voltages applied to the capacitors and the power devices of the converter.

Feed-forward control methods were proposed in [28] and [29] to overcome the effects of the low-frequency ripples in the output voltages. However, those methods have limitations related to the maximum amplitude of the ripples that can be compensated. Furthermore, the feed-forward methods cannot remove low-frequency voltage ripples; therefore, the capacitors and power devices of the converter have to withstand higher voltages due to the ripples.

In [27], a fast-processing modulation (FPM) method was proposed for the three-level NPC converter. With this method, the low-frequency NP voltage ripples are eliminated. Because of similitude with the NPC converter, the FPM method can be implemented in the SMC with two stacks, which has never been done before.

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A. M. Y. M. Ghias is with the Department of Electrical and Computer Engineering, University of Sharjah, Sharjah 27272, United Arab Emirates (e-mail: aghias@sharjah.ac.ae).

J. Pou is with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (email: j.pou@ntu.edu.sg).

P. Acuna, A. Heidari, and V. G. Agelidis are with the Australian Energy Research Institute and the School of Electrical Engineering and Telecommunications, The University of New South Wales, Sydney, N.S.W. 2052, Australia (e-mail: pablo.acuna@unsw.edu.au; alireza.heidari@unsw.edu.au; vassilios.agelidis@unsw.edu.au).

S. Ceballos is with the Energy and Environment Division, Tecnalia Research and Innovation, 48160 Derio, Spain (e-mail: salvador.ceballos@tecnalia.com).

A. Merabet is with the Division of Engineering, Saint Mary's University, Halifax, NS, B3H 3C3 Canada (e-mail: adel.merabet@smu.ca).

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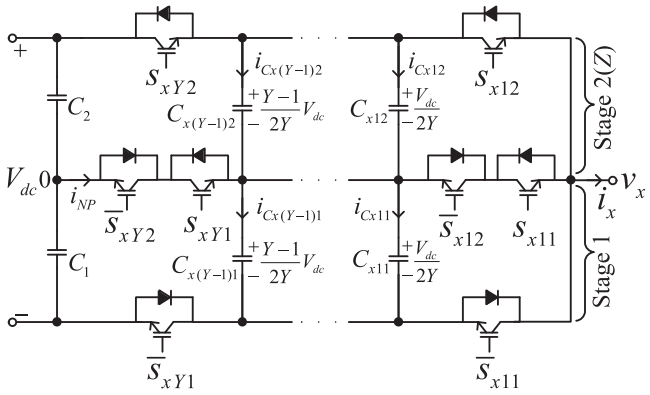


Fig. 1. Phase-leg of an $Y \times 2$ SMC.

This paper proposes implementing the FPM method in the SMC. A particularity of applying the FPM to the SMC is that two extra redundant states appear, which are used to achieve NP capacitor voltage balance. These redundant states generate the NP voltage level at the output, and they never appear when using standard modulation strategies [12]–[19], [25]. In the proposed method, cost functions are used to select the redundant states to be applied at any switching period. The proposed modulation method produces output voltages with lower weighted total harmonic distortion (WTHD) because the low-frequency voltage ripples are eliminated from all the capacitors integrated in the topology, enabling for a reduction in their capacitances. Furthermore, this paper presents switching frequency, capacitor voltage ripple, power losses in the semiconductors, computation burden, and compares them with those obtained from applying traditional phase-disposition pulse-width modulation (PD-PWM) [24].

The paper is organized as follows. Section II describes the fundamentals of the SMC and the traditional PD-PWM method. Section III presents the implementation of PD-PWM based on the FPM method. Section IV analyzes switching frequency, capacitor voltage ripples, power losses in the semiconductors, and the computation burden, comparing all of them with the traditional PD-PWM method. Section V presents simulation and experimental results obtained from a three-phase five-level SMC. Finally, the conclusions are summarized in Section VI.

## II. SMC

### A. Topology and Fundamentals

Fig. 1 shows the circuit diagram of an SMC phase-leg. It consists of $Y$ FC converter cells, which are integrated to form two stages/stacks ($Z = 2$). It is called a $Y \times 2$ SMC. The converter comprises $2(Y-1)$ FCs: the upper FCs ($C_{x12}, \ldots, C_{x(Y-1)2}$) in Stage 2, and the lower FCs ($C_{x11}, \ldots, C_{x(Y-1)1}$) in Stage 1, where the subscript $x$ is used for phase identification $x \in \{a, b, c\}$. The dc-link consists of two capacitors $C_1$ and $C_2$, each of which is regulated to half of the dc-link voltage ($V_{\rm dc}/2$). The output voltage $v_{x0}$ consists of $n$ $(Y \times 2 + 1)$ voltage levels, i.e., 0, $V_{\rm dc}/2Y, \ldots,$ $(Y-1)V_{\rm dc}/2Y$, and $V_{\rm dc}$. The switch control functions are defined as $s_{\rm xyz}$, where $y \in \{1, \ldots, Y\}$ indicates the switch number corresponding to a particular cell in the phase-leg $x$ of the SMC and $z$ defines a particular switch associated with the stage $z \in \{1, \ldots, Z\}$. In this paper, $Z$ is assumed to be 2 ($Z = 2$). The switch control functions can take two values $s_{\rm xyz} \in \{0, 1\}$, with 0 and 1 corresponding to the switch being OFF and ON, respectively. The switch pairs in each phase-leg ($s_{\rm xyz}$ and $\overline{s}_{\rm xyz}$) operate in a complementary manner. The method proposed in this paper is general for any $Y \times 2$ SMC, although the analysis has been focused on the five-level $2 \times 2$ SMC (see Fig. 2).

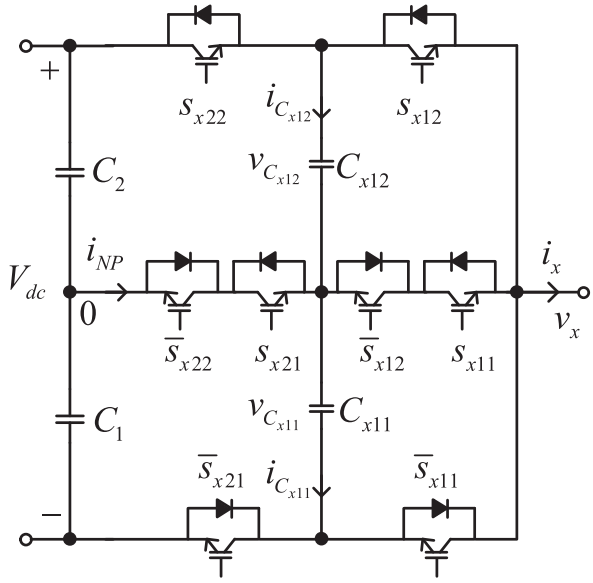

Fig. 2. Phase-leg of a five-level $2 \times 2$ SMC.

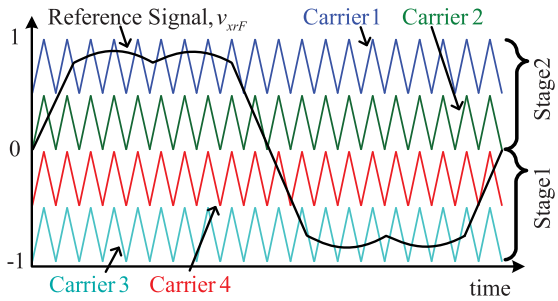


Fig. 3. Traditional PD-PWM in a five-level $2 \times 2$ SMC.

### B. PD-PWM and FC Voltage Balance

Four level-shifted carriers are needed when applying traditional PD-PWM to a five-level $2 \times 2$ SMC. Fig. 3 shows an example of a modulation signal and carriers. In three-phase systems, a zero sequence is commonly injected in the modulation signals to achieve maximum amplitude of the output voltage fundamentals under linear modulation [26]. The zero-sequence voltage ($v_0$) injected in the reference signal ($v_{\rm xr}$) in Fig. 3 is given by $(v_{\rm xr\,max} + v_{\rm xr\,min})/2$, where $v_{\rm xr\,max}$ and $v_{\rm xr\,min}$ are the maximum and minimum values of the modulation signals of the three phases, respectively. The modified voltage reference signal is given as

$$v_{{\rm xr}F} = v_{\rm xr} - v_0. \tag{1}$$

TABLE I
FIVE-LEVEL 2 × 2 SMC: VOLTAGE LEVELS, SWITCHING STATES, FC CURRENTS, AND EFFECTS ON THE FC VOLTAGES

| Output Voltage | | Switching States | | | | | FC Currents | | FC Voltages | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Level ($v_{x0}$) | | $s_{x22}$ | $s_{x12}$ | $s_{x21}$ | $s_{x11}$ | State | $i_{Cx11}$ | $i_{Cx12}$ | $v_{Cx21}$ | $v_{Cx12}$ | |
| 4 | $V_{\rm dc}$ | 1 | 1 | 1 | 1 | {16} | 0 | 0 | NC | NC | |
| 3 | $3\frac{V_{\rm dc}}{4}$ | 1 | 0 | 1 | 1 | {11} | 0 | $i_x$ | NC | ↑ | $v_{xref} > 0$ |
| | | 0 | 1 | 1 | 1 | {7} | 0 | -$i_x$ | NC | ↓ | |
| 2 | $\frac{V_{\rm dc}}{2}$ | 0 | 0 | 1 | 1 | {3} | 0 | 0 | NC | NC | |
| 1 | $\frac{V_{\rm dc}}{4}$ | 0 | 0 | 1 | 0 | {2} | $i_x$ | 0 | ↑ | NC | |
| | | 0 | 0 | 0 | 1 | {1} | -$i_x$ | 0 | ↓ | NC | $v_{xref} < 0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | {0} | 0 | 0 | NC | NC | |

Note: The charging/discharging effects in the FC are given assuming that $i_x$ is positive ($i_x > 0$) with the following notation:
↑ Capacitor voltage increases.
↓ Capacitor voltage decreases.
NC No change in the capacitor voltage.

The output voltage level that is activated at each phase of the converter is defined by comparing the modulation signal (1) with the carriers, as follows:

$$\left.\begin{array}{llll} \text{if} & v_{\text{xr}F} > \text{Carrier1}, & \text{then } s_{x22}=1; & \text{otherwise } s_{x22}=0 \\ \text{if} & v_{\text{xr}F} > \text{Carrier2}, & \text{then } s_{x12}=1; & \text{otherwise } s_{x12}=0 \\ \text{if} & v_{\text{xr}F} > \text{Carrier3}, & \text{then } s_{x21}=1; & \text{otherwise } s_{x21}=0 \\ \text{if} & v_{\text{xr}F} > \text{Carrier4}, & \text{then } s_{x11}=1; & \text{otherwise } s_{x11}=0 \end{array}\right\}. \tag{2}$$

When the carriers used in PD-PWM are associated with particular switches, as in the case of using (2), PD-PWM does not provide natural capacitor voltage balance to the FCs. Hence, an active capacitor voltage balance method must be implemented, such as that in [23] and [24], which is based on evaluating a cost function to select the optimal switching state among the redundant states available. Redundant states are different states that produce the same output voltage level. The cost function is defined as the absolute value of deviation of energy stored in all the FCs from the rated conditions, as follows:

$$J_{xz\,s} = \frac{1}{2}\sum_{j=1}^{Y-1} C_{\text{xjz}}(\Delta v_{C\text{xjz}})^2$$
$$\text{with } \Delta v_{C\text{xjz}} = v_{C\text{xjz}} - V^*_{C\text{xjz}} \tag{3}$$

where $x$ identifies the phase ($x \in \{a,b,c\}$), and $s$ is the switching state ($s \in \{0,..,16\}$) of stage $z$. For example, $J_{a2\,7}$ is the cost function calculated for phase $a$ ($x=a$), at stage 2 ($z=2$) and switching state 7 ($s=7$), i.e., $s_{a22}=0, s_{a12}=1, s_{a21}=1$, and $s_{a11}=1$ (see Table I). $j$ is the index used for identification of each FC, whereby $C_{\text{xjz}}$ is a particular FC and $V^*_{C\text{xjz}}$ is its reference voltage. In the case of a five-level 2 × 2 SMC, there is only one FC in each stack, and hence, $j=1$.

The cost function (3) is positively defined and becomes zero if all the FC voltages are at their reference values. Therefore, in order to maintain a tendency toward achieving capacitor voltage balance, the differential of (3) should be negative or zero. That is,

$$\frac{d}{dt}J_{xz\,s} = \frac{d}{dt}\frac{1}{2}\sum_{j=1}^{Y-1} C_{\text{xjz}}(\Delta v_{C\text{xjz}})^2$$
$$= \sum_{j=1}^{Y-1}(\Delta v_{C\text{xjz}} i_{C\text{xjz}}) \le 0 \tag{4}$$

where $i_{C\text{xjz}}$ is the current in each FC, which depends on the selected redundant switching state and load current, as shown in Table I. When the modulator defines two particular voltage levels for the following switching period at stage $z$, the cost function is evaluated for the redundant switching states available for those levels. Based on the calculated values for a particular output voltage level, the switching state that provides the minimum value to the cost function is the one selected and used for the gating signals:

$$\min\left[\sum_{j=1}^{Y-1}(\Delta v_{C\text{xjz}} i_{C\text{xjz}})\right]. \tag{5}$$

## III. PROPOSED METHOD TO ELIMINATE LOW-FREQUENCY RIPPLES

### A. FPM Method

In the FPM method, two modulation signals per phase-leg are used. The new signals is obtained from the original reference signals, as follows:

$$\begin{cases} v_{\text{xr}F1} = \dfrac{v_{\text{xr}} - \min(v_{\text{ar}}, v_{\text{br}}, v_{\text{cr}})}{2} \\ v_{\text{xr}F2} = \dfrac{v_{\text{xr}} - \max(v_{\text{ar}}, v_{\text{br}}, v_{\text{cr}})}{2} + 1. \end{cases} \tag{6}$$

The two modulation signals are compared with two carriers that are level-shifted to generate the voltage level $l_x$, as shown in

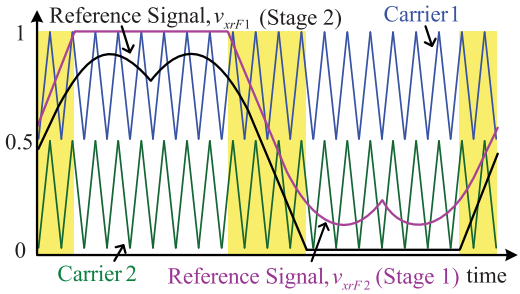


Fig. 4. Example of reference signals for one phase-leg used in the FPM method.

Fig. 4. The criteria used to determine the states of the switches are as follows:

$$\left.\begin{array}{l}\text{if } v_{\text{xr}F1} > \text{Carrier1, then } l_{x1} = 2\\ \text{if Carrier1} \geq v_{\text{xr}F1} > \text{Carrier2,}\\ \text{then } l_{x1} = 1\end{array}\right\} \text{otherwise } l_{x1} = 0$$

$$\left.\begin{array}{l}\text{if } v_{\text{xr}F2} > \text{Carrier1, then } l_{x2} = 2\\ \text{if Carrier1} \geq v_{\text{xr}F2} > \text{Carrier2,}\\ \text{then } l_{x2} = 1\end{array}\right\} \text{otherwise } l_{x2} = 0$$

$$l_x = l_{x1} + l_{x2}, x \in \{a, b, c\} \tag{7}$$

where $l_x$ can take five values, i.e., $l_x \in \{0, 1, 2, 3, 4\}$, which are the possible output levels for each phase. Whenever there is a redundant state that produces the NP voltage, i.e., level 2, the optimal redundant state will be selected by minimizing a cost function to achieve NP voltage balance. This is explained in more detail in the next section. As can be observed in Fig. 4, there are intervals (highlighted in yellow color), where neither of the two reference signals is clamped to 0 or 1. Analyzing those intervals in detail using natural PD-PWM [15] (see Fig. 5), the switching states 1010 and 0101 are produced, which define an output voltage level equal to the NP voltage but without connection to the dc-link NP (state 0011 is the only one connecting the dc-link NP directly to the output). Fig. 6 shows the path from the dc side to the output of the phase-leg with these two extra states. As can be observed, the current direction is the same in both FCs, but depends on the particular redundant state applied. The two redundant states, together with the direct connection to the dc-link NP (state 0011), can be used to regulate the dc-capacitor voltages to the reference value, i.e., half the dc-link voltage.

Fig. 7 shows the switching transition diagrams when using a single modulation signal per phase-leg [see Fig. 7(a)] [23], [24], and with FPM showing the two extra redundant states [see Fig. 7(b)].

### *B. NP Voltage Balance*

To achieve voltage balance in the dc-link capacitors, the NP voltage can be included in the cost function (3) to evaluate the states to be selected. Here is where the extra states begins to

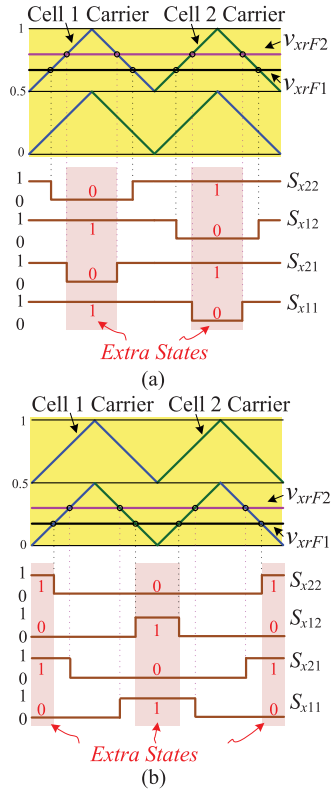


Fig. 5. Analysis of extra states using the FPM method. Examples with both reference signals (a) above and (b) below 0.5.

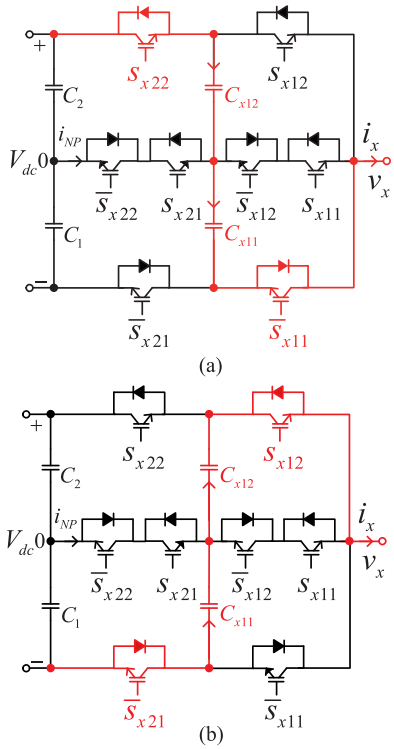


Fig. 6. Extra states that produce the NP voltage level at the output in a five-level 2 × 2 SMC. (a) State 1010. (b) State 0101.

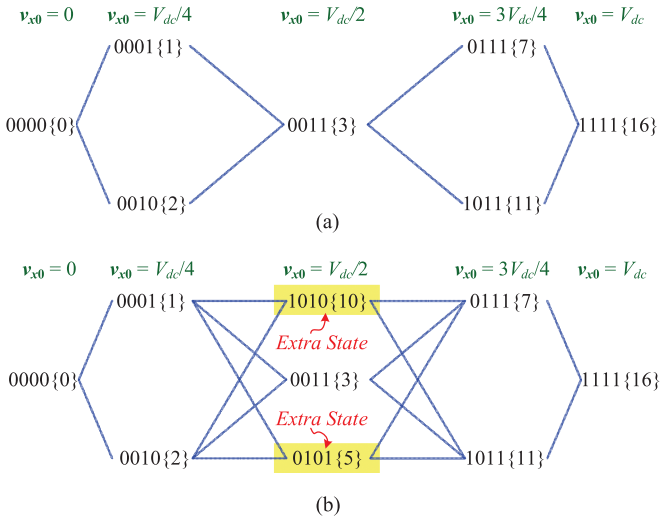


Fig. 7. Switching transitions between consecutive voltage levels in a five-level $2 \times 2$ SMC. (a) PD-PWM using one modulation signal per phase-leg [23], [24] and (b) with FPM using two modulation signals per phase-leg.

play a new role in the proposed cost function as follows:

$$J_{\text{xzs}} = k_{\text{NP}} \frac{C_1 + C_2}{2} (\Delta v_{\text{NP}})^2 + \frac{1}{2} \sum_{j=1}^{Y-1} C_{\text{xjz}} (\Delta v_{C\text{xjz}})^2 \quad (8)$$

where $\Delta v_{\text{NP}}$ is the NP voltage deviation defined as $\Delta v_{\text{NP}} = v_{\text{dc2}} - V_{\text{dc}}/2$, and $k_{\text{NP}}$ is a weighting parameter, which is usually defined according to the ratio of capacitances $k_{\text{NP}} = (C_1 + C_2)/C_{\text{fc}}$, $C_{\text{fc}}$ being the value of the FCs, i.e., $C_{\text{fc}} = C_{x11} = C_{x12}$. Applying differentiation, the function to be minimized is

$$\min \left[ -k_{\text{NP}} \Delta v_{\text{NP}} i_{\text{NP}} + \sum_{j=1}^{Y-1} (\Delta v_{C\text{xjz}} i_{C\text{xjz}}) \right] \quad (9)$$

where $i_{\text{NP}}$ is the NP current, which depends on the selected redundant switching state and the output current. When the modulator defines two particular voltage levels for the next switching period at stage $z$ ($z \in \{1,2\}$), the cost function is evaluated for the redundant switching states available for those levels. In the case of the NP voltage level, the states 1010, 0101, and 0011 are evaluated and one of them is selected.

## IV. Analysis Using the Traditional and Proposed PD-PWM Methods

In this section, the proposed PD-PWM method is applied to a five-level $2 \times 2$ SMC in MATLAB/Simulink [30] using PLECS Blockset [31]. The traditional and proposed PD-PWM methods are analyzed and compared in terms of average switching frequency, power losses, capacitor voltage ripples, and computation burden. In the simulations, the dc-link voltage is $V_{\text{dc}} = 3$ kV and a current source of $I_{\text{xrms}} = 80$ A is connected to the converter output. The value of the FCs ($C_{x11}$, and $C_{x12}$) and the dc-link capacitors ($C_1$ and $C_2$) is 100 μF. The fundamental and the carrier frequencies are

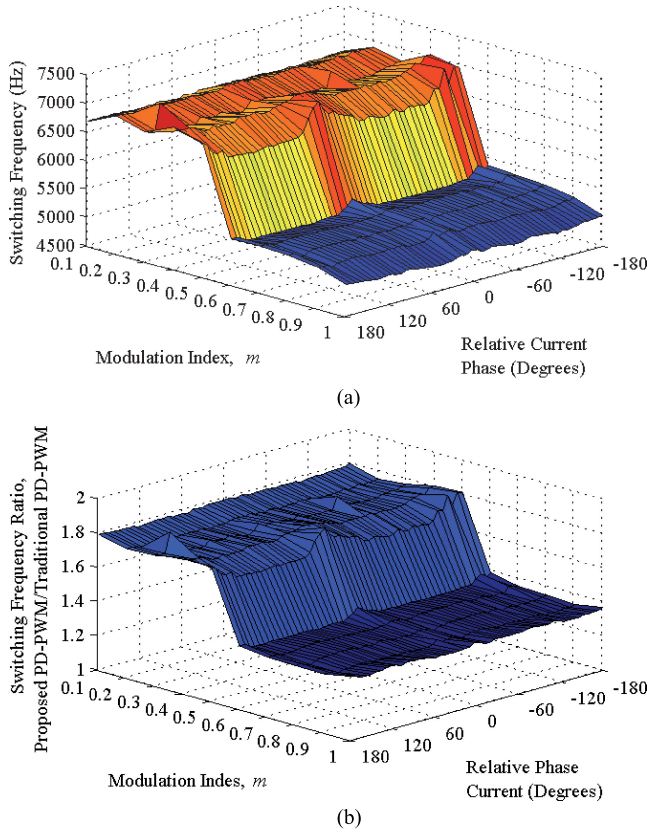


Fig. 8. Average switching frequencies of the power devices of a five-level $2 \times 2$ SMC using $m_f = 200$. (a) Proposed PD-PWM. (b) Switching frequencies ratio (proposed PD-PWM/traditional PD-PWM).

$f = 50$ Hz and $f_s = 10$ kHz, respectively, i.e., a frequency modulation index of $m_f = f_s/f = 200$.

### A. Switching Frequencies

Fig. 8(a) shows the average switching frequency of the power devices using the proposed PD-PWM method. It is calculated as

$$f_{sa,\text{avg}} = \frac{f_{sa11} + f_{sa12} + f_{sa21} + f_{sa22}}{4} \quad (10)$$

where $f_{\text{sa11}}$, $f_{\text{sa12}}$, $f_{\text{sa21}}$, and $f_{\text{sa22}}$ are the switching frequency of the switches $s_{a11}$, $s_{a12}$, $s_{a21}$, and $s_{a22}$, respectively. All possible relative current phase angles and modulation indices have been considered in this representation. In order to achieve the maximum amplitudes of the output voltage fundamentals operating under linear mode, a zero sequence has been added to the modulation signals of the three-phase system [26]. As it can be noticed from Fig. 8(a), the output current phase angle does not significantly affect the average switching frequency.

Fig. 8(b) shows the switching frequency ratio of the proposed PD-PWM over traditional PD-PWM, for all modulation indices and load power factors. It can be observed that with the proposed PD-PWM method, there is an increase in the switching frequency of about 30% on average for large modulation

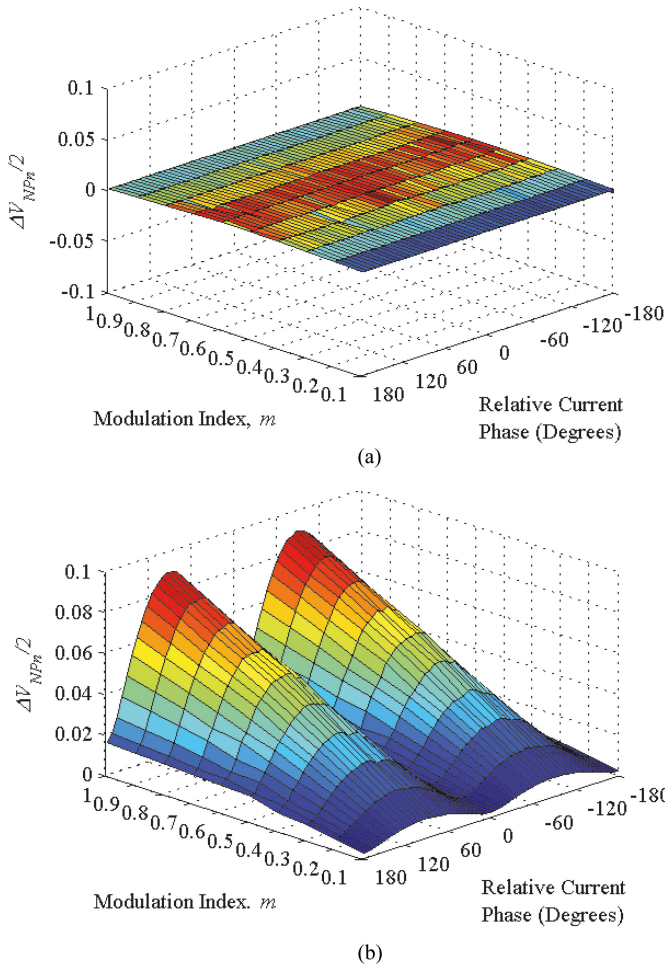


Fig. 9. Normalized amplitudes of the NP voltage ripples. (a) Proposed PD-PWM. (b) Traditional PD-PWM.

indices ($m = 0.6$ to $m = 1$). Such an increase in the switching frequency is significantly larger for low-modulation indices.

### *B. Low-Frequency Capacitor Voltage Ripples*

In this section, the amplitudes of the low-frequency NP voltage ripples using the proposed PD-PWM method are evaluated and compared with the traditional PD-PWM method. The voltage amplitudes are represented using a normalized magnitude in order to present general results that are useful for different applications and operating conditions, as follows:

$$\frac{\Delta V_{\mathrm{NP}n}}{2} = \frac{\Delta V_{\mathrm{NP}}/2}{I_{\mathrm{rms}}/fC} \tag{11}$$

where $\Delta V_{\mathrm{NP}}$ is the peak-to-peak low-frequency NP voltage ripple, $f$ is the low frequency, $I_{\mathrm{rms}}$ is the root mean square (rms) output current, which can be calculated from the rms value of the ac voltage ripple as: $I_{\mathrm{rms}} = V_{\mathrm{rms}}\omega C$ and $C$ is the value of the dc-link capacitor, i.e., $C = C_1 = C_2$.

Assuming sinusoidal output currents, Fig. 9 shows the amplitudes of the dc-link capacitor voltage ripples for all the operating conditions of the converter, i.e., modulation indices and phase current angles using the proposed and traditional PD-PWM methods. As observed, the low-frequency voltage ripples are completely removed using the proposed PD-PWM method. However, low-frequency voltage ripples are observed while using the traditional PD-PWM method. This information is very helpful to size the dc-link capacitor in a practical application. The maximum amplitude is produced when operating with a modulation index $m = 1$ and output current angle about $\theta = 90^\circ$ or $\theta = -90^\circ$. Under such conditions, the maximum normalized ripple is

$$\frac{\Delta V_{\mathrm{NP}n}}{2} = \frac{\frac{\Delta V_{\mathrm{NP}}}{2}}{\frac{I_{\mathrm{rms}}}{fC}} = 0.09. \tag{12}$$

If the values of the parameters in a particular application were, for instance, $I_{\mathrm{rms}} = 80$ A, $f = 150$ Hz, and $C = 100\,\mu$F, the maximum amplitude of the NP voltage ripple would be

$$\frac{\Delta V_{\mathrm{dc}}}{2} = \frac{\Delta V_{\mathrm{dc}n}}{2}\frac{I_{\mathrm{rms}}}{fC} = 0.09\,\frac{80}{150 \cdot 100 \cdot 10^{-6}} = 480\,\mathrm{V}. \tag{13}$$

Due to this voltage ripple, the capacitors and the power devices must withstand higher voltages. The reference voltage for the dc-link capacitor is $V\mathrm{dc}/2 = 1500\,\mathrm{V}$; however, the maximum voltage in the capacitors under this operating condition is

$$V_{\mathrm{dc\,Max}} = \frac{V_{\mathrm{dc}}}{2} + \frac{\Delta V_{\mathrm{NP}}}{2} = 1980\,\mathrm{V} \tag{14}$$

which is 32% larger.

Furthermore, the capacitor voltage ripples produce low-frequency distortion to the output voltages generated by the converter. This effect will eventually distort the output currents.

In this analysis, the switching-frequency voltage ripple in the capacitors is neglected because it is significantly smaller compared to the low-frequency ripple. This is generally acceptable and can be assumed in many applications. However, if the switching-frequency ripples were more significant, they should be taken into consideration and added to the calculated value of the maximum voltage (14).

The capacitor voltage ripples do not dependent on the particular value of each dc-link capacitor. This can be demonstrated from the dynamic model of the NP, where the NP voltage ripples depend on the parallel connection of the two dc-link capacitors instead, as it was demonstrated in [32].

The results of the above theoretical analysis can also be used to size the dc-link capacitors given the specification of maximum voltage ripple. This will provide an initial estimation of the capacitances based on which the converter can be designed to meet other operating criteria.

In the case of using the proposed PD-PWM method, the low-frequency NP voltage ripple is eliminated. Therefore, the frequency ripple produced at and around the carrier frequency is the predominant one when sizing the dc-link capacitors. Since this frequency is high, the values of the dc-link capacitors can be very small.

### C. Power Losses

In this section, the power losses associated with all the switches in the three-phase five-level $2 \times 2$ SMC are analytically estimated and compared between the traditional and the proposed PD-PWM methods. The power losses are classified into conduction and switching losses for both the transistors and freewheeling diodes. The power losses calculation method used in this paper is similar to the one discussed in [24], [26], and [33], which is based on extrapolating the information from the manufacturer's data sheet for conduction ($V_{\rm CE}$ verses $I_C$) and switching curves ($E$ versus $I_C$). For the calculation of conduction losses, the curves of the devices (the transistors and freewheeling diodes) are linearized by a dynamic resistor (reverse slope) and a threshold voltage, while the energy curves of the switching losses are approximated by using a MATLAB curve-fitting tool (polyfit) [30]. The power devices used in this study are the SKM100GB12T4 from SEMIKRON, rated at 1200 V and 100 A. The conduction losses of the transistor and freewheeling diode can be approximated as

$$P_{\rm Cl\_TR} = \frac{1}{T}\int_0^T (V_{\rm TR} + i_F\, R_{\rm TR}) i_F\, dt \tag{15}$$

$$P_{\rm Cl\_D} = \frac{1}{T}\int_0^T (V_{\rm D} + i_F\, R_{\rm D}) i_F\, dt, \tag{16}$$

where $P_{\rm Cl\_TR}$ and $P_{\rm Cl\_D}$ are the conduction losses of the transistor and diode, respectively, $V_{\rm TR}$ and $V_D$ are the threshold voltages of the transistor and diode, respectively, $R_{\rm TR}$ and $R_D$ are the dynamic resistors of the transistor and diode, respectively, $i_F$ is the forward current in the device (transistor and diode), and $T$ is the period of the fundamental frequency. The expression for the mean switching losses for the transistor and diode can be calculated by

$$P_{\rm Sw\_TR} = \frac{1}{T}\sum_{j=1}^{n} [E_{{\rm on}j}(i_F, v) + E_{{\rm off}j}(i_F, v)] \tag{17}$$

$$P_{\rm Sw\_D} = \frac{1}{T}\sum_{j=1}^{n} E_{{\rm rr}j}(i_F, v) \tag{18}$$

where $P_{\rm Sw\_TR}$ and $P_{\rm Sw\_D}$ are the switching losses of the transistor and diode, respectively, $n$ is the number of transitions in a fundamental period $T$, $E_{\rm on}$ and $E_{\rm off}$ are the energies dissipated during the turn-on and turn-off processes of the transistor, respectively. $E_{\rm rr}$ is the energy dissipated during the turn-off process of the diode. This information is available on the power device data sheet in the form of switching curves ($E$ versus $I_C$). These values depend on the voltage $v$ in the off-state and the current $i_F$ in the on-state of the power devices. According to the data sheet, the energy dissipated in the diode during the turn-on process is very small; therefore, it is neglected in this study.

Fig. 10 shows the total power losses (conduction and switching losses) for the three-phase five-level $2 \times 2$ SMC when the proposed and the traditional PD-PWM methods are applied. All possible relative current phase angles and modulation indices have been considered in these representations. A zero sequence has been added to the modulation signals of the three-phase system to extend the range of the modulation index under linear operation mode [26]. Fig. 10(c) shows the total power losses ratio of the proposed PD-PWM over the traditional PD-PWM. It can be observed that this ratio is larger than 1 for all the operating conditions, which means that the proposed PD-PWM produces more losses than the traditional one. This is because the switching frequency of the power devices is lower with the traditional PD-PWM because the switching happens between adjacent voltage levels all the times.

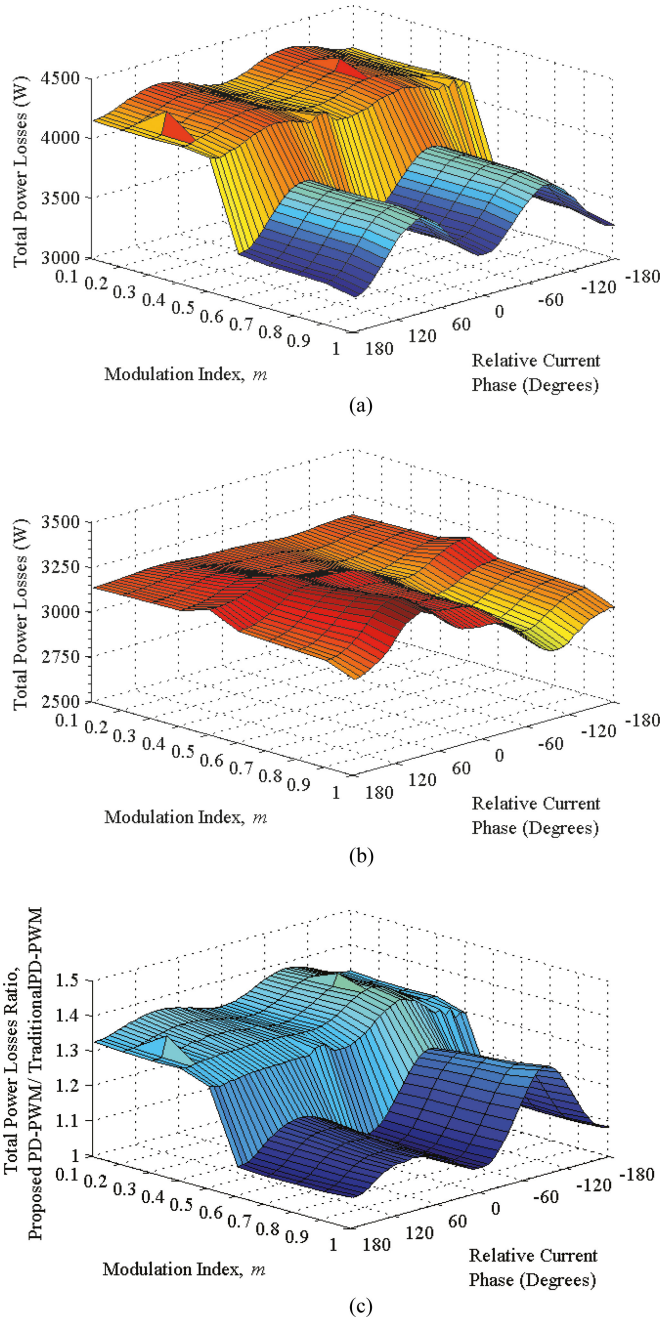


Fig. 10. Total power losses of a three-phase five-level $2 \times 2$ SMC using (a) the proposed PD-PWM and (b) the traditional PD-PWM. (c) Ratio of the proposed PD-PWM over traditional PD-PWM.

TABLE II
NUMBER OF CALCULATIONS OF THE STATE COST FUNCTION IN A FIVE-LEVEL 2×2 SMC

| | Transitions of the Output Voltage, $v_{x0}$ | | | |
|---|---|---|---|---|
| | $0 \leftrightarrow V_{\rm dc}/4$ | $V_{\rm dc}/4 \leftrightarrow V_{\rm dc}/2$ | $V_{\rm dc}/2 \leftrightarrow 3V_{\rm dc}/4$ | $3V_{\rm dc}/4 \leftrightarrow V_{\rm dc}$ |
| Traditional PD-PWM | 2 | 2 | 2 | 2 |
| Proposed PD-PWM | 2 | 5 | 5 | 2 |

### D. Computation Burden

In order to estimate and compare the computation burden for the traditional and proposed PD-PWM methods, the number of cost function calculations that need to be performed in a phase-leg of a five-level SMC are determined and shown in Table II. For this comparison, one cost function calculation is associated with a single switching state. For example, in the case of traditional PD-PWM and when switching between the levels $V_{\rm dc}/4 \leftrightarrow V_{\rm dc}/2$ [see Fig. 7(a)], the cost function has to be calculated for the switching states $0001\{1\}$ and $0010\{2\}$, i.e., two switching states in total. In the case of the proposed PD-PWM, the number of calculations of the cost function is the same as the number of redundant switching states involved in the levels $V_{\rm dc}/4$; however, two extra states appear for the level $V_{\rm dc}/2$, i.e., $1010\{10\}$ and $0101\{5\}$, along with the state $0011\{3\}$ [see Fig. 7(b)], which is five in this example. Table II shows the number of switching state cost function calculations to be performed with the traditional and proposed PD-PWM methods. One can conclude that the proposed PD-PWM method requires about 150% more processing time for two transitions, while the same time is required for the rest.

In summary, using the proposed method, the low-frequency NP voltage ripple can be eliminated at the expense of increasing switching frequencies and thus switching power losses in the converter. Nevertheless, widebandgap devices can be used to mitigate this problem, since switching power losses in those devices are much less significant. Eliminating the low-frequency NP voltage ripples is very important, since it enables the use of thin-film capacitors, which offer capacitances much lower than traditional electrolytic capacitors for the same weight and volume. This has an enormous impact on the reliability of converter, since thin-film capacitors offer a large lifespan, about three times that of electrolytic ones.

## V. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental results were obtained to test the performance of the proposed PD-PWM method based on FPM in a three-phase five-level $2 \times 2$ SMC, as shown in Fig. 12. MATLAB/Simulink and PLECS have been used for the simulation results [30], [31], while the experimental results were obtained from a low-power laboratory prototype using a controller DSPACE 1006 with integrated DS 5203 FPGA board [34]. The parameters of the converter are given in Table III and the hardware prototype is shown in Fig. 11.

Fig. 13 shows results when the converter operates with a linear load $RL$ (see Table III). Fig. 13(a) shows simulation

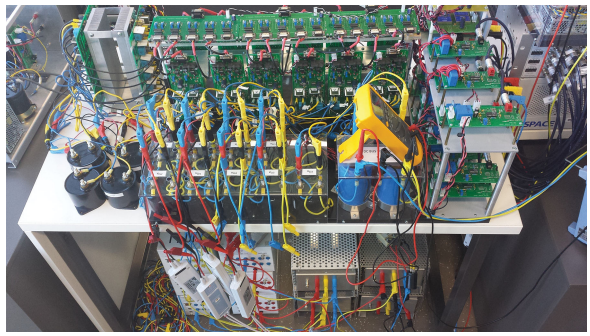

Fig. 11. Hardware prototype of a three-phase five-level $2 \times 2$ SMC.

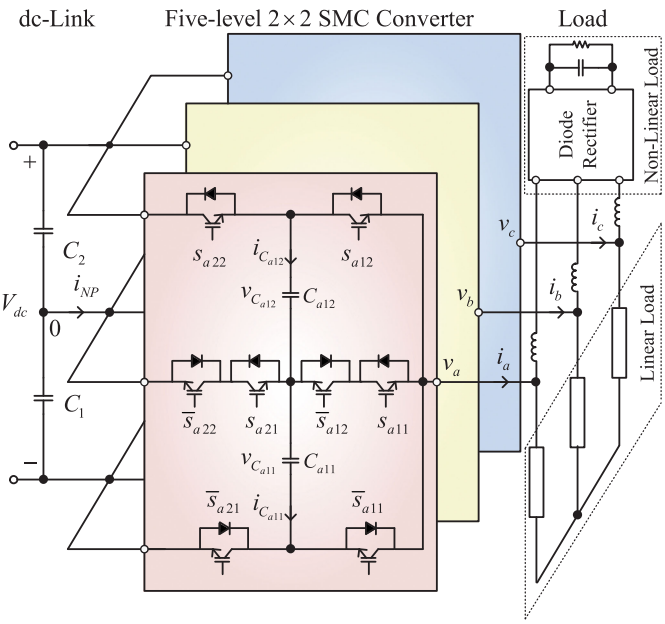


Fig. 12. Three-phase five-level $2 \times 2$ SMC.

TABLE III
SMC PARAMETERS

| Circuit Parameter | Value |
|---|---|
| dc-link voltage, $V_{\rm dc}$ | 100 V |
| dc-link capacitors, $C_1$ and $C_2$ | 23.5 μF |
| FCs, $C_{x11}$ and $C_{x12}$ | 47 μF |
| Linear load, $RL$ | $R = 10\,\Omega$, $L = 10$ mH |
| Nonlinear load | $R = 20\,\Omega$, $C = 1000$ μF |
| (Three-phase rectifier with an $RC$ load) | |
| Carrier frequency, $f_s$ | 10 kHz |
| Fundamental frequency, $f$ | 50 Hz |

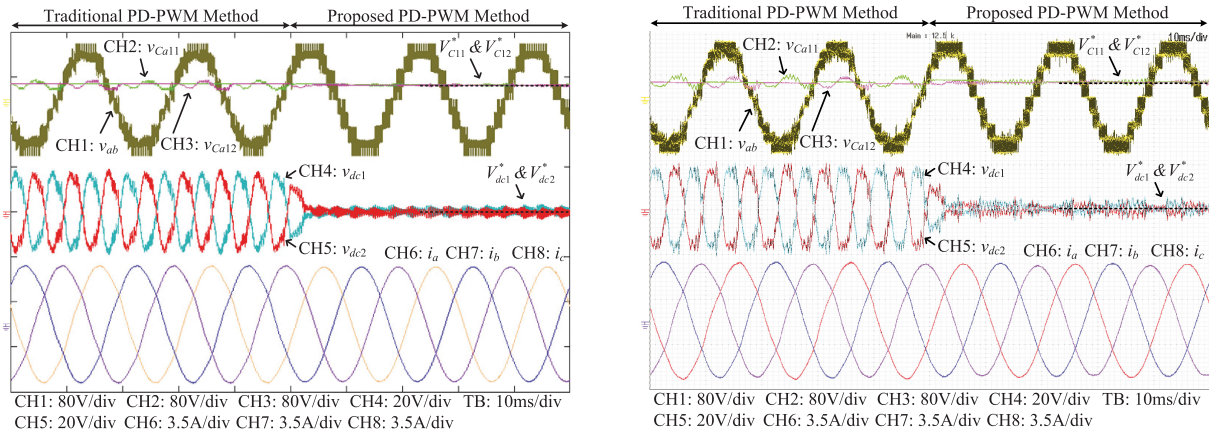


Fig. 13. Comparison between simulation and experimental results of the PD-PWM method [23], [24] with the proposed PD-PWM implementation operating with a linear load. Line-to-line voltage, FC voltages, dc-link voltages, and output currents: (a) simulation and (b) experimental results.

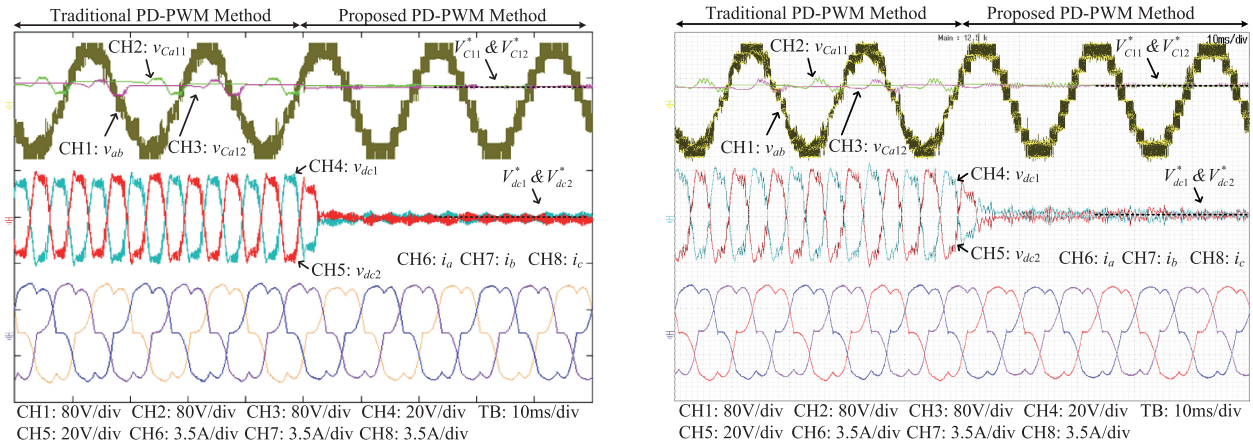


Fig. 14. Comparison between simulation and experimental results of the PD-PWM method [23], [24] with the proposed PD-PWM implementation operating with a nonlinear load. Line-to-line voltage, FC voltages, dc-link voltages, and output currents: (a) simulation and (b) experimental results.

results, while Fig. 13(b) shows experimental results under the same operating conditions. The waveforms presented in Fig. 13 are the line-to-line voltage ($v_{\mathrm{ab}}$), the FC voltages ($v_{\mathrm{Ca\,11}}$ and $v_{\mathrm{Ca\,12}}$), the dc-link voltages ($v_{\mathrm{dc1}}$ and $v_{\mathrm{dc2}}$), and the load currents ($i_a$, $i_b$, and $i_c$). Initially, the converter operates with PD-PWM with a single modulation signal per phase-leg [23], [24]. During this interval, the dc-link capacitors show low-frequency ripples, which produce voltage ripples in the FCs and distortion to the output currents. At $t = 50$ ms, the proposed PD-PWM based on FPM method is applied. As shown, the low-frequency ripples are eliminated from all the capacitors of the converter.

In Fig. 14, the SMC operates with a nonlinear load. Fig. 14(a) shows simulation results, while Fig. 14(b) shows experimental results under the same operating conditions. The load is a three-phase diode rectifier with a capacitor and resistor on the dc side with the values given in Table III. As it can be observed, the proposed method is able to remove the low-frequency voltage ripples completely, while all the capacitor voltages are regulated to their reference values, even when operating with such a strong nonlinear load.

Fig. 15(a) presents experimental THD values of the line-to-line voltages with the proposed PD-PWM method and the traditional PD-PWM [23], [24]. The first 6000 harmonics are considered. The THD values tend to be higher with the proposed method; nevertheless, the distortion is produced at higher frequency than with the traditional method; hence, it can be easily filtered. The WTHD is a better parameter to evaluate the quality of the line-to-line voltages since it considers the order of the harmonics, so that the low-frequency harmonics have more impact than the high-frequency ones. The WTHD is calculated as

$$\mathrm{WTHD} = \frac{\sqrt{\sum_{h=2}^{\infty}\left(\frac{V_h}{h}\right)^2}}{V_1} \times 100 \tag{19}$$

where $V_h$ and $V_1$ are rms values of the harmonic components and the fundamental, respectively.

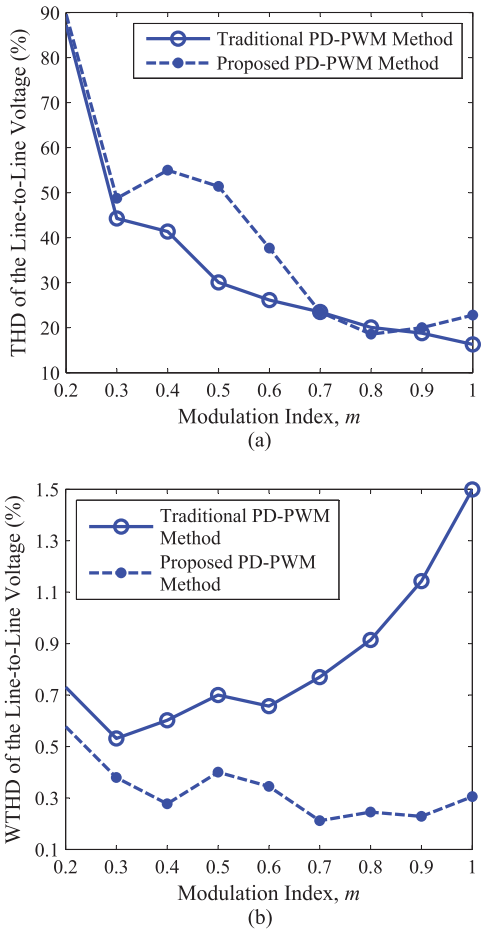


Fig. 15. Evaluation of the line-to-line voltages with the traditional PD-PWM method [23], [24] and the proposed one operating with a linear load (see Table III). (a) THD and (b) WTHD values.

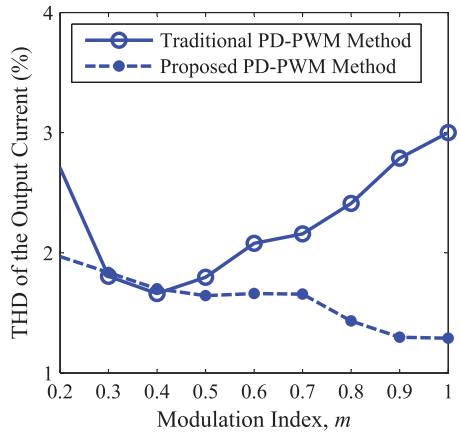


Fig. 16. Output current THD.

Fig. 15(b) shows WTHD values with both modulation methods. The first 6000 harmonics are considered. The proposed PD-PWM method produces voltages with lower WTHD values than the traditional PD-PWM.

Fig. 16 illustrates experimental THD values of the output currents with both modulation methods. The first 6000 harmonics are considered. Again, the proposed PD-PWM method produces less distortion, especially when operating with large modulation indices, which confirms the better quality of the output currents. This is due to the fact that the distortion produced by the proposed PD-PWM is less significant than the one produced with the traditional PD-PWM as a consequence of the low-frequency voltage ripple in the NP. Moreover, the THD of the output currents increases with the modulation index under traditional PD-PWM. This is because the amplitude of the output currents increases with the modulation index, which produces higher low-frequency voltage ripples in the dc-link capacitors and the FCs. As a consequence, the output voltages will contain more low-frequency distortion, which is directly reflected in the THD of the output currents (the inductive load barely filters low-frequency components).

## VI. Conclusion

This paper has proposed an implementation of PD-PWM in SMCs based on the FPM method. When the proposed PD-PWM is applied to a $Y \times 2$ SMC, two extra states appear, which are used for control of the NP voltage. These states are included in a cost function that accounts for deviations of both the NP and FC voltages. The cost function is evaluated to select the optimal redundant states to be used for capacitor voltage balance at any switching period. The proposed PD-PWM method is able to regulate the capacitor voltages to their reference values, and also to remove the low-frequency ripples in all the capacitors of the converter. Consequently, low capacitances can be used, which may lead to a significant reduction in the size of the converter. Moreover, it provides better quality of voltage/output currents (lower WTHD values). This also enables the use of film capacitors, which have a longer lifetime than electrolytic capacitors. Consequently, the life expectancy of the converter would increase significantly by substituting electrolytic capacitors by film capacitors. The method is applicable to converters with NP connection such as the NPC converter and the SMC with two stacks. In this paper, the proposed method has been applied to a five-level $2 \times 2$ SMC, but the method can be extended to SMCs with more cells, i.e., $Y \times 2$ SMCs.

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**Amer M. Y. M. Ghias** (S'10–M'14) received the B.Sc. degree in electrical engineering from Saint Cloud State University, Saint Cloud, MN, USA, in 2001, the M.Eng. degree in telecommunications from the University of Limerick, Limerick, Ireland, in 2006, and the Ph.D. degree in electrical engineering from the University of New South Wales (UNSW), Sydney, Australia, in 2014.

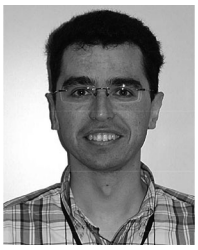
From February 2002 to July 2009, he had held various positions such as Electrical Engineer, Project Engineer, and Project Manager, while working with the top companies in Kuwait. In 2014, he was a Research Associate at the Australian Energy Research Institute, UNSW. He is currently an Assistant Professor in the Department of Electrical and Computer Engineering, University of Sharjah, Sharjah, United Arab Emirates. His research interests include model-predictive control of power electronics converter, hybrid energy storage, fault-tolerant converter, modulations, and voltage-balancing techniques for multilevel converter.

**Josep Pou** (S'97–M'03–SM'13) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Technical University of Catalonia (UPC), Catalonia, Spain, in 1989, 1996, and 2002, respectively.

In 1990, he joined the faculty of UPC as an Assistant Professor, where he became an Associate Professor in 1993. Since February 2013, he has been a Professor with the University of New South Wales (UNSW), Sydney, Australia. From February 2001 to January 2002, and February 2005 to January 2006, he was a Researcher at the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA. From January 2012 to January 2013, he was a Researcher at the Australian Energy Research Institute, UNSW. Since 2006, he has collaborated with TECNALIA Research & Innovation as a Research Consultant. He has authored more than 200 published technical papers and has been involved in several industrial projects and educational programs in the fields of power electronics and systems. His research interests include modulation and control of power converters, multilevel converters, renewable energy generation, energy storage, power quality, and high-voltage direct-current transmission systems.

**Pablo Acuna** (M'12) received the B.S. degree in electronics engineering, the Electronics Engineering Professional degree, and the Ph.D. degree in electrical engineering from the University of Concepción, Concepción, Chile, in 2004, 2007, and 2013 respectively.

He is currently a Research Associate at the Australian Energy Research Institute, School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, Australia. His research interests include electrical power conversion systems and its applications to industry, transportation, and utility.



**Salvador Ceballos** received the M.S. degree in physics from the University of Cantabria, Santander, Spain, in 2001, and the M.S. and Ph.D. degrees in electronic engineering from the University of the Basque Country, Bilbao, Spain, in 2002 and 2008, respectively.

Since 2002, he has been with Tecnalia Research and Innovation, Derio, Spain, where he is currently a Researcher in the Energy and Environment Division. From May 2008 to May 2009, he was a Visiting Researcher at the Hydraulic and Maritime Research Centre, University College Cork, Cork, Ireland. From November 2014 to May 2015, he was a Visiting Researcher at the Australian Energy Research Institute, University of New South Wales, Sydney, Australia. He has authored more than 100 published technical papers. His research interests include multilevel converters, fault-tolerant power electronic topologies, and renewable energy systems.

**Alireza Heidari** (S'12–M'16) received the M.Sc. degree in power engineering from the Iran University of Science and Technology, Tehran, Iran, in 2006. He is currently working toward the Ph.D. degree in power engineering at the University of New South Wales, Sydney, Australia.

From 2006 to 2012, he was with the Faculty of Engineering, University of Zabol, Zabol, Iran. His research interests include power system operation, power system security and reliability, renewable energy resource integration, and application of optimization in power systems.

**Vassilios G. Agelidis** (S'89–M'91–SM'00–F'16) was born in Serres, Greece. He received the B.Eng. degree in electrical engineering from the Democritus University of Thrace, Thrace, Greece, in 1988, the M.S. degree in applied science from Concordia University, Montreal, QC, Canada, in 1992, and the Ph.D. degree in electrical engineering from Curtin University, Perth, Australia, in 1997.

He has worked at Curtin University (1993–1999), University of Glasgow, U.K. (2000–2004), Murdoch University, Perth, Australia (2005–2006), and the University of Sydney, Australia (2007–2010). He is currently the Director of the Australian Energy Research Institute, University of New South Wales, Sydney, Australia.

Dr. Agelidis received the Advanced Research Fellowship from the U.K.'s Engineering and Physical Sciences Research Council in 2004. He was the Vice-President Operations within the IEEE Power Electronics Society from 2006 to 2007. He was an AdCom Member of the IEEE Power Electronics Society from 2007 to 2009 and the Technical Chair of the 39th IEEE Power Electronics Specialists Conference, Rhodes, Greece, 2008.

**Adel Merabet** (M'10) received the M.Sc. degree in automatic and applied computing from École Centrale de Nantes, Nantes, France, in 2002, and the Ph.D. degree in engineering from Université du Québecà Chicoutimi, Canada, in 2007.

He is an Associate Professor, and the Head of the Laboratory of Control Systems and Mechatronics, in the Division of Engineering, Saint Mary's University, Halifax, NS, Canada. His research interests include mechatronics systems, renewable (wind-solar) energy conversion systems, energy management, advanced control systems, and automation.