Design Optimization of Hybrid-Switch Soft-Switching Inverters Using Multiscale Electrothermal Simulation

John Reichl, Jih-Sheng Lai, Allen Hefner, José M. Ortiz-Rodríguez, and Tam Duong

***Abstract*—A multiscale electrothermal simulation approach is presented to optimize the design of a hybrid switch soft-switching inverter using a library of dynamic electrothermal component models parameterized in terms of electrical, structural, and material properties. Individual device area, snubber capacitor, and gate drive timing are used to minimize the total loss of the soft-switching inverter module subject to the design constraints including total device area and minimum on-time consideration. The proposed multiscale electrothermal simulation approach allows for a large number of parametric studies involving multiple design variables to be considered, drastically reducing simulation time. The optimized design is then compared and contrasted with an already existing design from the Virginia Tech Freedom Car Project using the generation II module. It will be shown that the proposed approach improves the baseline design by 16% in loss and reduces the cooling requirements by 42%. Validation of the electrical and thermal device models against measured data is also provided.**

***Index Terms*—Electrothermal effects, inverters, optimization.**

I. Introduction

HISTORICALLY simulating the electrical and thermal characteristics of power electronics circuits in the same simulation has resulted in major challenges with regards to simulation speed and convergence. The reason is because the electrical characteristics of power electronics circuits require very small time constants (<1 μs) to capture the switching behavior of the circuit while the thermal time constant typically requires very long time constants (>1 s) to reach thermal steady state. This presents a significant challenge if electrothermal simulation is to be used to parametrically evaluate multiple design variables with multiple design constraints for design optimization. A decoupling of the thermal and electrical model during the parametric evaluation is necessary without losing the thermal effects of the temperature-dependent electrical parameters. To achieve this, a "multiscale" electrothermal approach is suggested.

This paper describes a multiscale simulation process using electrothermal simulation that can be used to optimize the design of a hybrid switch soft-switching inverter using a library of dynamic electrothermal component models parameterized in terms of electrical, structural, and material properties. The multiscale electrothermal simulation process allows for a large number of parametric studies involving multiple design variables to be simulated in drastically reduced simulation times. As compared to traditional electrothermal simulation, where only junction temperatures of predetermined designs are calculated, the multiscale method proposed in this paper uses electrothermal simulation to guarantee an optimal design, thus truly minimizing cooling requirements and improving device reliability.

Using the proposed multiscale electrothermal approach, a step-by-step design optimization of a two-coupled magnetic hybrid soft-switching inverter is presented. First, the hybrid soft-switch inverter application is described in Section III. Next, the electrothermal device models used in the multiscale electrothermal approach are described along with model validation in Section IV. The design optimization procedure for the hybrid soft-switching inverter using the electrothermal multiscale simulation approach is presented in Section V. Two designs are compared in Section VI. One design utilizes the multiscale electrothermal approach described in Section V and the other design is an already existing design from the Virginia Tech Freedom Car Project using the generation II module. Finally, a full electrothermal simulation of the entire soft-switching inverter is performed in Section VII.

II. Literature Review

A. Electrothermal Model—Electrical

The most widely used method for implementation of the electrical device models is to use lookup tables or curve fits based on loss estimations obtained from a device datasheet [1]–[4]. When using the device lookup tables for determining switching loss, however, the energy curves available have already been averaged over a switching cycle under a specific test condition such as gate drive resistance and voltage. This may be good enough if the device model is used in the same manner such as a hard switching application. However, the energy curves are not valid for conditions where soft-switching techniques or gate drive timing techniques are used to reduce switching loss.

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The electrical portion of the electrothermal models proposed in this paper is based on the physics-based self-heating electrical device models developed by the authors in [5] and [6] with the appropriate temperature-dependent device parameters extracted using the procedures outlined in [7]. Physics-based models lend themselves to design optimization since device parameters such as the chip area are available for parametric study like the authors proposed in [8].

B. Electrothermal Model—Thermal

Fourier series-based thermal models proposed in [9]–[13] are parameterized in terms of structural and material properties but valid only for 1-D or 2-D single chip configurations where there is only a single heat source.

In [14]–[16], a 3-D Fourier series-based thermal model with multiple heat sources and multiple layers with different cross-sectional area is considered. This method is not a full analytical solution to the heat conduction equation and still relies on some numerical solution to determine the Fourier coefficients.

The most widely used method for thermal modeling of multichip power modules involves curve-fitting Foster *RC* cell networks to thermal transient curves from vendor provided data sheet thermal or 3-D finite-element method (FEM) solvers like Kojima *et al.* [17]–[20]. This method faithfully describes a 3-D module and the strong thermal coupling between chips but requires a full 3-D FEM and model extraction for any new module configuration resulting in an extra model synthesis step.

This paper proposes using finite differences methods (FDM), proposed by the authors of this work [21], which offer the most flexibility in representing thermal component models parameterized in terms of structural and material properties that can faithfully represent chip-to-chip thermal coupling for any geometry or dimension.

C. Multiscale Electrothermal Simulations

There are many methods for running electrothermal simulations. Average power loss-based simulations as suggested by the authors of [22] and [23] decouple the instantaneous power from the thermal model by averaging the instantaneous power over a switching cycle. This technique is a “multiscale” approach in that the instantaneous power from a separate analysis with a small time scale is averaged and used with a thermal simulation model with a much larger simulation time step. However, the average dissipated loss is obtained from using datasheet and lookup table methods. In this manner, there is no method for reproducing the instantaneous junction temperature within a switching cycle.

Instantaneous power-loss-based simulations which consider both the small time steps (<1 μs) required by the electrical switching devices and the longer time steps needed for thermal transient (>100 ms) are proposed in [24] and [25]. Iterative approaches are required for arriving to a thermal steady state. These methods are not practical for running multiple simulations for parametric evaluation. The major problem is simulation speed. If only considering short-term high dissipated power effects like short-circuit condition [26] and [27], instantaneous power loss-based simulation is appropriate.

Fig. 1. Phase leg of the coupled-magnetic type soft-switching inverter.

The authors in [28] use a multiscale approach to run the electrical simulation separately from a 3-D thermal FEM simulation tool with the aid of parallel computing. However, this approach would not work for design optimization. It is not possible to couple the 3-D FEM analysis tool into the electrical simulation where the instantaneous power dissipation is a dynamic heat flux.

The multiscale electrothermal approach proposed in this paper uses instantaneous power-based simulations for determination of the design variables that result in the minimized total device loss subject to defined design constraints. Next, average power-based simulations are used to determine the cooling convection coefficients to keep the peak junction temperatures to the operating temperature assumed during the design optimization. Finally, a full electrothermal simulation, using initial conditions from the average power-based simulation, is run to evaluate and check the design performance such as the instantaneous junction temperatures of the device within a switching cycle.

III. Application

A. Inverter Circuit

Fig. 1 shows a couple-magnetic type soft-switching inverter circuit adopting a hybrid switch [29]. The hybrid switch is comprised of a MOSFET in parallel with an insulated-gate bipolar transistor (IGBT). The concept of the hybrid switch in a soft-switching inverter is to have the MOSFET conduct during the beginning of the inverter line cycle where the current is lower and the IGBT to conduct the higher currents within the inverter cycle.

The purpose of the coupled-magnetic is to facilitate the soft-switching action through the auxiliary switch by storing energy in the leakage inductance of the transformer which resonates with the capacitance across the main switch, aligning the hybrid switch with zero volts prior to turn-on resulting in zero voltage switching (ZVS). A two-coupled magnetic approach is adopted to solve the magnetizing current reset problem [30]. A variable timing scheme is adopted to turn-on the hybrid switch

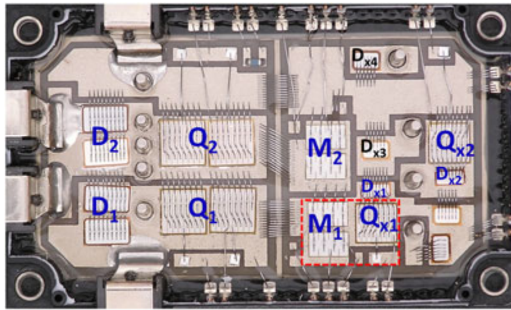

Fig. 2. Generation II soft-switching module components.

TABLE I
THERMAL MODEL DEVICE PARAMETERS

Material units	Thermal conductivity (W/(cm·K))	Density (g/cm^3)	Specific heat (J/g·K)	Thickness (cm)
Silicon	1.56	2.33	0.71	0.0275
AlN	2.17	3.24	1.05	0.0635
Copper	4.01	8.98	0.39	0.0305
Solder	0.57	8.17	0.16	0.162

at the moment the voltage across the switch is detected to be zero [31].

Referring to Fig. 1, each module contains the main switching elements of the inverter circuit made up of IGBTs Q_1 and Q_2 operated in parallel with MOSFETs M_1 and M_2, respectively. Free-wheeling diodes for the main switching elements are also included and designated D_1 and D_2, respectively. In addition to the main switching elements, auxiliary IGBTs Q_{x1} and Q_{x2} and auxiliary diodes D_{x3} and D_{x4} are also included in each module.

B. Packaging

Each module utilizes direct bond copper (DBC) technology where copper is directly bonded to a ceramic substrate such as aluminum nitride, AlN. Fig. 2 shows the module making up the inverter circuit in Fig. 1 for the generation II module.

It is desired to have a compact thermal model parameterized in terms of structural and material properties. Table I shows the material information for each layer of the DBC.

IV. Electrothermal Model Development

A. Electrothermal Model Validation—Electrical

The electrical models used in this paper are based on the physics-based electrical models available in the SABER circuit simulator. The IGBT model is based upon the model developed by Hefner [5]. The diode models are based upon the model developed in [32]. The MOSFET model is based on the model developed in [33] and [34] where the internal MOSFET model within the Hefner IGBT model has been modified for a CoolMOS device.

Table II shows the baseline devices that are used for characterizing devices within the generation II module shown in Fig. 2. The device model parameters are extracted over temperature from the baseline devices in Table II and scaled using the chip area scaling parameter, a_{ref}, to correspond to the actual chip areas used in the generation II module. The MOSFET area for the generation II module is 1.14 cm^2. The main IGBT area is 2.88 cm^2 while the auxiliary IGBT area is 1.16 cm^2. The area for the silicon diode is 1.7 cm^2.

TABLE II
REFERENCE CHIPS FOR PARAMETER EXTRACTION

Chip	Rating	Part number
IGBT	600 V,300 A	CM300DY-12NF
CoolMOS	600 V,60 A	SDB06S60
Si PiN Diode	600 V,150 A	CM300DY-12NF

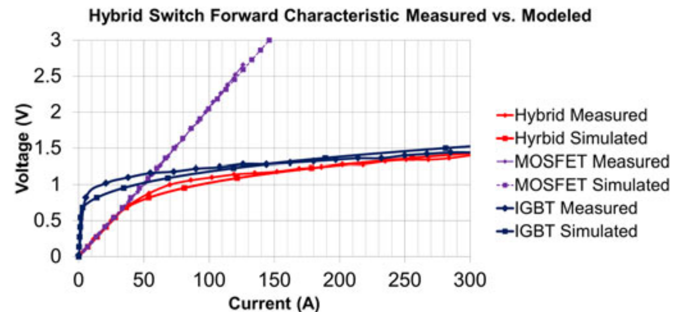

Fig. 3. Hybrid switch on-state characteristic versus measurement.

The resulting IGBT and MOSFET device models are tied in parallel to represent the hybrid switch, and the simulated on-state characteristics have been compared against measurement with the result shown in Fig. 3.

Also shown in Fig. 3 are the individual on-state characteristics of the IGBT and MOSFET along with the resulting combined hybrid switch. The agreement is good indicating that device scaling by using the reference chip area parameter is a valid procedure. This lends itself to a parametric study without having to validate new devices during each parametric evaluation during the design optimization process.

The diode on-state and reverse recovery characteristics as compared to measurement are shown in Fig. 4. The diode on-state model accurately captures the diode on-state across temperature. The reverse recovery characteristic shows good agreement for two different current levels.

A switching characteristic comparing the hybrid switch model versus measurement operating under soft-switching condition at turn-on and the turn-off characteristic of the individual IGBT under two different current levels are shown in Fig. 5. The hybrid switch device voltage (V_{CE}) along with the transformer current (I_{LR}) and device gate voltage (V_{GE}) is shown in Fig. 5(a). The parasitic package stray inductance responsible for the voltage overshoot at turn-off was measured as 21 nH and is included in the model. A gate drive resistance of 6.7 Ω was used for driving the IGBT gate. The turn-off loss of the IGBT is what drives the switching loss of the hybrid switch inverter due to the well-known IGBT turn-off “tail current” which is shown in Fig. 5(b).

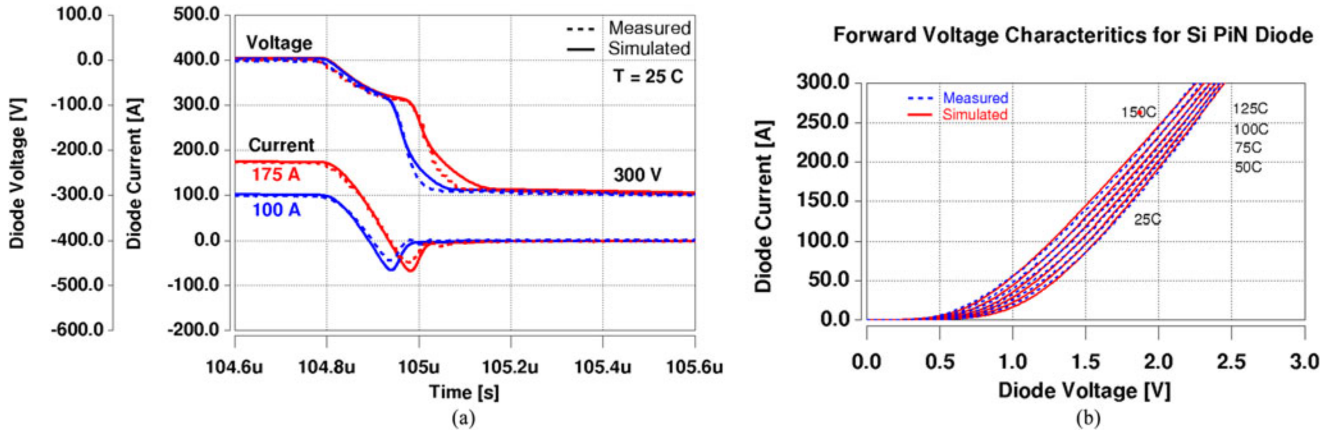

Fig. 4. (a) Diode forward voltage characteristics versus measurement. (b) Diode switching characteristic versus measurement.

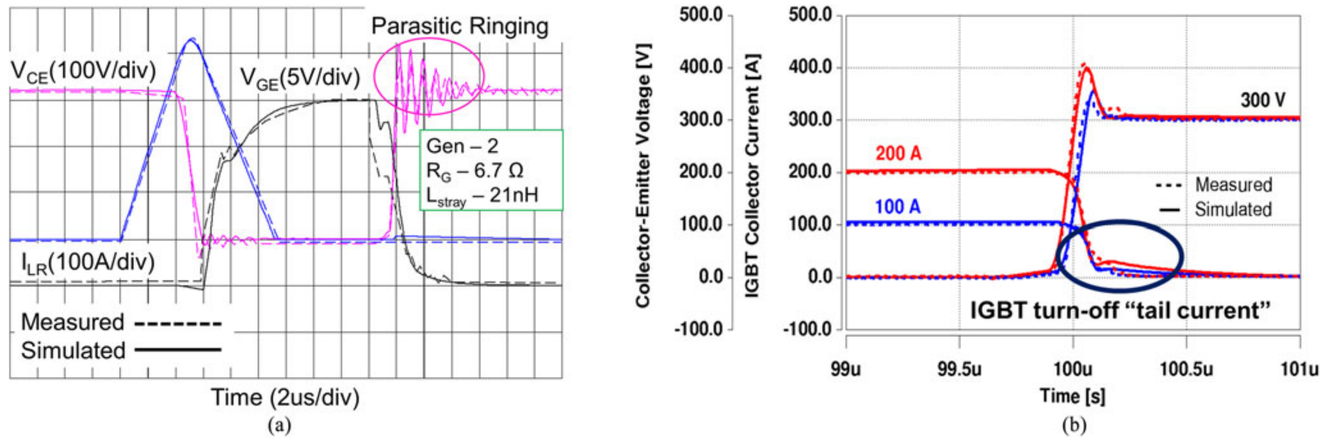

Fig. 5. (a) Hybrid device switching characteristic versus measurement. (b) IGBT turn-off versus measurement.

B. Electrothermal Model Validation—Thermal

The FDM thermal model for the generation II module is validated against measured data generated from a newly developed high-speed double chip temperature-sensitive parameter (TSP) transient measurement. By using the device threshold voltage as a time-dependent TSP, the thermal transient of a single device, along with the thermal coupling effect among nearby devices sharing common (DBC) substrates, can be studied under a variety of pulsed power conditions. Details of this procedure, developed by the authors in this work, can be found in [21].

Referring to the chip references in Fig. 2, Fig. 6 shows the measured junction temperatures obtained from TSP measurement versus the FDM thermal model prediction for various pulse widths of 100 W for $Qx1$. The root mean square error (rmse) is displayed for each power condition. Both the heating and cooling portions of the curves show good agreement thus validating the entire DBC under a variety of conditions.

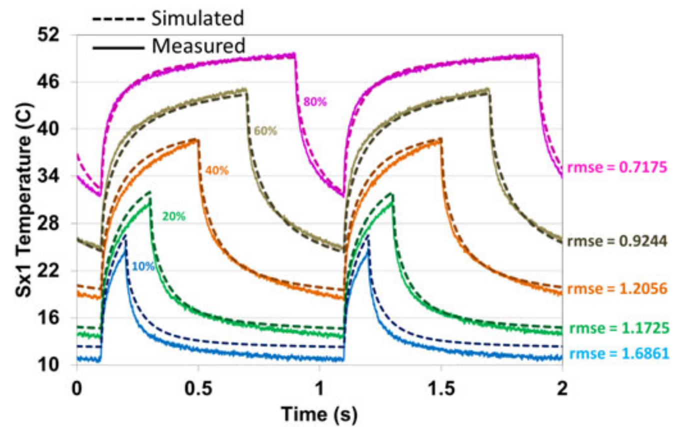

Fig. 6. $Qx1$ transient heating measured versus simulated.

Fig. 7 shows a 3-D FEM transient simulation for each layer within the DBC and is compared against the FDM thermal model. Table III summarizes the rmse of the temperatures at the top of each layer under transient and steady-state condition between the proposed FDM model and FEM analysis. The errors are small validating that the mesh density of the proposed FDM model is adequate. The reason the rmse is smaller when comparing the FDM model to the FEM analysis as compared to the TSP is because the material properties between the FDM and FEM were kept the same. There is no way to know the actual

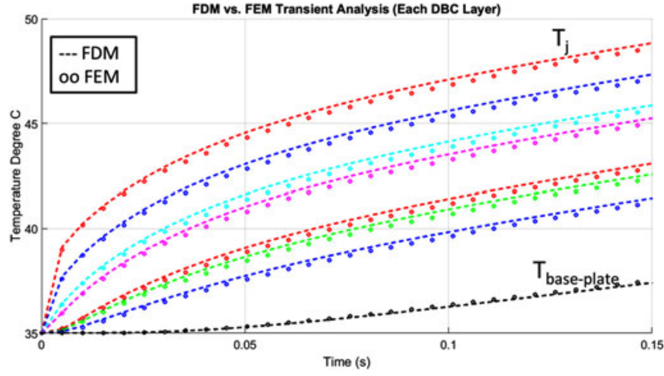

Fig. 7. FDM model versus 3-D FEM.

TABLE III
RMS ERROR TRANSIENT AND STEADY-STATE FDM VERSUS FEM

Layer	Transient RMS error	Steady-state RMS error
Silicon	0.2032	0.0296
Solder	0.2026	0.0325
Copper	0.2013	0.0305
ALN	0.2003	0.0314
Copper	0.1924	0.0315
Solder	0.1894	0.0294
Copper plate-top	0.1821	0.0339
Copper plate-bot	0.0994	0.2357

TABLE IV
DESIGN VARIABLES

Design variable	Independent variable	Symbol
IGBT chip die area	Yes	A_q
MOSFET chip die area	Yes	A_m
Diode chip area	No	A_{diode}
Resonant capacitor	Yes	C_{res}
Transformer primary leakage	No	$L_{\mathrm{lk-pri}}$
Convection coefficient	Yes	h_c

thermal properties of the actual measured module and hence a bigger rmse as seen in Fig. 6.

V. DESIGN OPTIMIZATION PROCEDURE

A. *Design Problem*

The design objective is to minimize the total device loss and cooling requirements of the coupled-magnetic type soft-switching inverter. This is achieved by using the chip area of the IGBT, MOSFET, and diode along with the turn-off snubber capacitor to minimize the total conduction and switching loss. By minimizing the total device loss, the heat that has to be removed from the cooling unit, and thus the convection coefficient, has been minimized.

The design variables considered for the optimum design of the soft-switching module are shown in Table IV. There are four independent variables and two dependent variables. The two dependent variables are determined from two design constraints: the minimum device on-time, and maximum chip area design constraints. Table V shows the design inputs for the soft-switching inverter design considered in this paper.

TABLE V
DESIGN INPUTS

Design input	Symbol	Value
Bus voltage	V_{dc}	280 V
Power	*Power*	61 kW
Power factor	*pf*	0.83
Output voltage	V_{out}	80 $\mathrm{V_{rms}}$
Auxiliary IGBT chip die area	A_{aux}	1.16 cm^2
Sine-triangle SPWM frequency	f_{sw}	20 kHz
Operating junction temperature	$T_{\mathrm{operating}}$	90 °C
Transformer magnetizing inductance	L_M	293 μH
Total device area	A_{max}	5.72 cm^2
Primary turns for coupled magnetic	N_1	14
Secondary turns for coupled magnetics	N_2	19
Cooling temperature	T_α	30 °C

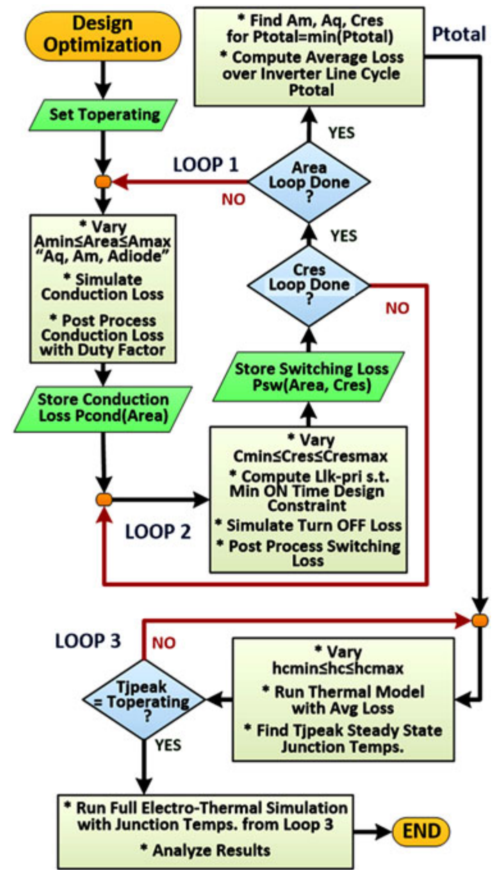

Fig. 8. Optimization process for hybrid switch soft-switching inverter.

B. *Multiscale Electrothermal Simulation Approach*

A multiscale electrothermal simulation approach is proposed to perform the design optimization procedure and is shown in Fig. 8. Three separate simulations designated Loop 1, Loop 2, and Loop 3 in Fig. 8 are used to calculate the conduction loss, switching loss, and peak device junction temperatures, respectively. Each simulation is based on a reduced order circuit such

that multiple parametric evaluations can be performed quickly. For example, calculating conduction loss in Loop 1 does not require full pulse width modulated (PWM) operation of the device models and, conversely, calculating switching loss in Loop 2 only needs to consider turn-off loss since turn-on loss is approximately zero due to soft switching.

The design problem begins with the definition of an operating temperature, $T_{\text{operating}}$. This temperature is defined as the desired operating junction temperature of the devices as determined from a reliability engineer. Loops 1 and 2 are instantaneous power-based simulations and are used to determine the conduction and switching loss as a function of the design variables subject to design constraints. The design resulting in the minimized total loss from Loops 1 and 2 is used in an average power-based electrothermal simulation, Loop 3, to determine the convection coefficient that results in a peak operating junction temperature that is equal to the user-defined operating temperature, $T_{\text{operating}}$. At the conclusion of Loop 3, a full electrothermal simulation of the hybrid switch soft-switching inverter is run where the initial conditions have been determined from Loop 3. Since initial conditions have been established in Loop 3, only one inverter line cycle is necessary to arrive at both the electrical and thermal steady-state saving hours of computation time. The user can analyze the results of the inverter within the switching cycles and, if necessary, revisit the original operating temperature and change if necessary thus repeating the entire optimization process again. The details of each loop are discussed next.

1) Loop 1—Conduction Loss Calculation: The first loop is used to calculate the conduction loss. The chip areas for the MOSFET, IGBT, and DIODE are parametrically varied under the defined operating junction temperature $T_{\text{operating}}$. Loop 1 is subject to the maximum chip area design constraint in (1). The total hybrid device die area $A_{\max}$ is an input set by the designer. This allows the designer to determine how much of the total switch area should be made up of IGBT, MOSFET or DIODE to result in the smallest overall device loss. The total hybrid device die area $A_{\max}$ will be based on the total chip area, not including the auxiliary IGBT, for the generation II module which is 5.72 cm^2

$$A_{\max} = A_{\text{diode}} + A_q + A_m. \tag{1}$$

Fig. 9 shows the design space of the IGBT and MOSFET chip areas as a result of the maximum chip area design constraint. The diode area is calculated from the design space using the constraint in (1).

The conduction loss simulation in Fig. 10 uses a sine-varying current-source representative of the inverter load that conducts through the hybrid switch. The hybrid switch is biased on with a gate drive voltage of 15 V and the on-state voltage v_{main} is measured. The current source also flows through another CoolMOS MOSFET model in parallel with a silicon DIODE to determine the on-state voltage, v_{sync}, as a result of device conduction during the free wheel portion of the switching cycle.

Each device is a four terminal device where three of the terminals represent the traditional electrical connections while the fourth terminal represents the thermal terminal. The electrical terminals have current as through variables and voltage as the across variables. The thermal terminal, tied to the junction temperature, has power as the through variable and temperature as the across variable. For Loop 1 simulation, the thermal terminal is tied to a constant temperature source which is equal to the operating temperature $T_{\text{operating}}$.

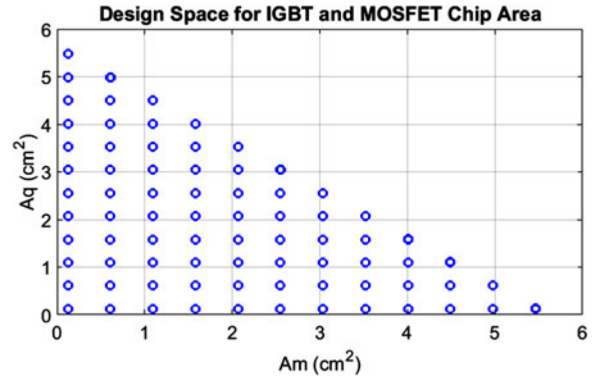

Fig. 9. Design space for IGBT and MOSFET chip area.

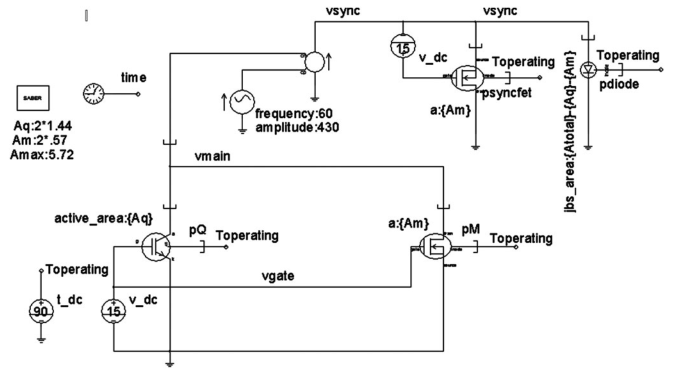

Fig. 10. Loop 1 test circuit.

The resulting on-state voltages from the simulation are postprocessed to take into account the duty cycle variation that would occur in a pulsed width modulated simulation and are given by

$$P_{c-\text{main}} = \frac{1}{2\pi}\int_0^{\pi} v_{\text{main}}(t) I_{\text{peak}} \sin(\omega t) \, [0.5 + 0.5M\sin(\omega t + \phi)]\, d\omega t \tag{2}$$

$$P_{c-\text{free-wheel}} = \frac{1}{2\pi}\int_{\pi}^{2\pi} v_{\text{sync}}(t) I_{\text{peak}} \sin(\omega t) \, [0.5 - 0.5M\sin(\omega t + \phi)]\, d\omega t \tag{3}$$

where I_{peak} is the peak load current, *wt* the inverter line angle, *M* is the modulation index, and φ is the phase shift due to power factor. Postprocessing the on-state voltages in this manner results in a much faster simulation for optimization study since switching of the device models is not necessary to study the optimum conduction loss. The total conduction loss is the sum of (2) and (3) calculated at each chip area within the design space.

$$P_{\text{cond}} = \left.(P_{c-\text{main}} + P_{c-\text{freewheel}})\right|_{A_q, A_m}. \tag{4}$$

2) Loop 2—Switching Loss Calculation: Soft switching allows for the reduction of turn-on loss by aligning the main switch

with zero volts prior to turn on. However, turn-off loss can still be significant due to the IGBT turn-off tail. And this loss is very dominant, especially at higher temperatures where the loss associated with the IGBT turn-off tail is increased. There are several ways to reduce the turn-off loss. One method is to introduce a snubber capacitor which provides an alternate current path so that the IGBT anode voltage rise is slowed, thus resulting in reduced turn-off loss. In addition, since a hybrid switch is being used, the IGBT can be turned off earlier than the MOSFET so that the IGBT turn-off tail current induced loss is minimized. This is assuming that the MOSFET has been adequately sized to support the full load during this time.

A simulation consisting of just the hybrid switch is biased initially on with a constant load current at time zero. The gate drive for the IGBT is removed at time zero followed by the removal of the MOSFET after a time delay, $T_{R\max}$. The chip area is still varied in the same manner as Loop 1 and is subject to the maximum chip area constraint. In addition, a resonant snubber capacitor $c_{\rm res}$ is varied along with load current from zero to full load.

The instantaneous dissipated powers as determined by the device models are integrated over time to determine the switching energy versus load current relationships for chip area and resonant capacitor combination in the design space. The required simulation time, t_f, can be very short (<4 μs) such that all of the parametric sweeps including chip area, snubber capacitor, and load current can finish in minutes. The turn-off energy for each simulation is determined from the integration over time of the dissipated power:

$$E_{\rm off}|_{A_m, A_q, c_{\rm res}, I_{\rm load}} = \int_0^{t_f} p(t)dt. \tag{5}$$

The turn-off energy is calculated versus load current for each chip area and resonant capacitor configuration. These energy versus load current profiles are then postprocessed and curve fit to a fourth-order polynomial. The average dissipated loss of the main switch under inverter operation is then determined from the following equation:

$$P_{\rm sw-main}|_{A_m, A_Q, c_{\rm res}} = \frac{1}{2\pi}\int_0^{\pi} f_{\rm sw}\begin{pmatrix} a_4\left(I_{\rm peak}\sin\omega t\right)^4 \\ +a_3\left(I_{\rm peak}\sin\omega t\right)^3 \\ +a_2\left(I_{\rm peak}\sin\omega t\right)^2 \\ +a_1\left(I_{\rm peak}\sin\omega t\right)^1 \\ +a_0 \end{pmatrix} d\omega t \tag{6}$$

where the coefficients a_0–a_4 are determined through curve fit, and $I_{\rm peak}$ is the maximum load current of an assumed sinusoidal current. The integral in (6) is evaluated using a numerical trapezoidal integration. The total switching loss, including the loss induced in the auxiliary switch, is shown in

$$P_{\rm swtotal}(A_m, A_q, C_{\rm res}) = P_{\rm sw-main}(A_m, A_q, C_{\rm res}) + P_{\rm sw-aux}(C_{\rm res}). \tag{7}$$

All the loss that incurs in the auxiliary switch is due to conduction and occurs during main switch turn on. The turn-on energy of the auxiliary switch can be calculated versus load current for each resonant capacitor configuration using (8) where the resonant relationships are derived in [30]. The auxiliary switch power is calculated after the energy curve profiles are fit to fourth-order polynomials in the same manner as the switching loss using. The auxiliary on-state voltage $v_{\rm saux}$ is determined by performing a one-time forward characteristic simulation using the electrothermal model and curve fitting to a fourth-order polynomial

$$\begin{aligned} E_{\rm auxon}|_{c_{\rm res}, I_{\rm load}} &= \int_{t21} \frac{k^2 V_{\rm dc}}{L_r} t v_{\rm saux}(t)dt \\ &+ \int_{t32} k\left(I_{\rm load} + \frac{\sin(\omega_r t)\, kV_{\rm dc}}{Z_r}\right) v_{\rm saux}(t)dt \\ &+ \int_{t43} k\begin{pmatrix} \frac{kV_{\rm dc}}{Z_r}\sin\left(\cos^{-1}\left(\frac{k-1}{k}\right)\right) \\ +I_{\rm load} - \frac{V_{\rm dc}}{L_r}(1-k)t \end{pmatrix} v_{\rm saux}(t)dt \end{aligned} \tag{8}$$

where

$$\omega_r = \frac{1}{\sqrt{L_r 2C_{\rm res}}} \tag{9}$$

$$k = \frac{N_2}{N_1 + N_2} \tag{10}$$

$$t_{21} = I_{\rm load}\frac{L_r}{kV_{\rm dc}} \tag{11}$$

$$t_{32} = \frac{1}{\omega_r}\cos^{-1}\left(\frac{k-1}{k}\right) \tag{12}$$

$$t_{43} = \left\{\begin{array}{l} \frac{L_r}{Z_r}\left[\begin{array}{l} \pi - \cos^{-1}\left(\frac{N_1}{N_2}\right) + \\ \left(\frac{N_2}{N_1}\right)\sqrt{1-\left(\frac{N_1}{N_2}\right)^2} \end{array}\right] \\ +\frac{L_r}{V_{\rm dcmin}/I_{\rm omax}}\left(2 + \frac{N_1}{N_2} + \frac{N_2}{N_1}\right) \end{array}\right\} - t_{21} - t_{32} \tag{13}$$

$$Z_r = \sqrt{\frac{L_r}{(2C_{\rm res})}} \tag{14}$$

$$L_r = 2L_{\rm lk-pri}\left(\frac{N_2/N_1}{1+N_2/N_1}\right)^2. \tag{15}$$

The dependent variable, $L_{\rm lk-pri}$, is determined from the minimum on time design constraint and has to allow enough time for a proper resonant transition to achieve ZVS and enough time for the coupled magnetics to properly reset [30]. This minimum on time impacts the regulation of the inverter and should be kept to a minimum. Therefore, the minimum on time should be less than 3% of the PWM period. The minimum on-time design constraint was derived in [30] and is given by

$$T_{\rm onmin} = \left(1 + \frac{N_1}{N_1 + N_2}\right) T_{R\max} < 3\% \frac{1}{f_{\rm sw}} \tag{16}$$

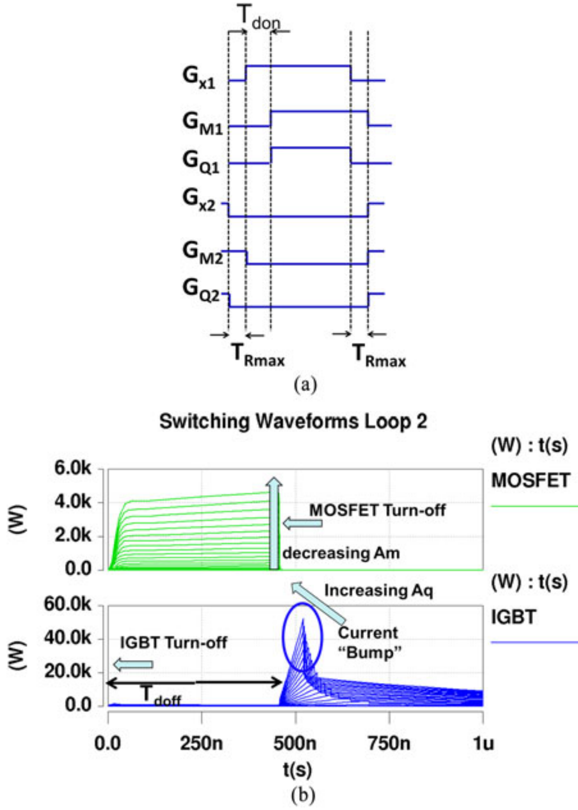

Fig. 11. (a) Gate drive timing diagram. (b) Loop 2 simulation result.

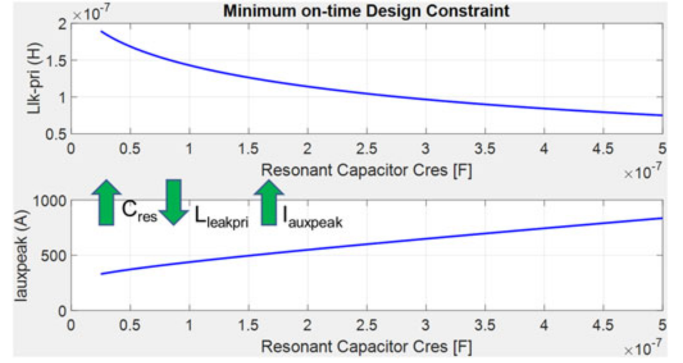

Fig. 12. Primary leakage inductance and auxiliary current versus resonant capacitor.

where the maximum reset time of the coupled magnetic is given by

$$T_{R\max} = \frac{L_m + L_r}{L_m}\frac{N_1}{N_1 + N_2}\left\{\begin{array}{l}\frac{L_r}{Z_r}\left[\begin{array}{l}\pi - \cos^{-1}\left(\frac{N_1}{N_2}\right) + \\ \left(\frac{N_2}{N_1}\right)\sqrt{1 - \left(\frac{N_1}{N_2}\right)^2}\end{array}\right] \\ + \frac{L_r}{V_{\mathrm{dcmin}}/I_{\mathrm{peak}}}\left(2 + \frac{N_1}{N_2} + \frac{N_2}{N_1}\right)\end{array}\right\} \quad (17)$$

where L_m is the transformer magnetizing inductance, and I_{peak} is the maximum peak load current.

In order for this reset time to be achieved and reset every PWM switching cycle, a fixed turn-off delay time equal to the transformer reset time, $T_{R\max}$, between the main switch and the auxiliary switch is required. Fig. 11(a) shows the gate drive timing taking into account the transformer reset condition. The designer can use this delay to reduce the switching loss of the IGBT. If the IGBT is turned off at the same time as the auxiliary switch, the IGBT turn-off tail current induced loss can be minimized. However, this turn-off delay still results in a zero-current window similar to the one described in [35] for zero-current turn-off soft-switching schemes. A tail-current bump is observed if the carriers in the IGBT have not had time to fully recombine and is larger for narrower time durations of $T_{R\max}$, and also larger for higher temperatures. Fig. 11(b) shows the total instantaneous power in Watts for both the IGBT and MOSFET using the proposed gate drive timing scheme as a function of the parametric sweeps of chip area.

The primary leakage inductance-dependent variable, $L_{\mathrm{lk-pri}}$, can be calculated using the minimum on-time design constraint. The relationship is nonlinear, and a Newton–Raphson method is required to solve for the leakage inductance as a function of the resonant capacitor. A design tradeoff exists as the resonant capacitor is varied. Increasing the snubber capacitor, C_{res}, reduces the losses associated with the current tail bump of the IGBT, but results in an increased current stress in the auxiliary switch. The peak current in the auxiliary switch is directly proportional to the resonant surge impedance, Z_r, and is shown next [30]

$$I_{\mathrm{auxpeak}} = \frac{N_2}{N_1 + N_2}\left(I_{\mathrm{peak}} + \frac{N_2}{N_1 + N_2}\frac{V_{\mathrm{dc}}}{Z_r}\right). \quad (18)$$

In order to illustrate the design tradeoffs, Fig. 12 shows the leakage inductor versus resonant capacitor to maintain the minimum on-time design constraint, and also shown is the peak auxiliary current.

It can be seen that the required resonant inductor becomes smaller as the resonant capacitor increases. This results in an increased peak auxiliary current. As the peak current increases in the auxiliary IGBT, the device begins to enter the active region of operation where the voltage drop is significantly increased. Not only does this increased voltage drop increase the conduction loss of the auxiliary switch resulting in possible thermal failure, it also reduces the amount of voltage available to charge the leakage inductance, resulting in reduced energy available for soft switching of the main switch.

3) Loop 3—Convection Coefficient: The final loop involves optimizing the cooling system. Since it has already been designed for minimum loss, this implies that the cooling system has been optimized because the amount of dissipated power as heat has been minimized. The convection coefficient, h_c, is a variable and will be adjusted until the peak junction temperature during steady state has reached the operating temperature assumed by the design optimization, $T_{\mathrm{operating}}$.

The power from Loop 1 and the energy curves mapped to power dissipations from Loop 2 are averaged over a switching period and implemented as power sources into the thermal model for each device. Therefore, Loop 3 is an average power-based simulation.

TABLE VI
OPTIMIZED DESIGN VARIABLES

Design variable	Value
A_m	4.56 cm^2
A_q	1.04 cm^2
$A_{\rm diode}$	0.1 cm^2
$C_{\rm res}$	37.5 nF
$L_{\rm lk-pri}$	178 nH
$T_{\rm doff}$	450 ns

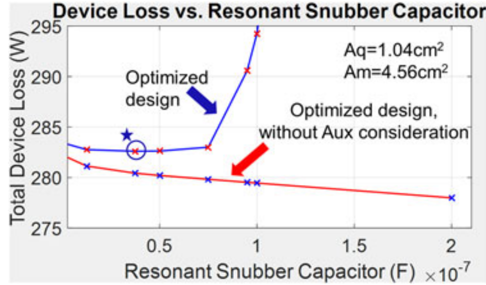

Fig. 13. Total loss versus resonant capacitor for two design points.

The thermal models are based on finite differences programmed in the SABER MAST language and are parameterized in terms of structural and material geometry for any 1–3 D configuration [21]. A convection boundary condition is forced at the bottom of the copper baseplate layer. The assumed liquid cooling temperature is 30 °C. The convection boundary condition is implemented with a finite difference equation and connects to the bottom nodes of the DBC.

VI. DESIGN OPTIMIZATION RESULTS AND DISCUSSION

The total loss from Loops 1 and 2 are summed together per the flow diagram in Fig. 8

$$P_{\rm total}(A_m, A_q, C_{\rm res}) = P_{\rm swtotal}(A_m, A_q, C_{\rm res}) + P_{\rm cond}(A_m, A_q). \quad (19)$$

The design variables that minimize the total device loss while meeting the two design constraints using the procedures outlined in Section V are summarized in Table VI.

Fig. 13 shows the total loss at the optimal design points for the chip area as a function of $C_{\rm res}$, and the result if the auxiliary chip loss is not considered. In the optimized design with auxiliary chip consideration, the total losses start to increase at a resonant capacitor value of 100 nF. The reason for this is because a larger capacitor, while reducing the turn-off loss in the IGBT, results in a larger peak auxiliary current as shown in Fig. 12. The auxiliary losses start to dominate as a result of forced active region conduction. If either the auxiliary chip loss is not considered or if the auxiliary chip is made large enough to avoid entering the active region of operation, the IGBT turn-off loss would continue to decrease with increased snubber capacitor.

Fig. 14 shows the total loss at the optimal design point for the resonant capacitor $C_{\rm res}$ as a function of A_q and A_m. Fig. 15 shows a breakdown of conduction loss and switching loss. The results indicate that if one was only considering conduction loss, the IGBT wants to be the bigger area as compared to the MOSFET. This makes sense since the R_{dson} of the MOSFET increases with temperature, and the threshold voltage for the IGBT decreases with temperature. However, there is a big penalty to pay for switching loss at high temperature for the IGBT.

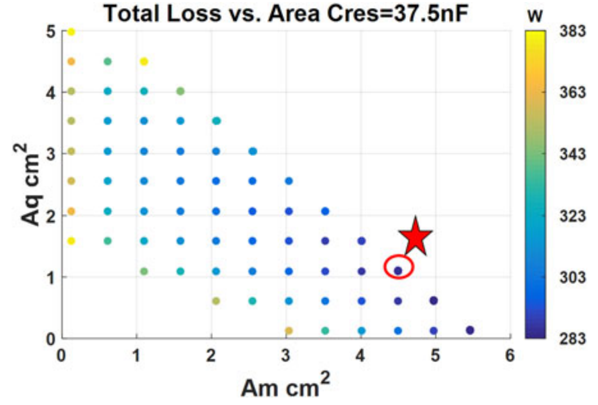

Fig. 14. Total loss versus chip area ($C_{\rm res} = 37.5$ nF)

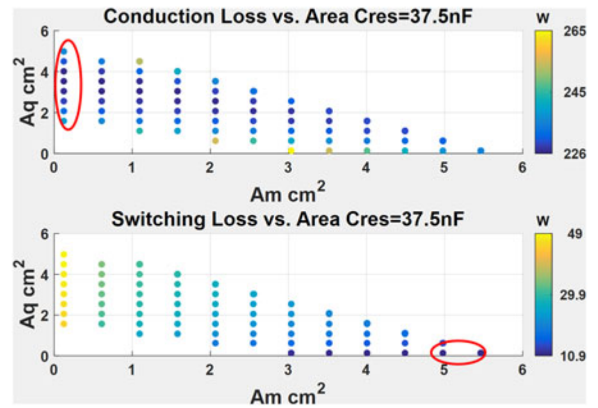

Fig. 15. Conduction loss versus switching loss ($C_{\rm res} = 37.5$ nF).

TABLE VII
COMPARISON BASELINE DESIGN AND PROPOSED OPTIMIZED DESIGN

Design variables	Optimized	Base-line Gen 2
$C_{\rm res}$	37.5 nF	100 nF
A_M	4.56 cm^2	1.14 cm^2
A_Q	1.04 cm^2	2.88 cm^2
$L_{\rm lk-pri}$	178 nH	168 nH
$A_{\rm diode}$	0.1 cm^2	1.7 cm^2
$A_{\rm aux}$	1.16 cm^2	1.16 cm^2
$T_{d-\rm off}$	450 ns	450 ns
h_c	25 000 W/cm^2/°C	43 000 W/cm^2/°C
IGBT loss $P_{\rm SW}$	25 W	94 W
IGBT loss $P_{\rm Cond}$	47 W	137 W
MOSFET loss $P_{\rm SW}$	3 W	9.5 W
MOSFET loss $P_{\rm Cond}$	200 W	38 W
Aux-IGBT loss	2 W	2.4 W
Diode loss	5 W	53 W
Total loss	**282 W**	**334 W**

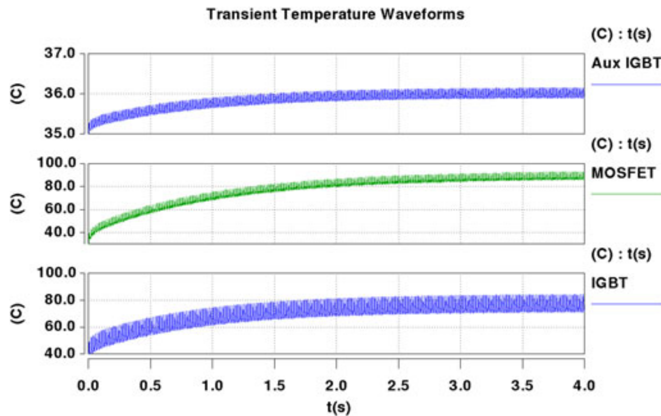

Fig. 16. Loop 3 transient response.

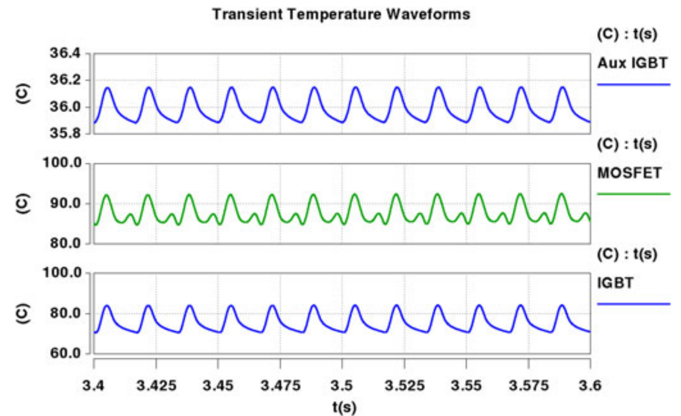

Fig. 17. Loop 3 steady-state response.

Table VII shows a design comparison with the baseline generation II soft-switching module and the proposed optimized design. The results show an improvement in total loss over the current generation II design of almost 16%. The total chip area remained the same, but an additional 52 W was saved by reallocating the individual device areas. In addition, the baseline design required a heating coefficient 42% higher than the optimized proposed design to keep the peak device junction temperature, in this case the IGBT, to the operating temperature of 90 °C. The baseline design results in a "hotspot," since the IGBT incurs a larger percentage of the loss, thus driving the cooling requirements. The new proposed design distributes the heat better reducing the required cooling coefficient.

In the baseline design, most of the losses were due to conduction in the IGBT, but due to the amount of current in the IGBT, the turn-off loss of the IGBT was much higher than the proposed optimized design. In the proposed design, most of the loss is due to conduction in the MOSFET. And since the MOSFET conducts most of the current, there is less turn-off loss in the IGBT where the savings are noticed.

Since the results indicate that a larger MOSFET chip area is required, the proposed multiscale electrothermal approach could easily consider an IGBT which is more optimized for switching loss rather than conduction. This paper used an IGBT which is more optimal for conduction loss and, as indicated by the optimization results, shows there is potential for even further design optimization if a different IGBT is considered. However, that is beyond the scope of this paper. This paper describes a process for optimizing a hybrid switch soft-switching inverter using electrothermal simulation so the designer can easily consider different device technologies using the procedures described in this paper. Also important is operating temperature as determined from the reliability engineer. A lower operating temperature would result in a larger percentage of IGBT area.

Fig. 16 shows the transient response for the IGBT, MOSFET, and auxiliary junction temperatures from the Loop 3 average power-based simulation. It takes almost 4 s to reach steady state. By averaging the dissipated power over the switching period, it is not unreasonable to run a simulation this long with a full FDM model. The cooling coefficient was adjusted so the peak junction temperature observed at the hottest, in this case the MOSFET, operating under steady state is equal to the operating temperature $T_{\text{operating}}$. As shown in the figure, the MOSFET conducts during the main and free-wheel portions as evident by the small temperature rise when the IGBT is cooling. Fig. 17 shows the temperatures zoomed in during steady state.

VII. Full Electrothermal Simulation

Now that the optimum design has been reached and the convection coefficient has been determined to maintain the operating junction temperature of the inverter, $T_{\text{operating}}$, a full electrothermal simulation in which the instantaneous dissipated power and temperature within a switching cycle is available for analysis. The full electrothermal device models with corresponding thermal networks are run with a sine varying current source to represent the load.

Since the simulation takes much longer due to the required small time step to adequately represent the switching waveforms, initial conditions can be used to bring the inverter to steady-state temperature within one inverter line cycle. This is done by using the results obtained from the Loop 3 simulation. The average steady-state temperature is determined and used as an initial condition in the full electrothermal simulation. This allows only a few inverter cycles ($<$100 ms) to reach steady state compared to the Loop 3 simulation which required 4 s of simulation time to reach steady state.

Fig. 18 shows the steady-state MOSFET and IGBT average temperatures operating at the designed operating temperature, $T_{\text{operating}}$. Large temperature spikes occur within the IGBT. They represent the energy dissipated at turn off of the IGBT. This is due to the tail current loss, which has been minimized using the time delay between the MOSFET and IGBT. It is noted that these temperature spikes do not occur during the turn on since the devices turn on under zero-voltage switching condition.

To observe the effects of energy leading to dissipated power within the switching cycle, Fig. 19 shows the IGBT energy along with temperature and MOSFET gate voltage for reference during one switching cycle. It is observed that there is no increase in energy incurred at turn on further validating that the device is operating under soft-switching condition. Turn off shows the

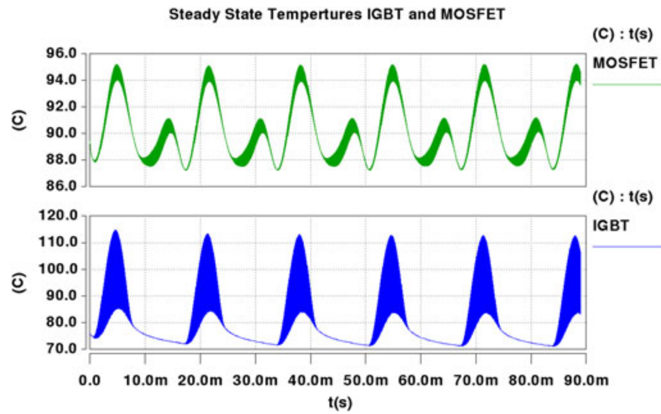

Fig. 18. Steady-state temperatures IGBT and MOSFET.

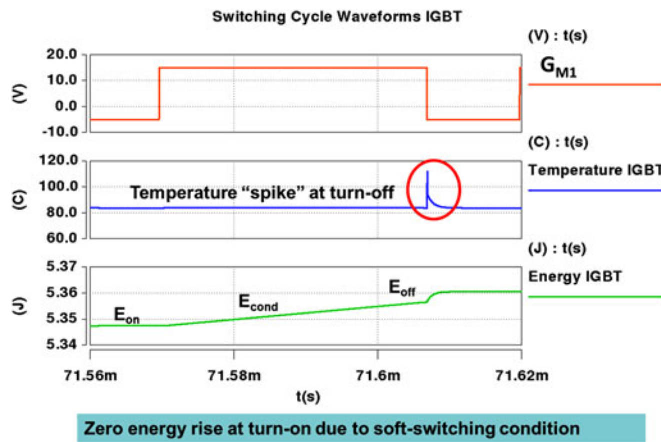

Fig. 19. Electrothermal waveforms within switching cycle—IGBT.

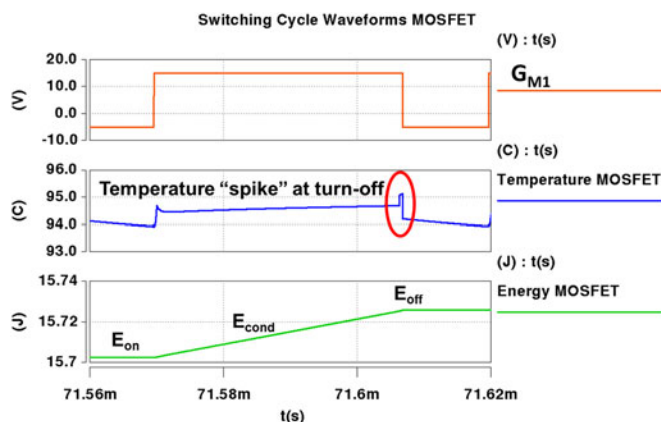

Fig. 20. Electrothermal waveforms within switching cycle—MOSFET.

large increase in energy due to the turn-off tail induced loss leading to the temperature spikes seen in Fig. 19.

Fig. 20 shows the energy profile for the MOSFET along with the MOSFET gate voltage for reference during one switching cycle. As expected, there is no energy rise at turn-on due to ZVS. There is a small increase in the energy observed at turn-off resulting from the MOSFET having to conduct the full-load current when the MOSFET was turned off prior to the IGBT. Both sets of waveforms show the energy rise during conduction.

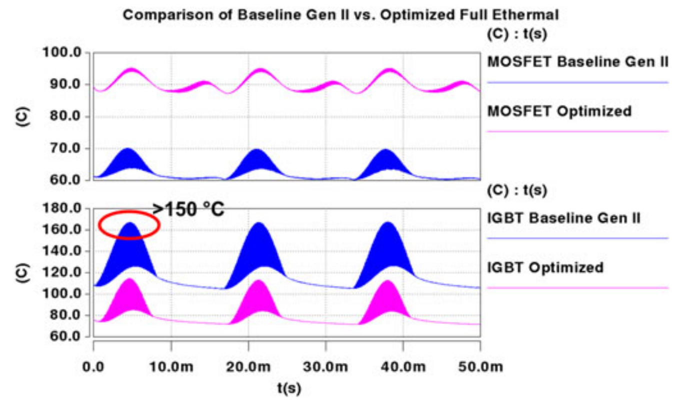

Fig. 21. Comparison of Baseline Gen II versus Optimized Design—full electrothermal.

As a comparison between the optimized and baseline designs, a full electrothermal simulation of the baseline design is run with the required cooling coefficient, 25 000 W/cm^2/°C, from the proposed optimized design. The device junction temperatures for both designs are plotted and shown in Fig. 21. The baseline IGBT temperature is much higher than the proposed optimized design and the peak temperature comes close to exceeding the maximum junction temperature rating. Therefore, better cooling would be required for the baseline design leading to higher system cost. While the MOSFET of the baseline design runs cooler, the heat distribution of the baseline design is poor since all the heat is dissipated in the IGBT.

VIII. Conclusion

This paper proposed a multiscale approach for design optimization of a hybrid switch soft-switching inverter using electrothermal simulation. The multiscale approach uses a library of dynamic electrothermal component models parameterized in terms of electrical, structural, and material properties making parametric evaluations for design optimization possible.

The optimized design using the proposed multiscale electrothermal approach was compared to an existing soft-switching module design from the generation II freedom car module from Virginia Tech. The result was a 16% improvement in device loss, and a 42% reduction in required cooling convection coefficient. Finally, a full electrothermal simulation was run to steady state in just one inverter line cycle by using the results of the Loop 3 analysis as an initial condition for the simulation. This enables the designer to study both the instantaneous junction temperature and dissipated power within a switching cycle at thermal steady state in a fraction of time.

In conclusion, this paper pulled every aspect of electrothermal modeling together creating a process whereby the engineer can gain valuable insight early on in the design phase. No longer is electrothermal simulation just used to predict temperatures, but now as a way to make valuable recommendations to the engineer in a very reasonable amount of time.

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