Avoiding Divergent Oscillation of a Cascode GaN Device Under High-Current Turn-Off Condition

Xiucheng Huang, *Student Member, IEEE*, Weijing Du, Fred C. Lee, *Life Fellow, IEEE*, Qiang Li, *Member, IEEE*, and Wenli Zhang

***Abstract*—The cascode structure is widely used for high-voltage normally-on GaN devices. However, the capacitance mismatch between the high-voltage GaN device and the low-voltage normally-off Si MOSFET may induce several undesired features, such as Si MOSFET reaches avalanche during turn-off and the high-voltage GaN device loses zero-voltage switching turn-on condition internally during a soft-switching turn-on process in every switching cycle. This paper presents another issue associated with the capacitance mismatch in the cascode GaN devices. Divergent oscillation could occur at high-current turn-off condition and, eventually, destroys the device. The intrinsic reason of this phenomenon is analyzed in detail in this paper. A simple solution is proposed by adding an additional capacitor whose position is critical and should be optimized. Experimental results validate the theoretical analysis and show that the proposed method improves device performance significantly under high-current turn-off condition.**

***Index Terms*—Avalanche, capacitance mismatch, cascode, divergent oscillation, gallium nitride device.**

I. Introduction

HIGH efficiency and high power density are always being pursued rigorously in advanced power conversions for all forms of consumer electronics. High switching frequency is the major catalyst for size reduction, but it is seemly at the detriment of efficiency when using silicon-based devices. The emerging gallium nitride (GaN) power devices have a much lower gate charge and lower output junction capacitance than silicon MOSFETs and, therefore, are capable of operating the switching frequency ten times higher. GaN devices seem to be the game-changing devices in the applications such as point-of-load converters, offline switching power supplies, battery charger, and motor drives [1]–[8]. To realize the benefits of GaN devices resulting from significantly higher operating frequency, a number of issues have to be addressed, such as converter topology, magnetics, control, packaging, and thermal management.

Manuscript received November 26, 2015; revised January 21, 2016; accepted February 14, 2016. Date of publication February 19, 2016; date of current version September 16, 2016. This work was supported by the U.S. Department of Energy, Office of Energy Efficiency and Renewable Energy, under the project of High-Efficiency High-Density GaN-Based 6.6-kW Bidirectional On-board Chargers for PEVs, through Delta Products Corp. This work was also supported in part by the Power Management Consortium in CPES, Virginia Tech. Recommended for publication by Associate Editor A. Lindemann.

The authors are with the Center for Power Electronics Systems, The Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA (e-mail: xiucheng@vt.edu; weijing@vt.edu; fclee@vt.edu; lqvt@vt.edu; wzhang11@vt.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2532799

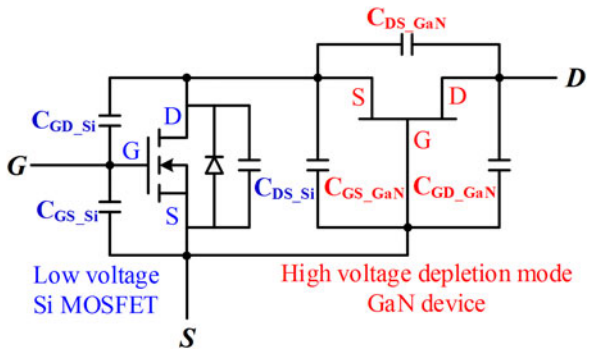


Fig. 1. Cascode structure for a high-voltage depletion-mode GaN device with all junction capacitances.

The high-voltage GaN devices can be categorized into two types: enhancement mode and depletion mode. One of the desirable features for enhancement-mode GaN devices is gate overdrive protection. The recommended gate drive voltage is close to the breakdown voltage, which requires dedicated driving circuit design to avoid device failure. For depletion-mode GaN devices, a low-voltage Si MOSFET is typically connected in series to control the ON–OFF state of high-voltage GaN device, which is well known as a cascode structure and is shown in Fig. 1 with all junction capacitors been marked [9]. The external driving circuit is simple with sufficient margin. The evaluations and applications of cascode GaN have been studied in the literature [10]–[23]. Compared to the enhancement-mode GaN devices, the cascode GaN devices have smaller turn-off loss at higher current condition due to intrinsic current-source turn-off mechanism [14], [15]. This feature makes cascode GaN devices very attractive in pulse-width-modulation converter with high turn-off current applications, such as totem-pole bridgeless PFC [6], [21].

In the cascode configuration, interaction between the two devices may result in instability due to the large package parasitic inductance [24]. An advanced package method, such as chip-on-chip technique, can dramatically reduce the package inductance and avoid instability [10], [23]. On the other hand, junction capacitances of the two devices also play an important role in the dynamic performance of the cascode device. The capacitance charge of high-voltage GaN device is typically larger than that of the low-voltage silicon MOSFET. Capacitance mismatch between the high-voltage GaN and the low-voltage Si MOSFET may induce several undesired features, such as Si MOSFET reaches avalanche during turn-off transition in every switching cycle, and the high-voltage GaN switch loses zero-voltage

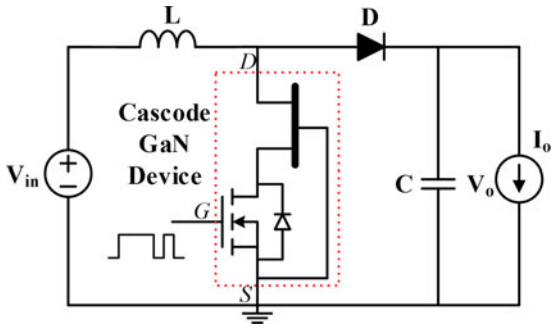


Fig. 2. Boost converter with a cascode GaN device.

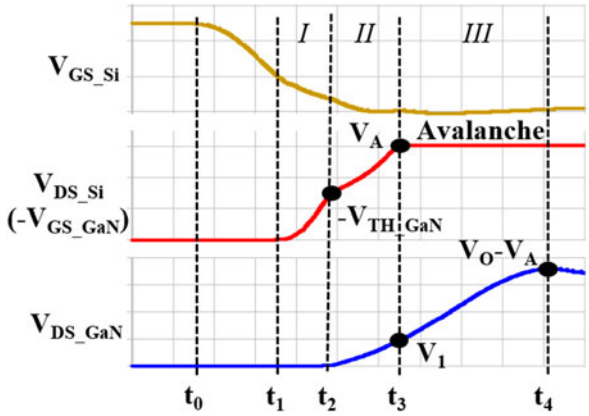


Fig. 3. Voltage waveforms of a cascode GaN device during turn-off transition period.

switching (ZVS) turn-on internally even when a ZVS technique is applied [22]. These issues can be solved by adding an additional capacitor in parallel with the drain–source terminals of Si MOSFET to compensate the capacitance mismatch [22]. This solution may slightly increase the turn-off switching loss, but, in general, the switching loss is negligible due to intrinsic current-source turn-off mechanism.

This paper presents another issue related to the capacitance mismatch in the cascode GaN devices, which would cause device and circuit failure. The parasitic ringing during turn-off transition may trigger the GaN device to internally turn ON at high-current condition. The parasitic resonant impedance network changes when GaN is turned ON, and it absorbs more energy from source. The resonant amplitude gradually increases and becomes divergent oscillation. This phenomenon may result in the cascode GaN device and other circuit components failure. This failure mode can be theoretically avoided by the same method proposed in the literature [22]. However, the packaging of the additional capacitor is critical to the failure. The detailed illustration of the divergent oscillation is presented in Section II. The analysis of different packaging impacts on the failure mode is presented in Section III. Finally, the theoretical analysis is validated by experimental results shown in Section IV. It is worthwhile to point out that the theoretical analysis and the proposed solution are applicable to all kinds of cascode devices.

II. Analysis of Divergent Oscillation Issue

To better understand the divergent oscillation issue, Si MOSFET avalanche and GaN internally turn-on mechanism in the cascode device with capacitance mismatch should be briefly reviewed first. A boost converter is used as an example, which is shown in Fig. 2. The bottom switch is the cascode GaN device.

A. Si MOSFET Avalanche and GaN Internally Turn-On Mechanism in the Cascode Structure [22]

The key waveforms of Si MOSFET reaching avalanche during turn-off transition is shown in Fig. 3 and the simplified equivalent circuits are shown in Fig. 4. The turn-off signal is applied at t_0, and $C_{\mathrm{OSS\_Si}}$ and $C_{\mathrm{GS\_GaN}}$ are charged up in parallel by turn-off current flowing through the channel of GaN until GaN is pinched off at t_2 when $V_{\mathrm{DS\_Si}}$ which is also $V_{\mathrm{GS\_GaN}}$ with inverse polarity reaches $-V_{\mathrm{TH\_GaN}}$. During stage II (t_2–t_3),

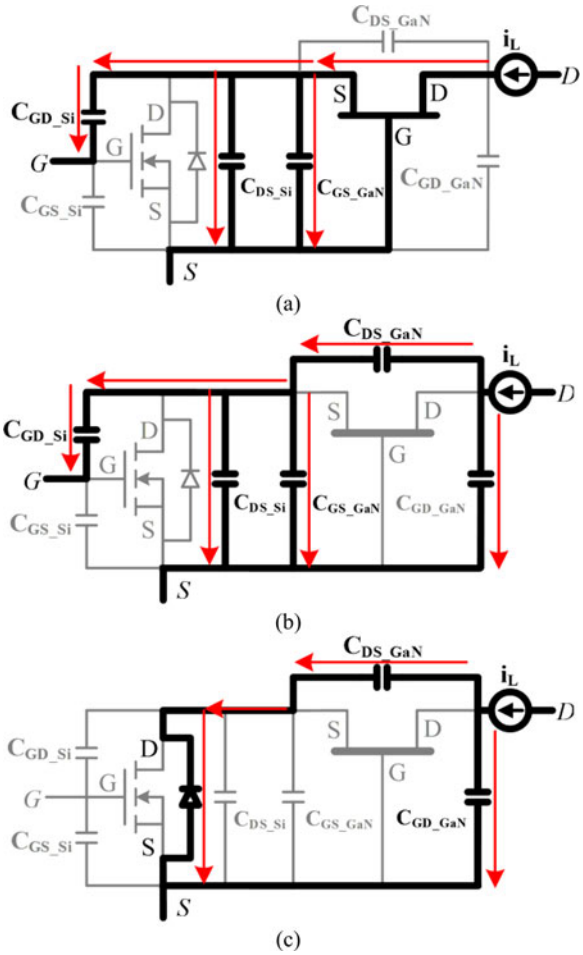


Fig. 4. Equivalent circuit of turn-off transition period. (a) Stage I: t_1–t_2. (b) Stage II: t_2–t_3. (c) Stage III: t_3–t_4.

$C_{\mathrm{DS\_GaN}}$ is charged in series with $C_{\mathrm{OSS\_Si}}$ and $C_{\mathrm{GS\_GaN}}$. When $V_{\mathrm{DS\_Si}}$ is driven to avalanche voltage V_{A} at t_3, $V_{\mathrm{DS\_GaN}}$ only rises up to V_1, which is lower than its steady-state voltage $V_{\mathrm{O}} - V_{\mathrm{A}}$. The amount of charge stored in $C_{\mathrm{DS\_GaN}}$ during t_2–t_3 is defined as $\mathrm{Q_{II}}$, which is the same with the charge stored

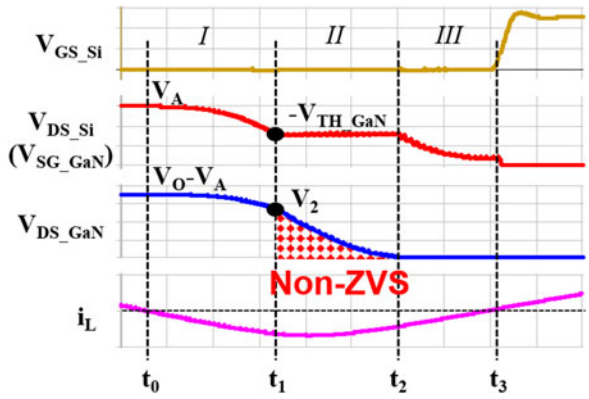


Fig. 5. Voltage waveforms of a cascode device during ZVS turn-on transition period.

in $C_{\mathrm{OSS\_Si}}$ and $C_{\mathrm{GS\_GaN}}$. After t_3, Si MOSFET stays in the avalanche status. $C_{\mathrm{DS\_GaN}}$ is charged through the avalanche path independently and the amount of charge during stage III is defined as mismatched charge $\mathrm{Q_{III}}$. This amount of charge flows through the avalanche path, and it causes additional loss which is proportional to the mismatch charge, switching frequency, and avalanche voltage.

The ZVS turn-on transition is the reverse process of turn-off transition. The key waveforms are shown in Fig. 5 and the equivalent circuits are shown in Fig. 6. During t_0–t_1, $C_{\mathrm{DS\_GaN}}$ is discharged in series with $C_{\mathrm{OSS\_Si}}$ and $C_{\mathrm{GS\_GaN}}$. When $V_{\mathrm{DS\_Si}}$ decreases to $V_{\mathrm{TH\_GaN}}$ at t_1, $V_{\mathrm{DS\_GaN}}$ only decreases to V_2. Total charge being discharged during this period is $\mathrm{Q_{II}}$, which is exactly the same as the charge stored during stage II of the turn-off process. After t_1, the GaN switch is triggered to turn ON internally, and remaining charge $\mathrm{Q_{III}}$ is dissipated through the channel directly. After all the charge been dissipated, the remaining external current continues to discharge $C_{\mathrm{OSS\_Si}}$ and $C_{\mathrm{GS\_GaN}}$ to almost 0 V. The waveform of $V_{\mathrm{DS\_GaN}}$ makes the terminal waveform of the cascode GaN device appear to have ZVS turn-on. However, the majority of the energy stored in $C_{\mathrm{DS\_GaN}}$ is actually dissipated internally due to a mismatch in charge. This phenomenon always occurs, regardless of what kind of ZVS techniques are applied. The internal switching loss is related to the mismatch charge and switching frequency.

B. Divergent Oscillation Issue of the Cascode GaN Device Under High-Current Turn-Off Condition

The Si MOSFET avalanche and GaN internal switching loss may increase the additional loss significantly. The divergent oscillation caused by the capacitance mismatch may be fatal to the device and circuit. The key waveforms of divergent oscillation are shown in Fig. 7 and the simplified equivalent circuits are shown in Fig. 8.

The turn-off process is the same as mentioned above in Section II-A. After Si MOSFET reaches avalanche, $V_{\mathrm{DS\_GaN}}$ is charged up to V_{peak}, and turn-off transition is over. Junction capacitance resonates with L_{P} and the initial voltage of $V_{\mathrm{DS\_GaN}}$ and $V_{\mathrm{DS\_Si}}$ is V_{peak} and V_{A}, respectively. The initial

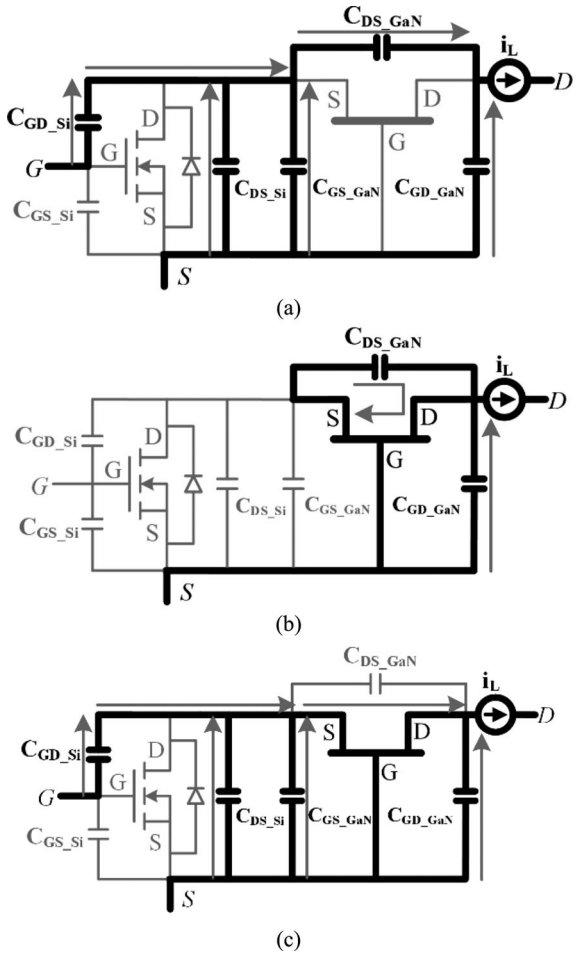


Fig. 6. Equivalent circuit of ZVS turn-on transition period (a) Stage I: t_0–t_1. (b) Stage II: t_1–t_2. (c) Stage III: t_2–t_3.

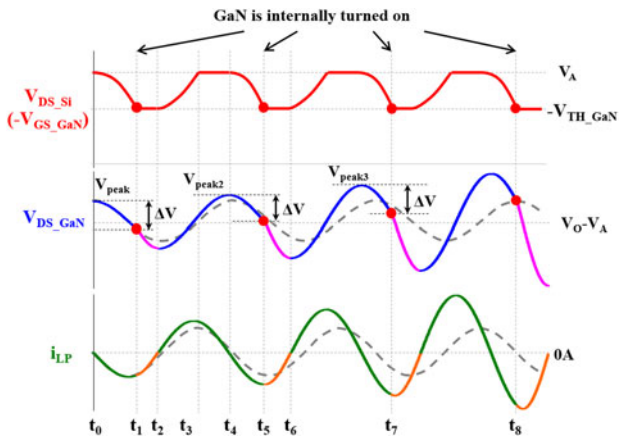


Fig. 7. Key waveforms of divergent oscillation during ringing period after the cascode GaN device been turned OFF.

oscillation current of L_{P} is 0 A. Ideal oscillation waveforms are the dash lines shown in Fig. 7. Detailed operation are described as follows:

[t_0–t_1]: L_{P} resonates with two capacitance branches. Branch I is $C_{\mathrm{DS\_GaN}}$ in series with $C_{\mathrm{OSS\_Si}}$ and $C_{\mathrm{GS\_GaN}}$. An equivalent

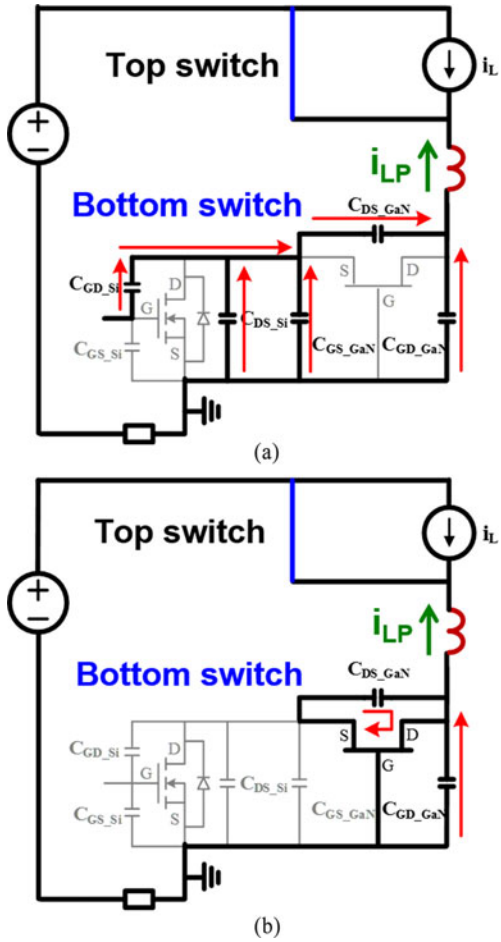


Fig. 8. Equivalent oscillation circuit during ringing period. (a) t_0–t_1 equivalent circuit. (b) t_1–t_2 equivalent circuit.

capacitance value of this branch $C_{\rm equ}$ is shown in (1). Branch II is $C_{\rm GD\_GaN}$. The equivalent circuit of this period is shown in Fig. 8(a). $C_{\rm DS\_GaN}$ is discharged in series with $C_{\rm OSS\_Si}$ and $C_{\rm GS\_GaN}$ by part of the loop inductance current $i_{\rm LP}$ during this stage, and very similar to stage I of the ZVS turn-on process shown in Fig. 6(a). State equations of this period are shown in (2), in which $V_{\rm DS}$ is the drain–source terminal voltage of bottom switch and $R_{\rm L}$ is the total loop resistance including on-resistance of top switch and current shunt. With large enough ringing amplitude, at t_1 instant, $V_{\rm DS\_Si}$ reaches $-V_{\rm TH\_GaN}$, while $V_{\rm DS\_GaN}$ only drops ΔV, which is smaller than the ideal resonant peak–peak amplitude. The charge removed in capacitance branch I during this stage is $\rm Q_{II}$, which is the same charge stored during stage II of the turn-off process mentioned above

$$C_{\rm equ}=\frac{(C_{\rm OSS\_Si}+C_{\rm GS\_GaN})\cdot C_{\rm DS\_GaN}}{C_{\rm OSS\_Si}+C_{\rm GS\_GaN}+C_{\rm DS\_GaN}} \tag{1}$$

$$\begin{cases}(C_{\rm equ}+C_{\rm GD\_GaN})\cdot\dfrac{dV_{\rm DS}}{dt}=i_{\rm LP}\\ V_{\rm in}-L_{\rm P}\cdot\dfrac{di_{\rm LP}}{dt}-i_{\rm LP}\cdot R_L=V_{\rm DS}\\ V_{\rm DS}=V_{\rm GD\_GaN}.\end{cases} \tag{2}$$

[t_1–t_2]: After t_1, GaN is internally turned ON and $C_{\rm DS\_GaN}$ is bypassed by the GaN channel directly. Therefore, the loop inductance $L_{\rm P}$ only resonates with branch II $C_{\rm GD\_GaN}$ and the resonant structure changes to Fig. 8(b). State equations of this period are shown in (3). The resonant period reduces due to smaller capacitance, and characteristic impedance becomes larger. With the same current and voltage initial conditions at t_1, larger characteristic impedance means larger resonant amplitude of capacitance voltage. So, the voltage drop of $V_{\rm DS}$ increases compared with an ideal case. $V_{\rm GS\_GaN}$ remains almost constant during this stage with the same reason described in [22]. Although $C_{\rm DS\_GaN}$ does not participate in oscillation during [t_1–t_2], $V_{\rm DS\_GaN}$ and $V_{\rm GD\_GaN}$ still satisfy the Kirchhoff voltage law, which is shown in (4). Therefore, at t_2, $i_{\rm LP}$ reaches 0 A, and $V_{\rm DS\_GaN}$ reaches the valley point, which is lower than the ideal case

$$\begin{cases}C_{\rm GD\_GaN}\cdot\dfrac{dV_{\rm DS}}{dt}=i_{\rm LP}\\ V_{\rm in}-L_{\rm P}\cdot\dfrac{di_{\rm LP}}{dt}-i_{\rm LP}\cdot R_{\rm L}=V_{\rm DS}\end{cases} \tag{3}$$

$$V_{\rm DS\_GaN}=V_{\rm GD\_GaN}-|V_{\rm TH\_GaN}|=V_{\rm DS}-|V_{\rm TH\_GaN}|. \tag{4}$$

[t_2–t_3]: After t_2, the next oscillation period starts. The values of $V_{\rm DS\_Si}$, $V_{\rm DS\_GaN}$, and $i_{\rm LP}$ at t_2 instant become the initial conditions of the next oscillation cycle. $V_{\rm DS\_Si}$ reaches avalanche at t_3, and the charge stored in $C_{\rm DS\_GaN}$ during this period is $\rm Q_{II}$, which is the same as the charge removed during [t_0–t_1].

[t_3–t_4]: $V_{\rm DS\_Si}$ stays in the avalanche region and $V_{\rm DS\_GaN}$ continues increasing to the second peak value $V_{\rm peak2}$. $V_{\rm peak2}$ should be larger than $V_{\rm peak}$, and the resonant current also increases due to lower voltage initial condition.

[t_4–t_5]: This stage is similar to stage [t_0–t_1]. $V_{\rm DS\_Si}$ and $V_{\rm DS\_GaN}$ decrease simultaneously, and $V_{\rm DS\_Si}$ reaches $-V_{\rm TH\_GaN}$ when $\rm Q_{II}$ is removed by resonant current at t_5. GaN is internally turned ON again and relatively earlier than stage [t_0–t_1] due to higher resonant current.

[t_5–t_6]: The resonant structure changes to Fig. 8(b) again. Higher resonant current amplitude results in even lower valley voltage of $V_{\rm DS\_GaN}$ at t_6.

In the following oscillation periods, GaN is internally turned ON in every oscillation cycle and each turn-on instant moves earlier compared to previous cycle. The ringing amplitude of $V_{\rm DS\_GaN}$ and $i_{\rm LP}$ increase cycle by cycle due to resonant structure change, and the oscillation eventually becomes divergent.

III. Effective Solution to Avoid Divergent Oscillation for Cascode GaN Devices

Based on the analysis above, the fundamental reason of the divergent oscillation issue is the capacitance mismatch between Si MOSFET and GaN in the cascode configuration. It is triggered by parasitic ringing at certain amplitude, which is determined by turn-off current, loop inductance, and junction capacitance.

One way to avoid the divergent oscillation is to parallel *RC* snubber circuit to suppress the voltage spike and damp the

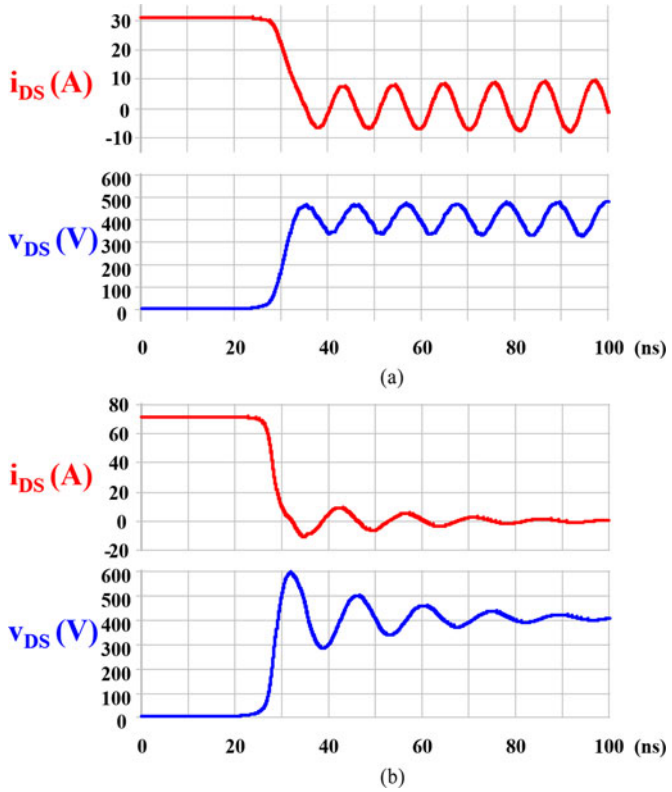


Fig. 9. Comparison of simulated results under high-current turn-off condition. (a) Divergent oscillation @ 30 A without *RC* snubber circuit. (b) Turn-off current = 70 A with *RC* snubber circuit ($R = 7.5\ \Omega$, $C = 100$ pF).

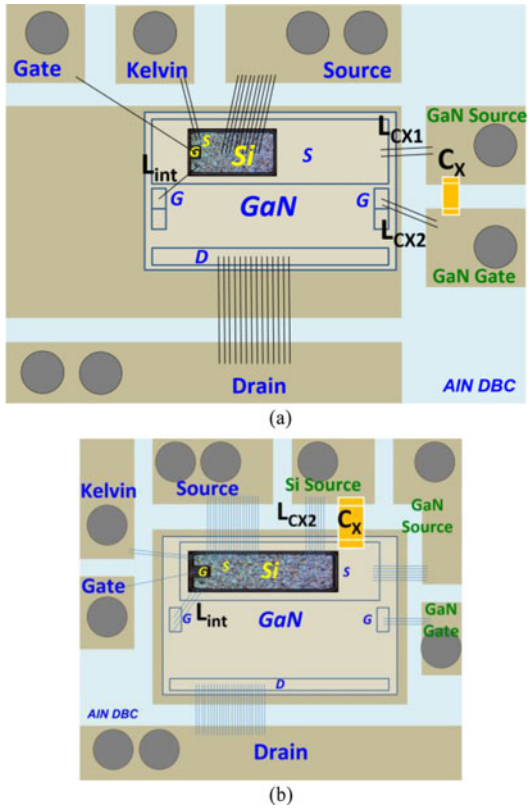


Fig. 10. Two possible packaging approach with C_{X}.

parasitic ringing, which is a common practice for devices switching at high current. Comparison of the simulation results is shown in Fig. 9. The cascode GaN device simulation model is provided by Transphorm. It is obvious that the divergent oscillation occurs at 31 A without an *RC* snubber circuit, while the devices can safely switch 70 A and above with an *RC* snubber circuit. The power dissipation on the *RC* snubber circuit is around 10 μJ, which is acceptable for the switching frequency lower than few hundreds of kilohertz.

The power dissipation becomes significant at megahertz frequency range, which requires bulky resistance. Moreover, the Si MOSFET avalanche and GaN internal switching loss cannot be solved by adding snubber circuit, which also induce significant loss at high frequency.

A fundamental solution to compensate the capacitance mismatch by adding an additional capacitor C_{X} is proposed in the literature [22]. The Si MOSFET avalanche and GaN internal switching loss can be effectively eliminated. This method will not increase the driving loss and only has very little impact on the turn-off loss. As mentioned in Section II-A, the total mismatched charge in the cascode device is $\mathrm{Q_{III}}$. The required minimum value of C_{X} should satisfy the expression as shown below:

$$C_{\mathrm{X}} \geq \frac{\mathrm{Q_{III}}}{V_{\mathrm{A}} - V_{\mathrm{TH\_GaN}}}. \tag{5}$$

Ideally, $V_{\mathrm{SG\_GaN}}$ is equal to V_{CX} as well as $V_{\mathrm{DS\_Si}}$ after capacitance compensation. However, integrating C_{X} in the cascode package always creates parasitic inductance, which induces parasitic ringing internally. The parasitic inductance and the position of C_{X} are critical to achieve optimal performance. Fig. 10 shows two possible packaging diagrams, which integrate the capacitor C_{X}.

The Si MOSFET is on top of GaN switch source pad in order to reduce interconnect parasitic inductance. The C_{X} is on side of GaN switch in packaging A and on top of GaN switch source pad in packaging B, respectively. As shown in the diagram of packaging A, one terminal of the external capacitor C_{X} is connected to the GaN source pad through L_{CX1}. The other terminal is connected to one of the GaN switch gate pad through wire bonding, and then connected to the source pad of Si MOSFET through the other gate pad of GaN switch for easy wire bonding consideration. L_{CX2} is consisted of two parts: one is the wire between C_{X} and gate pad, and the other is the two gate connection inside the GaN switch. Actually, the packaging A is used to demonstrate the benefits of the proposed solution in the literature [22]. In packaging B, one terminal of C_{X} is connected directly to the source pad of GaN switch, and the other terminal is connected to the source pad of Si MOSFET through L_{CX2}. The equivalent circuit considering the parasitic inductance is shown in Fig. 11. The parasitic inductances of these two packaging approaches are listed in Table I, which are derived based on Ansoft Q3D FEA simulation. It shows that packaging B has smaller parasitic inductance.

It is noticed that $V_{\mathrm{SG\_GaN}}$ is the sum of $V_{\mathrm{DS\_Si}}$ and $V_{L\mathrm{int}}$, which is the voltage across L_{int}. Therefore, the parasitic ringing

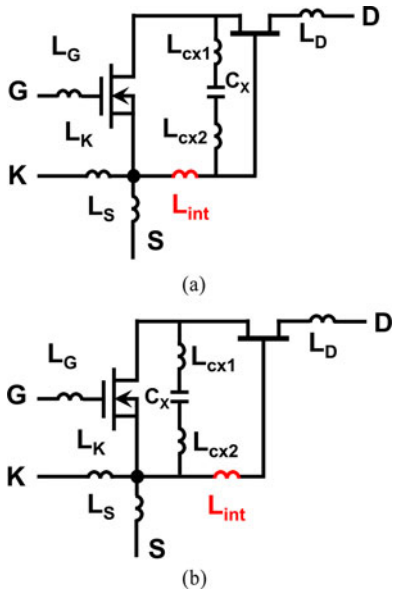


Fig. 11. Equivalent circuit of two different packaging approaches. (a) Packaging A. (b) Packaging B.

TABLE I
PARASITIC INDUCTANCE OF DIFFERENT PACKAGING

	Packaging A	Packaging B
$L_{\rm int}$	1.0 nH	1.0 nH
$L_{\rm CX1}$	1.0 nH	N/A
$L_{\rm CX2}$	2.1 nH	1.0 nH

on $V_{\rm SG\_GaN}$ can be significantly reduced by minimizing $V_{L\rm int}$. The amplitude of $V_{L\rm int}$ is determined by the current flowing through $L_{\rm int}$. The two packages put $C_{\rm X}$ in different positions and, therefore, result in different current flowing through the $L_{\rm int}$. In packaging A, $C_{\rm X}$ is on the right side of $L_{\rm int}$. During turn-off transition, $i_{\rm off\_1}$ and $i_{\rm off\_2}$ flow through $L_{\rm int}$, which is shown in Fig. 12(a). $i_{\rm off\_1}$ is the turn-off current flowing through $C_{\rm GD\_GaN}$ and $C_{\rm GS\_GaN}$.$i_{\rm off\_2}$ is the current charging $C_{\rm X}$. $i_{\rm off\_3}$ is the current flowing through Si MOSFET branch. The amplitudes of three current are determined by impedance. The $C_{\rm X}$ value is typically much larger than any other junction capacitance; therefore, $i_{\rm off\_2}$ is much higher than $i_{\rm off\_3}$. It is worthwhile to point out that $C_{\rm DS\_GaN}$ is typically much larger than $C_{\rm GD\_GaN}$ at high voltage range due to the nonlinear characteristic of GaN junction capacitances. As a result, $i_{\rm off\_2}$ is also much larger than $i_{\rm off\_1}$. In packaging B, $C_{\rm X}$ is on the left side of $L_{\rm int}$. Only $i_{\rm off\_1}$ flows through $L_{\rm int}$ during turn-off period, while $i_{\rm off\_2}$ directly flow to the source of Si MOSFET. An equivalent circuit is shown in Fig. 12(b). It is obvious that packaging B reduces the current flowing through $L_{\rm int}$, which induces less voltage drop $V_{L\rm int}$.

Moreover, smaller parasitic inductance also helps to reduce the current flowing through $L_{\rm int}$. As mentioned above, the current distributions of $i_{\rm off\_1}$, $i_{\rm off\_2}$, and $i_{\rm off\_3}$ are determined by impedance. In the packaging B approach, minimizing $C_{\rm X}$ and $L_{\rm CX2}$ branch impedance increases $i_{\rm off\_2}$ and reduces $i_{\rm off\_1}$. As a result, $V_{L\rm int}$ is further reduced by inductance reduction.

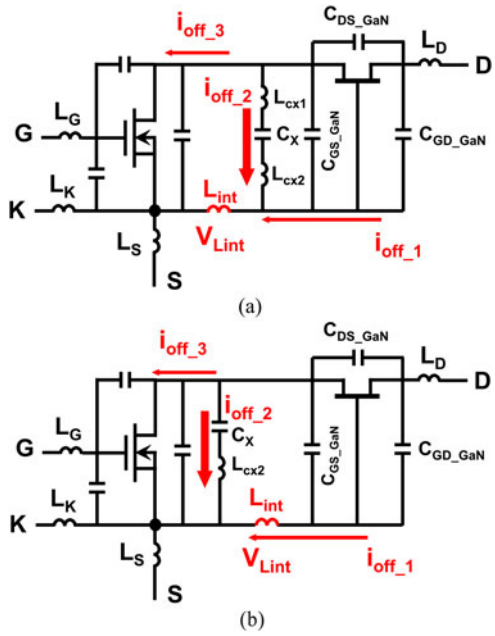


Fig. 12. Current distribution in different packaging. (a) Packaging A. (b) Packaging B.

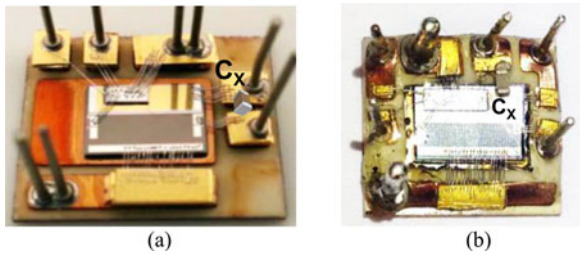


Fig. 13. Prototypes of two different packaging approaches.

Overall, packaging B bypasses the majority of turn-off current by good position and small parasitic inductance. Smaller $V_{L\rm int}$ results in smaller resonant amplitude in the GaN gate loop, and as a result, $V_{\rm GS\_GaN}$ is far from touching turn-on threshold value, which is the trigger of divergent oscillation. The packaging B approach is preferred for cascode GaN operating at high current turn-off condition.

IV. EXPERIMENT VALIDATION AND DISCUSSION

To validate the analysis of divergent oscillation and the proposed solution for cascode GaN device, two cascode GaN devices are fabricated with the two packaging diagram mentioned in Section III, as shown in Fig. 13. The 600 V normally-on GaN switch with 35 A continuous current capability is provided by Transphorm Inc. The threshold voltage is around -20 V and the maximum source-gate voltage is around -40 V. Therefore a 30 V Si MOSFET is selected to control the on/off state of the GaN as well as to protect the GaN gate by clamping the source-gate voltage of the GaN to the avalanche value of the Si MOSFET, which is 30 V. Another criterion for choosing the Si MOSFET is to minimize the driving loss at high frequency. Therefore the junction capacitance of this 30 V Si MOSFET is usually much smaller than the GaN switch. The estimated mismatch charge

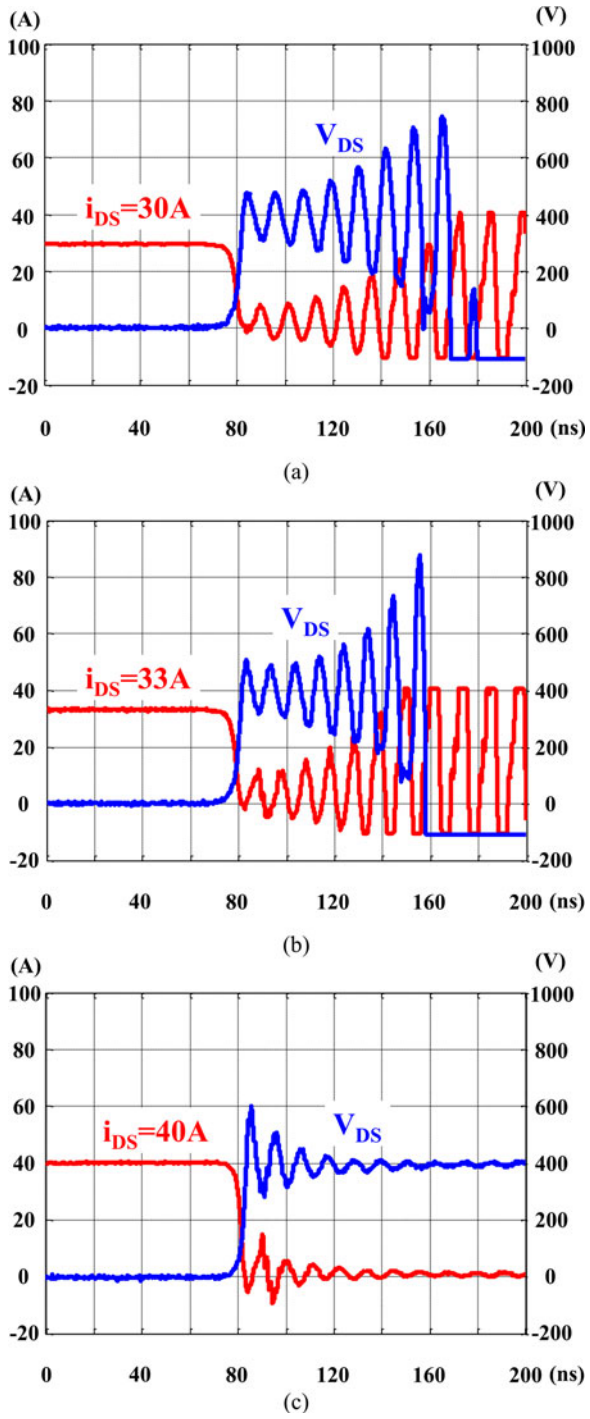


Fig. 14. Experimental results with different packaging approaches. (a) Packaging A and B without C_X. (b) Packaging A with C_X. (c) Packaging B with C_X.

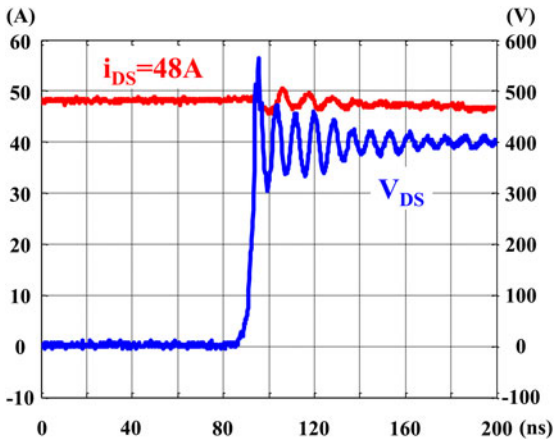


Fig. 15. Experiment with packaging B, without shunt resistance.

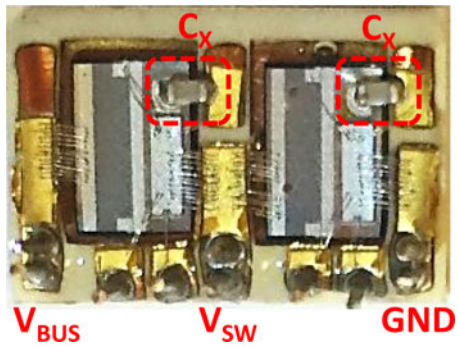


Fig. 16. Half-bridge module of cascode GaN devices with the packaging B approach.

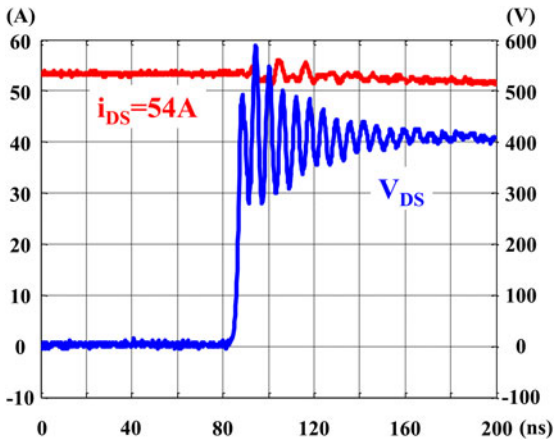


Fig. 17. Experiment with the half-bridge module of cascode GaN devices with the packaging B approach.

is about 33 nC, and therefore, a 3.6 nF capacitor is added according to (5).

The Si MOSFET avoids avalanche and the GaN switch achieves true ZVS with the additional capacitor. The experimental verification will not be repeated here. The evaluation of high-current turn-off condition is carried on double-pulse-test circuit. Input voltage is 400 V. Fig. 14 shows the experimental waveforms of different packaging approaches. Fig. 14(a) shows that packaging A and B without C_X causes divergent oscillation at 30-A turn-off condition. The packaging A with C_X can switch to slightly higher turn-off current, but it still causes divergent oscillation at 33 A turn-off condition as shown in Fig. 14(b). The major reason is the position of C_X as mentioned in Section III. The prototype using the packaging B approach can successfully switch under 40 A turn-off condition without oscillation as shown in Fig. 14(c).

It is noticed that the voltage spike is close to 600 V due to relatively large power loop inductance in order to accommodate the shunt resistance (SSDN-10, T&M Research Products Inc.) on the PCB board. The turn-off current can go up to 48 A by removing the shunt resistance, as shown in Fig. 15. The red curve is the inductor current. The parasitic ringing period reduces from 12 to 8.5 ns based on Figs. 14(c) and 15. It indicates about 50% reduction in the power loop inductance by removing the shunt resistance. The voltage spike is about 570 V.

In order to further reduce the power loop inductance, a half-bridge module is fabricated, as shown in Fig. 16. The loop inductance reduces about 50% compared to the one with two discrete devices. The devices are capable to switch at 54-A turn-off current, as shown in Fig. 17. The proposed solution of adding C_{X} at right position can significantly extend the high turn-off current capability.

V. Conclusion

A cascode structure is widely used for high-voltage normally-on GaN devices. However, the capacitance mismatch between GaN switch and Si MOSFET may result in divergent oscillation issue at high-current turn-off condition. The amplitude of voltage ringing formed by loop inductance and junction capacitance may exceed the threshold and trigger GaN internally turn-on mechanism during ringing period after cascode device is turned OFF and, therefore, leads to a divergent oscillation. Adding an additional capacitor C_{X} in parallel with Si MOSFET can compensate the mismatched charge and solve the problem. Considering all the parasitic inductances induced by adding C_{X}, the position of C_{X} is critical to achieve optimal performance. Experimental results validate the theoretical analysis and effectiveness of the proposed method. The proposed method extends the high-current turn-off capability and improves device performance significantly.

It is worthwhile to point out that the theoretical analysis and the proposed solution are applicable to all kinds of cascode devices.

Acknowledgment

This work was conducted with the use of GaN device samples by Transphorm of the CPES Industry Consortium Program.

References

[1] M. A. Khan, G. Simin, S. G. Pytel, A. Monti, E. Santi, and J. L. Hudgins, "New developments in gallium nitride and the impact on power electronics," in *Proc. IEEE Power Electron. Spec. Conf.*, 2005, pp. 15–26.

[2] N. Kaminski, "State of the art and the future of wide band-gap devices," in *Proc. IEEE Power Electron. Appl.*, 2009, pp. 1–9.

[3] Y. Wu, M. J. Mitos, M. Moore, and S. Heikman, "A 97.8% efficient GaN HEMT boost converter with 300W output power at 1 MHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 824–826, Aug. 2008.

[4] B. Hughes, J. Lazar, S. Hulsey, D. Zehnder, D. Matic, and K. Boutros, "GaN HFET switching characteristics at 350V-20A and synchronous boost converter performance at 1 MHz," in *Proc. IEEE Appl. Power Electron. Conf.*, 2012, pp. 2506–2508.

[5] J. Delaine, P. Olivier, D. Frey, and K. Guepratte, "High frequency DC-DC converter using GaN device," in *Proc. IEEE Appl. Power Electron. Conf.*, 2012, pp. 1754–1761.

[6] L. Zhou, Y.-F. Wu, and U. Mishra, "True bridgeless totem-pole PFC based on GaN HEMTs," in *Proc. PCIM Eur.*, 2013, pp. 1017–1022.

[7] X. Zhang, C. Yao, X. Lu, E. Davidson, M. Sievers, M. J. Scott, P. Xu, and J. Wang, "A GaN transistor based 90W AC/DC adapter with a buck-PFC stage and an isolated quasi-switched-capacitor DC/DC stage," in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 109–116.

[8] X. Huang, T. Liu, B. Li, F. C. Lee, and Q. Li, "Evaluation and applications of 600V/650V enhancement-mode GaN devices," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, 2015, pp. 113–118.

[9] B. J. Baliga and M. S. Adler, "Composite circuit for power semiconductor switching," Eur. Patent EP 0 063 749 B1, 1982.

[10] Z. Liu, X. Huang, W. Zhang, F. C. Lee, and Q. Li, "Evaluation of high-voltage cascode GaN HEMT in different packages," in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 168–173.

[11] S. She, W. Zhang, X. Huang, W. Du, Z. Liu, F. C. Lee, and Q. Li, "Thermal analysis and improvement of cascode GaN HEMT in stack-die structure," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 5709–5715.

[12] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014.

[13] R. Mitova, R. Ghosh, U. Mhaskar, D. Klikic, M.-X. Wang, and A. Dentella, "Investigations of 600-V GaN HEMT and GaN diode for power converter applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2441–2452, May 2014.

[14] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014.

[15] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2208–2219, May 2014.

[16] Y.-F. Wu, J. Gritters, L. Shen, R. P. Smith, and B. Swenson, "kV-class GaN-on-Si HEMTs enabling 99% efficiency converter at 800V and 100 kHz," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2634–2637, Jun. 2014.

[17] T. Hirose, M. Imai, K. Joshin, K. Watanabe, T. Ogino, Y. Miyazaki, K. Shono, T. Hosoda, and Y. Asai, "Dynamic performances of GaN-HEMT on Si in cascode configuration," in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 174–181.

[18] W. Zhang, F. Wang, L. M. Tolbert, B. J. Blaloc, and D. Costinett, "Investigation of soft-switching behavior of 600V cascode GaN HEMT," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 2865–2872.

[19] L. C. M. Carrasco and A. J. Forsyth, "Energy analysis and performance evaluation of GaN cascode switches in an inverter leg configuration," in *Proc. IEEE Appl. Power Electron. Conf.*, 2015, pp. 2424–2431.

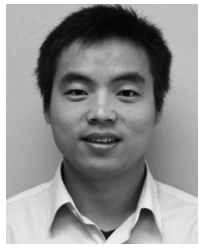
[20] X. Huang, Z. Liu, F. C. Lee, and Q. Li, "Characterization and enhancement of high-votlage cascode GaN devices," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 270–277, Feb. 2015.

[21] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz totem-pole PFC rectifier," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 682–688.

[22] X. Huang, W. Du, F. C. Lee, Q. Li, and Z. Liu, "Avoiding Si MOSFET avalanche and achieving zero-voltage-switching for cascode GaN devices," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 593–600, Jan. 2016.

[23] W. Zhang, X. Huang, Z. Liu, F. C. Lee, S. She, W. Du, and Q. Li, "A new package of high-voltage cascode gallium nitride device for megahertz operation," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1344–1353, Feb. 2016.

[24] R. Siemieniec, G. Nobauer, and D. Domes, "Stability and performance analysis of a SiC-based cascode switch and an alternative solution," *Microelectron. Rel.*, vol. 52, no. 3, pp. 509–518, Mar. 2012.



Xiucheng Huang (S'12) was born in Zhejiang, China, in 1986. He received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2008 and 2011, respectively. He is currently working toward the Ph.D. degree at the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA.

His main research interests include high-frequency high-power-density power conversion, soft-switching techniques, and power architecture.

Weijing Du was born in Shanxi, China, in 1985. She received the B.S. and Ph.D. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2008 and 2013, respectively. She is currently a Visiting Scholar at the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA.

Her current research interests include high-frequency high-density power converters and gallium nitride device applications.

Fred C. Lee (S'72–M'74–SM'87–F'90–LF'12) received the B.S. degree in electrical engineering from the National Cheng Kung University, Tainan, Taiwan, in 1968, and the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, USA, in 1972 and 1974, respectively.

He is currently a University Distinguished Professor at Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA, USA, and the Founder and Director of the Center for Power Electronics Systems. He holds 72 U.S. patents and has published 252 journal articles and 639 refereed technical papers.

Dr. Lee has served as the President of the IEEE Power Electronics Society (1993–1994). He received the William E. Newell Power Electronics Award in 1989, the Arthur E. Fury Award for Leadership and Innovation in 1998, the Honorary Sun Yuen Chuan Chair Professor at National Tsinghua University, Taiwan, in 2001, the Outstanding Alumni Award from National Cheng Kung University in 2004, the Ernst–Blickle Award for achievement in the field of power electronics in 2005, and the Honorary Kwoh-Ting Li Chair Professor Award at National Cheng Kung University, Taiwan, in 2011. He is a member of the National Academy of Engineering, USA, and an academician of Academia in Taiwan.

Qiang Li (M'11) received the B.S. and M.S. degrees in power electronics from Zhejiang University, Hangzhou, China, in 2003 and 2006, respectively, and the Ph.D. degree from Virginia Tech, Blacksburg, VA, USA, in 2011.

He is currently an Assistant Professor at the Center for Power Electronics Systems, Virginia Tech. His research interests include high-density electronics packaging and integration, high-frequency magnetic components, and high-frequency power conversion.

Wenli Zhang received the B.S. and M.S. degrees in materials science and engineering from the Beijing University of Technology, Beijing, China, in 2003 and 2006, respectively, and the Ph.D. degree from the University of Kentucky, Lexington, KY, USA, in 2011, in the area of advanced ceramic materials and processing.

He joined the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, in 2011, as a Research Assistant Professor. His research interests include piezoelectric and magnetic ceramics, LTCC materials and technology, high-density packaging, and integration of power electronics modules.