A Time Delay Compensation Method Based on Area Equivalence For Active Damping of an *LCL*-Type Converter

Chen Chen, Jian Xiong, Zhiqiang Wan, Ji Lei, and Kai Zhang

***Abstract*—Control of the *LCL*-type three-phase grid-connected converter is difficult due to high resonance peak of the *LCL* filter. Active damping is the state-of-the-art solution to this problem, but the damping performance will be affected by the inherent time delay of digital control, especially for high-power low switching frequency applications. Based on a discrete-time stability analysis of an *LCL*-type converter with capacitor-current-feedback active damping, a simple and effective time delay compensation method, which is based on area equalization concept, is proposed. The method can reduce the negative impact of the computation delay significantly. It has the potential to serve as a general solution to time delay compensation of a digitally controlled PWM converter. The validity of the proposed method is proved by experimental results.**

***Index Terms*—Active damping, digital control, *LCL* filter, time delay compensation.**

I. Introduction

DISTRIBUTED power generation systems (DPGSs) based on renewable energy, such as solar energy, wind energy, and so on, are making more and more contribution to the world-wide energy production [1]. Consequently, grid-connected converters as the interface between the DPGSs and the power grid are becoming increasingly popular and of greater concern [2]. In the grid-connected converter, an *L* or *LCL* filter is usually adopted in order to attenuate the switching harmonics. The *LCL* filter is often preferred for its superior harmonic suppressing ability [3], [4]. However, due to the resonant characteristic of the *LCL* filter, the converter may become unstable without proper damping.

Passive damping is to insert a passive resistor into the filter network. The design is simple and no changes are needed in the control algorithm, but it results in considerable power loss. Compared with passive damping, a more efficient and more flexible method is presented [5], [6], which is so-called active damping solution. Active damping changes the control strategies in order to satisfy system stability without using dissipative elements. It is to add extra feedback to provide the damping effect. Among the various active damping solutions, the capacitor-current-feedback active damping has drawn more attention for its flexible and simple implementation. This method has been addressed in some publications [7]–[12]. A step-by-step design method was proposed to design the grid-current regulator parameters and the capacitor-current-feedback coefficient [7]. This design method is straightforward, but it is performed without considering the time delay effect in digital control. In the digitally controlled system, the inherent computation delay will change system phase-frequency characteristic and thus may affect system stability, which imposes severe limit on the control bandwidth. As reported in [9], under one-step delay, when the resonance frequency is higher than one-sixth of the sampling frequency ($f_s/6$), there is a pair of poles outside the unit circle, which makes the system unstable. However, the time delay is indeed variable when the duty-ratio update mode varies [14], [16], [17].

In order to analyze the influence of different time delays, Zhang *et al*. [13] considered three typical cases, in which the delay time is 0.5 $T_{\rm sw}$, $T_{\rm sw}$, and 1.5 $T_{\rm sw}$ ($T_{\rm sw}$ being the switching period), respectively. By studying the influence of arbitrary delay time on system stability, a simple and effective delay-time control method is proposed for *LCL*-type inverters with single-loop control [15]. Applying this method into capacitor-current-feedback active damping, Pan *et al*. [9] proposed a scheme with reduced computation delay, which is achieved by shifting the capacitor current sampling instant toward the PWM reference update instant. Although the severe influence to system stability can weaken by changing the duty-ratio update instant, the computation time delay effect still exits.

Based on an investigation of the relationship between delay time and system stability, this paper proposes a simple and effective time delay compensation method. It can improve system stability and achieve better dynamic performance.

This paper is organized as follows. In Section II, the *Z*-domain model of the *LCL*-type grid-connected converter with capacitor-current-feedback active damping is established using modified *Z*-transform, and the relationship between delay time and system stability is studied. In Section III, the time delay compensation method is presented based on the concept of area equalization. In Section IV, a case design is provided to better explain the proposed method, and the comparison between the proposed method and reduced computation delay method is given out. Experimental results are presented in Section V to validate the proposed method. Section VI concludes this paper.

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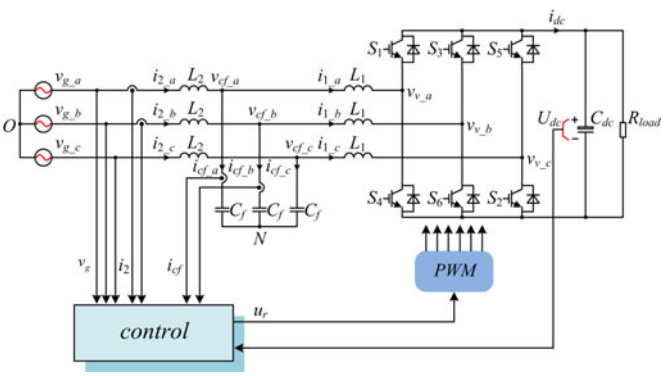


Fig. 1. Schematic diagram of the three-phase *LCL*-type PWM rectifier with capacitor-current-feedback active damping.

II. Modeling and Stability Analysis of the *LCL*-Type PWM Converter Active Damping Loop

The system to be analyzed is shown in Fig. 1. A three-phase voltage source converter is connected to the grid through an *LCL* filter. Power switches $S_1 \sim S_6$ and their antiparallel diodes form the converter. The *LCL* filter consists of converter-side inductors L_1, filter capacitors C_f, and grid-side inductors L_2. The grid current is controlled so that it can be synchronized with the grid voltage, which is expressed as v_g. The grid voltage is measured to obtain its phase angle through a phase-locked loop (PLL) [18]–[21].

A. Model of the Active Damping Loop

According to Fig. 1, applying Kirchhoff's laws, the mathematic model in the stationary *a-b-c* frame of the three-phase *LCL*-type grid-connected converter is described as [22]

$$\begin{cases} L_1 \dfrac{di_{1\_\mathrm{abc}}}{dt} = v_{\mathrm{cf\_abc}} - v_{v\_\mathrm{abc}} \\ L_2 \dfrac{di_{2\_\mathrm{abc}}}{dt} = v_{g\_\mathrm{abc}} - v_{\mathrm{cf\_abc}} - v_{NO} \\ C_f \dfrac{dv_{\mathrm{cf\_abc}}}{dt} = i_{2\_\mathrm{abc}} - i_{1\_\mathrm{abc}} \end{cases} \tag{1}$$

where i_{1_abc} are the three-phase converter-side inductor currents, i_{2_abc} are the three-phase injected grid currents, $v_{\mathrm{cf\_abc}}$ are the three-phase ac filter capacitor voltages referred to point *N*, v_{v_abc} are the three-phase midpoint voltages of the three converter legs referred to point *N*, v_{g_abc} are the three-phase grid voltages referred to point *O*, and $v_{NO}(t)$ is the voltage between points *N* and *O*. The equivalent series resistors of L_1, C_f, and L_2 are relatively small and ignored here.

By taking Clarke transformation, (1) can be expressed as

$$\begin{cases} L_1 \dfrac{di_{1\_\alpha\beta}}{dt} = v_{\mathrm{cf}\_\alpha\beta} - v_{v\_\alpha\beta} \\ L_2 \dfrac{di_{2\_\alpha\beta}}{dt} = v_{g\_\alpha\beta} - v_{\mathrm{cf}\_\alpha\beta} \\ C_f \dfrac{dv_{\mathrm{cf}\_\alpha\beta}}{dt} = i_{2\_\alpha\beta} - i_{1\_\alpha\beta} \end{cases} \tag{2}$$

where $i_{1\_\alpha\beta}, i_{2\_\alpha\beta}, v_{\mathrm{cf}\_\alpha\beta}, v_{v\_\alpha\beta}$, and $v_{g\_\alpha\beta}$ are complex space vectors in the form $\Phi_{\alpha\beta} = \Phi_\alpha + j\Phi_\beta$.

The definition of delay time in a digital control system is the time difference between the sampling instant of feedback variables and the updating instant of the control output, i.e., the sum of sampling time and algorithm execution time. But the delay time might be as large as one sampling period T_s in many digital controlled converters. If sampling and the PWM reference updating are set at the same instant, when the PWM reference is ready, the updating chance has passed, so the PWM reference has to update at the next period. That is the reason of the so called "one step delay." Shifting the sampling instant slightly ahead of the PWM reference update instant, the time delay can be reduced [23], [24]. And, it is easy to realize by programing. Thus, an unspecified computation delay time $\tau T_s (0 \le \tau \le 1)$ is used for a general purpose, and it can be modeled as $e^{-s\tau T_s}$. Obviously, $\tau = 1$ corresponds to the one-step delay.

The zero-order hold (ZOH) effect keeps the PWM reference constant after it has been updated. It is inevitable when the continuous system is discretized. When the discrete transfer function is derived, the ZOH delay effect is already considered and inherently exists in the discrete system. It can be modeled as

$$G_h(s) = \frac{1 - e^{-sT_s}}{s} \approx T_s e^{-s \cdot 0.5 T_s}. \tag{3}$$

Considering (2), the model of the digitally controlled system can be derived as shown in Fig. 2. As it is a digitally controlled system, the sampler and zero-order holder are displayed. The feedback of capacitor currents is used to damp the resonance of the *LCL* filter, which is equivalent to a virtual resistor connected in parallel with each ac filter capacitor [25]. The feedback coefficient K_c can be tuned according to the active damping design. $i^*_{2\_\alpha\beta}$ represent the references of injected grid currents, $G_i(z)$ is the injected grid current regulator in the stationary $\alpha\beta$ frame, $v_{r\_\alpha\beta}$ are the output signals of the injected grid current regulators, and $v_{m\_\alpha\beta}$ are the modulating signals. $e^{-s\tau Ts}$ represents the computation delay. K_{PWM} is the gain of the PWM converter.

According to Fig. 2, the loop gain $T_c(s)$ can be derived as

$$T_c(s) = \frac{K_{\mathrm{PWM}} G_i(s) \cdot e^{-(\tau+0.5)sT_s}}{s^3 L_1 L_2 C_f + s^2 L_2 C_f K_c K_{\mathrm{PWM}} e^{-(\tau+0.5)sT_s} + s(L_1 + L_2)}. \tag{4}$$

By ignoring the grid voltage, Fig. 2 can be transformed into Fig. 3. Since the control structures of α-axis and β-axis are exactly the same, the derivations of following formulas take α-axis components as an example. $G_{2v}(s)$ is the transfer function from $v_{v\_\alpha}(s)$ to $i_{2\_\alpha}(s)$.$H_{\mathrm{cv}}(s)$ is the transfer function from $v_{v\_\alpha}(s)$ to $i_{\mathrm{cf}\_\alpha}(s)$. The expressions of $G_{2v}(s)$ and $H_{\mathrm{cv}}(s)$ are given by

$$G_{2v}(s) = \frac{i_{2\_\alpha}(s)}{v_{v\_\alpha}(s)} = \frac{1}{L_1 L_2 C_f s(s^2 + \omega_r^2)} \tag{5}$$

$$H_{\mathrm{cv}}(s) = \frac{i_{\mathrm{cf}\_\alpha}(s)}{v_{v\_\alpha}(s)} = \frac{s}{L_1(s^2 + \omega_r^2)} \tag{6}$$

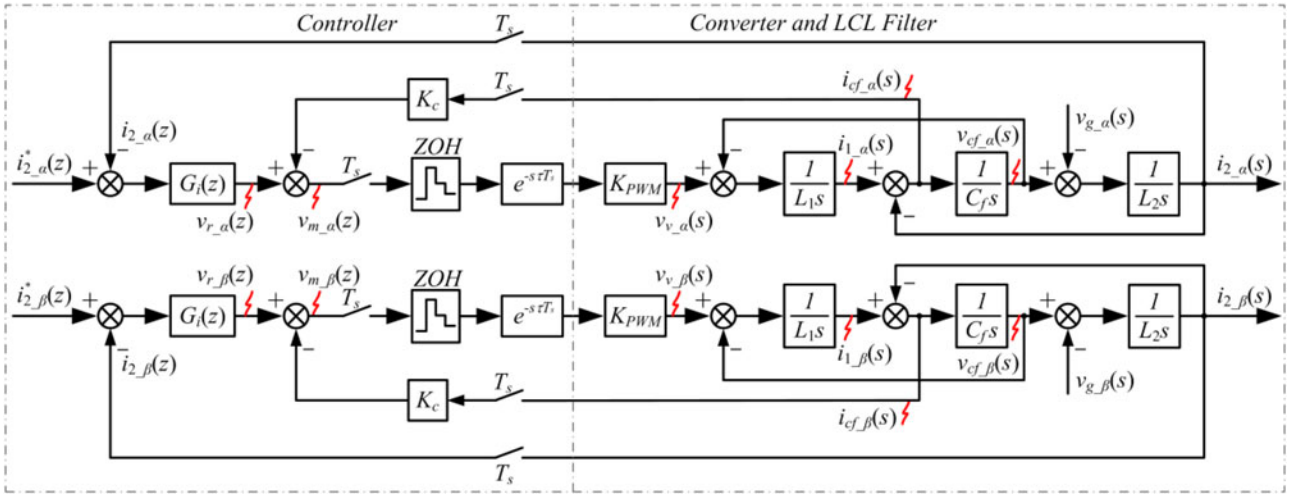


Fig. 2. Control block diagram of the digitally controlled *LCL*-type grid-connected converter with capacitor-current-feedback active damping.

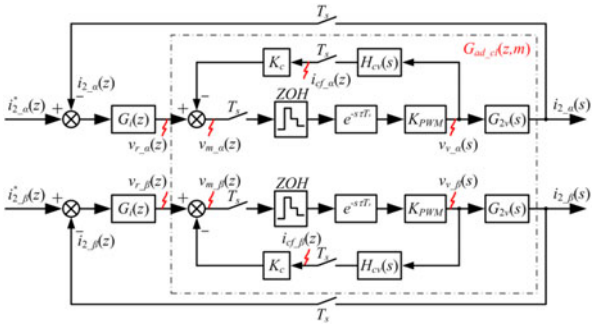


Fig. 3. Equivalent mathematic model of the digitally controlled *LCL*-type grid-connected converter.

where ω_r is the resonance angular frequency of the *LCL* filter, expressed as

$$\omega_r = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}}. \tag{7}$$

and the resonance frequency is $f_r = \omega_r/(2\pi)$.

Fig. 3 shows the equivalent mathematic model of the digitally controlled *LCL*-type grid-connected converter. If the delay time is a multiple of the sampling period T_s, the continuous system is easily converted into a discrete-time model using Z-transform. But the computation delay can be arbitrarily changed by shifting the sampling instant toward the PWM reference update instant. Using modified Z-transform, the authors in [16] and [17] can obtain more precise Z-domain model. Considering the variation of delay time, define

$$m = 1 - \tau \tag{8}$$

where $0 \le m \le 1$. Applying modified Z-transform to $G_{2v}(s)$ and $H_{\rm cv}(s)$ with ZOH, it yields

$$\begin{aligned} G_{2v}(z,m) &= \frac{i_{2\_\alpha}(z)}{v_{m\_\alpha}(z)} = Z_m\left[\frac{1-e^{-sT_s}}{s}\cdot K_{\rm PWM}G_{2v}(s)\right] \\ &= \frac{K_{\rm PWM}}{L_T}\left[\frac{mT_s(z-1)+T_s}{z(z-1)} - \frac{z-1}{\omega_r z}\cdot\frac{A}{B}\right] \end{aligned} \tag{9}$$

$$\begin{aligned} H_{\rm cv}(z,m) &= \frac{i_{{\rm cf}\_\alpha}(z)}{v_{m\_\alpha}(z)} = Z_m\left[\frac{1-e^{-sT_s}}{s}\cdot K_{\rm PWM}H_{\rm cv}(s)\right] \\ &= \frac{K_{\rm PWM}(z-1)}{\omega_r L_1 z}\cdot\frac{A}{B} \end{aligned} \tag{10}$$

where $L_T = L_1 + L_2$, $A = z\sin(m\omega_r T_s) + \sin[(1-m)\omega_r T_s]$, and $B = z^2 - 2z\cos(\omega_r T_s) + 1$. By the rigorous derivation, the closed-loop transfer function of this inner active damping loop is expressed as

$$\begin{aligned} G_{\rm ad\_cl}(z,m) &= \frac{i_{2\_\alpha}(z)}{v_{r\_\alpha}(z)} = \frac{G_{2v}(z,m)}{1+K_c H_{\rm cv}(z,m)} \\ &= \frac{L_1 K_{\rm PWM}\left[B\omega_r T_s(mz+1-m) - A(z-1)^2\right]}{L_T(z-1)\left[B\omega_r L_1 z + AK_{\rm PWM}K_c(z-1)\right]}. \end{aligned} \tag{11}$$

When $m = 1$, there is no computation delay. Obviously, $m = 0$ represents the one-step delay.

B. Capacitor-Current-Feedback Active Damping With Different Computation Delay

In a digitally controlled grid-connected converter, one of the most important factors that limit the dynamic performance and the maximum achievable control bandwidth is the delay time between the sampling instant and the PWM reference update instant. It is a common practice to sample state variables at the beginning or in the middle of the switching period, which is called the symmetrical regular sampling. However, this mechanism usually introduces a delay that is equal to one switching period, strongly limiting the control bandwidth. The computation delay can be reduced to half of the switching period in the asymmetric regular sampling mode, where state variables are sampled at the beginning and in the middle of the switching period. The PWM reference is updated twice in one switching period. The sampling frequency f_s is twice the switching frequency $f_{\rm sw}$.

Fig. 4 shows PWM generation mechanism of one-step delay based on asymmetric regular sampling. The delay time is equal to one sampling period T_s. $U_m(k)$ represents the PWM

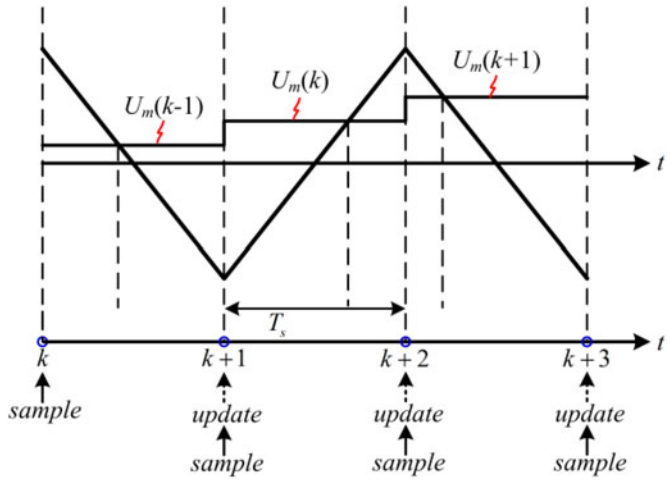


Fig. 4. Asymmetric regular sampling PWM schematics.

TABLE I
PARAMETERS OF THE TEST SETUP

Parameter	Symbol	Value
Grid phase voltage(RMS)	V_g	220 V
Power rating	P_o	300 kW
Fundamental frequency	f_o	50 Hz
Switching frequency	$f_{\rm sw}$	2 kHz
Sampling frequency	f_s	4 kHz
Converter-side inductor	L_1	180 μH
Grid-side inductor	L_2	90 μH
Filter capacitor	C_f	450 μH
Resonance frequency	f_r	968 Hz
DC-bus voltage	$U_{\rm dc}$	750 V

reference signal of step *k*. At time step *k*, the currents are sampled to calculate the PWM reference. Since the digital signal processor (DSP) updates data at the beginning and in the middle of the switching period, the PWM reference is not reloaded until time step $k+1$ [26]. Thus, one-step delay is introduced.

Such a one-step delay may affect system stability. With different relationship between f_r and $f_s/6$ [8], [9], [12], the stability analysis is different. However, by reducing computation delay, the severe influence to system stability can be effectively reduced [33].

Phase-frequency characteristic varies significantly with delay time, but amplitude–frequency characteristic does not change with it. If the computation delay time is small enough, the gain margin at the cross $-180°$ crossover frequency would be positive, indicating a stable system.

Table I shows the parameters of the test setup system. Using these parameters and (11), the active damping closed-loop pole maps for delay time variation from 0 to T_s is illustrated in Fig. 5, under different capacitor-current-feedback coefficients. Different values of *m* in the range [0, 1] are investigated with a step of 0.1. The stability of the system varies significantly with the delay time. When the delay time is small enough, the active damping closed-loop poles are located inside the unit circle, indicating that the system is stable. However, in practical applications, the minimum value of τ is limited by the time

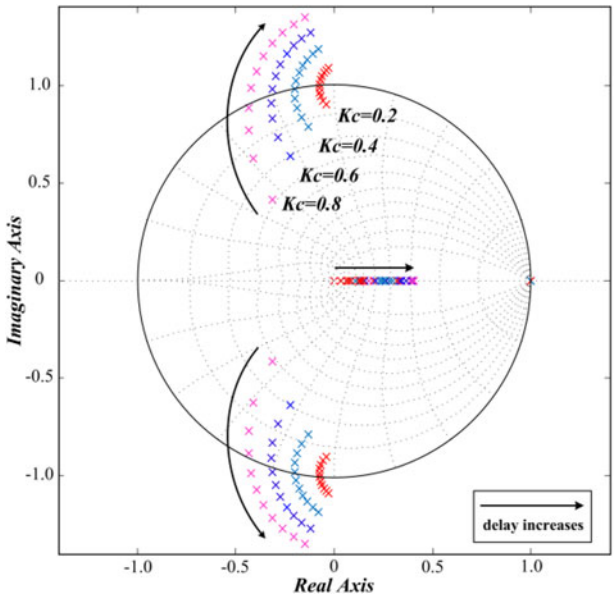


Fig. 5. Active damping closed-loop pole maps for different K_c with delay time variations.

required for the AD sampling, the control algorithm complexity, and the DSP that is used. Therefore, $\tau = 0$ is unprocurable. In other words, there will always be some delay time.

III. AREA COMPENSATION SCHEME FOR TIME DELAY

A. Proposed Area Compensation Scheme

Fig. 6(a) shows the reduced computation delay scheme under the asymmetric regular sampling PWM. The time between sampling and PWM reference update varies with shifting the sampling instant, which is labeled as τT_s. In other words, the DSP gives out PWM reference $U_m(k)$ of *k* sampling instant after the time interval τT_s. So during the τT_s time slice, the output is still $U_m(k-1)$, and the equivalent pulse in step *k* is not $U_m(k)$, but $\tau U_m(k-1) + (1-\tau)U_m(k)$.

To eliminate the influence of the time delay τT_s, the updating value $U_m(k)$ will be adjusted to keep the active pulse in step *k* unchanged. Based on this conception, the area compensation scheme is proposed. It attempts to maintain the PWM pulse intensity of the present sampling period.

Fig. 6(b) shows how to modify the pulsewidth. Suppose *R*(*k*) is the PWM reference which is given by the control algorithm. In the PWM mode of Fig. 6(a), $U_m(k)$ is set equal to *R*(*k*). While in the PWM mode of Fig. 6(b), $U_m(k)$ is set to satisfy the following:

$$R(k) = \tau U_m(k-1) + (1-\tau)U_m(k). \tag{12}$$

Assuming *R*(*k*) is larger than $U_m(k-1)$, which is shown in Fig. 6(b), (12) means that the area loss of *R*(*k*), which is marked with S_1 in time slice τT_s, is compensated by the area S_2 in time slice $(1-\tau)T_s$. So the actual PWM output of step *k* remains unchanged. Obviously, (10) is still valid if *R*(*k*) is less than $U_m(k-1)$.

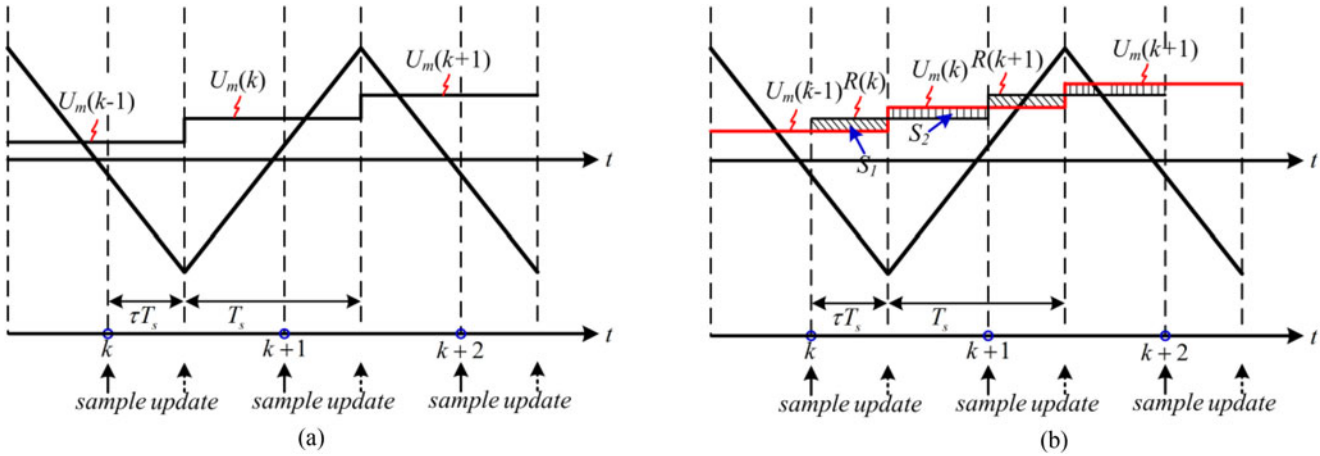


Fig. 6. Asymmetric regular sampling PWM schematics. (a) Reduced computation delay scheme. (b) Area compensation scheme.

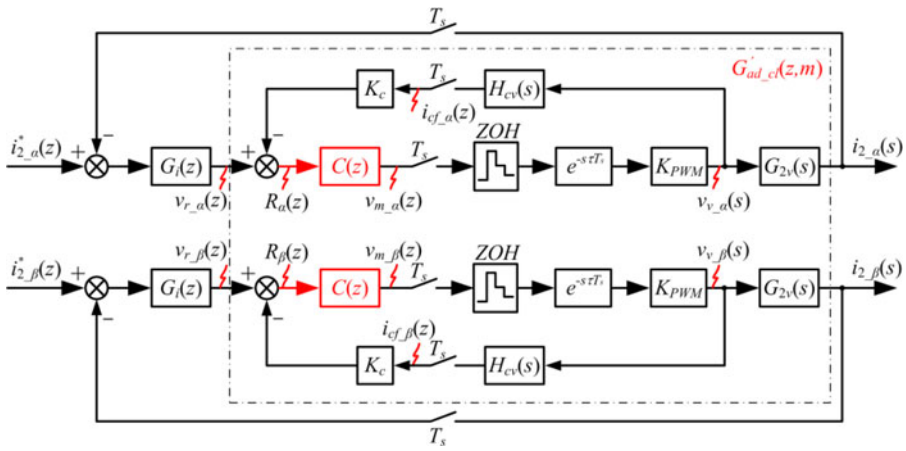


Fig. 7. Control block diagram of capacitor-current-feedback active damping with area compensation $C(z)$.

Substituting (8) into (12) yields

$$R(k) = (1-m)U_m(k-1) + mU_m(k). \tag{13}$$

Equation (13) is rewritten in the form of the discrete domain, i.e.,

$$U_m(z) = \frac{z}{mz+1-m}R(z). \tag{14}$$

Therefore, the area compensation link is expressed as

$$C(z) = \frac{z}{mz+1-m}. \tag{15}$$

In Fig. 7, $v_{m\_\alpha\beta}$ are the new PWM references. After introducing the area compensation scheme, the new closed-loop transfer function of the inner active damping loop is expressed as

$$G'_{\mathrm{ad\_cl}}(z,m) = \frac{C(z)G_{2v}(z,m)}{1+K_cC(z)H_{\mathrm{cv}}(z,m)} = \frac{L_1K_{\mathrm{PWM}}\left[B\omega_rT_s(mz+1-m)-A(z-1)^2\right]}{L_T(z-1)\left[B\omega_rL_1(mz+1-m)+AK_{\mathrm{PWM}}K_c(z-1)\right]}. \tag{16}$$

Compared with (11), they have same zeros but different poles. Thus, incorporating the area compensation link changes distribution of the active damping closed-loop poles.

B. Performance Evaluation of the Proposed Area Compensation Scheme

Taking into account the range of delay time τT_s, five typical cases are analyzed in Figs. 8 and 9, using the parameters listed in Table I. The difference between the reduced computation delay scheme and area compensation scheme is illustrated with the active damping closed-loop pole maps. Different values of capacitor-current-feedback coefficient K_c in the range [0, 0.8] are investigated with a step of 0.1.

When the delay time is zero in Fig. 8(a), the two schemes are the same and all poles are inside the unit circle, as expected. In Fig. 8(b), although both methods can make the active damping loop stable when the delay time is small enough, the area compensation scheme can achieve larger damping ratio and better dynamic performance than the reduced computation delay scheme. With the increasing of the delay time, the stability of the reduced computation delay scheme which is uncompensated becomes worse. As shown in Fig. 8(c), when τ increases to 0.5,

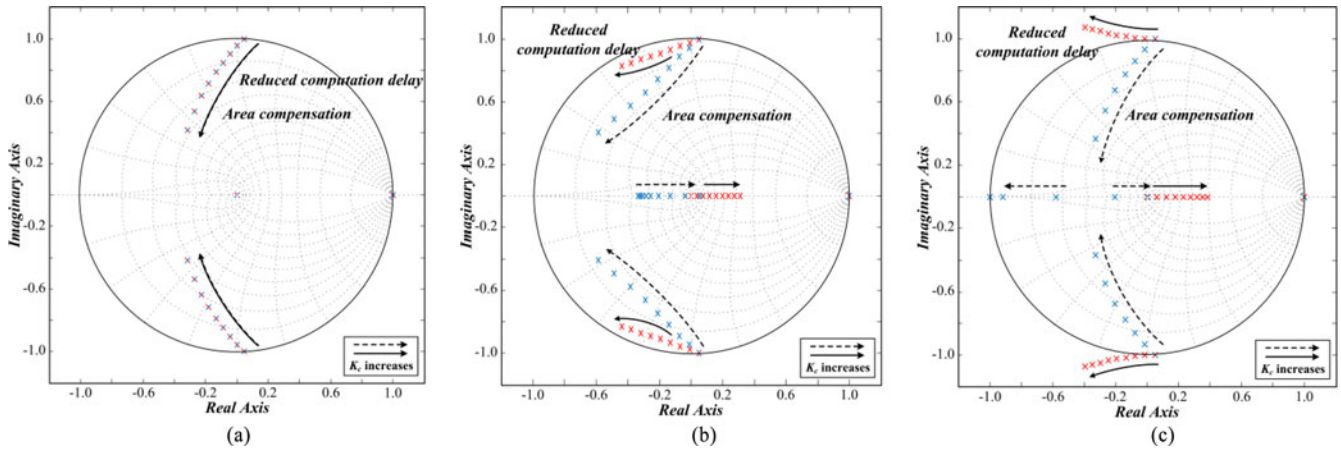


Fig. 8. Active damping loop pole maps with K_c variation for reduced computation delay and area compensation scheme. (a) $\tau = 0$. (b) $\tau = 0.25$. (c) $\tau = 0.5$.

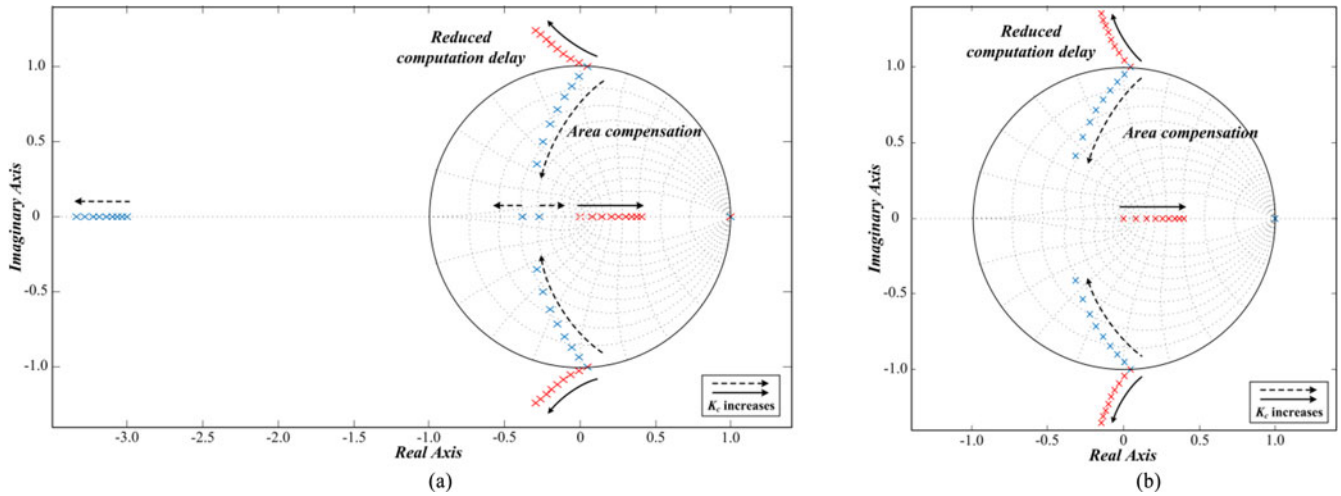


Fig. 9. Active damping loop pole maps with K_c variation for reduced computation delay and area compensation scheme. (a) $\tau = 0.75$. (b) $\tau = 1$.

poles of the area compensation scheme are still inside the unit circle, but the uncompensated active damping loop cannot be stable.

If the computation delay is larger than 0.5 T_s, as shown in Fig. 9(a), no matter how K_c varies, there will always be closed-loop unstable poles outside the unit circle, even with the area compensation scheme. The reason is that the pole of $C(z)$ will be less than –1. In the case of one-step delay, or $\tau = 1$, as shown in Fig. 9(b), the uncompensated active damping loop is unstable. With the proposed area compensation scheme, it seems that the closed-loop poles can still be kept within the unit circle and a reasonable damping ratio can be realized by selecting the proper value of K_c. However, in this circumstance, the area compensation link $C(z) = z$ cannot be realized physically.

According to the above analysis, the area compensation scheme is suitable when $\tau \leq 0.5$ or $m \geq 0.5$ is satisfied. In practical applications, especially for high-power applications where the switching frequency is relatively low, $\tau \leq 0.5$ or $m \geq 0.5$ is easily met. Compared with the reduced computation delay scheme, the proposed scheme can obtain larger damping ratio and better stability margin.

C. Phase-Frequency Characteristic

In order to reduce or eliminate the adverse effects caused by time delay in digital control, the lead-lag network is used [27]–[29]. The general form of the lead-lag network consists of the following transfer function:

$$G_{ll}(s) = A_L \frac{1 + s\alpha T}{1 + sT}. \tag{17}$$

Using bilinear transformation (Tustin method), the discrete equivalent of (17) has the form $k_z(z + z_0)/(z + p_0)$. But the design process is relatively complex and the compensation effect depends on the experience of the designer.

As (15) shows, the area compensation scheme is also a lead-lag network. Once τ is decided, the compensator $C(z)$ will be automatically determined, without any extra design effort. It can also be seen that $C(z)$ is independent of the plant parameters. Therefore, it can be used as a universal compensation scheme for digitally controlled converters. Of course, the parameter τ, which is mainly decided by the performance of the DSP, should be chosen as small as possible.

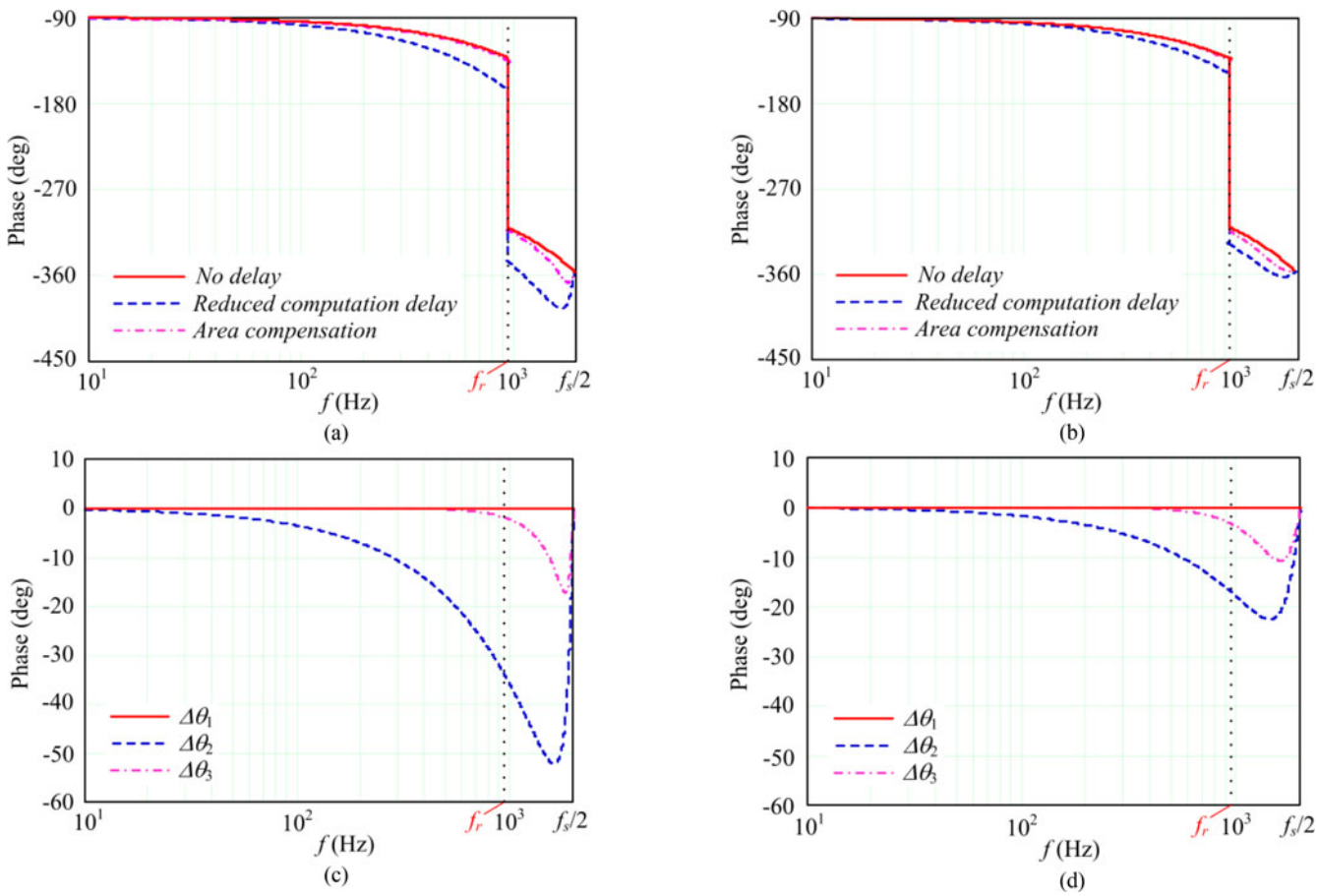


Fig. 10. Phase comparison among three different cases. (a) Phase-frequency plot with $m = 0.6$. (b) Phase-frequency plot with $m = 0.8$. (c) Phase errors among three cases with $m = 0.6$. (d) Phase errors among three cases with $m = 0.8$.

To verify the compensation effect of the proposed scheme, phase-frequency characteristics with the ideal case (no delay time), with the reduced computation delay scheme, and with the proposed area compensation scheme, are investigated. For the *LCL* filter, after introducing the area compensation link, the new transfer function is derived

$$G_{2\mathrm{vc}}(z,m) = C(z) \cdot G_{2v}(z,m). \tag{18}$$

Due to the restriction of $\tau \le 0.5$, in order to fully demonstrate the superiority of proposed scheme, $m = 0.6$ and $m = 0.8$ are selected.

Fig. 10 shows the comparison results using parameters listed in Table I. As shown in Fig. 10(a) and (b), although phase lag exists for both two schemes, the area compensation scheme could obtain much smaller phase lag compared with the reduced computation delay scheme. To illustrate more clearly the superiority of the area compensation scheme, the following phase errors are depicted in Fig. 10(c) and (d)

$$\begin{cases} \Delta\theta_1 = \angle G_{2v}(z,1) - \angle G_{2v}(z,1) \\ \Delta\theta_2 = \angle G_{2v}(z,m) - \angle G_{2v}(z,1) \\ \Delta\theta_3 = \angle G_{2\mathrm{vc}}(z,m) - \angle G_{2v}(z,1). \end{cases} \tag{19}$$

The area compensation scheme has obvious effect for phase lag compensation in low- and medium-frequency range. It is helpful to improve system stability.

To sum up, the lead-lag network tuning is complicated and should introduce a large amount of calculation. Comparatively, the area compensation scheme is effective and easy to realize, which is only derived by m. Due to simplicity of the design, it is suitable for the engineering application. To obtain a more explicit understanding, a design example will be given in the following section.

IV. Comparison Between Reduced Computation Delay Scheme and Area Compensation Scheme

The design example is presented in this section to make an intuitive understanding of the proposed scheme. Table I lists the parameters of a 300-kW three phase *LCL*-type PWM rectifier test setup. The digital controller employs a TMS320F2812 DSP. Asymmetric regular sampling is used. The *LCL* filter is designed with the method proposed in [28], [30], and [31], and with $f_r = 968$ Hz.

In this paper, the PI current regulator is employed and tuned considering the overall system dynamics. Its transfer function can be expressed as

$$G_i(s) = K_p + \frac{K_i}{s} \tag{20}$$

where K_p is the proportional coefficient and K_i is the integral coefficient. The discrete transfer function of the PI regulator is $G_i(z) = K_p + K_i T_s z/(z-1)$. K_p and K_i are determined by the desired unity gain crossover frequency f_c and phase margin *PM*, respectively.

Since the crossover frequency f_c is lower than the resonance frequency f_r, the influence of the capacitor on the *LCL* filter can be ignored when calculating the magnitude of the loop gain at frequencies up to f_c [7], [32]. Thus, the magnitude of the current loop gain can be simplified as

$$|T_c(s)| \approx \left| \frac{K_{\mathrm{PWM}} G_i(s)}{s(L_1+L_2)} \right|. \tag{21}$$

Meanwhile, the PI regulator can be reduced to a proportional gain at the crossover frequency. Then, substituting $|G_i(s)| \approx K_p$ into (21) yields

$$K_p \approx \frac{2\pi f_c (L_1+L_2)}{K_{\mathrm{PWM}}}. \tag{22}$$

Equation (22) shows that f_c is almost proportional to K_p. Therefore, a larger K_p means a faster dynamic response and a larger loop gain at low frequencies.

The possible region of K_p, K_i, and K_c will be obtained with requirements on steady-state error and stability margins. Considering the high complexity in *z*-plane, the design method is carried out in the continuous system.

The compensator *C*(z) is derived in the discrete domain. Setting $z = e^{sTs}$, and mapping *C*(z) into the continuous domain, we obtain

$$C(s) = \frac{1}{m + (1-m)e^{-sT_s}}. \tag{23}$$

After introducing the area compensation scheme, the new loop gain $T_c'(s)$ can be derived as (24) shown at the bottom of the page.

The case of reduced computation delay scheme can be described with $C(s) = 1$.

The PM of the new loop system can be expressed as

$$\mathrm{PM} = 180^o + \angle\, T_c'(s)|_{s=j2\pi f_c}. \tag{25}$$

Substituting (20) into (25) yields

$$\mathrm{PM} = \frac{\pi}{2} - \arctan\frac{K_i}{2\pi f_c K_p} - (2\tau+1)\pi f_c T_s - \arctan\frac{C}{D} \tag{26}$$

where

$$\begin{aligned} C =\ & 2\pi\left(f_c^2 - f_r^2\right) L_1 \tau \sin\left(2\pi f_c T_s\right) \\ & + f_c K_c K_{\mathrm{PWM}} \cos\left[(2\tau+1)\,\pi f_c T_s\right], \\ D =\ & 2\pi\left(f_r^2 - f_c^2\right) L_1 \left[m + \tau\cos\left(2\pi f_c T_s\right)\right] \\ & + f_c K_c K_{\mathrm{PWM}} \sin\left[(2\tau+1)\,\pi f_c T_s\right]. \end{aligned}$$

According to (22), (26) can be rewritten as

$$K_i = \frac{4\pi^2 f_c^2 L_T}{K_{\mathrm{PWM}}} \cdot \frac{D - C\cdot\tan[\mathrm{PM} + (2\tau+1)\pi f_c T_s]}{D\cdot\tan[PM + (2\tau+1)\pi f_c T_s] + C}. \tag{27}$$

The phase plot will cross over $-180°$ only once at the resonance frequency f_r. Therefore, the gain margin is expressed as

$$\mathrm{GM} = -20\log_{10}|T_c(j2\pi f_r)| \tag{28}$$

where $|T_c(j2\pi f_r)|$ can be given as

$$|T_c(j2\pi f_r)| \approx \frac{K_p L_1}{K_c L_T} \approx \frac{2\pi f_c L_1}{K_c K_{\mathrm{PWM}}}. \tag{29}$$

Substituting (29) into (28), the capacitor-current-feedback coefficient K_c with respect to f_c under the constraint GM can be derived as

$$K_c \approx 10^{\frac{\mathrm{GM}}{20}} \cdot \frac{2\pi f_c L_1}{K_{\mathrm{PWM}}}. \tag{30}$$

According to [7], the integral coefficient K_i under the constraint steady-state error can be obtained as

$$K_i = \frac{4\pi^2 f_o L_T}{K_{\mathrm{PWM}}} \cdot \sqrt{(10^{\frac{T_{\mathrm{fo}}}{20}} f_o)^2 - f_c^2} \tag{31}$$

where T_{fo}, the magnitude of the loop gain at the fundamental frequency f_o, reflects steady-state error constraint.

Compared with the area compensation scheme, the GM and steady-state error constraints for the reduced computation delay scheme are the same. However, the PM constraint is different. The PM of the reduced computation delay loop system is expressed as

$$\mathrm{PM}_{\mathrm{rc}} = 180^\circ + \angle\, T_c(s)|_{s=j2\pi f_c}. \tag{32}$$

Substituting (20) into (32), leads to

$$\begin{aligned} \mathrm{PM}_{\mathrm{rc}} = & \frac{\pi}{2} - \arctan\frac{K_i}{2\pi f_c K_p} - (2\tau+1)\pi f_c T_s - \arctan \\ & \times \frac{f_c K_c K_{\mathrm{PWM}} \cos[(2\tau+1)\pi f_c T_s]}{2\pi(f_r^2 - f_c^2)L_1 + f_c K_c K_{\mathrm{PWM}} \sin[(2\tau+1)\pi f_c T_s]}. \end{aligned} \tag{33}$$

According to (22), (33) can be rewritten as (34) shown at the next of the page.

As described in Section III-C, two cases of time delay ($m = 0.6$ and $m = 0.8$) are analyzed. The following analysis and experiments will only consider the case with larger time delay ($m = 0.6$). According to (27), (31), and (34), shown at the bottom of the page, the possible regions of the K_i and f_c for reduced computation delay and area compensation schemes are drawn in Fig. 11, using the parameters listed in Table I.

$$\begin{aligned} T_c'(s) =\ & \frac{K_{\mathrm{PWM}} G_i(s)\cdot e^{-(\tau+0.5)sT_s} C(s)}{s^3 L_1 L_2 C_f + s^2 L_2 C_f K_c K_{\mathrm{PWM}} e^{-(\tau+0.5)sT_s} C(s) + s(L_1+L_2)} \\ =\ & \frac{K_{\mathrm{PWM}} G_i(s)\cdot e^{-(\tau+0.5)sT_s}}{s^3 L_1 L_2 C_f [m + (1-m)e^{-sT_s}] + s^2 L_2 C_f K_c K_{\mathrm{PWM}} e^{-(\tau+0.5)sT_s} + s(L_1+L_2)[m + (1-m)e^{-sT_s}]} \end{aligned} \tag{24}$$

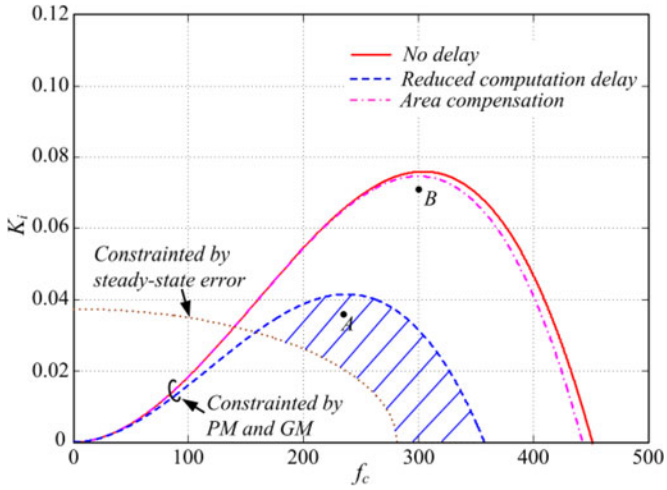


Fig. 11. Region of K_i and f_c constrained by GM, PM, and $T_{\rm fo}$ in the delay time of 0.4 T_s.

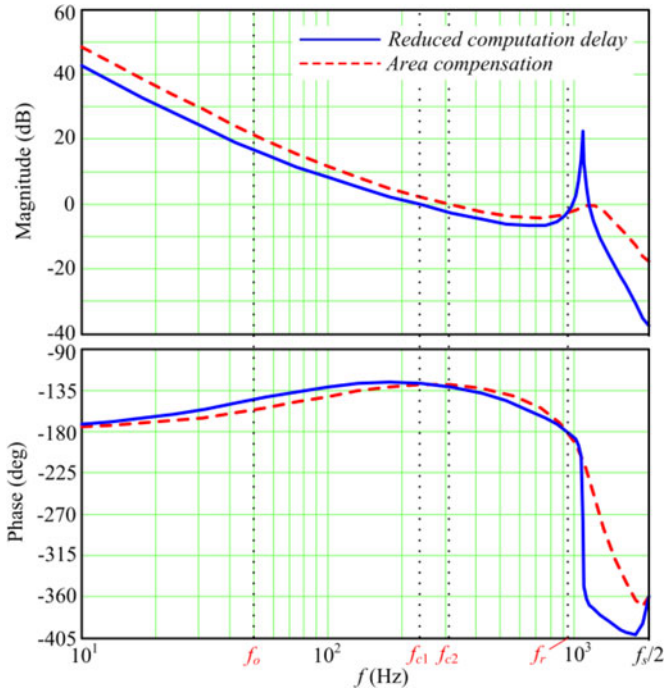


Fig. 12. Bode diagram of the grid current open-loop in the delay time of 0.4 T_s.

As shown in Fig. 11, the shaded area is the available region for the reduced computation delay method. When the area compensation method is incorporated, the region becomes larger as depicted with the dash-dotted line. It allows the use of larger K_i and f_c to improve both the steady-state and dynamic performance. The solid line shows the boundary with no computation delay. It can be seen that the parameter region of the proposed area compensation scheme is very close to this ideal situation.

V. Experimental Verification

Experiments were made on the 300-kW test setup with the parameters already listed in Table I. The grid voltage v_g, which is used in the PLL, is sensed by two voltage sensors. The grid current i_2 and capacitor current $i_{\rm cf}$ are sensed by two current sensors, respectively. The capacitor-current-feedback active damping is tested in the PWM rectifier shown in Fig. 1, where the d-axis component reference of i_2 is set by a dc-link voltage control. The dc-link control is based on a PI controller.

To guarantee the good dynamic performance and enough stability margins, the specifications are given by PM $\geq 45°$ and GM ≥ 3 dB. Meanwhile, the magnitude of the loop gain at the fundamental frequency should be larger than 15 dB to ensure good steady-state performance [7].

Referring to the region of K_i and f_c with the delay time of 0.4 T_s shown in Fig. 12, point A is chosen as the optimized controller parameter for the reduced computation delay method. The proposed method can achieve higher crossover frequency, and point B is chosen as the optimized controller parameter for the area compensation method. The controller parameters and corresponding performance index are listed in Table II. The voltage loop proportional coefficient and integral coefficient are 0.8831 and 0.003, respectively.

TABLE II
Parameters of the Controller

	Reduced computation delay	Area compensation
K_p	0.35	0.42
K_i	0.035	0.07
K_c	0.28	0.4
GM	2.67 dB	2.69 dB
PM	52°	51.2°
f_c	230 Hz	300 Hz

The Bode diagrams of the loop gain with two methods are shown in Fig. 12. As depicted in Fig. 12, the gain curve with the reduced computation delay method has a high resonance peak which is larger than 0 dB in the delay time of 0.4 T_s. With the area compensation scheme though, the gain curve is well damped and without any resonance peak. Apparently the crossover frequency f_c can be further increased with the proposed method to achieve even better dynamic performance.

Experiments are carried out to compare the performance achieved with the two schemes. Both the transient and steady-state responses of two schemes are investigated for $\tau = 0.4$. Fig. 13 shows the transient experimental results when the reactive current reference steps from 0 to -600 A. Obviously, the overshoot of the uncompensated system is larger than the

$$K_i = \frac{4\pi^2 f_c^2 L_T}{K_{\rm PWM}} \cdot \frac{\sin[(2\tau+1)\pi f_c T_s] + \frac{2\pi L_1 (f_r^2 - f_c^2)}{f_c K_c K_{\rm PWM}} - \cos[(2\tau+1)\pi f_c T_s] \cdot \tan[{\rm PM} + (2\tau+1)\pi f_c T_s]}{\left\{\sin[(2\tau+1)\pi f_c T_s] + \frac{2\pi L_1 (f_r^2 - f_c^2)}{f_c K_c K_{\rm PWM}}\right\} \cdot \tan[{\rm PM} + (2\tau+1)\pi f_c T_s] + \cos[(2\tau+1)\pi f_c T_s]} \tag{34}$$

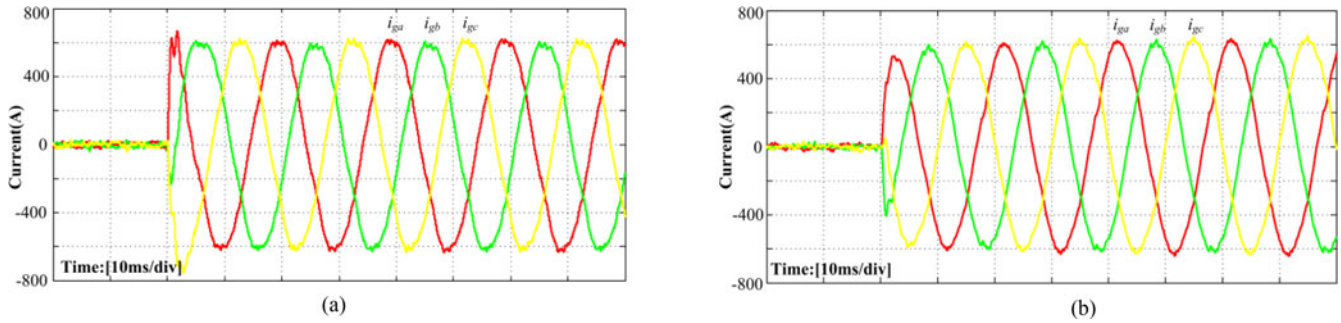


Fig. 13. Transient experimental results when reactive current steps between 0 and −600 A for $\tau = 0.4$. (a) Reduced computation delay scheme. (b) Area compensation scheme.

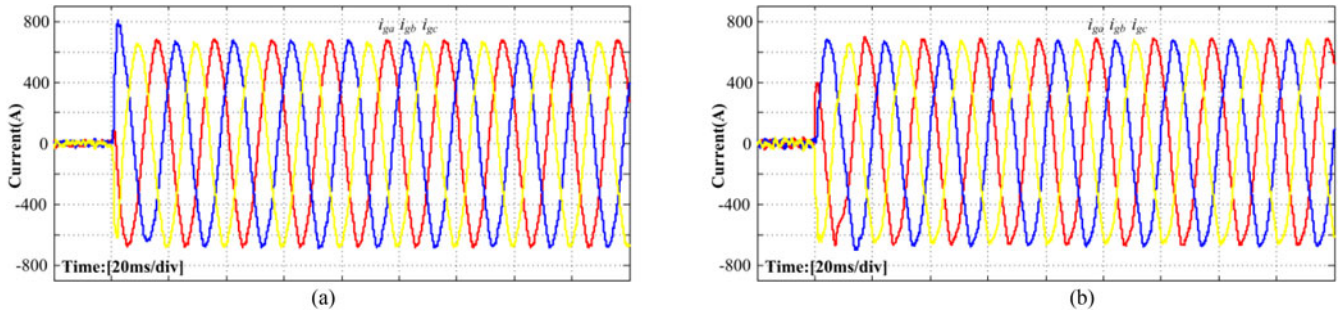


Fig. 14. Grid-side current in view of a dc-load step from no-load to full-load for $\tau = 0.4$. (a) Reduced computation delay scheme. (b) Area compensation scheme.

compensated system. Fig. 14 shows the experimental results of the grid-side current in view of a dc-load step from no-load to full-load. The total harmonic distortion for the uncompensated and the compensated system is 2.54% and 4.11%, respectively.

The experimental results show that, using the proposed area compensation scheme, the *LCL*-type grid-connected converter not only can remain with satisfactory steady-state performance but also achieve better dynamic performance. Although, the current distortion is a bit larger with the proposed method, it still satisfies the relevant requirement for grid-connected converters.

VI. Conclusion

Active damping (typically through capacitor current feedback) is an effective solution to suppress the resonance peak of *LCL*-type grid-connected converters. But inherent time delay associated with digital control can adversely affect the damping performance, or even endanger system stability. By shifting the sampling instant toward the PWM reference updating instant, the reduced computation delay scheme can alleviate the problem to some extent.

This paper presents the influence of time delay on system stability of the *LCL*-type grid-connected converter. A comprehensive investigation of the digitally controlled modeling with capacitor-current-feedback active damping has been conducted. Based on area equalization, this paper proposed a time delay compensation scheme to further improve the damping performance. Both the theoretical analysis and the experimental results have shown that, using the proposed area compensation method, the *LCL*-type grid-connected converter can achieve better dynamic performance than with the reduced computation delay scheme alone. As a general solution to time delay compensation, the proposed method can be readily applied in other digitally controlled converters.

References

[1] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[2] Y. Tang, P. C. Loh, P. Wang, F. H. Choo, and F. Gao, "Exploring inherent damping characteristic of *LCL*-filters for three-phase grid-connected voltage source inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1433–1443, Mar. 2012.

[3] W. Li, X. Ruan, D. Pan, and X. Wang, "Full-feedforward schemes of grid voltages for a three-phase *LCL*-type grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2237–2250, Jun. 2013.

[4] B. Bahrani, M. Vasiladiotis, and A. Rufer, "High-order vector control of grid-connected voltage-source converters with *LCL*-filters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2767–2775, Jun. 2014.

[5] Y. W. Li, "Control and resonance damping of voltage-source and current source converters with *LC* filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1511–1521, May 2009.

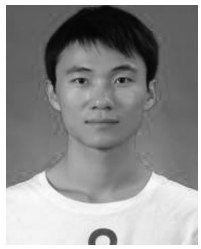
[6] K. Hatua, A. K. Jain, D. Banerjee, and V. T. Ranganathan, "Active damping of output *LC* filter resonance for vector-controlled VSI-fed AC motor drives," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 334–342, Jan. 2012.

[7] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Step-by-step controller design for *LCL*-type grid-connected inverter with capacitor-current-feedback active-damping," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1239–1253, Mar. 2014.

[8] S. G. Parker, B. P. McGrath, and D. G. Holmes, "Regions of active damping control for *LCL* filters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 424–432, Jan./Feb. 2014.

[9] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-current-feedback active damping with reduced computation delay for improving robustness of *LCL*-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3414–3427, Jul. 2014.

[10] Y. Tang, P. C. Loh, P. Wang, F. H. Choo, F. Gao, and F. Blaabjerg, "Generalized design of high performance shunt active power filter with output *LCL* filter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1443–1452, Sep. 2011.
[11] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 263–272, Jan. 2006.
[12] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Optimized controller design for *LCL*-type grid-connected inverter to achieve high robustness against grid-impedance variation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1537–1547, Mar. 2015.
[13] X. Zhang, J. W. Spencer, and J. M. Guerrero, "Small-signal modeling of digitally controlled grid-connected inverters with *LCL* filters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3752–3765, Sep. 2013.
[14] D. M. VandeSype, K. DeGusseme, F. M. L. L. DeBelie, A. P. Vanden-Bossche, and J. A. Melkebeek, "Small-signal z-domain analysis of digitally controlled converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 470–478, Mar. 2006.
[15] C. Zou, B. Liu, S.Duan, and R. Li, "Influence of delay on system stability and delay optimization of grid-connected inverters with *LCL* filter," *IEEE Trans. Ind. Informat.*, vol. 10, no. 3, pp. 1775–1784, Aug. 2014.
[16] K. J. Astrom and B. Wittenmark, *Computer Controlled Systems*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1990, pp. 209–243.
[17] B. K. Kuo, *Digital Control Systems*. Champaign, IL, USA: SRL Publishing, 1977.
[18] Md. S. Reza, M. Ciobotaru, and V. G. Agelidis, "A modified demodulation technique for single-phase grid voltage fundamental parameters estimation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3705–3713, Jun. 2015.
[19] S. Vazquez, J. A. Sanchez, M. R. Reyes, J. I. Leon, and J. M. Carrasco, "Adaptive vectorial filter for grid synchronization of power converters under unbalanced and/or distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1355–1367, Mar. 2014.
[20] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 765–778, Feb. 2013.
[21] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of phase locked loops for power converters under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2039–2047, Dec. 2009.
[22] E. Wu and P. Lehn, "Digital current control of a voltage source converter with active damping of *LCL* resonance," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1364–1373, Sep. 2006.
[23] P. Mattavelli, F. Polo, F. D. Lago, and S. Saggini, "Analysis of control delay reduction for the improvement of UPS voltage-loop bandwidth," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2903–2911, Aug. 2008.
[24] H. Deng, R. Oruganti, and D. Srinivasan, "PWM methods to handle time delay in digital control of a UPS inverter," *IEEE Trans. Power Electron.*, vol. 3, no. 1, pp. 1–6, Mar. 2005.
[25] P. A. Dahono, "A control method to damp oscillation in the input *LC* filter of AC-DC PWM converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Cairns, Australia, 2002, pp. 1630–1635.
[26] B. P. McGrath, S. G. Parker, and D. G. Holmes, "High performance current regulation for low-pulse-ratio inverters," *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 149–158, Jan./Feb. 2013.
[27] J. Kukkola and M. Hinkkanen, "Observer-based state-space current control for a three-phase grid-connected converter equipped with an *LCL* filter," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2700–2709, Jul./Aug. 2014.
[28] K. Jalili and S. Bernet, "Design of *LCL* filters of active-front-end two level voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1674–1689, May 2009.
[29] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*. Upper Saddle River, NJ, USA: Prentice-Hall, 2002.
[30] W. Wu, Y. He, and F. Blaabjerg, "An *LLCL* power filter for single-phase grid-tied inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 782–789, Feb. 2012.
[31] A. Reznik, M. G. Simoes, A. Al-Durra, and S. M. Muyeen, "Filter design and performance analysis for grid-interconnected systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1255–1232, Mar./Apr. 2014.
[32] D. Yang, X. Ruan, and H. Wu, "A real-time computation method with dual sampling modes to improve the current control performance of the *LCL*-type grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4563–4572, Jul. 2015.
[33] Z. Wan, J. Xiong, J. Lei, and C. Chen, "Analyze and reduce the impact of sampling delay on *LCL* converter with capacitor current feedback active damping," in *Proc. IEEE 11th Int. Conf. Power Elect. Drive Syst.*, Jun. 2015, pp. 539–545.



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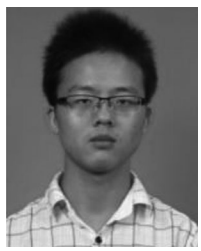

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