A Sensitivity-Improved PFM *LLC* Resonant Full-Bridge DC–DC Converter With *LC* Antiresonant Circuitry

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***Abstract*—An *LLC* resonant circuit-based full-bridge dc–dc converter with an *LC* antiresonant tank for improving the performance of pulse frequency modulation (PFM) is proposed in this paper. The proposed resonant dc–dc converter, named as *LLC-LC* converter, can extend a voltage regulation area below the unity gain with a smaller frequency variation of PFM by the effect of the antiresonant tank. This advantageous property contributes for protecting overcurrent in the case of the short-circuit load condition as well as the start-up interval in the designed band of switching frequency. The circuit topology and operating principle of the proposed converter is described, after which the design procedure of the operating frequency and circuit parameters is presented. The performances on the soft switching and the steady-state PFM characteristics of the *LLC-LC* converter are evaluated under the open-loop control in experiment of a 2.5-kW prototype, and its actual efficiency is compared with an *LLC* converter prototype. For revealing the effectiveness of the *LLC-LC* resonant circuitry, voltages and currents of the series and antiresonant tanks are analyzed, respectively, with state-plane trajectories based on calculation and experiment, whereby the power and energy of each resonant tank are demonstrated. Finally, the feasibility of the proposed converter is evaluated from the practical point of view.**

***Index Terms*—Antiresonant tank, buck and boost voltage regulations, *LLC* resonant converter, *LLC-LC* resonant converter, overcurrent protection (OCP), pulse frequency modulation, zero-current soft switching (ZCS), zero-voltage soft switching (ZVS).**

NOMENCLATURE

f_s	Switching frequency.
ω_s	Angular switching frequency ($\omega_s = 2\pi f_s$).
M	Input / output voltage conversion ratio ($M = V_o/V_{\text{in}}$).
a	High-frequency transformer windings turns ratio ($a = N_1/N_2$).
f_{rs}	Series-resonant frequency ($f_{\text{rs}} = 1/(2\pi\sqrt{L_s C_s})$).
f_{rm}	*LLC* resonant frequency($f_{\text{rm}} = 1/(2\pi\sqrt{(L_s+L_m)C_s})$).
F_{rs}	Switching frequency normalized to series-resonant frequency ($F_{\text{rs}} = f_s/f_{\text{rs}}$).
F_{rm}	Switching frequency normalized to *LLC* resonant frequency ($F_{\text{rm}} = f_s/f_{\text{rm}}$).
f_{r1}	First resonant frequency of *LLC-LC* resonant converter [referred to (4)].
f_{r2}	Second resonant frequency of *LLC-LC* resonant converter [referred to (5)].
f_{rp}	Antiresonant frequency ($f_{\text{rp}} = 1/(2\pi\sqrt{L_p C_p})$).
F_{rp}	Switching frequency normalized to antiresonant frequency ($F_{\text{rp}} = f_s/f_{\text{rp}}$).
S	*LLC* resonant-tank inductors ratio ($S = L_m/L_s$).
γ_L	Series/antiresonant inductors ratio ($\gamma_L = L_s/L_p$).
γ_C	Series/antiresonant capacitors ratio ($\gamma_C = C_s/C_p$).
R_{ac}	AC equivalent load resistance ($R_{\text{ac}} = 8a^2 R_o/\pi^2$).
Z_{rs}	Series-resonant characteristics impedance ($Z_{\text{rs}} = \sqrt{L_s/C_s}$).
Z_{rm}	*LLC* resonant characteristics impedance ($Z_{\text{rm}} = \sqrt{(L_s + L_m)/C_s}$).
Z_{rp}	Antiresonant characteristics impedance ($Z_{\text{rp}} = \sqrt{L_p/C_p}$).
Q_{rs}	Series-resonant loaded quality factor ($Q_{\text{rs}} = Z_{\text{rs}}/R_{\text{ac}}$).
λ_{rs}	Series/antiresonant characteristics impedances ratio ($\lambda_{\text{rs}} = Z_{\text{rs}}/Z_{\text{rp}}$).
λ_{rm}	*LLC*/antiresonant characteristics impedances ratio ($\lambda_{\text{rm}} = Z_{\text{rm}}/Z_{\text{rp}}$).

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I. INTRODUCTION

AN asymmetrical half-bridge *LLC* resonant dc–dc converter has been gaining the popularity in a variety of switching power supplies encompassing from a small power ICT equipment, LED lighting, battery chargers for electric vehicles, to a dc microgrid power distribution system due to a soft-switching operation over the wide range of load power: zero-voltage soft switching (ZVS) of active switches and zero-current soft switching (ZCS) of rectifier diodes [1]–[11]. The wide range of soft-switching operation in the *LLC* converter is attractive for a full-bridge dc–dc converter topology as well, while a typical phase-shift pulse-width-modulation (PWM) full-bridge circuit topology suffers from a severely limited range of soft switching for load power variations.

The primary modulation scheme of the *LLC* converter is PFM since the magnetizing current of the high-frequency (HF) transformer can be utilized for ZVS under the wide load conditions, as treated in the majority of the reference papers [1]–[15]. In contrast to the advantageous characteristics mentioned above, the operation of *LLC* converter is inherently allocated over the unity gain of the input–output voltage ratio, which is named herein as "boost area," for ensuring the excellent soft-switching performance and lower switching noise emission. This constraint of

voltage regulation poses another performance limitation on the *LLC* converter especially under the short-circuit and overload conditions due to a moderate sensitivity in the PFM-controlled voltage ratio characteristics [16], [17]. Therefore, overcurrent might occur in building up the output voltage quickly at the start-up process of the *LLC* converter, where the dc power is fed from the dc bus that is tightly controlled to 380 V into the low-voltage dc load as appears in a dc microgrid system [18].

As a solution for this technical problem, a pulse modulation strategy that incorporates an asymmetrical PWM into PFM has been proposed in [16]. Although it can be effective for the start-up process, no overcurrent protection (OCP) is guaranteed for the short-circuit load condition by the hybrid pulse modulation scheme. This technical problem will affect feasibility and reliability of power converters in the dc-source power supplies such as microgrid and transportation applications.

A circuitry-oriented method for the OCP has been proposed in [19]. This converter features an auxiliary circuit for clamping the resonant capacitor voltage in case of the short-circuit load, thereby limits the overcurrent in the primary-side inverter. This technique is, however, effective only for a low-output-voltage application since the clamping voltage depends on the output voltage, accordingly not suitable for the full-bridge topology. In addition, the auxiliary transformer and rectifier diodes will lead to increase of power losses and deteriorate the efficiency under light-load conditions.

As a more advantageous solution for the OCP, the antiresonant circuitry-applied dc–dc converter has been proposed in [20]–[25]. Among those literature studies, an *LLC* asymmetrical half-bridge dc–dc converter with a notch filter has been reported in [20]. However, the main idea of the converter is to actively inject the third-harmonic current by the effect of the antiresonance due to the notch filter and utilize the harmonic component as the active power. Another literature [21] also dealing with the antiresonant tank-based *LLC* converter has been presented for protecting it from the overcurrent under the short-circuit and overload conditions as well as the start-up process. However, the main argument of the literature is focused on exploring a method of magnetic integration of resonant inductors and utilizing the third-harmonic components as well as the discussion in [20]. Injection of the harmonics components will lead to decrease of the most useful component: fundamental frequency (switching frequency) active power; consequently, the converter efficiency might deteriorate especially for the full-bridge *LLC* converter applications. Both of the two reference papers include no evaluation on the actual performances of the multiresonant dc–dc converter, and no circuit parameter design guideline is deeply discussed with experimental verifications.

The *LLC* resonant full-bridge dc–dc converter with an *LC* antiresonant tank, named as "*LLC-LC* resonant converter" has been proposed by the authors of this paper in [22]–[25]. The original idea of the proposed resonant converter is to achieve OCP with a designed antiresonant frequency and characteristic impedance, while the operating principle of the *LLC* converter is retained under the normal load condition between two series-resonant frequencies. Accordingly, it can be ensured to supply the fundamental frequency components of HF resonant current and active power to the load while precluding the harmonics components. The circuit topology and the PFM scheme contribute for a wider range of buck voltage regulation with a smaller band of switching frequency variations besides the inherent boost operation. Thus, the buck and boost voltage regulations that are tantamount to a pulse-amplitude-modulation-based input dc voltage control can be attained in the *LLC-LC* converter.

The relevant papers [22]–[24] have verified the buck and boost voltage regulations of the proposed converter. In addition, the dual-pulse modulation scheme suitable for the *LLC-LC* dc–dc converter has been investigated in [25], whereby it has been verified that power conversion efficiency can improve by adopting pulse density modulation for the light-load conditions.

This paper presents the performance of the *LLC-LC* resonant converter with the complete experimental results on soft-switching performance, output voltage and power regulations, and power conversion efficiency and loss analysis, including the design consideration of resonant tank parameters, all of which are not mentioned or evaluated in any past reference papers. Performance comparison between the *LLC* and the proposed converters are presented in the experiment; then, the feasibility of the *LLC-LC* resonant topology is proven. Furthermore, the steady-state characteristics of the series- and antiresonant tanks are originally analyzed by the state-plane trajectory, which is truly effective for demonstrating the power and energy within the resonant tanks [26].

The rest of this paper is organized as follows. The steady-state performances on the voltage and power regulations of the *LLC* converter are theoretically described in Section II, whereby the low sensitivity of PFM for the buck voltage regulation is pointed out by the relevant characteristic curves. The circuit configuration and operation principle of the proposed *LLC-LC* converter are explained in Section III, after which the series- and antiresonant frequencies are explained in conjunction with the resonant tank impedances as well as the input impedance of the proposed converter. The design procedure of the circuit parameters and resonant frequencies are described in Section IV. The essential performances on the wide range of output voltage and power regulations with soft switching are demonstrated by the time-domain analysis with both the calculation and measured state-plane trajectories under the various load conditions including the short load in Section V, and compared with the *LLC* converter. Finally, the experimental verifications ate summarized; then, effectiveness of the multielement resonant dc–dc converter topology is originally revealed from a practical point of view in Section VI.

II. PFM Characteristics of *LLC* Resonant DC–DC Converter

The circuit diagram of *LLC* resonant full-bridge dc–dc converter is depicted in Fig. 1. The series inductor L_s includes the leakage inductance of the HF transformer, while the resonant capacitor C_s is additionally inserted in the primary-side HF inverter.

The steady-state characteristics of the *LLC* converter can be derived from the fundamental harmonic approximation (FHA)

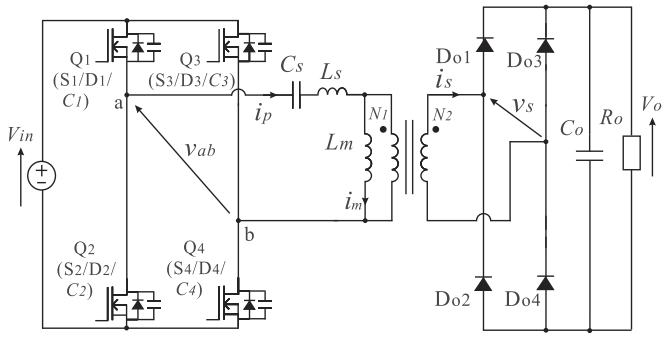

Fig. 1. Circuit diagram of the conventional *LLC* resonant full-bridge dc–dc converter.

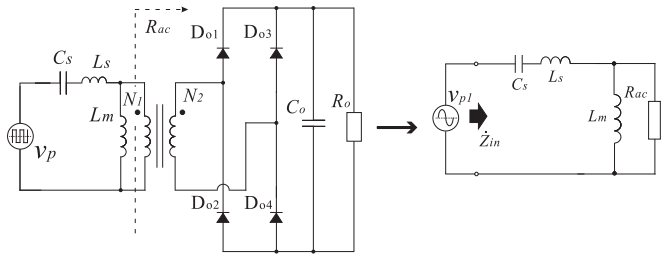

Fig. 2. Simplified equivalent circuits of the *LLC* converter based on the FHA method.

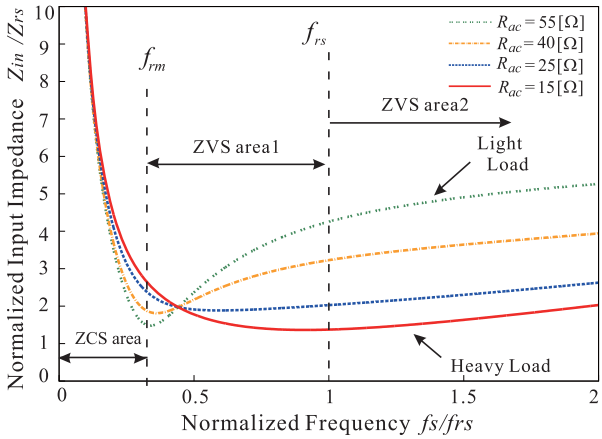

Fig. 3. Theoretical input impedance characteristics of the *LLC* converter.

[27]. This analysis method is based on the simplified equivalent circuit of the *LLC* converter as shown in Fig. 2, where the fundamental component v_{p1} of the rectangular voltage v_p in the HF inverter is defined by

$$v_{p1}(t) = \frac{4}{\pi} V_{\text{in}} \sin \omega_s t. \tag{1}$$

The input impedances Z_{in} of the *LLC* converter are defined from Fig. 2 as

$$Z_{\text{in}} = \left|\dot{Z}_{\text{in}}\right| = \left| \frac{\omega_s L_m \left(1 - F_{\text{rs}}^2\right) - j R_{\text{ac}} \left(1 - F_m^2\right)}{\omega_s C_s \left(R_{\text{ac}} + j \omega_s L_m\right)} \right|. \tag{2}$$

The input impedance versus switching frequency curves are drawn in Fig. 3 by referring to (2).

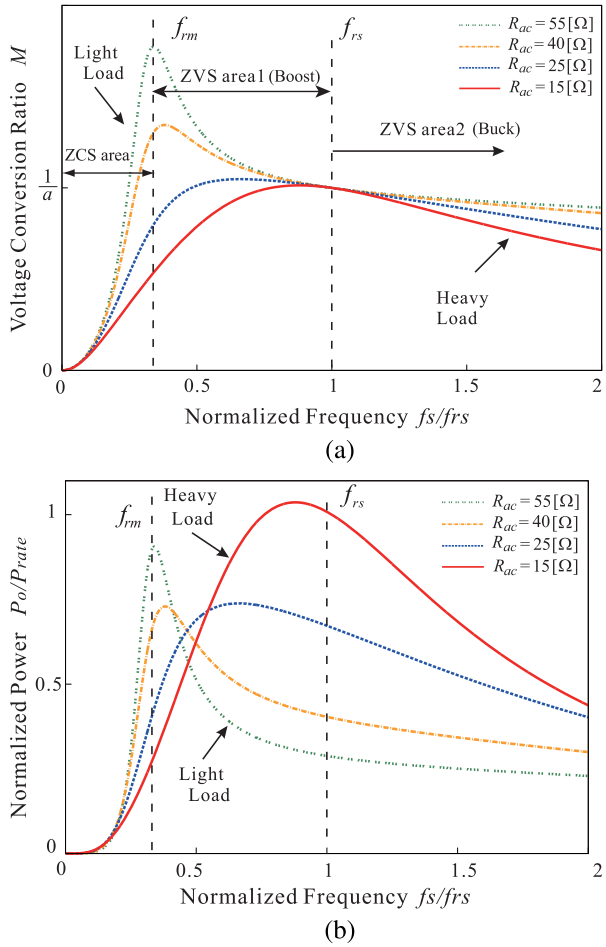

Fig. 4. Theoretical characteristics of the *LLC* converter: (a) M—normalized f_s, and (b) normalized P_o—normalized f_s.

The voltage conversion ratio $M = V_o/V_{\text{in}}$ of the *LLC* converter can be derived from Fig. 2 as

$$M = \frac{1}{a\sqrt{\left(1 + \frac{1}{S} - \frac{1}{SF_{\text{rs}}^2}\right)^2 + {Q_{\text{rs}}}^2 \left(F_{\text{rs}} - \frac{1}{F_{\text{rs}}}\right)^2}}. \tag{3}$$

Based on (3), the theoretical characteristics of the voltage conversion ratio and output power versus normalized switching frequency for the *LLC* converter are depicted in Fig. 4(a) and (b), respectively. The frequency area between f_{rm} and f_{rs} is defined as "ZVS area 1" and dedicates for the boost operation. The frequency area over f_{rs} is defined as "ZVS area 2" and performs the buck operation. The voltage conversion ratio M in the frequency area $f_s > f_{\text{rs}}$ exhibits the flat curve due to the low-sensitivity impedance of the series-resonant tank; consequently, the output power cannot also be regulated widely for the load power variations. It should be noted here that the frequency area below f_{rm} represents the ZCS area, which is not suitable for the *LLC* converter because the soft switching is lost at the turn-on transitions of Q_1–Q_4.

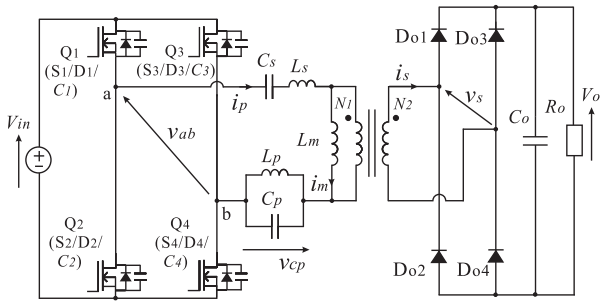

Fig. 5. Proposed *LLC-LC* resonant full-bridge dc–dc converter.

III. Proposed *LLC-LC* Resonant DC–DC Converter

A. Circuit Topology and Operating Principle

The proposed *LLC-LC* resonant full-bridge dc–dc converter is schematically depicted in Fig. 5 [22]–[24]. The antiresonant tank (L_pC_p) is employed in series with the series-resonant network (L_sC_s) in the primary-side HF inverter.

The proposed converter has two series-resonant frequencies: the first resonant frequency f_{r1} and the second resonant frequency f_{r2} are defined, respectively as shown at the bottom of this page, where $Q_{\rm rp}$ ($= Z_{\rm rp}/R_{\rm ac}$) denotes the impedance ratio with respect to the antiresonant tank. The series- and antiresonant tank impedances Z_s and Z_p are defined, respectively, as

$$Z_s = \left|\dot{Z}_s\right| = \left|j\left(\omega_s L_s - \frac{1}{\omega_s C_s}\right)\right| \tag{6}$$

$$Z_p = \left|\dot{Z}_p\right| = \left|\frac{j\omega_s L_p}{1-\omega_s^2 L_p C_p}\right|. \tag{7}$$

Based on (6) and (7), the typical characteristics of series- and antiresonant tank impedances versus switching frequency are illustrated in Fig. 6. According to the PFM scheme, Z_s and Z_p are correlatively expressed as

$$f_{r2} \le f_s < f_{r1} \Rightarrow Z_s \gg Z_p \tag{8}$$

$$f_s = f_{r1} \Rightarrow Z_s = Z_p \tag{9}$$

$$f_{r1} < f_s < f_{\rm rp} \Rightarrow Z_s < Z_p \tag{10}$$

$$f_s = f_{\rm rp} \Rightarrow Z_p \to \infty. \tag{11}$$

The HF transformer primary-side current I_p^* under the short-circuit and overload conditions can be theoretically expressed at $f_s = f_{\rm rp}$ as (4) and (5), shown at the bottom of the page

$$I_p^* = \frac{V_{\rm rp,max}}{Z_p} = \frac{4V_{\rm in}(1-\omega_s^2 L_p C_p)}{\pi\omega_s L_p} \to 0 \tag{12}$$

where Z_p is defined by (11).

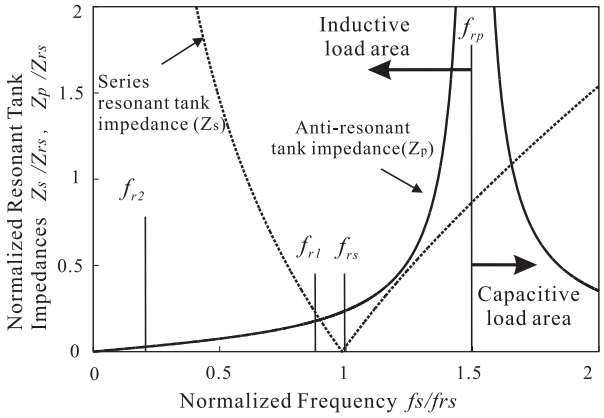

Fig. 6. Theoretical characteristics of the series- and antiresonant impedances versus switching frequency in the proposed *LLC-LC* converter.

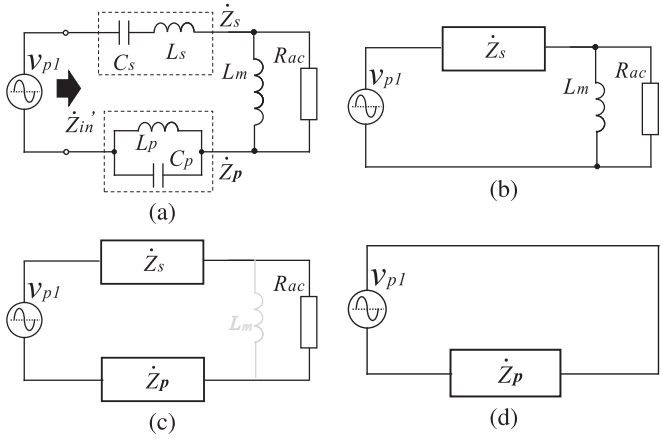

Fig. 7. Simplified equivalent circuits of the *LLC-LC* converter. (a) Common topology and modified for (b) $f_{r2} \le f_s < f_{r1}$, (c) $f_{r1} \le f_s < f_{\rm rp}$, (d) $f_s = f_{\rm rp}$.

The frequency-domain equivalent circuits of the proposed *LLC-LC* converter are illustrated in Fig. 7, where the frequency-dependent modifications are included in accordance with (8)–(11). The input impedance $Z'_{\rm in}$ can be defined in (13) on the basis of Fig. 7

$$Z'_{\rm in} = \left|\dot{Z}'_{\rm in}\right| = \left|\frac{\omega_s L_m\left[1-\left(1-f_{\rm rs}^2\right)f_{\rm rp}^2-(1+1/\gamma_L)f_{\rm rs}^2\right]}{\omega_s C_s\left(1-f_{\rm rp}^2\right)\left[R_{\rm ac}+j\omega_s L_m\right]} - j\frac{R_{\rm ac}\left[1-\left(1-f_{\rm rp}^2\right)F_m^2-(1+\gamma_c)f_{\rm rp}^2\right]}{\omega_s C_s\left(1-f_{\rm rp}^2\right)\left[R_{\rm ac}+j\omega_s L_m\right]}\right| \tag{13}$$

$$f_{r1} = \sqrt{\frac{f_{\rm rs}^2+\lambda_{\rm rs}^{-1}f_{\rm rs}f_{\rm rp}+f_{\rm rp}^2-\sqrt{\left(f_{\rm rs}^2+\lambda_{\rm rs}^{-1}f_{\rm rs}f_{\rm rp}+f_{\rm rp}^2\right)^2-4f_{\rm rs}^2f_{\rm rp}^2}}{2}} \tag{4}$$

$$f_{r2} = \sqrt{\frac{f_{\rm rm}^2+\lambda_{\rm rm}^{-1}f_{\rm rm}f_{\rm rp}+f_{\rm rp}^2-\sqrt{\left(f_{\rm rm}^2+\lambda_{\rm rm}^{-1}f_{\rm rm}f_{\rm rp}+f_{\rm rp}^2\right)^2-4f_{\rm rm}^2f_{\rm rp}^2}}{2}} \tag{5}$$

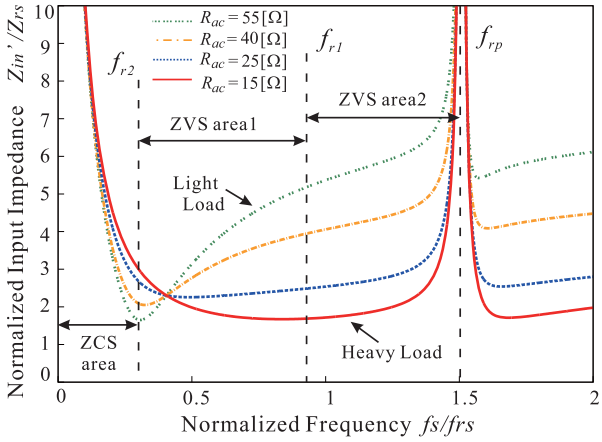

Fig. 8. Theoretical input impedance characteristics of the *LLC-LC* converter.

Based on (13), the input impedance versus switching frequency curves are depicted in Fig. 8. In $f_{r2} \le f_s \le f_{r1}$, ZVS area 1 $Z'_{\rm in}$ exhibits the property similar to $Z_{\rm in}$ in Fig. 3; thus, no significant difference on the operating characteristics appears between the *LLC* and *LLC-LC* converters. On the other hand, $Z'_{\rm in}$ escalates with a high sensitivity in $f_{r1} < f_s \le f_{\rm rp}$, ZVS area 2. In order to mitigate the influence of antiresonant tank in ZVS area 1, the input impedance of the *LLC-LC* converter should be designed as compatible with the *LLC* converter.

The theoretical voltage conversion ratio M of the proposed converter can be derived similarly from FHA in (14) and (15)

$$M = \frac{1}{a\sqrt{\left(1+\frac{\xi}{\omega L_m}\right)^2 + \left[Q_{\rm rs}\left(F_{\rm rs}-\frac{1}{F_{\rm rs}}\right) - Q_{\rm rp}\left(F_{\rm rp}-\frac{1}{F_{\rm rp}}\right)^{-1}\right]^2}} \tag{14}$$

$$\xi = Z_{\rm rs}\left(F_{\rm rs}-\frac{1}{F_{\rm rs}}\right) - Z_{\rm rp}\left(F_{\rm rp}-\frac{1}{F_{\rm rp}}\right)^{-1}. \tag{15}$$

Based on (14), the theoretical curves of the voltage conversion ratio and output power versus the normalized switching frequency are shown in Fig. 9. Those curves indicate the dc voltage conversion ratio decreases due to the high sensitivity of PFM in ZVS area 2; consequently, the output voltage can be regulated over the wide range of load power variations by the effect of the antiresonant tank. It should be remarked the FHA-based analysis is effective for the proposed converter since the harmonics in the resonant currents of the primary- and secondary-side circuits can be suppressed by designing $f_{\rm rp}$ and $Z_{\rm rp}$.

B. Switching-Mode Transitions

The key operating waveforms and mode-transition equivalent circuits of the proposed converter for ZVS area 1 (boost voltage regulation) are shown in Fig. 10(a) and (b), respectively. The circuit operation during one switching cycle can be divided into ten modes as follows.

1) *Mode 1 (power transfer mode (i_m reverses its polarity and linearly increases): $t_0 \le t < t_1$):* The polarity of the magnetizing current i_m reverses from negative to positive at $t = t_0$. During this interval, the active switches Q_1 and Q_4 are ON, then the power starts to be fed from the input voltage source $V_{\rm in}$ to the load R_o. The primary-side HF inverter current i_p gradually decays toward zero by the effect of series resonance.
2) *Mode 2 (D_{o1}, D_{o4} ZCS turn-off mode: $t_1 \le t < t_2$):* The primary-side current i_p decreases gradually due to the series resonance by L_s and C_s; then, it corresponds to i_m at $t = t_1$. The secondary-side current i_s naturally becomes zero; as a result, D_{o1} and D_{o4} can be turned OFF by ZCS with a minimized reverse recovery current. During this interval, i_m appears only in the primary-side HF inverter, while the secondary-side rectifier gets into the discontinuous conduction current mode (DCM).
3) *Mode 3 (Q_1, Q_4 ZVS turn-off mode: $t_2 \le t < t_3$):* The gate signals for Q_1 and Q_4 are removed at $t = t_2$. Then, their voltages v_{Q1} and v_{Q4} rise gradually from zero with the effects of parasitic or the lossless snubber capacitors C_1–C_4, while the voltages v_{Q2} and v_{Q3} across Q_2 and Q_3 decrease gradually from $V_{\rm in}$ to zero. ZVS turn-off herein can be attained by i_m in Q_1 and Q_4. During this interval, the ZVS condition is defined by

$$\frac{1}{2}L_m i_m(t_2)^2 > 2C_r V_{\rm in}^2 \tag{16}$$

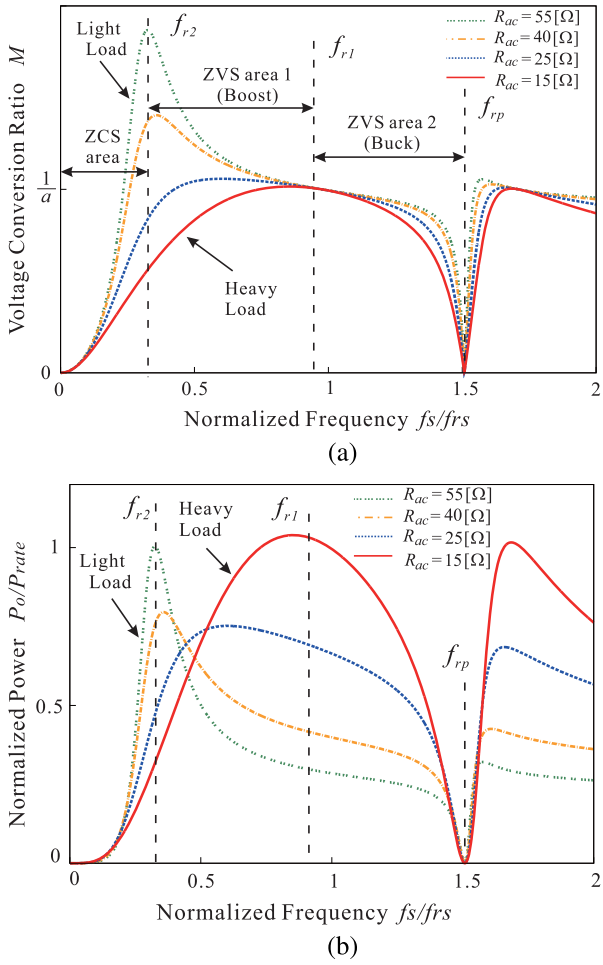

Fig. 9. Theoretical characteristics of the *LLC-LC* converter : (a) M–normalized f_s, and (b) normalized P_o–normalized f_s.

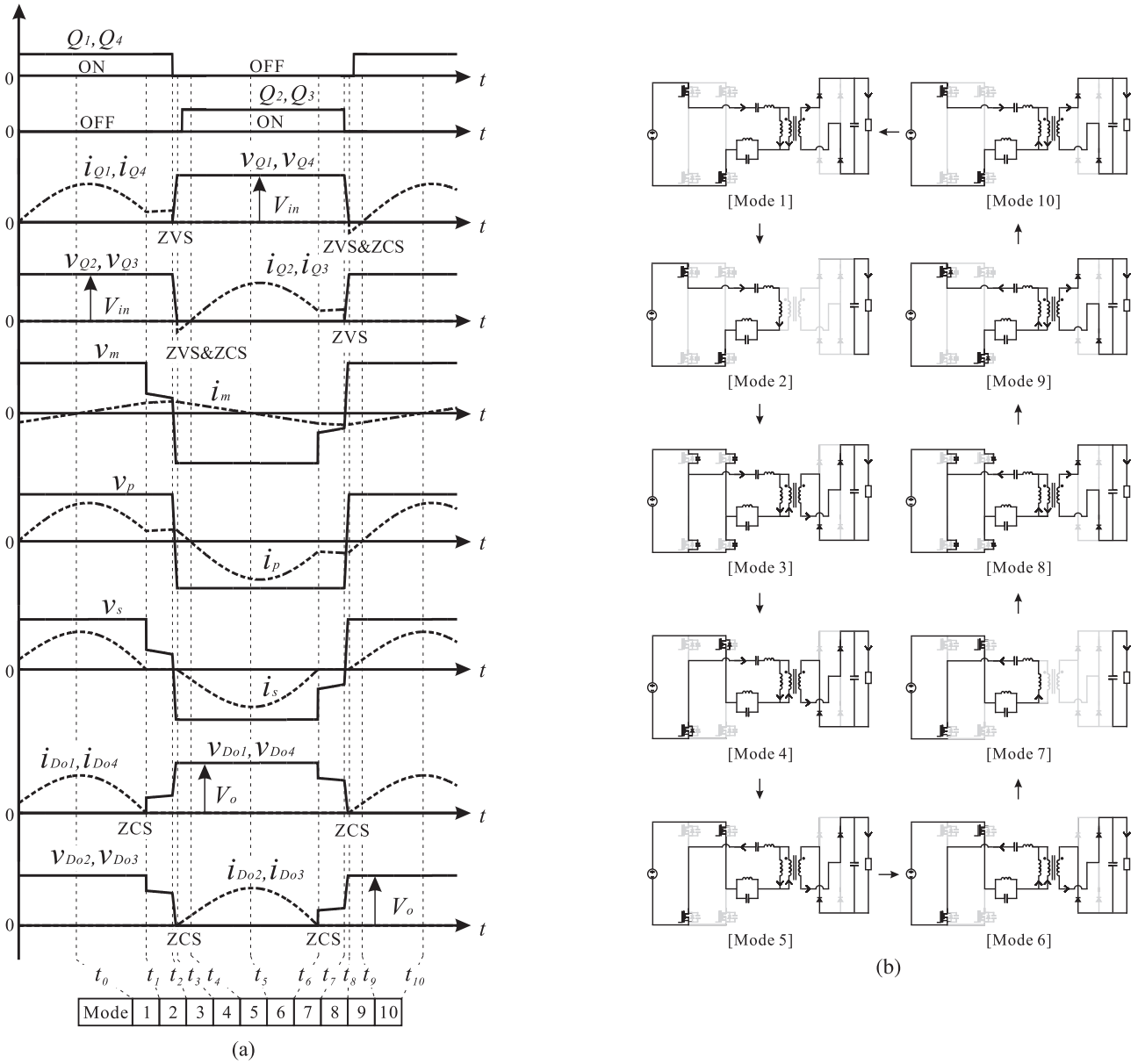

Fig. 10. Key voltage and current waveforms, and switch-mode transitions operating in $f_{r2} \leq f_s \leq f_{r1}$ (ZVS area 1): (a) voltage and current waveforms during one switching-cycle, and (b) equivalent circuits.

where C_r represents the lossless snubber capacitor $C_1 = C_2 = C_3 = C_4$.

4) *Mode 4 (*$\mathrm{Q_2}$, $\mathrm{Q_3}$ *ZVS and ZCS turn-on /* $\mathrm{D_{o2}}$, $\mathrm{D_{o3}}$ *ZCS turn-on mode:* $t_3 \leq t < t_4$*):* The voltages v_{Q2} and v_{Q3} across $\mathrm{Q_2}$ and $\mathrm{Q_3}$ reach to zero at $t = t_3$ due to the edge-resonance sustaining from Mode 3, thereby $\mathrm{D_2}$ and $\mathrm{D_3}$ are forward-biased. During this interval, the gate terminals of $\mathrm{Q_2}$ and $\mathrm{Q_3}$ are triggered, thereby ZVS and ZCS turn-on commutation can be achieved in the two switches. At the same time, i_p reverses its polarity; then, i_s begins to rise gradually from zero. Thus, ZCS turn-on can be obtained in $\mathrm{D_{o2}}$ and $\mathrm{D_{o3}}$.
5) *Mode 5 (power transfer mode (*i_m *linearly decreases):* $t_4 \leq t < t_5$*):* At $t = t_4$, the current through $\mathrm{Q_2}$ and $\mathrm{Q_3}$ commutate from $\mathrm{D_2}$ and $\mathrm{D_3}$ to $\mathrm{S_2}$ and $\mathrm{S_3}$. Accordingly, power transfers from V_{in} to R_o in the resonant behavior.
6) *Mode 6 (power transfer mode (*i_m *reverses its polarity and linearly decreases):* $t_5 \leq t < t_6$*):* The polarity of i_m reverses from positive to negative at $t = t_5$. During this interval, $\mathrm{Q_2}$ and $\mathrm{Q_3}$ are ON; then, power starts to be fed from V_{in} to R_o. Accordingly, i_p gradually decays toward zero by the effect of series resonance.
7) *Mode 7 (*$\mathrm{D_{o2}}$, $\mathrm{D_{o3}}$ *ZCS turn-off mode:* $t_6 \leq t < t_7$*):* The primary side i_p decreases gradually due to the series resonance by L_s and C_s, and it corresponds to i_m at $t = t_6$. Then, the secondary-side i_s naturally becomes zero; as a result, $\mathrm{D_{o2}}$ and $\mathrm{D_{o3}}$ can be turned OFF by ZCS with a minimized reverse recovery current. During this interval, i_m appears only in the primary-side circuit, while the secondary-side power stage gets into DCM.
8) *Mode 8 (*$\mathrm{Q_2}$, $\mathrm{Q_3}$ *ZVS turn-off mode:* $t_7 \leq t < t_8$*):* The gate signals for $\mathrm{Q_2}$ and $\mathrm{Q_3}$ are removed at $t = t_7$. Then,

their voltages v_{Q2} and v_{Q3} rise gradually from zero with the effects of parasitic or the lossless snubber capacitors $C_1 - C_4$, while the voltages across Q_1 and Q_4 decrease gradually from V_{in} to zero. ZVS turn-off herein can be attained by i_m in Q_2 and Q_3. During this interval, the ZVS condition is expressed by

$$\frac{1}{2} L_m i_m(t_7)^2 > 2 C_r V_{\mathrm{in}}^2. \tag{17}$$

9) *Mode 9 (Q_1, Q_4 ZVS and ZCS turn-on / D_{o1}, D_{o4} ZCS turn-on mode: $t_8 \le t < t_9$):* The terminal voltages v_{Q1} and v_{Q4} reach to zero at $t = t_8$ due to the edge-resonance sustaining from Mode 8; then, D_1 and D_4 are forward-biased. During this interval, the gate terminals of Q_1 and Q_4 are triggered, thereby ZVS and ZCS turn-on commutation can be achieved in those switches. At the same time, i_p reverses its polarity; then, i_s begins to rise gradually from zero. Thus, ZCS turn-on can be obtained in D_{o1} and D_{o4}.
10) *Mode 10 (power transfer mode (i_m linearly increases): $t_9 \le t < t_{10}$):* At $t = t_9$, the current through Q_1 and Q_4 commutate from D_1 and D_4 to S_1 and S_4. Accordingly, the power transfer stars from V_{in} to R_o in the resonant behavior.

The voltage and current waveforms for the ZVS area 2 (buck voltage regulation) are depicted in Fig. 11(a), and the corresponding circuit transitions are illustrated in Fig. 11(b), respectively. The secondary-side current i_s is naturally continuous in the ZVS area 2, so the operating and commutation process is similar to ZVS area 1 with the exception of Mode 2 and Mode 7 mentioned above.

The time-domain formulas with high-order differential equations are summarized in Table I for ZVS area 1 and the ZVS area 2, respectively. The resonant capacitor voltage v_{cs} of the series-resonant tank is selected as the state valuable to express the steady-state operations of the proposed coverer. Accordingly, the current i_{Ls} through L_s, current i_{Lp} through L_p, and voltage v_{cp} across C_p can be expressed on the basis of v_{cs} as

$$i_{Ls} = C_s \frac{dv_{\mathrm{cs}}}{dt},\ i_{\mathrm{Lp}} = \frac{-\omega_s^2 L_p C_p i_{Ls}}{1 - \omega_s^2 L_p C_p},\ v_{\mathrm{cp}} = L_p \frac{di_{\mathrm{Lp}}}{dt}. \tag{18}$$

IV. Design Procedure of Circuit Parameters

A. Resonant Frequencies

The first resonant frequency f_{r1} and the second resonant frequency f_{r2} of the proposed *LLC-LC* converter are designed as close to f_{rs} and f_{rm} of the *LLC* converter, respectively. The antiresonant frequency f_{rp} should be set well less than three times f_{r1} for precluding the harmonics from i_p, while the switching frequency variation from f_{r1} should be small as much as possible for a better response of the OCP. This idea on setting the resonant frequencies leads to a design guideline of $f_{\mathrm{rp}} = 1.5 f_{r_1}$.

Once f_{rs} and f_{rm} are set as 90 and 30 kHz in consideration of the wide-range ZVS operation in the *LLC* converter, the antiresonant frequency f_{rp} can be designed as

$$f_{\mathrm{rp}} = 1.5 f_{r1} = 135\,\mathrm{kHz}. \tag{19}$$

The resonant tank characteristics impedances ratios of the proposed converter are given by considering F_{rp} for Z'_{in} as $\lambda_{\mathrm{rs}} = 5$ and $\lambda_{\mathrm{rm}} = 15$. As a result, the first and second resonant frequencies are designed from (4) and (5) as $f_{r1} = 86\,\mathrm{kHz}$ and $f_{r2} = 27\,\mathrm{kHz}$, respectively. Thus, the switching frequency band of PFM for the proposed converter can be determined as

$$f_{r2} = 27\,\mathrm{kHz} \le f_s \le f_{r1} = 86\,\mathrm{kHz}\ \text{(for ZVS area 1)} \tag{20}$$

$$f_{r1} = 27\,\mathrm{kHz} < f_s \le f_{\mathrm{rp}} = 135\,\mathrm{kHz}\ \text{(for ZVS area 2)} \tag{21}$$

where the minimum and maximum switching frequencies can also be expressed as 27 and 135 kHz.

B. Resonant Inductors and Capacitors

By setting the lossless snubber capacitor C_r ($= C_1 = \cdots = C_4$) as 1 nF to attain a low dv/dt rate sufficient for the ZVS turn-off transitions of Q_1–Q_4 with the constant dc input voltage V_{in} ($= 220$ V), the magnetizing inductance L_m of the HF transformer can be determined from (16) and (17) as

$$L_m = \frac{4 C_r V_{\mathrm{in}}^2}{i_{m,\min}^2} = 190\,\mu\mathrm{H} \tag{22}$$

where $i_{m,\min}$ represents the magnetizing current of the HF transformer at the turn-off transitions of Q_1–Q_4 under the minimum load condition, and assumed $= 1$ A herein. The series-resonant-tank inductor L_s is designed as

$$L_s = \frac{L_m}{S} \simeq 16\,\mu\mathrm{H} \tag{23}$$

where S is selected more than 10 in order to suppress the circulating current in the primary-side HF inverter.

The series- and antiresonant inductors ratio γ_L should be given by considering Z'_{in} characteristics in the ZVS area 1 of Fig. 8. When γ_L is selected as greater than 5, the antiresonant inductor L_p can be determined as

$$L_p = \frac{L_s}{\gamma_L} \simeq 2.5\,\mu\mathrm{H}. \tag{24}$$

The series-resonant capacitor C_s and the antiseries-resonant capacitor C_p can be determined from (4) and (5) with (23) and (24), respectively, as

$$\begin{aligned} C_s &= \frac{f_{\mathrm{rs}}^2 - f_{\mathrm{rp}}^2}{(2\pi f_{\mathrm{rs}}^2)\left[\left(f_{\mathrm{rs}}^2 - f_{\mathrm{rp}}^2\right) L_s - f_{\mathrm{rp}}^2 L_p\right]} \\ &= \frac{1}{(2\pi f_{\mathrm{rs}}^2) L_s \left[1 + \frac{1}{\gamma_L \left\{1 - \left(\frac{f_{\mathrm{rs}}}{f_{\mathrm{rp}}}\right)^2\right\}}\right]} \simeq 170\,\mathrm{nF} \end{aligned} \tag{25}$$

$$C_p = \frac{1}{{\omega_{\mathrm{rp}}}^2 L_p} = \frac{1}{(2\pi f_{\mathrm{rp}})^2 L_p} = \frac{\gamma_L}{(2\pi f_{\mathrm{rp}})^2 L_s} \simeq 550\,\mathrm{nF}. \tag{26}$$

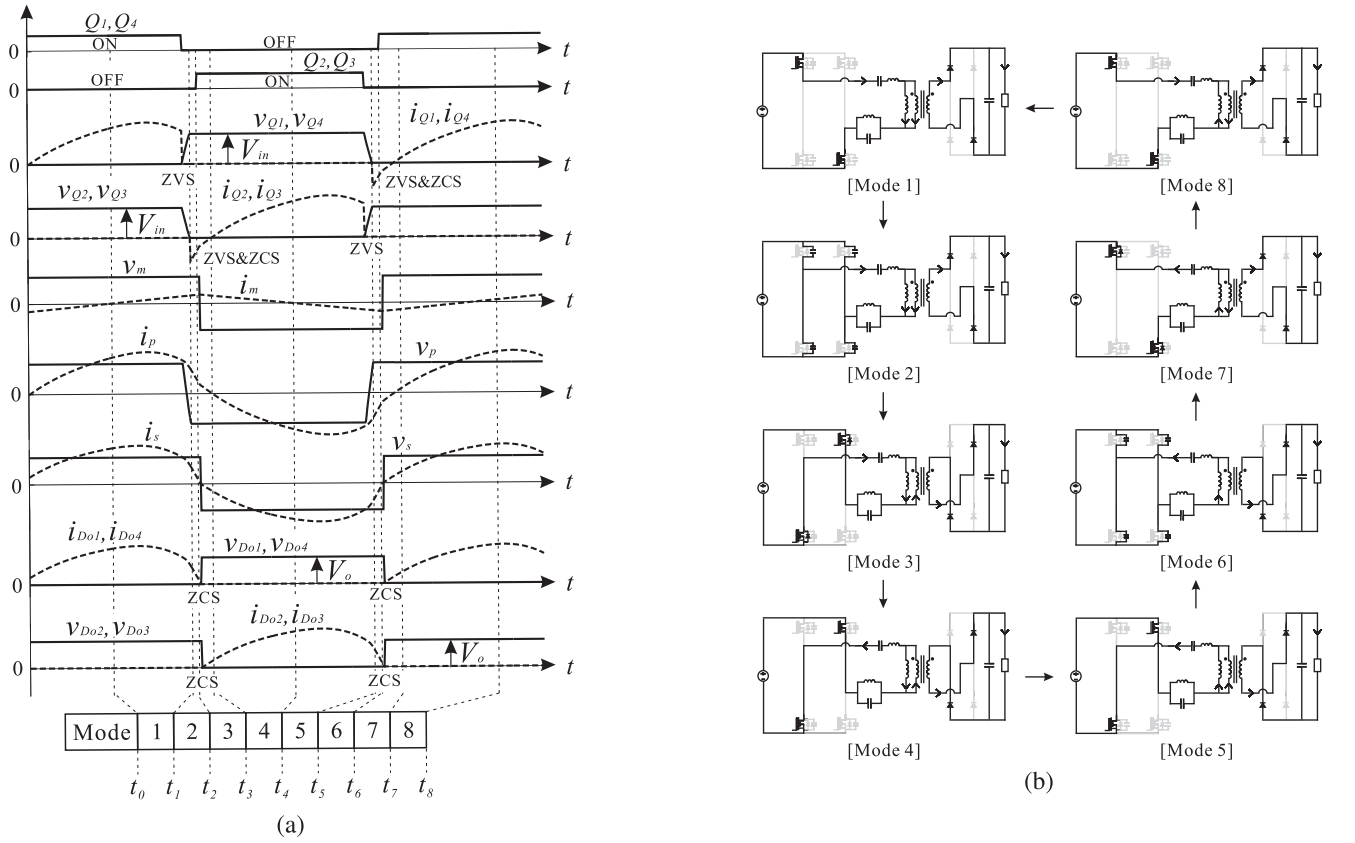

Fig. 11. Key voltage and current waveforms, and switch-mode transitions operating in $f_{r1} < f_s \le f_{\rm rp}$ (ZVS area 2). (a) Voltage and current waveforms during one switching cycle. (b) Equivalent circuits.

TABLE I
STEADY-STATE TIME-DOMAIN FORMULAS OF THE SERIES-RESONANT CAPACITOR VOLTAGE

Intervals	ZVS area 1 (secondary-side DCM)
$*t_0 \le t < t_1$	$\frac{d^4 v_{\rm cs}(t)}{dt^4} + \left(\omega_{\rm rs}^2 + \omega_{sp1}^2 + \omega_{\rm rp}^2\right) \frac{d^2 v_{\rm cs}(t)}{dt^2} + \omega_{\rm rs}^2 \omega_{\rm rp}^2 v_{\rm cs}(t) = \omega_{\rm rs}^2 \omega_{\rm rp}^2 (V_{\rm in} - aV_o)$
$t_1 \le t < t_2$	$\frac{d^4 v_{\rm cs}(t)}{dt^4} + \left(\omega_m^2 + \omega_{sp2}^2 + \omega_{\rm rp}^2\right) \frac{d^2 v_{\rm cs}(t)}{dt^2} + \omega_m^2 \omega_{\rm rp}^2 v_{\rm cs}(t) = \omega_m^2 \omega_{\rm rp}^2 V_{\rm in}$
$t_2 \le t < t_3$	$\frac{d^4 v_{\rm cs}(t)}{dt^4} + \left[\left(1 + \frac{C_s}{C_{sp}}\right)\omega_m^2 + \omega_{sp2}^2 + \omega_{\rm rp}^2\right] \frac{d^2 v_{\rm cs}(t)}{dt^2} + \left(1 + \frac{C_s}{C_{sp}}\right)\omega_m^2 \omega_{\rm rp}^2 v_{\rm cs}(t) = 0$
Intervals	ZVS area 2 (secondary-side CCM)
$**t_0 \le t < t_1$	$\frac{d^4 v_{\rm cs}(t)}{dt^4} + \left(\omega_{\rm rs}^2 + \omega_{sp1}^2 + \omega_{\rm rp}^2\right) \frac{d^2 v_{\rm cs}(t)}{dt^2} + \omega_{\rm rs}^2 \omega_{\rm rp}^2 v_{\rm cs}(t) = \omega_{\rm rs}^2 \omega_{\rm rp}^2 (V_{\rm in} - aV_o)$
$t_1 \le t < t_2$	$\frac{d^4 v_{\rm cs}(t)}{dt^4} + \left[\left(1 + \frac{C_s}{C_{sp}}\right)\omega_{\rm rs}^2 + \omega_{sp1}^2 + \omega_{\rm rp}^2\right] \frac{d^2 v_{\rm cs}(t)}{dt^2} + \left(1 + \frac{C_s}{C_{sp}}\right)\omega_{\rm rs}^2 \omega_{\rm rp}^2 v_{\rm cs}(t) = -\omega_{\rm rs}^2 \omega_{\rm rp}^2 aV_o$
$t_1 \le t < t_2$	$\frac{d^4 v_{\rm cs}(t)}{dt^4} + \left(\omega_{\rm rs}^2 + \omega_{sp1}^2 + \omega_{\rm rp}^2\right) \frac{d^2 v_{\rm cs}(t)}{dt^2} + \omega_{\rm rs}^2 \omega_p^2 v_{\rm cs}(t) = \omega_{\rm rs}^2 \omega_{\rm rp}^2 (V_{\rm in} + aV_o)$
$C_{sp} = \frac{C_s + C_p}{C_s C_p}, \omega_{\rm rs} = \frac{1}{\sqrt{L_s C_s}}, \omega_{sp1} = \frac{1}{\sqrt{L_s C_p}}, \omega_{\rm rp} = \frac{1}{\sqrt{L_p C_p}}, \omega_m = \frac{1}{\sqrt{(L_s + L_m) C_s}}, \omega_{sp2} = \frac{1}{\sqrt{(L_s + L_m) C_p}}, a = \frac{N_1}{N_2}$	

*Following to previous Mode 8 in Fig. 10, **Following to previous Mode 8 in Fig. 11.

Based on those circuit parameters of the series- and antiresonant tanks, the input impedance characteristics of the *LLC* and *LLC-LC* converters are depicted in Fig. 12 for the rated output power and voltage condition. Due to the circuit parameters designed above, the *LLC-LC* converter exhibits the comparable characteristics to those of the *LLC* converter in ZVS area 1.

V. EXPERIMENTAL RESULTS AND EVALUATIONS

A. Specification of Prototype

The performances of the proposed *LLC-LC* converter are evaluated in experiment using a 2.5-kW laboratory prototype by comparison with an *LLC* converter prototype. The exterior

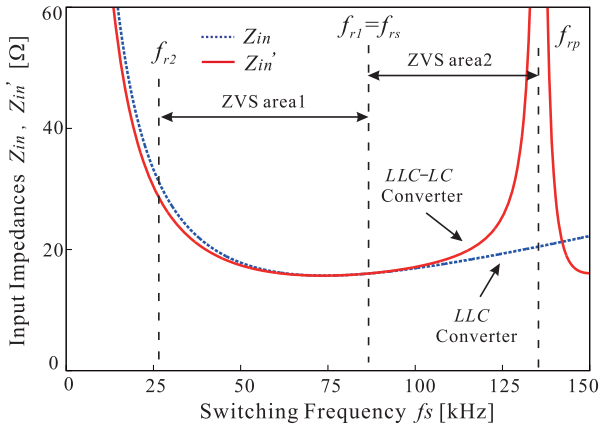

Fig. 12. Input impedance characteristics of the *LLC* and *LLC-LC* converters with the circuit parameters based on the design procedure.

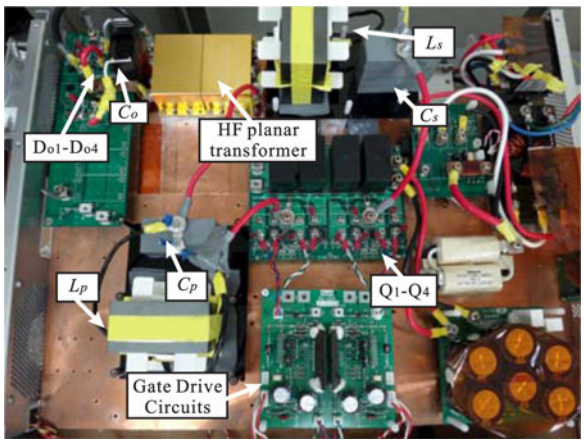

Fig. 13. Exterior appearance of the *LLC-LC* converter prototype.

appearance of the proposed converter prototype with an HF planer transformer is depicted in Fig. 13, and the circuit parameters and specifications which are introduced in Section IV are listed in Table II, respectively. The superjunction-power MOSFETs (IXYS IXKN 40N 60C: 600 V–40 A) are applied for Q_1–Q_4, while the fast recover diodes (IXYS DSEI 2x31-06C: 600 V–60 A) are implemented for D_{o1}–D_{o4}.

B. Soft-Switching Performance

The switching waveforms of the *LLC-LC* converter prototype under a heavy-load condition (80% output power) are shown in Fig. 14. ZVS and ZCS commutations can be actually confirmed from those results.

Fig. 15 shows the switching waveforms under a light-load condition (20% output power), which proves ZVS and ZCS commutations can achieve for the light-load area as well.

The switching voltage and current waveforms for the open-circuit load condition are depicted in Fig. 16. ZVS commutations of the active switches due to i_m can be confirmed from those waveforms. Thus, it is verified the advantageous characteristics of the *LLC* converter can be maintained in the *LLC-LC* converter.

TABLE II
CIRCUIT PARAMETERS AND SPECIFICATION OF PROTOTYPES

Item,Symbol	Value
Input dc voltage V_{in}	220 V
Rated output voltage V_o	240 V
Rated output power P_o	2.5 kW
HF transformer windings turns ratio $a(=N_1/N_2)$	$1(=6/6)$
HF transformer magnetizing inductance L_m	190 μH
Series resonant-tank inductor L_s	16 μH
Series resonant capacitor C_s	170 nF
Anti-resonant inductor L_p	2.5 μH
Anti-resonant capacitor C_p	550 nF
Lossless snubber capacitors $C_r = C_{1-4}$	1 nF
Output smoothing capacitor C_o	20 μF
First series-resonant frequency (LLC) f_{rs}	90 kHz
Second series-resonant frequency(LLC) f_{rm}	30 kHz
First series-resonant frequency (LLC-LC) f_{r1}	86 kHz
Second series-resonant frequency(LLC-LC) f_{r2}	27 kHz
Anti-resonant frequency f_{rp}	135 kHz

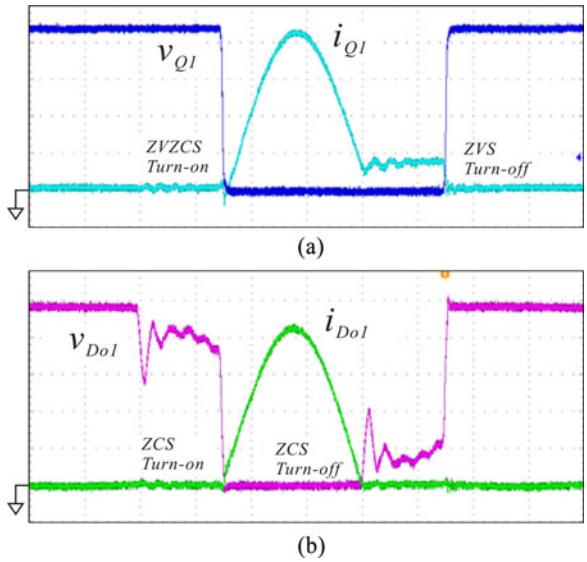

Fig. 14. Observed waveforms of the *LLC-LC* converter prototype at $f_s = 61$ kHz and $P_o = 2$ kW. (a) Active switch Q_1. (b) Rectifying diode D_{o1} (100 V/div, 5 A/div, 2 μs/div).

The switching voltage and current waveforms for the short-circuit load condition are demonstrated in Fig. 17. The peak currents through the active switches and diodes are suppressed as less than the peak value of 20 A for the heavy-load condition of Fig. 14 by setting f_s to f_{rp}, while ZVS and ZCS operations still maintain. Furthermore, the switching currents, which are identical with the primary side i_p, exhibit the 90° lagging-phase behavior; thereby, the inductive impedance characteristics of the antiresonant tank is actually confirmed.

The enlarged waveforms and voltage–current trajectory are revealed in Fig. 18 under the condition of full load (100% output power). The ZVS and ZCS turn-on of the active switch is toward the critical condition around the full load because the switching frequency approaches gradually the second resonant frequency f_{rm}, the boundary point of inductive and capacitive load areas

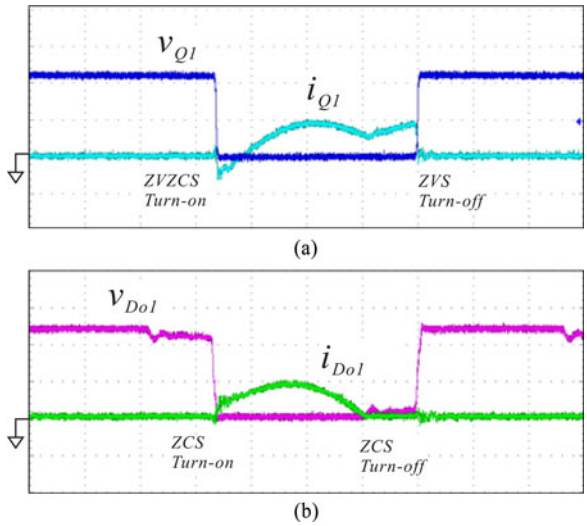

Fig. 15. Observed waveforms of the *LLC-LC* converter prototype at $f_s = 67\,\mathrm{kHz}$ and $P_o = 0.5\,\mathrm{kW}$. (a) Active switch Q_1. (b) Rectifying diode D_{o1} ($100\,\mathrm{V/div}$, $5\,\mathrm{A/div}$, $2\,\mu\mathrm{s/div}$).

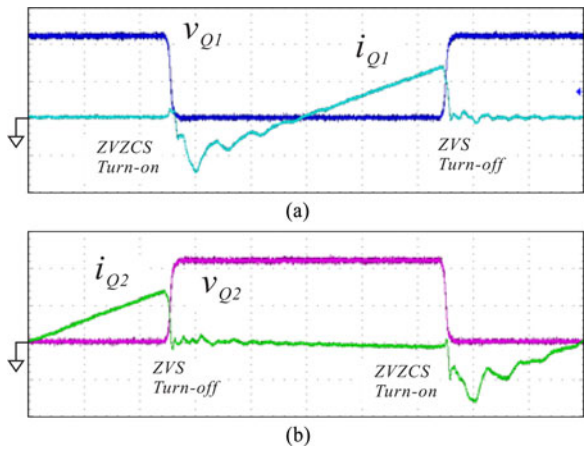

Fig. 16. Observed waveforms of the *LLC-LC* converter under the open-circuit load condition at $f_s = 100\,\mathrm{kHz}$. (a) Active switch Q_1. (b) Active switch Q_2 ($100\,\mathrm{V/div}$, $2\,\mathrm{A/div}$, $1\,\mu\mathrm{s/div}$).

of the *LLC-LC* converter. However, the ZVS transitions can be still maintained by adjusting the dead time interval; thereby, no significant current surge appears at the turn-off transitions. Thus, the switching power losses are well reduced as compared to the hard switching behavior. The margin of inductive load area for the load power variations exhibits the tradeoff relation between the ZVS performance and circulating current in the primary-side power stage. It should be noted here the small part of voltage and current overlapping in the first quadrant of Fig. 18(b) is due to charging of the parasitic output capacitance at the turn-off transition of power MOSFET.

C. Steady-State Characteristics

The steady-state characteristics of the proposed converter are compared with the *LLC* converter under the open-loop control in the experiment.

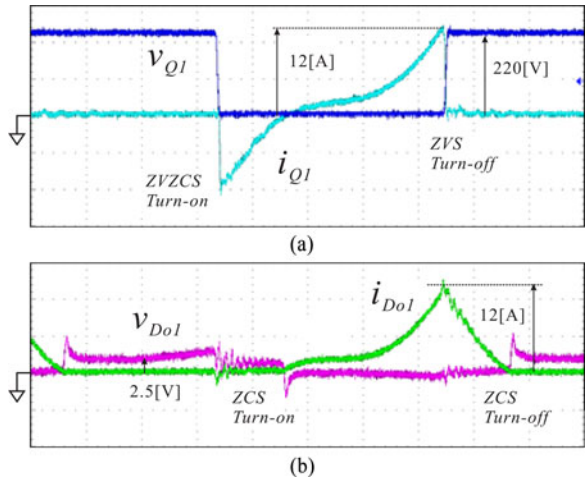

Fig. 17. Observed voltage and current waveforms of the *LLC-LC* converter under the short-circuit load condition at $f_s = 131\,\mathrm{kHz}$. (a) Active switch Q_1 ($50\,\mathrm{V/div}$, $5\,\mathrm{A/div}$, $1\,\mu\mathrm{s/div}$). (b) Rectifying diode D_{o1} ($5\,\mathrm{V/div}$, $5\,\mathrm{A/div}$, $1\,\mu\mathrm{s/div}$).

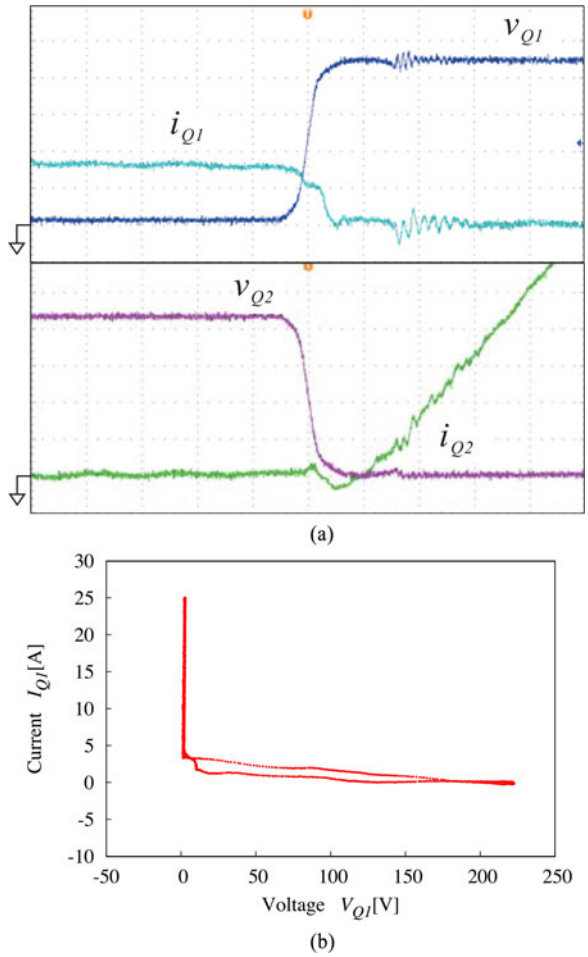

Fig. 18. Commutation of the active switch at the boundary of inductive and captive load areas at $f_s = 60\,\mathrm{kHz}$ and $P_o = 2.5\,\mathrm{kW}$. (a) Switching waveforms ($50\,\mathrm{V/div}$, $2\,\mathrm{A/div}$, $200\,\mathrm{ns/div}$). (b) Voltage and current trajectory.

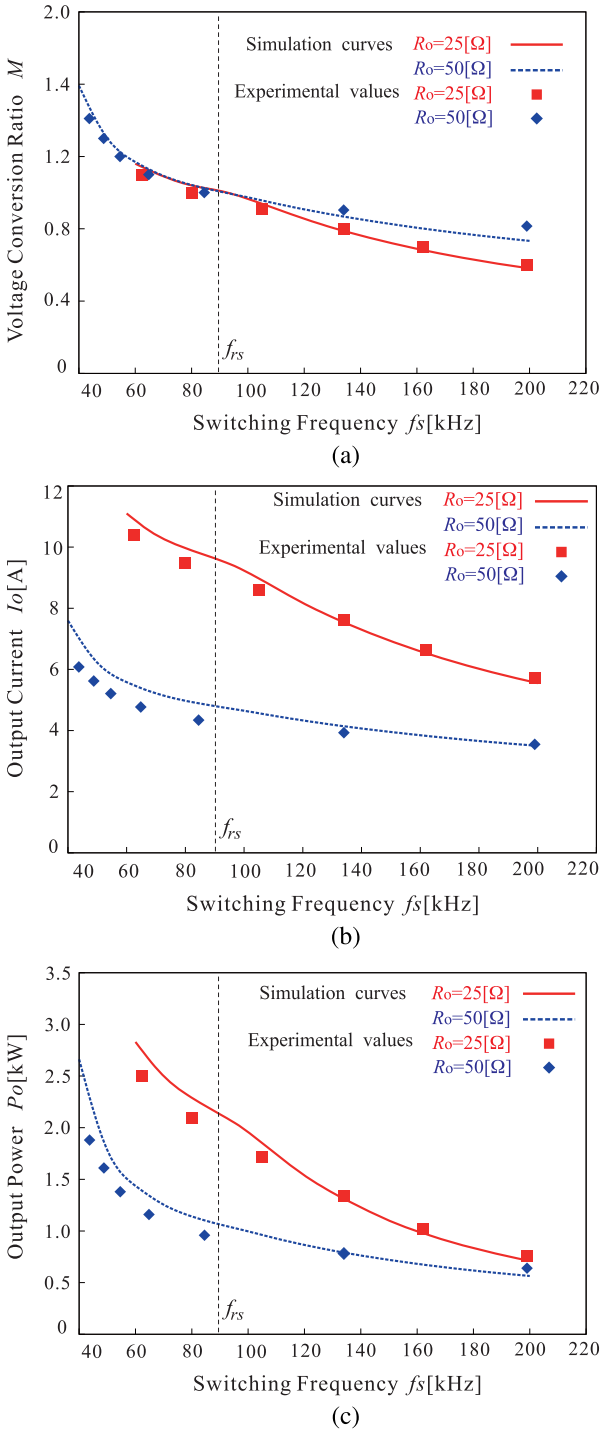

Fig. 19. Measured steady-state characteristics of the *LLC* converter under the open-loop control: (a) M–f_s, (b) I_o–f_s, and (c) P_o–f_s ($f_{\rm rs} = 90\,{\rm kHz}$ and $f_{\rm rm} = 30\,{\rm kHz}$).

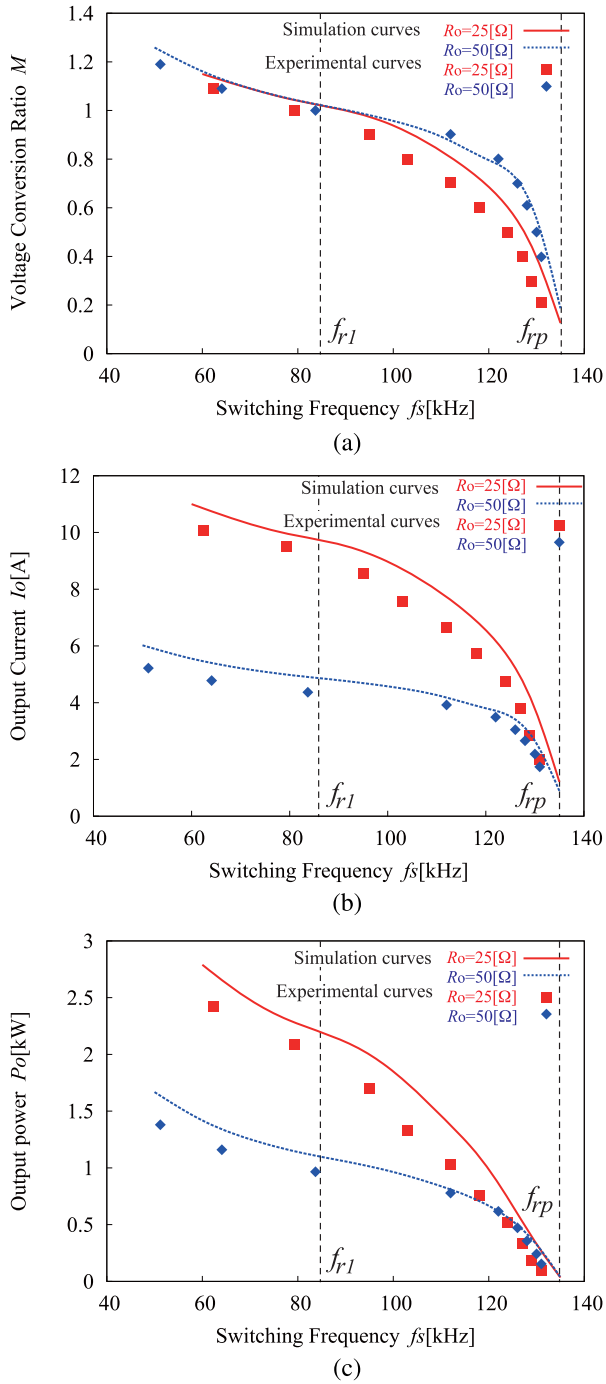

Fig. 20. Measured steady-state characteristics of the *LLC-LC* converter under the open-loop control: (a) M–f_s, (b) I_o–f_s, and (c) P_o–f_s ($f_{r1} = 86\,{\rm kHz}$, $f_{r2} = 27\,{\rm kHz}$, and $f_{\rm rp} = 135$).

The measured steady-state characteristics of the *LLC* converter prototype are demonstrated in Fig. 19 for variations of R_o in comparison with the simulation values. In ZVS area 1 ($30\,{\rm kHz} \le f_s \le 90\,{\rm kHz}$), the voltage conversion ratio varies from 1.0 to 1.2 by changing f_s between 44 and 86 kHz. Consequently, the output power is regulated in the range of 1.0–2.5 kW. In contrast to that, the voltage conversion ratio changes from 1.0 to 0.6 even by extending f_s from 86 to 200 kHz in ZVS area 2. Thus, the minimum output power is 0.65 kW (26% output power) at $f_s = 200\,{\rm kHz}$ ($F_{\rm rs} = 2.3$).

The measured steady-state characteristics of the *LLC-LC* converter are presented in Fig. 20 with the same parameters of R_o for the *LLC* converter. Compared to the results in Fig. 19, it can be understood that the wider range of output voltage and power as well as current can be controlled in the *LLC-LC* converter: $0.2 \le M \le 1.2$ and $0.1\,{\rm kW} \le P_o \le 2.5\,{\rm kW}$. In particular, the

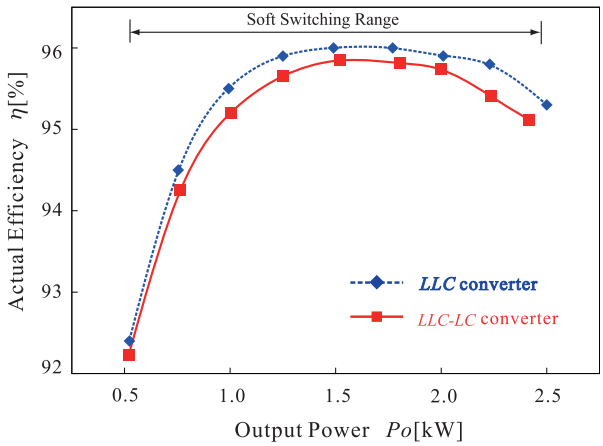

Fig. 21. Comparison on the actual efficiencies between *LLC* and *LLC-LC* converters ($V_o = 240\,\mathrm{V}$).

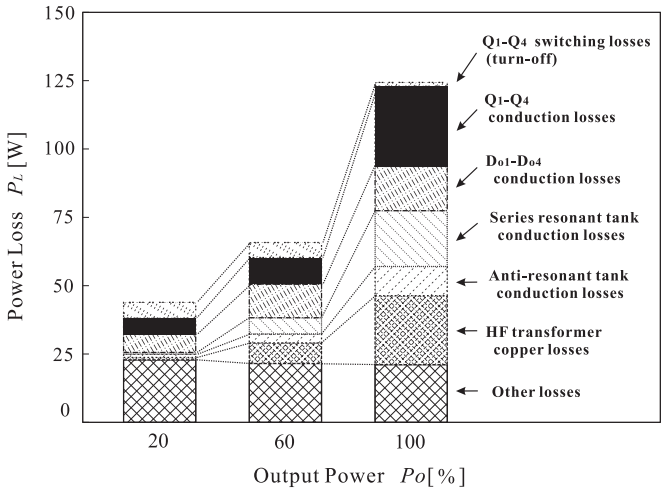

Fig. 22. Power loss analysis of the *LLC-LC* converter prototype ($V_o = 240\,\mathrm{V}$).

PFM adaptable range is successfully extended to ZVS area 2 with the smaller frequency variation 86–131 kHz; consequently, the minimum output power is obtained as 0.1 kW (less than 10% output power) at $f_s = 131\,\mathrm{kHz}$ ($F_{\mathrm{rs}} = 1.5$). It might be hard to perform the voltage regulation practically around f_{rp} in ZVS area 2 under the light-load condition.

D. Actual Efficiency and Power Loss Analysis

The actual power conversion efficiencies of the *LLC* and *LLC-LC* converters are compared under the rated output voltage condition of $V_o = 240\,\mathrm{V}$ in Fig. 21. It should be remarked herein that the soft-switching operations (ZVS in $\mathrm{Q_1}$–$\mathrm{Q_4}$, and ZCS in $\mathrm{D_{o1}}$–$\mathrm{D_{o4}}$) can achieve through the whole output power in both the resonant converters. The maximum efficiency of the *LLC-LC* converter is measured at $P_o = 1.5\,\mathrm{kW}$ (60% output power), and high efficiency over 95% can be maintained in the power range 1–2.5 kW (40–100% output power) due to the wide range of soft-switching operation. The efficiency drop from the *LLC* converter is suppressed within 0.4% through the whole load power. It can be said no significant power loss emerges from the antiresonant tank; thereby, effectiveness of the design process that is introduced in Section IV is verified.

The power loss analysis of the *LLC-LC* converter prototype is depicted in Fig. 22. Note here that the turn-on power loss of the active switch is neglected due to the ZVS and ZCS commutation, so is the turn-on power loss of rectifying diode due to the ZCS operation. The iron power loss of the HF planar transformer and wire copper loss of the prototype are included in the "Other losses." It can be observed from the power loss breakdown that the turn-off power losses of $\mathrm{Q_1}$–$\mathrm{Q_4}$ keep in a low profile by the effect of ZVS, and the turn-off power losses of $\mathrm{D_{o1}}$–$\mathrm{D_{o2}}$ as well as the reverse recovery currents can also be minimized owing to the ZCS over the wide range of load power. The turn-off power loss at the full load condition that corresponds to the boundary of inductive and capacitive load regions accounts for a small part of the total amount as pointed out in Fig. 18. The conduction loss of the antiresonant tank is measured 3–9% of the total power loss at each output power setting when the converter operates in ZVS area 1.

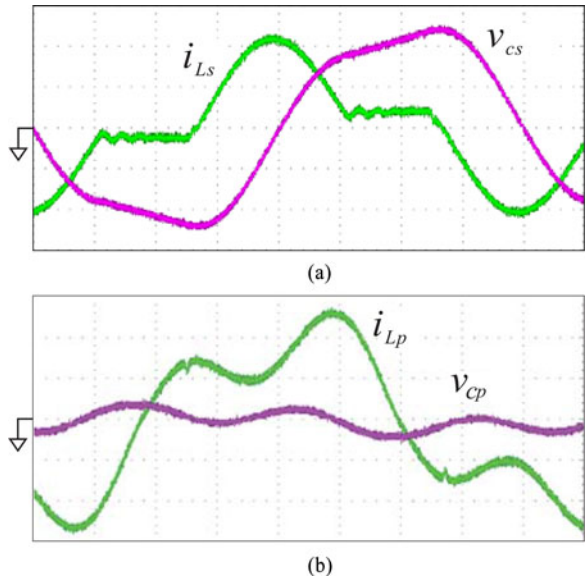

Fig. 23. Observed waveforms of the series- and antiresonant tanks in the *LLC-LC* converter at $P_o = 2\,\mathrm{kW}$, $M = 1.1$, and $f_s = 61\,\mathrm{kHz}$. (a) Series-resonant tank. (b) Antiresonant tank ($100\,\mathrm{V/div}$, $10\,\mathrm{A/div}$, $2\,\mu\mathrm{s/div}$).

E. State-Plane Analysis of Resonant Tanks

The power and energy levels of each resonant tank can be portrayed by the state-plane trajectory, which helps to understand the proprieties of the *LLC-LC* resonant tanks.

The observed voltage and current waveforms in the series- and antiresonant tanks are shown in Fig. 23 under the condition $P_o = 2\,\mathrm{kW}$, $f_s = 61\,\mathrm{kHz}$, and $M = 1.1$. The relevant state-plane trajectories of series- and antiresonant tanks are depicted in Fig. 24 as compared to the calculation result, which is obtained from Table I and (18). Fig. 24(a) exhibits the elliptical trace with respect to v_{cs}, which verifies the series resonance in the *LLC-LC* converter. Fig. 24(b) displays the elliptical trace with respect to i_{Lp}, which represents the antiresonance. The trajectory of Fig. 24(a) is greater than that of Fig. 24(b);

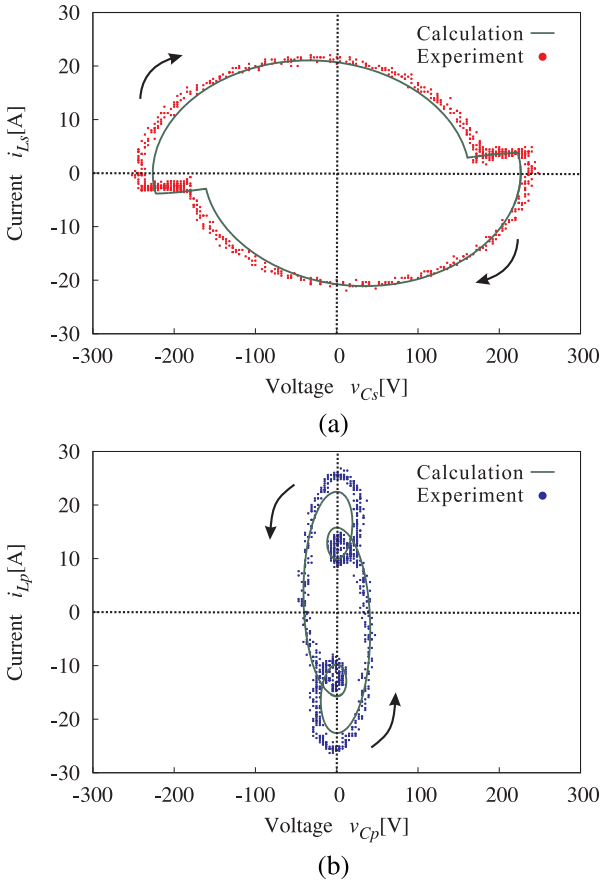

Fig. 24. Measured and calculated state-plane trajectories of the resonant tanks in the *LLC-LC* converter at $P_o = 2\,\mathrm{kW}$, $M = 1.1$, and $f_s = 61\,\mathrm{kHz}$. (a) Series-resonant tank. (b) Antiresonant tank.

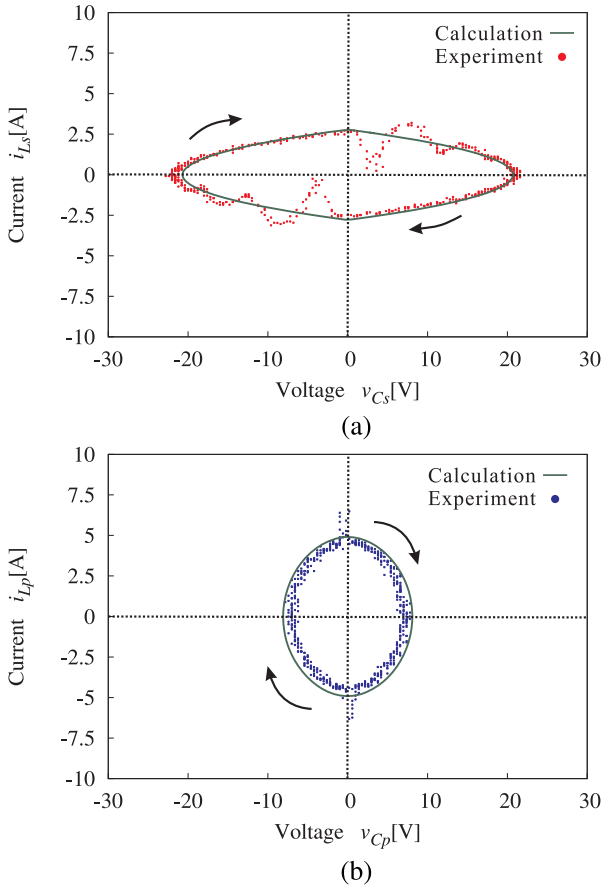

Fig. 26. Measured and calculated state-plane trajectories of the series- and antiresonant tanks under the open-circuit load condition. (a) Series-resonant tank. (b) Antiresonant tank.

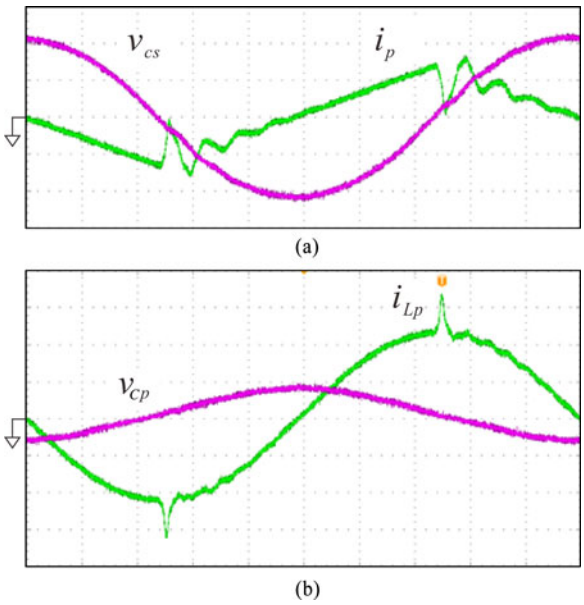

Fig. 25. Observed waveforms of the series- and antiresonant tanks under the open-circuit load condition at $f_s = 100\,\mathrm{kHz}$. (a) Series-resonant tank. (b) Antiresonant tank ($10\,\mathrm{V/div}$, $5\,\mathrm{A/div}$).

accordingly, it is proven that the series-resonant tank operates more effectively under the normal load condition.

The voltage and current waveforms of the series- and antiresonant tanks under the open-circuit load condition are depicted in Fig. 25. The state-plane trajectories corresponding to those waveforms are shown in Fig. 26. It can be confirmed from the results that the trajectories shrink both in the series- and antiresonant tanks as compared to those of the normal load condition in Fig. 24.

The voltage and current waveforms of the series- and antiresonant tanks under the short-circuit load condition are depicted in Fig. 27. In addition, the state-plane trajectories corresponding to those waveforms are shown in Fig. 28. It can be observed from those figures that the trajectories of series-resonant tank are reduced well under that of the normal load condition in Fig. 24(a). On the other hand, the trajectories of the antiresonant tank swell out as compared to those of Fig. 24(b), which verifies the performance of the antiresonant tank under the short-circuit load condition.

It should also be remarked in the state-plane analysis that no dc voltage appears in either v_{cs} or v_{cp} of Figs. 24, 26, and 28; accordingly, high efficiency can keep through the entire load conditions in the *LLC-LC* converter.

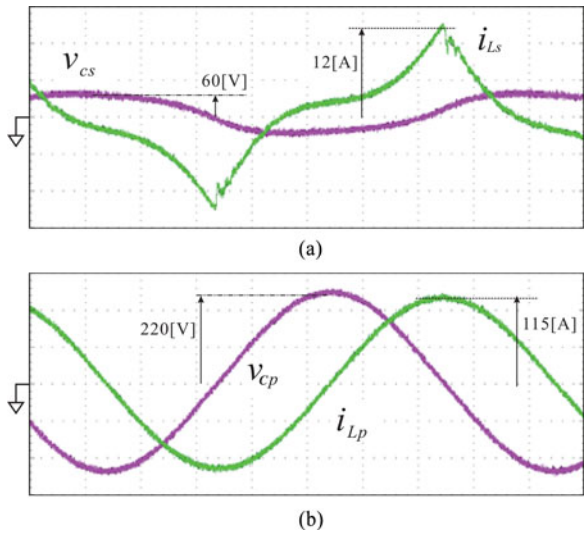

Fig. 27. Observed waveforms of the series- and antiresonant tanks under the short-circuit load condition at $f_s = 131\,\mathrm{kHz}$. (a) Series-resonant tank ($100\,\mathrm{V/div}$, $5\,\mathrm{A/div}$). (b) Antiresonant tank ($100\,\mathrm{V/div}$, $50\,\mathrm{A/div}$).

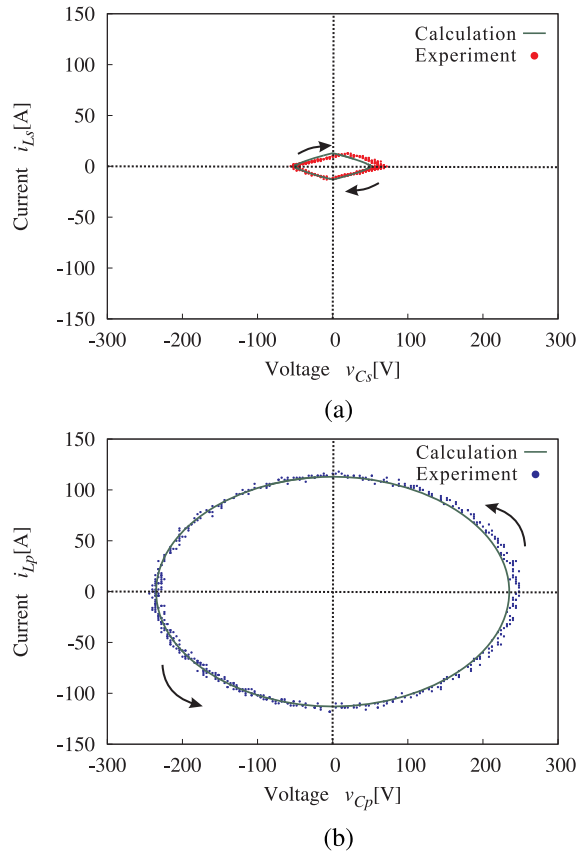

Fig. 28. Measured and calculated state-plane trajectories of the series- and antiresonant tanks under the short-circuit load condition. (a) Series-resonant tank. (b) Antiresonant tank.

VI. Conclusion

This paper presents an *LLC-LC* resonant soft-switching dc–dc converter with the sensitivity-improved PFM scheme. The OCP for the short-circuit load condition as well as a start-up interval can be ensured in a smaller band of switching frequency, which is designed on the basis of the series- and antiresonant frequencies. The circuit topology and the PFM scheme are also effective for extending the voltage regulation area especially in the buck mode, which is advantageous for realizing a single-stage buck and boost voltage regulations in the resonant converter.

The steady-state characteristics of a voltage conversion ratio and output power have been theoretically described in the frequency-domain analysis with the FHA strategy. In addition, the design guideline of series- and antiresonant tanks as well as the resonant frequencies for the *LLC-LC* converter has been introduced with consideration for the input impedance and the resonant tank characteristics impedances.

The performances of the *LLC-LC* converter have been demonstrated in experiment of the 2.5-kW prototype under the open-loop control. The excellent characteristics of the proposed converter have been clarified as follows.

1) A voltage conversion ratio M can be extended to the wider range between $M = 0.2$ and $M = 1.2$, thereby enlarging the output power regulation range between 2.5 and $0.1\,\mathrm{kW}$ in the *LLC-LC* converter. The voltage step-down ratio increases by triple, and the output power range can improve by 30% as compared to an *LLC* converter.
2) The current through the power devices and components under the short-circuit load condition are reduced 44% as compared to the full-load condition owing to the effect of the antiresonant tank in the *LLC-LC* converter, where the antiresonant frequency is designed in just 50% higher than the first resonant frequency.
3) Energy of the antiresonant tank as well as the series-resonant tank is visualized by the state-plane trajectories of the resonant inductor currents and resonant capacitor voltage. The observed trajectories actually demonstrate the practical effect of the antiresonant tank, which helps to design the circuit parameters with consideration for the power loss in the resonant tanks.
4) Wide-range soft commutations in the active switches and rectifier diodes attain from the full-load ($Po = 2.5\,\mathrm{kW}$) to no-load condition, keeping the same switching performance as the *LLC* converter. This excellent property contributes for achievement of the maximum efficiency 95.9% at $Po = 1.5\,\mathrm{kW}$, even by taking power consumption of the antiresonant tank into account.
5) The efficiency of the *LLC-LC* converter is comparative with the *LLC* converter, and it might be more advantageous over the two-stage *LLC* converter with a front-end dc voltage regulator.

Implementation of a high-performance controller and evaluations on the transitional behaviors of the *LLC-LC* converter will be a future challenge of this research.

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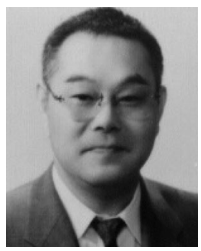

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