A Quasi-Resonant Current-Fed Converter With Minimum Switching Losses

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***Abstract*—A quasi-resonant dc–dc converter with high voltage gain and low current stresses on switches is proposed in this paper. This converter preserved inherent advantages of current-fed structures, for instance, zero magnetizing dc offset, low input ripple, and low transformer turn ratio. Moreover, by employing the active-clamp circuit, the voltage spikes across the main switch, due to the existence of leakage inductance of the isolating transformer, is absorbed, and switches work in zero voltage switching. Since quasi-resonant switching strategy is employed, turn-off current (TOC) and losses of switches are considerably reduced. Because of zero current switching (ZCS), reverse recovery problem of diodes is alleviated. Experimental results on a 150-W prototype are provided to validate the proposed concept.**

***Index Terms*—Current-fed, half-bridge, high step-up converter, PWM controlled quasi-resonant converter, quasi-resonant converter (QRC), soft switching.**

I. Introduction

MAJORITY of renewable sources such as photovoltaic (PV) panels and fuel cells (FC) stacks have low-voltage and high-current characteristics, and require low current ripple [1]–[6]. In order to utilize these power sources, a dc–dc converter with voltage isolation, low input current ripple, and high step-up capabilities resulting in high efficiency is required. In addition, high switching frequency is essential for having a high-power density conversion. Even so, high switching frequency causes some problems such as high switching losses, high voltage and/or current spikes, and electromagnetic interference. To eliminate these problems, soft-switching operation is employed in dc–dc converters [2]–[14]. In order to provide the soft-switching condition, an auxiliary switch is added to a regular dc–dc converter [15]–[17]. The converters which are used for renewable energy resources can be classified into two major categories, which are current-fed and voltage-fed converters. Voltage-fed converters have many advantages like, low switch voltage and simple implementation, but they need high transformer turn ratio [18]. Consequently, the leakage inductance will be large, and it causes high voltage spikes on the switches. However, some important advantages of the current-fed converters are high voltage gain, low input current, galvanic isolation between input and load, and neutral protection in short-circuit fault [19]. These converters are more suitable for high-power and low-voltage applications, for instance, FC's and PV's [2]–[4], [13], [18]–[21]. The most utilized topologies for current-fed converters are full-bridge, half-bridge, and push–pull converters [22]. Full-bridge converters are used in high-power applications. In [23], a full-bridge current-fed converter with active clamp is introduced. Although zero voltage switching (ZVS) is employed for main switches, active clamp has a high current, and its switching frequency is three times the main switching frequency [24], but by employing ZCS turn-off of primary switches and ZVS turn-on of secondary switches in a wide variation of output power in [3], switching low efficiently is reduced which allows the converter to operate in high frequencies. The proposed push–pull converter in [25] adopted the minimum number of components. However, it operates under hard-switching condition. So, the voltage spikes on switches increase converter losses dramatically. In [26], an active-clamped current-fed push–pull converter is introduced which adopted ZVS and lossless clamp circuit, which have improved its efficiency. Although a current-fed push-pull converter has been proposed in [4] which adopted ZVS and ZCS for switches, it suffers from high voltage stress on switches. On the other side, the component number of converter and its complexity have increased which increases the cost. *L*-type half-bridge current-fed converters have the lowest transformer turns ratio which causes low ohmic loss. Although they require additional snubber circuits, they cannot operate under ZVS condition for the wide range of input voltage and load variation [22]. In [27]–[29], *LLC* resonant converters are proposed which are well suited for high-voltage and high-frequency applications. Nevertheless, they have good performance just around the resonant frequency, so they cannot be used in wide-input-voltage-variable applications. To obtain high voltage gain, transformer magnetizing inductance must be small which rises magnetizing current as well as higher conduction and core losses.

In this paper, a half-bridge current-fed quasi-resonant is proposed (see Fig. 1). An active-clamp circuit is added to a conventional boost converter. Adopting active-clamp circuit introduces soft switching for the converter. A high-frequency transformer provides galvanic isolation and improves voltage gain. Moreover, a voltage doubler circuit at the output eliminates the reverse-recovery problem of the output diode and doubles the voltage gain. Furthermore, the converter operates in a quasi-resonant condition. In this situation, switches current stress and loss of switches will be reduced to its minimum value, while the converter still can be controlled by the pulse width modulation (PWM) method. Actually, the proposed converter adopts the

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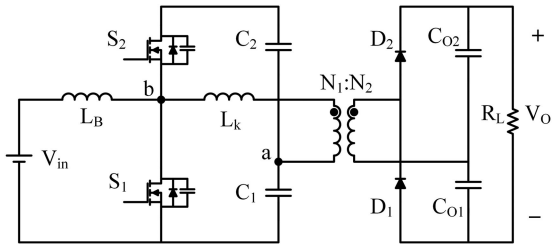


Fig. 1. Proposed quasi-resonant converter.

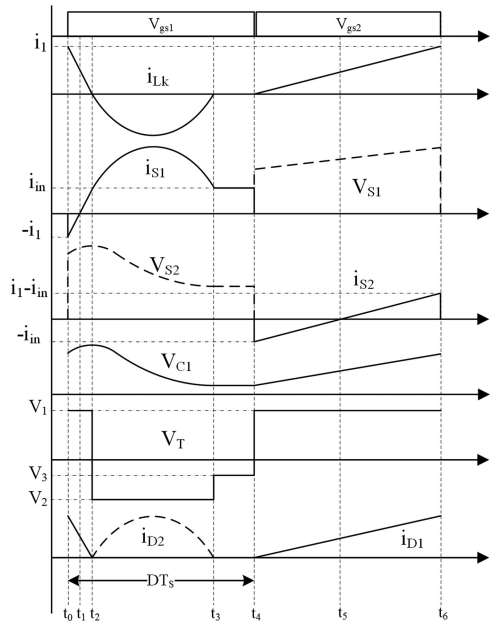


Fig. 2. Operating waveforms of the quasi-resonant converter.

soft-switching merit of resonant converters and control and implementation simplicity of the conventional PWM converters. By reducing the switching loss of the proposed converter, it can operate in higher switching frequencies. Also, the number of the components is low. Consequently, the proposed converter's volume and weight of the proposed converter are decreased, and its power density is increased. Almost the same topology is presented in [30] as a dual active bridge converter for aerospace application. This converter retains soft switching in a wide range of load variation, but switches suffer from high switches current stress. The same topologies are proposed in [31] and [32]. The converter in [31] is proposed for plug in hybrid electric vehicle, and it is bidirectional. However, the same as one in [30], it has high current stress of switches. The converter in [32] is proposed for PV system. Although it operates in resonant mode, main switch has zero current switching (ZCS) in both turn-on and turn-off moments, and auxiliary switch operates in hard switching condition, which result in high switching loss.

II. Operation Principle and Analysis

The proposed converter circuit is shown in Fig. 1. Input boost circuit consists of inductance L_B and switch S_1. Leakage inductance of transformer in primary side is modeled as L_k and resonant circuit is provided by C_1 and leakage inductance L_k. Active-clamp circuit is made of C_2 and S_2. In secondary side of the transformer, diodes D_1 and D_2 make a full-wave rectifier which provide voltage doubler circuit with capacitors C_{o1} and C_{o2} in the output.

Due to ZCS on the output diodes, fast diodes are not necessary anymore. Moreover, load resistance is modeled as R_L. N_1 and N_2 are primary and secondary of transformer turn ratio, respectively. "*n*" is defined as $n = N_2/N_1$. Also, f_s and f_r are switching and resonant frequency, respectively.

The operation of the proposed converter is described through six intervals. In Fig. 2, important currents and voltage curves are plotted, and circuit operating modes are shown in Fig. 3. At the time before t_0, S_2 is turned ON. It is assumed that input current has constant value I_in because inductance L_B is large enough to alleviate input current ripple. The other assumption is that voltage of C_2 has constant value V_{C2}.

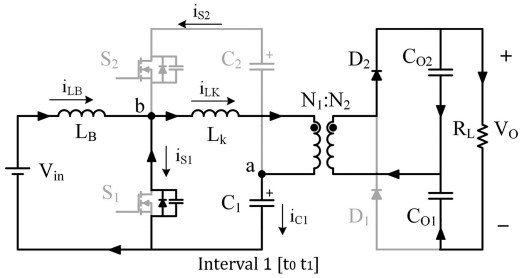
1) Interval 1 [t_0 t_1]
At t_0, S_2 goes OFF, and difference of input and the transformer current charges and discharges parasitic capacitors of S_2 and S_1, respectively. After that, the current flows through the body diode of switch S_1. As long as this current flows through the body diode, voltage across S_1 is zero. As a result, to achieve ZVS, gate pulse can be applied. This interval will finishes when reverse current of S_1 reaches to zero.
2) Interval 2 [t_1 t_2]
At t_1, current of switch S_1 changes its direction and flows through the switch because S_1 has been turned ON in the previous interval. I_in circulates through S_1 and the source, and V_in charges input inductor L_B. Via transformer primary winding, voltage V_{o2}/n has been applied to the C_1 and L_k since t_0. i_{lk} decreases to zero and this interval will finishes. In the output, D_2 is conducting. So

$$-i_1 = \frac{-V_{o2}/n - V'_{C1}}{L_k} d_1 T_s \tag{1}$$

$$d_1 T_s = t_2 - t_0. \tag{2}$$

V'_{C1} is the voltage of capacitor C_1 at the time t_0.
3) Interval 3 [t_2 t_3]
At t_2, the transformer current direction changes and voltage of output capacitor C_{o1} is reflected via transformer to the primary side of transformer and C_1 and L_k make resonance. This interval will finish when i_{lk} reaches to zero. During this interval, current of input inductance rises as a result of V_in across the input inductance L_B. Because of the change in direction of transformer current in this interval, direction of secondary current is also changed, so D_1 is conducting at output doubler circuit, and supplies output capacitor C_{o1}. For this interval,

$$i_{lk}(t) = \frac{V_{o1}/n - V'_{C1}}{\sqrt{\frac{L_k}{C_1}}} \sin \omega_r (t - t_2) \tag{3}$$



$$d_2 T_s = t_3 - t_2 \tag{4}$$

$$i_{lk}(t_3) = \frac{V_{o1}/n - V'_{C1}}{\sqrt{\frac{L_k}{C_1}}} \sin(\omega_r d_2 T_s) = 0 \tag{5}$$

$$d_2 T_s = \pi \sqrt{L_k C_1}. \tag{6}$$

V_{o1}/n is voltage of capacitor C_{o1} which is reflected to the primary side of the transformer.

4) Interval 4 [t_3 t_4]
When the current of transformer reaches to zero, this interval begins. Capacitor C_1 and inductor L_k transfer their energy to the output and the operation of converter enters discontinuous conduction mode. Voltage across the transformer and capacitor C_1 reaches to V_3, but the current of S_1 remains I_{in} during the whole of this entire interval and the power supply charges the inductor L_B. Based on the diagrams shown in Fig. 2,

$$d_3 T_s = t_4 - t_3 = (1 - D) T_s - d_1 T_s - d_2 T_s \tag{7}$$

and by applying volt–second balance to the transformer's primary winding:

$$d_1 V_1 + d_3 V_3 = d_2 V_2 \tag{8}$$

$$V_3 = \frac{d_2 V_2 - d_1 V_1}{d_3}. \tag{9}$$

At the output, since secondary current is zero, diodes are turned OFF. So in this interval, output capacitors (C_{o1} and C_{o2}) supply the load.

5) Interval 5 [t_4 t_5]
At t_4, S_1 turns off, and difference of input and the current of transformer charges and discharges parasitic capacitors of S_1 and S_2, respectively. After that the current flows through the body diode of switch S_2 and charges C_2. As long as the body diode is conducting, voltage across S_2 is zero, and gate pulse can be applied to achieve ZVS. In output, D_2 is conducting and supplies output capacitor C_{o2}. When reverse current of S_2 reaches zero, this interval will finish.

6) Interval 6 [t_5 t_6]
When current of the body diode of S_2 reaches zero, its direction changes, and it flows through switch S_2, which has been turned ON in the previous interval. Just like the previous interval, the current of transformer is rises. Capacitor C_1 has been charged since t_4, because input constant current flows through the transformer.

This Interval finishes by removing gate pulse S_2 gate pulse. The current of transformer rises linearly from 0 to i_1 during the t_4 to t_6 interval. So,

$$i_1 = \frac{V_{C2} - V_{o2}/n}{L_k}(1 - D) T_s \tag{10}$$

$$(1 - D) T_s = t_6 - t_4 \tag{11}$$

where V_{C2} is the voltage of clamp capacitor voltage and V_{o2}/n is the voltage of C_{o2} voltage on the output which was reflected to the primary side of the transformer, and D is the duty cycle of switch S_1.

III. Theoretical Analysis

A. Comparing Switching Losses in Above and Below Resonance Operations

Turn-off and conduction loss of the switches can be calculated by following relations [33]:

$$P_{\text{turn-off}} = \frac{1}{2} V_{\text{turn-off}} i_{\text{turnoff}} \left(\frac{t_r}{T_S} \right) \tag{12}$$

$$P_{\text{conduction}} = R_{\text{on}} I_{\text{rms}}^2 \tag{13}$$

where $V_{\text{turn-off}}$ and $i_{\text{turn-off}}$ are voltage and current of switch at the turn-off moment, respectively, and t_r is the rise time of the switch. In (12), t_r is restricted to the switch's characteristic, but $V_{\text{turn-off}}$ and $i_{\text{turn-off}}$ depend on converter's operation characteristic of the converter. R_{on} is the conduction resistance of switch. So switching losses can be obtained from

$$P_{\text{switching}} = P_{\text{turn-off}} + P_{\text{conduction}}. \tag{14}$$

Resonance operations of converters in above-resonance and below-resonance conditions are discussed in [34], and their advantages and disadvantages are mentioned. Operation of S_1 and S_2 in different resonant mode is depicted in Fig. 4(a), respectively. As shown in Fig. 4(a), S_1 has much more TOC in above-resonance than below-resonance. As a result, operating in above-resonance will cause high switching loss. Fig. 4(b) shows measured turn-off and RMS current of the switch S_1 according to proportional resonance frequency at $D = 0.62$ and $P_o = 150$ W. The two different operation mode sectors are shown. It is clear that in below-resonance condition, TOC is much lower and variation of RMS current in both operation modes is very low.

To achieve minimum switching loss, S_1 has to operate in below-resonance to satisfy the following in-equation:

$$f_{r1} > f_s/2D_{\min} \tag{15}$$

where $D_{\min}$ is the minimum duty cycle, and f_{r1} (resonance frequency for C_1 and L_k) is expressed as follows:

$$f_{r1} = 1/2\pi\sqrt{L_k C_1}. \tag{16}$$

According to (16), if $D_{\min}$ and f_s are assumed 0.35 and 100 kHz, respectively, for S_1 operates in below-resonance condition over whole duty cycle range and has minimum switching losses, its resonant frequency (f_r) has to be slightly above 90 kHz.

Fig. 4(a) shows different resonant operations for switch S_2. By operating in above-resonance, S_2 will have positive TOC. TOC in below-resonance is negative. Consequently, ZVS condition for S_1 will be eliminated and switching loss of S_1 will increase, and reverse recovery loss of S_2 body diode will increase switching loss too. As a result, S_2 should not operate in below-resonance, and has to operate in above-resonance. Also, measured turn-off and RMS current of S_2 is presented in Fig. 4(c). Although in frequencies between 250 and 300 kHz, TOC is low, by decreasing duty cycle, it would be possible for S_2 to enter below-resonance region, leading to an increase in switching loss. Resonance frequency of C_2 and L_k (f_{r2}) should

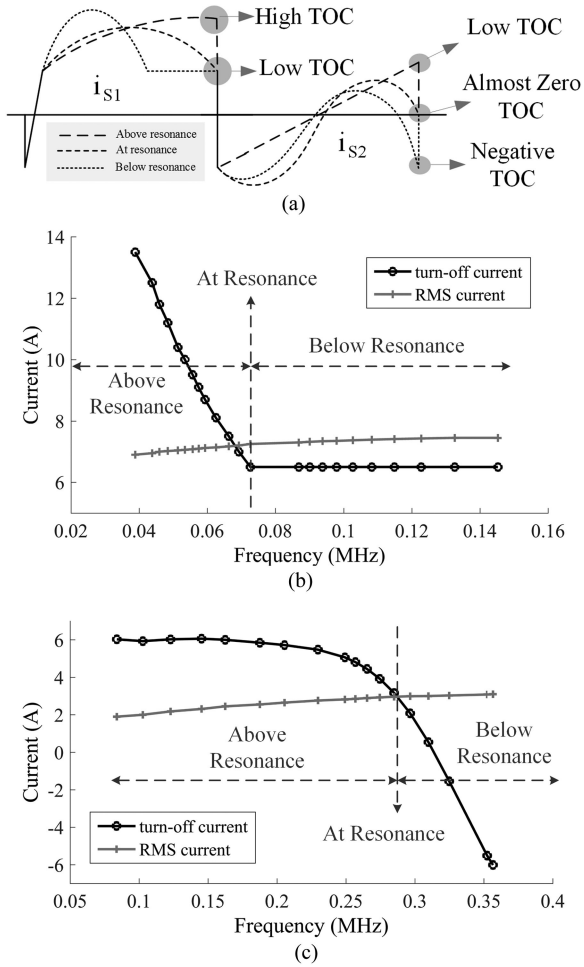


Fig. 4. Analysis of switches current. (a) Different resonant operation of S_1 and S_2. (b) Turn-off and RMS current of S_1. (c) Turn-off and RMS current of S_2.

be chosen far from boundary frequency to ensure the following equation:

$$f_{r2} < f_s/2(1 - D_{\min}). \tag{17}$$

f_{r2} is expressed as

$$f_{r2} = 1/2\pi\sqrt{L_k C_2}. \tag{18}$$

Also, it will be shown that by operating in lower frequencies for f_{r2}, analysis and control of proposed converter will be simpler.

B. ZVS Condition

According to time interval 5, when switch S_1 goes OFF, current of input inductance L_B flows through the body diode of S_2, and parasitic capacitor of S_2 and S_1 are discharged and charged, respectively. So, following condition should be satisfied to ensure ZVS for S_2:

$$-i_{S2}(t_4) = i_{lk}(t_4) - i_{\text{in}}(t_4) = i_1 - I_{\text{in}} = I_{\text{in}}. \tag{19}$$

The current of body diode of S_1 is always I_{in}, so this means that ZVS for switch S_2 is achieved for all load range (in next section it will be shown that $i_1 = 2I_{\text{in}}$).

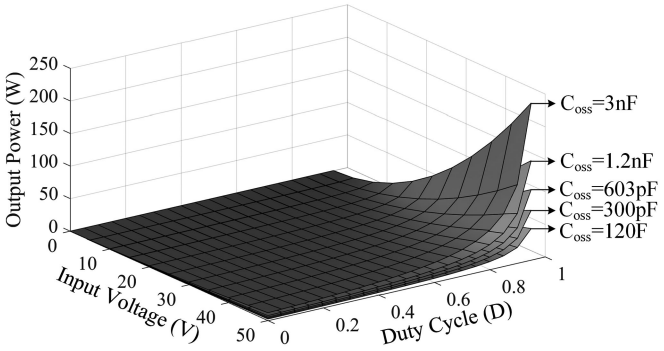


Fig. 5. ZVS condition of lower switch according to output power, input voltage, and duty cycle for some values of $C_{\rm OSS}$.

At t_0 when $\rm S_2$ turns off, deference of $i_{\rm in}$ and i_{lk} flows through the body diode of $\rm S_1$. So,

$$\frac{1}{2}L_B I_{\rm LB}^2 = \frac{1}{2}L_B \left(I_{\rm in}\right)^2 > \frac{1}{2}C_{\rm oss,total}\left(\frac{V_{\rm in}}{1-D}\right)^2 \quad (20)$$

$$C_{\rm oss,total} = C_{{\rm oss},S1} + C_{{\rm oss},S2}. \quad (21)$$

$C_{\rm oss}$ is the parasitic capacitor of switches. The marginal plate of ZVS condition according to the output power, input voltage, and duty cycle for some values of $C_{\rm oss}$ is plotted in Fig. 5. It demonstrates the consistence of ZVS condition of lower switches in the whole load range.

C. Voltage Gain

Here the assumptions that capacitors C_2, C_{o1}, and C_{o2} voltages and input current $I_{\rm in}$ have constant values is needed. As Fig. 1 shows, by applying KCL to node "a," average current of C_1, C_2, and L_k is zero

$$\langle i_{\rm Lk}\rangle + \langle i_{C1}\rangle + \langle i_{C2}\rangle = 0 \quad (22)$$

where "$\langle\blacksquare\rangle$" means the average value of "$\blacksquare$" here. According to average model, average current of capacitors is zero, so

$$\langle i_{C1}\rangle = \langle i_{C2}\rangle = 0 \quad (23)$$

where i_{C1} and i_{C2} are the current of capacitors C_1 and C_2 currents, respectively, and

$$\langle i_{\rm Lk}\rangle = 0. \quad (24)$$

During the time interval $(1-D)T_s = t_6 - t_4$, said the following relation can be written:

$$i_{C2} + I_{\rm in} = i_{\rm Lk}. \quad (25)$$

In which $I_{\rm in}$ is the average input current. Average current of switch $\rm S_2$ is zero because it is in series with capacitor C_2 ($i_{C2} = i_{S2}$). From Fig. 2, during the time $(1-D)\,T_s$, average current of $i_{\rm Lk}$ is equal to $I_{\rm in}$, then

$$\frac{1}{2}i_1(1-D)T_s = I_{\rm in}(1-D)T_s \quad (26)$$

$$i_1 = 2I_{\rm in}. \quad (27)$$

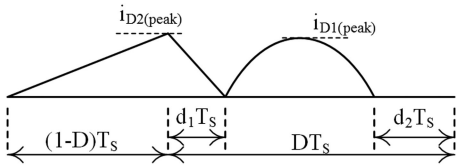


Fig. 6. Output diodes current.

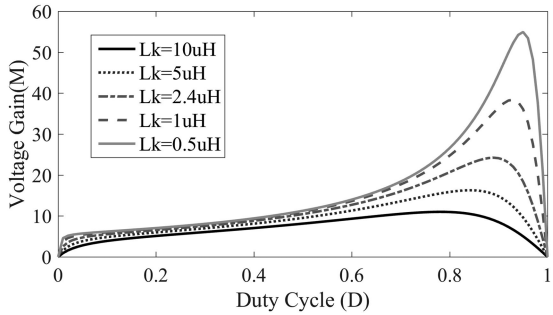


Fig. 7. Voltage gain at different duty cycle.

By applying Kirchhoff's voltage law (KVL):

$$\langle V_{\rm in}\rangle = \langle V_{\rm LB}\rangle + \langle V_T\rangle + \langle V_{\rm Lk}\rangle + \langle V_{C1}\rangle. \quad (28)$$

In steady state, average voltage of the windings of transformer windings and inductors are zero, so

$$V_{\rm in} = \langle V_{C1}\rangle. \quad (29)$$

From time t_4 to t_6, as shown in Fig. 3, $I_{\rm in}$ flows through C_1, and then the current of C_1 jumps to i_1 and after that it decreases almost linearly to zero; in the meanwhile, the voltage of capacitor C_1 during the time t_4 to t_6 increases linearly. Afterwards, C_1 current resonates and reaches its peak at t_2, its minimum happens at t_3, and it remains constant to the end of the period.

During time t_4 to t_6, voltage C_1 increases linearly. The time interval between t_0 to t_2 is too short, so it can be assumed that in this interval, voltage of capacitor C_1 is constant. So, from (29), it can be said that

$$\Delta V_{C1} = \frac{I_{\rm in}}{C_1}(1-D)T_s \quad (30)$$

$$V'_{C1} = V_{C1}\left(t_0\right) = V_{\rm in} + \frac{\Delta V_{C1}}{2} = V_{\rm in} + \frac{I_{\rm in}}{2C_1}(1-D)T_s. \quad (31)$$

By applying volt–second product equations to output capacitors and from Fig. 6, relations between V_{o1}, V_{o2}, and V_o can be easily obtained as follows [35]:

$$V_{o1} = \left(1-D+d_1\right)V_o \quad (32)$$

$$V_{o2} = \left(D-d_1\right)V_o \quad (33)$$

and also V_{C2} can be represented as:

$$V_{C2} = \left(\frac{D}{1-D}\right)V_{\rm in}. \quad (34)$$

TABLE I
VOLTAGE AND CURRENT PERFORMANCE OF SEMICONDUCTORS IN BOTH CONVERTERS

		Maximum voltage	Maximum current	TOV	TOC
The Proposed Converter	S_1	$\frac{V_{\rm in}}{1-D}+\frac{I_{\rm in}}{2C_1}(1-D)T_s$	$I_{\rm in}+\frac{\frac{(1-D+d_1)V_o}{n}-V_{\rm in}-\frac{I_{\rm in}}{2C_1}(1-D)T_s}{\sqrt{L_k/C_1}}$	$\frac{V_{\rm in}}{1-D}-\frac{I_{\rm in}}{2C_1}(1-D)T_s$	$I_{\rm in}$
	S_2	$\frac{V_{\rm in}}{1-D}+\frac{I_{\rm in}}{2C_1}(1-D)T_s$	$I_{\rm in}$	$\frac{V_{\rm in}}{1-D}+\frac{I_{\rm in}}{2C_1}(1-D)T_s$	$I_{\rm in}$
L–L-type half-bridge converter [36]	S_{M1-2}	$\frac{V_{\rm in}}{1-D}$	$\frac{3I_{\rm in}}{2}+\frac{V_{\rm in}}{2f_s(L_S+L'_S)}$	$\frac{V_{\rm in}}{1-D}$	$\frac{I_{\rm in}}{2}+\frac{V_{\rm in}}{2f_s(L_S+L'_S)}$
	Sa_{1-2}	$\frac{V_{\rm in}}{1-D}$	$\frac{I_{\rm in}}{2}+\frac{V_{\rm in}}{2f_s(L_S+L'_S)}$	$\frac{V_{\rm in}}{1-D}$	$\frac{I_{\rm in}}{2}+\frac{V_{\rm in}}{2f_s(L_S+L'_S)}$

From (1), (9), (31), (32), and (34), d_1 can be obtained as follows:

$$d_1=\frac{(1-D)\cdot\left(\frac{D}{1-D}V_{\rm in}-(D-d_1)V_o/n\right)}{(D-d_1)V_o/n+V_{\rm in}+\frac{I_{\rm in}}{2C_1}(1-D)T_s}. \tag{35}$$

Since average current of capacitors are zero, average current of each output diodes is equal to the output current, so

$$I_o=\frac{1}{2}i_{\rm D1(peak)}\cdot d_2. \tag{36}$$

Also,

$$I_o=\frac{1}{2}i_{\rm D2(peak)}\cdot(1-D+d_1). \tag{37}$$

From Fig. 2 and (16)

$$i_{\rm D2(peak)}\cdot n=i_1=2I_{\rm in}. \tag{38}$$

By using (9), (36), and (38), output current can be obtained as follows:

$$\begin{aligned}I_o&=\frac{\left[\frac{D}{1-D}V_{\rm in}-(D-d_1)V_o/n\right]}{2nL_k}\cdot(1-D)(1-D+d_1)T_s\\&=\frac{V_o}{R_L}.\end{aligned} \tag{39}$$

Form (39), voltage gain can be expressed as:

$$M=\frac{D}{\left(\frac{2nL_kf_s}{R_L(1-D+d_1)}+(D-d_1)\cdot\frac{1-D}{n}\right)}. \tag{40}$$

In the ideal condition, leakage inductance would be neglected and voltage gain will be simplified as $M=n/(1-D)$. Voltage gain as a function of duty cycle for $R_L=963\,\Omega$, $f_s=100\,\text{kHz}$, and some L_k values are plotted in Fig. 7. As shown in Fig. 7, voltage gain for duty cycles range from 0.1 to 0.7 is strictly increasing. Moreover, the proposed converter can be controlled by the traditional PWM method. Also, the proposed converter can be easily controlled by the PWM method.

D. Input Current Ripple

During the time DT_s, switch S_1 is turn on and voltage across L_B is $V_{\rm in}$. So input current ripple can be derived as follows:

$$\Delta i_{\rm in}=\frac{V_{\rm in}}{L_B}DT_s. \tag{41}$$

TABLE II
PROPOSED CONVERTER COMPONENT SELECTION

Component	Specification	Description
Switches	150 V, 75 A	**FAIRCHILD HUF75852G3**, $R_{\rm on}=16$ mΩ, fall time = 107 ns
Diodes	400 V, 8 A	**FAIRCHILD MUR840**, $V_f=0.4\sim0.7$ (according to diode current)
Capacitors	$C_1=1\,\mu$F	C_1 = **MKP385**, 160 VDC esr = 12 mΩ
	$C_2=47\,\mu$F	C_2 = **MKP385**, 160 VDC, esr = 5 mΩ
	$C_{O1}=C_{O2}=470\,\mu$F	$\mathbf{C_{O1}}$ **and** $\mathbf{C_{O2}}$ = **MAL205253471E3**, 250 VDC, esr = 0.15 Ω
Input inductor	$L_B=250\,\mu$H	**ETD34 ferrite gapped core**, $R_{\rm wiring}=27.5$ mΩ, $B_{\rm max}=0.3$ T
Transformer	$L_k=2\,\mu$H, $n=7$	**ETD24 ferrite core**, $R_{\rm primery}=6.7$ mΩ, $R_{\rm secondary}=0.134\,\Omega$, $B_{\rm max}=0.3$ T

E. Voltage and Current Stresses of Semiconductors

As mentioned before, voltage of C_1, during interval t_3 to t_4, is constant. Voltage of switch S_1 builds up linearly to its peak, and then the switch turns on, and S_2 turns off. After that, voltage of S_2 decreases sinusoidal until t_3. By applying KVL to S_1, S_2, C_1, and C_2 at t_3, maximum voltage of both switches can be expressed as follows:

$$\begin{aligned}V_{\rm S1,max}&=V_{\rm S2,max}=V_{C2}(t_3)+V'_{C1}\\&=\frac{V_{\rm in}}{1-D}+\frac{I_{\rm in}}{2C_1}(1-D)T_s.\end{aligned} \tag{42}$$

As switches operate in ZVS condition, turn-on losses can be neglected, but turn-off losses have to be considered. So, it is important to obtain TOV and TOC. As depicted in Fig. 2, TOV of S_1 and S_2 occurs at t_4 and t_0, respectively,

$$\begin{aligned}V_{\rm S1,turn-off}&=V_{C2}(t_3)+V_{C1}(t_4)\\&=\frac{D}{1-D}V_{\rm in}+V_{\rm in}-\frac{I_{\rm in}}{2C_1}(1-D)T_s\\&=\frac{V_{\rm in}}{1-D}-\frac{I_{\rm in}}{2C_1}(1-D)T_s\end{aligned} \tag{43}$$

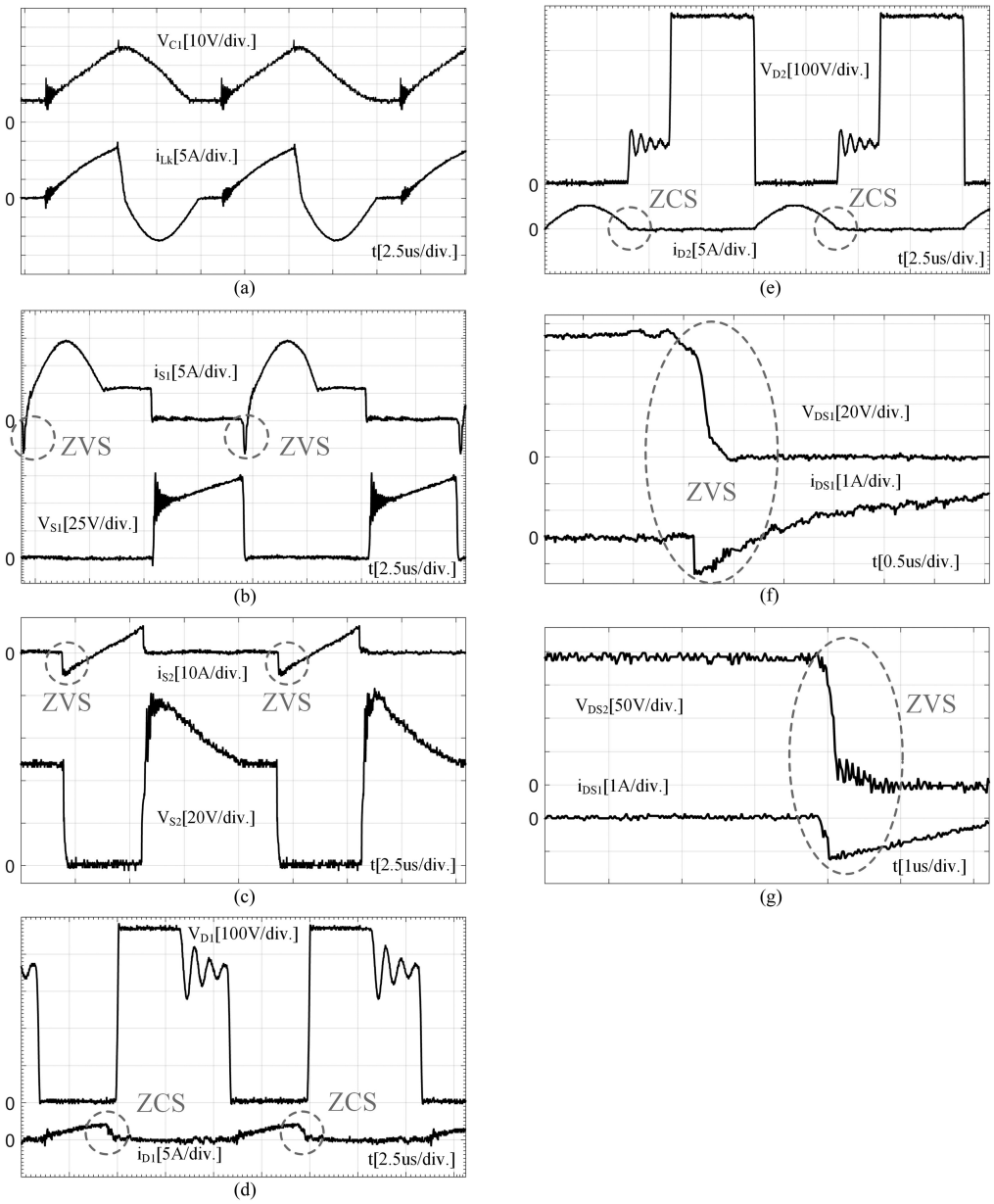


Fig. 8. Experimental waveforms of the proposed converter. (a) i_{LK} and V_{C1} (b) i_{S1} and V_{S1}. (c) i_{S2} and V_{S2}. (d) i_{D1} and V_{D1}. (e) i_{D2} and V_{D2}. (f) ZVS condition for switch S_1 at 20% load. (g) ZVS condition for switch S_2 at 20% load.

$$\begin{aligned} V_{\mathrm{S2,turn-off}} &= V_{C2}(t_3) + V_{C1}(t_0) \\ &= \frac{D}{1-D}V_{\mathrm{in}} + V_{\mathrm{in}} + \frac{I_{\mathrm{in}}}{2C_1}(1-D)T_s \\ &= \frac{V_{\mathrm{in}}}{1-D} + \frac{I_{\mathrm{in}}}{2C_1}(1-D)T_s. \end{aligned} \tag{44}$$

Maximum current of S_1 happens during t_2 to t_3:

$$\begin{aligned} i_{\mathrm{S1,max}} &= I_{\mathrm{in}} + \frac{V_{o1}/n - V'_{C1}}{\sqrt{L_k/C_1}} \\ &= I_{\mathrm{in}} + \frac{(1-D+d_1)V_o/n - V_{\mathrm{in}} - \frac{I_{\mathrm{in}}}{2C_1}(1-D)T_s}{\sqrt{L_k/C_1}}. \end{aligned} \tag{45}$$

TOC of both switches and maximum current of S_2 is equal to I_{in}:

$$i_{\mathrm{S1,turn-off}} = i_{\mathrm{S2,turn-off}} = i_{\mathrm{S2,max}} = I_{\mathrm{in}}. \tag{46}$$

Maximum voltage of diodes is equal to output voltage

$$V_{\mathrm{D1,2-max}} = V_o. \tag{47}$$

Due to ZCS in output diodes, their TOC is zero. TOV and maximum voltage and currents of the proposed converter switches are compared with an *L–L*-type half-bridge converter [36] in Table I. It can be observed from Table I, that although TOC in [36] compared with the proposed converter is approximately half of the one in the proposed converter, number of the switches are twice the proposed one. Furthermore, TOV of S_1 and S_2 are lower and higher

TABLE III
MEASURED CURRENTS AND VOLTAGES OF BOTH CONVERTERS IN DIFFERENT OUTPUT POWER

	The proposed converter			L-L type half-bridge converter [36]			
	P_O=25w, V_{in}=24V D=0.52	P_O=150w, V_{in}=24V D=0.62	P_O=250w, V_{in}=28V D=0.56		P_O=25w, V_{in}=24V D=0.72	P_O=150w, V_{in}=24V D=0.78	P_O=250w, V_{in}=28V D=0.75
S_1-TOC(A)	2.36	6.5	9.8	$S_{M1\&2}$-TOC(A)	0.84	3.7	5.2
S_2-TOC(A)	1.18	6.4	9.4	$S_{M1\&2}$-TOC(A)	0.78	3.5	4.83
$i_{S1,rms}$(A)	0.39	9.3	13.9	$i_{SM1-2,rms}$(A)	0.56	3.5	5.9
$i_{S2,rms}$(A)	0.39	2.5	3.7	$i_{Sa1-2,rms}$(A)	0.24	1	1.5
S_1-TOV(V)	50	48.6	46	$S_{M1\&2}$-TOV(V)	92	120	110
S_1-TOV(V)	50	74.5	82	$S_{M1\&2}$-TOV(V)	92	120	110
$i_{D1-2,Ave.}$ (A)	0.03	0.39	0.66	$i_{D1-4,Ave.}$ (A)	≈0	0.2	0.33
$i_{C1,rms}$(A)	0.3	2.5	3.7	$i_{C1,rms}$(A)	0.07	1.14	2.12
$i_{C2,rms}$(A)	0.39	6.4	10.2				
$i_{co1-2-rms}$(A)	0.05	0.6	1.1	$i_{Co,rms}$(A)	0.07	0.45	0.75
$i_{LB,peak}$(A)	0.55	6.9	9.8	$i_{L1-2,peak}$(A)	0.26	3.77	5.3
$i_{LB,rms}$(A)	0.3	6.6	9.5	$i_{L1-2,rms}$(A)	0.15	3.5	5
$i_{T,peak}$(A)	1	13.2	18.3	$i_{T,peak}$(A)	0.59	7.9	9.4
$i_{T,rms}$(A)	0.4	6.8	10.8	$i_{T,rms}$(A)	0.48	2.6	4

than corresponding switches in [36], respectively, and their average is equal. Totally, the number of switches in the proposed converter is halved, but switches rating is higher.

IV. EXPERIMENTAL RESULTS

In this section, experimental results of a 150-W prototype is presented and compared with an *L–L*-type half-bridge converter in [36]. Output and input voltages are chosen as 380 and 24 V, respectively, and switching frequency is 100 kHz. Input inductance L_B is obtained 250 μH from (41) by considering 10% input current ripple. Transformer turns ratio is $n = 7$ and resulting in a 2-μH leakage inductance. As discussed in Section III-A, resonant frequency should be more than 80 kHz, and also from (43), C_1 should be large enough to keep S_1 TOV always be positive. These two constrains from (15) and (43) yield

$$\frac{I_{\text{in}}}{2V_{\text{in}}}(1-D)^2 T_S \le C_1 \le \frac{1}{4\pi^2 f_{r1}^2 L_k} \tag{48}$$

$$0.33\,\mu\text{F} \le C_1 \le 1.98\,\mu\text{F}. \tag{49}$$

So, C_1 is selected as 1 μF 160 V, and clamp capacitor C_2 is chosen as 47 μF, 160 V. The output capacitors are opted to be 470 μF 250 V. The components specifications and part number are listed in Table II.

Experimental waveforms of the proposed QRC are shown in Fig. 8. Fig. 8(a) shows current and voltage of leakage inductor and capacitor C_1, respectively. It can be seen that L_k current in some intervals is zero, so as mentioned before, the proposed converter operates in below-resonance mode. The voltage of capacitor C_1 is not constant which causes variation on voltage of switches. Fig. 8(b) and (c) shows the current and voltage

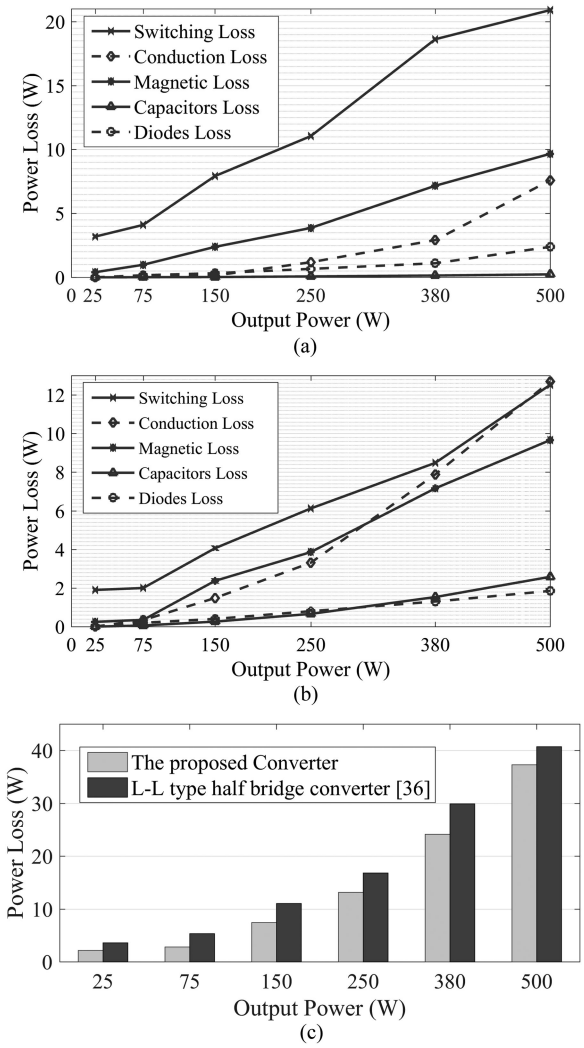


Fig. 9. (a) Detailed power loss of *L–L* type half bridge converter [36]. (b) Detailed power loss of the proposed converter. (c) Total power loss of the both converters.

of switches S_1 and S_2 of the proposed QRC, respectively, and their ZVS operations. Also, it can be seen that the voltage across the switches is not constant that is caused by C_1 voltage variation. This will have effect on switching loss which will be discussed later. The maximum voltage of switches is about 78 V. Moreover, TOV of switches S_1 and S_2 is about 48 and 75 V, respectively. Moreover, maximum current of switches S_1 and S_2 is 16 and 6.5 A and TOC of both of them is 6.5 A. Fig. 8(d) and (e) shows current and voltage of output diodes D_1 and D_2, respectively, and their ZCS operations. Maximum voltage of diodes is 380 V, which agrees with theoretical analysis. Furthermore, maximum current of D_1 and D_2 is 2 and 2.3 A, respectively. ZVS performances of QRC switches S_1 and S_2 at 20% load is shown in Fig. 8(f) and (g), respectively.

V. EFFICIENCY CALCULATION AND COMPARISON

The proposed converter's efficiency has been compared with an *L–L*-type half-bridge converter in [36] at different output powers. Both converters have been simulated in the same

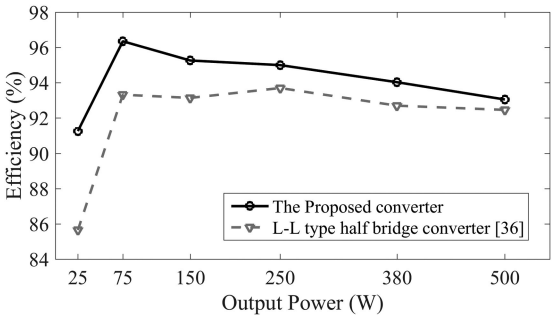


Fig. 10. Efficiency comparison of the proposed converter and *L–L*-type half-bridge converter [36].

conditions. Currents and voltages corresponding to the components associated with losses are listed in Table III. The data are compared at three different output powers. As the converter in [36] works in high duty cycles, to obtain for higher output power, input voltage is increased. The same condition is provided for the proposed converter; though, it works in lower duty cycles. Dissipation losses of both converters are calculated based on the provided data in Table II, and depicted in Fig. 9. Fig. 9(a) and (b) shows detailed power losses of each converter, and total power loss of the converters at different output powers is depicted in (c). As mentioned in Section III-E in the proposed converter number of switches are halved, but TOC has almost been doubled that can be seen in Table III. However, as an *L–L*-type half-bridge converter [36] operates in higher duty cycle, its TOV is considerably more than the proposed converter, which dramatically escalates switching loss. The concept is clearly shown in Fig. 9(b) and (c). The switching loss in the proposed converter is significantly reduced because of the quasi-resonant operation. On the other hand, at higher output powers, the switches conduction loss dramatically rises, which causes efficiency reduction. As shown in Fig. 9(a) and (b), switches conduction loss in the proposed converter increases slightly more than an *L–L*-type converter [36], but switching loss is considerably lower. Generally, total switches dissipation power in the proposed converter is significantly reduced.

The other components loss goes up almost the same in both converters. Generally, the total power loss in the proposed converter is reduced thanks to the quasi-resonant operation, and the efficiency is improved. Efficiency curve is plotted in Fig. 10.

VI. Conclusion

In this paper, analysis and experimental results of a new quasi-resonant converter have been presented. Both switches of the proposed converter work under ZVS condition. Also, the main switch operates in below-resonant mode, while the active-clamp switch operates in above-resonant mode in order to retain ZVS condition for the main switch, making switching losses are minimum. The leakage inductance of transformer has been employed to make the resonant circuit with clamp capacitor. Low input current ripple which is appropriate for FC applications has been made by using a boost circuit at the input of the converter. At the output, to obtain high voltage gain, a voltage doubler circuit has been used. ZCS conditioin achieved for output diodes working under ZCS alleviates their reverse recovery problem and reduces their switching losses. Finally, the proposed converter power loss has been compared with an *L–L*-type half-bridge converter [36], and it was concluded that by employing quasi-resonant performance, total power loss has been reduced effectively.

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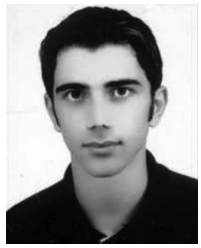

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