A Power Supply Achieving Titanium Level Efficiency for a Wide Range of Input Voltages

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***Abstract*—To achieve the highest possible grade for server or computer power supplies in terms of efficiency, various solutions for high line input already exist on the market. In this paper, a new topology is investigated closely, showing that the titanium grade may be achievable at low line input with traditional silicon devices by the utilization of low voltage MOSFETs, which have an excellent figure of merits, by connecting two converter stages in parallel for low line input or in series for high line input. This paper presents simulation results which are verified with measurements from a developed prototype for 1 kW of power and 12 V output consisting of a triangular current mode power factor correction followed by a well-known phase shifted zero voltage switched bridge. Furthermore, a detailed description of the loss estimation by simulation, enhanced with additional calculations, is presented.**

I. Introduction

THE voluntary certification program for efficient energy use in power supplies for computers and servers, the 80 PLUS organization [1], introduced recently the new titanium level efficiency requirements for low line. Due to the higher necessary input currents at low line and accordingly higher conduction losses in the power factor correction stage, titanium level presents a challenge. The goal of this paper is to achieve the required efficiencies for titanium level regardless of low or high line input in all load conditions by the utilization of low-voltage MOSFETs, which further reduces the required cooling and therefore decreases energy costs twice. This paper describes the PFC stage and the PS-ZVS bridge for the dc/dc conversion and compares the efficiencies obtained from simulation with measurements from the prototype shown in Fig. 1. The design of one module was done with the idea that it should be possible to stack two modules into each other for a higher power density. The dimensions for two modules are 100 mm × 200 mm × 50 mm (b × w × h), achieving a total power density of 1 kW/dm^3. Furthermore, the presented power supply reaches a maximum operation temperature of 95 °C at full load operation as measured with a thermal camera in which the hotspot is the transformer of the dc/dc converter, all with passive cooling.

The new idea is to use a modular approach, which is able to divide the input voltage at high line to utilize low voltage MOSFETs like OptiMOS [2]. Low-voltage MOSFETs can achieve a better switching FOM, especially the latest new generation, when compared to higher voltage MOSFETs like CoolMOS. A FOM describes the performance of a power MOSFET, here by the product of the total gate charge Q_g and on-resistance $R_{\rm on}$. In hard-switching topologies, the output capacitance $C_{\rm OSS}$ also matters, which adds an extra loss $\Delta P_{\rm sw-on} = 1/2 \cdot U_{\rm sw}^2 C_{\rm OSSeq}$ at every turn-on event, where $C_{\rm OSSeq}$ is the energy equivalent output capacity of the MOSFET. In a resonant-switched circuit, the output capacitance is not important for the efficiency since the MOSFETs are always switched ON under a zero voltage condition, not losing the output charge, reducing significantly the switching loss.

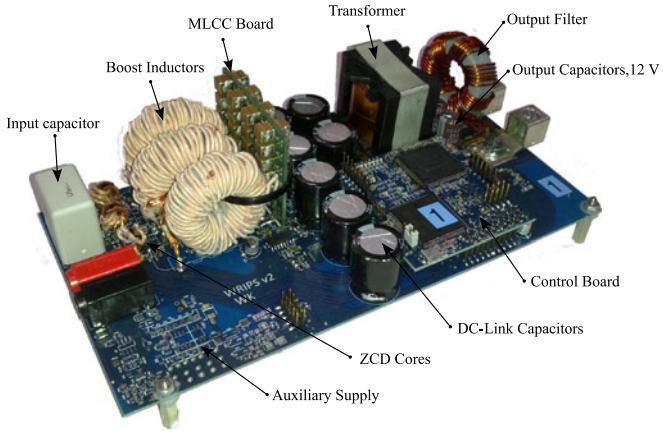

Fig. 1. Picture of the prototype for one module.

Today, several solutions for power supplies which fulfill the titanium requirement for high line or low line already exist on the market, none of which achieves the low line titanium criteria would also achieve the high line titanium criteria efficiencies at low line. Currently, the best option listed in [1] is from the company Super Flower which achieves, except at 50% load, all efficiencies required to fulfill the titanium high line criteria, where it only achieves 95.03%. Research shows that a bridgeless PFC is most likely the best-suited topology for achieving high efficiencies, like in [3] this topology achieves an efficiency of 99.1% with traditional silicon devices and boost diodes in continuous conduction mode (CCM) operation. By replacing the boost diodes with MOSFETs and running the PFC in a TCM pattern, a peak efficiency of 99.23% could be achieved at high line input [3], [4]. The TCM pattern allows always to switch ON under zero voltage and will be investigated closer later.

For the dc/dc conversion where isolation is required, an *LLC* converter is probably the best solution in terms of efficiency, but not complexity. To keep the control simple, a PS-ZVS bridge

Manuscript received July 23, 2015; revised November 26, 2015; accepted February 8, 2016. Date of publication February 24, 2016; date of current version September 16, 2016. Recommended for publication by Associate Editor T. Shimizu.

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Digital Object Identifier 10.1109/TPEL.2016.2532962

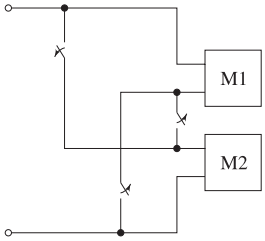

Fig. 2. Schematic for switching the modules between serial and parallel connection.

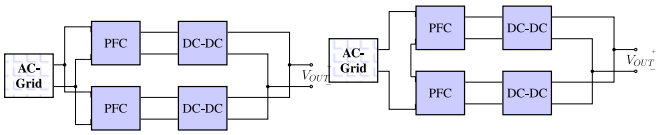

Fig. 3. Proposed principle schematic for low line input (left) and high line input (right).

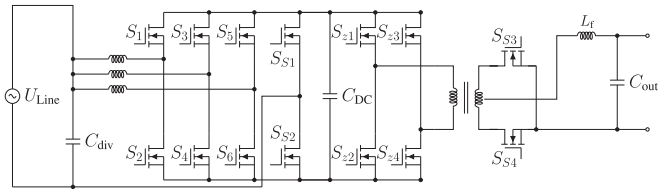

Fig. 4. Principal schematic of the power stage for a single module.

was chosen which is capable of achieving high efficiencies for higher loads, as shown in [3], where an efficiency of 98.5% with a power density of 3.3 kW/dm^3 was achieved for a telecom supply with 48-V output voltage. Another highly efficient PS-ZVS bridge is presented in [5], where an efficiency of 99.2% is achieved at 50% load with a power density of 2.2 kW/dm^3.

Utilizing low-voltage MOSFETs for high voltage applications has recently gained interest. As shown in [6]–[8] a highly efficient power supply for telecom is presented; one which achieves an efficiency of 98% and a power density of 2.2 kW/dm^3.

In Section II, this paper both presents the new idea which allows for the division of high input voltage into smaller voltages for each module and briefly describes the topologies used for the prototype. Section III gives a quick overview of the implementation of the control and the PFC and the dc/dc stage will be closer investigated in Sections IV and V, respectively. Details about the simulation and the foregoing loss calculation are outlined in Section VI which is verified in Section VII by measurements. Section VIII points out some possible hints for future prototypes to further improve the efficiency, along with a quick summary of this paper.

II. Proposed Solution

The power supply consists of two modules with each able to deliver 500 W of output power. The input ac voltage is capacitively divided for high line input, where the modules operate in a series connection. At low line, both stages operate in parallel (see Fig. 2). The switchover between the different configurations can be handled with simple relays as shown in Fig. 2 or semiconductors with bidirectional blocking capability. For this paper, the minimum required number of two modules was chosen, necessitating 250 V MOSFETs. The proposed solution works with any even number of modules. Reducing the required blocking voltage of the MOSFETs by increasing the module count can further increase the efficiency. The drawback to an increasing number of modules for this PFC solution is a reduction in power density, since serial operation at high line requires all modules to have the same current. Therefore, the boost inductor will not reduce in size with an increasing number of modules. Another solution for the PFC, as presented in [6]–[8], might be preferable if even lower voltage MOSFETs should be utilized.

With the proposed solution every module always operates with the same input voltage, independent of 110 or 240 V; therefore the efficiency is also independent of the input voltage. Each module consists of a TCM resonant PFC circuit [9]–[14] (TCM-PFC) with a PS-ZVS full bridge as an isolating dc/dc converter afterward and center tap on the secondary side. To supply the gate driver, control and measurement circuits with all required voltages, which are all different and isolated, an auxiliary supply in the form of a quasi-resonant flyback was chosen, which is integrated into each module.

For a single module, the circuit comprises a three-phase interleaved TCM PFC, a dc link capacitor, and a PS-ZVS bridge for dc/dc conversion (see Fig. 4). The capacitor at the input which divides the input voltage is chosen relatively small (around 5μF) to minimize the phase-shift between the line voltage and the input current and as well to save on space and cost.

Investigations concerning an electromagnetic interference (EMI) filter which has not been implemented for the presented prototype should already include the boost inductors and the input capacitors in the filter design. The decision to choose multiple EMI filters for each module over a single global EMI filter at the input can be explained as follows: an EMI filter for each module is preferable since it is possible to design the filters for a lower current and a lower voltage. A global EMI filter would have to be designed for twice the current for low line (both modules in parallel) and twice the voltage for high line (both modules in series), thus increasing the filter's volume. This is proportional to the stored energy in case of comparatively low high-frequency losses versus low frequency losses as shown in [15]. With the inclusion of an EMI filter, the overall efficiency will be slightly reduced. Due to the low line frequency, the core losses will be negligible, resulting in mainly conduction loss. Therefore, the filter is expected to significantly diminish the efficiency only for higher load conditions; this should not interfere with achieving titanium certification.

III. Control Strategy

The PFC stage is implemented with three interleaved fast-switching phases (S_1 to S_6) and one leg which switches at the much lower line frequency (S_{S1} and S_{S2}). All switches are low-voltage MOSFETs with a maximum blocking voltage of 250 V.

The small capacitors on the input C_{div} divide the input voltage in case of high line input. The PFC stage boosts the voltage to a dc-link voltage of 200 V and in order to reduce the equivalent series resistance (ESR) of the dc-link capacity and therefore further minimize the losses, the dc-link capacity is partitioned into electrolytic caps and an additional stacked multi layer ceramic capacitor (MLCC) board. For each phase, the control requires the zero current crossings through the boost inductor. These crossings are detected with saturating transformer cores [4], [16] for the prototype. The measurement of the zero current crossings is important for synchronizing the precalculated current with the real current and therefore preventing a current run-away situation. Other solutions for the zero current detection (ZCD) could be to measure the current across a shunt resistor, as shown for instance in [14] and [17], with the disadvantage that this solution offers no galvanic isolation if multiple interleaved phases are needed. Another resistor-free method was shown in [18] where only the PFC's input and output voltage are measured. It is then possible to estimate the zero current crossings by integration of the mentioned voltages. The aforementioned concept was implemented on a custom chip which makes it difficult to reproduce and was therefore dismissed as a viable solution for the prototype. Although in light of future developments especially with upcoming new semiconductor devices and higher switching frequencies this concept might warrant further investigation.

The heart of the control for the prototype forms a combination of a microcontroller and a field programmable gate array (FPGA). The job of the microcontroller is to calculate the switching timings for the PFC as well as the required duty cycle for the dc/dc stage and send the timing values to the FPGA over quad serial peripheral interface (qSPI). All pulse width modulation (PWM) signals for the PFC and the PS-ZVS bridge are generated on the FPGA with the data received from the microcontroller. The control ground is the same as the output ground on the secondary side of the dc/dc converter. To measure the floating voltages in reference to the microcontroller, the dc-link voltage and the voltages across the input capacitors are measured utilizing error isolation amplifiers. The error amplifiers used in the prototype are the ADUM3190 from Analog Devices. Further, the control is located on the secondary side and the signals for the primary switches are isolated via the Si8235 gate driver from Silicon Labs. Note that a possibility for the future is to integrate the control into an application specific integrated circuit (ASIC), especially for the PFC in which no integrated solutions are commercially available for the triangular current modulation is a possibility for the future.

IV. Power Factor Correction

A. Introduction

The key difference of the new idea is the change from high-voltage MOSFETs to low-voltage MOSFETs like OptiMOS which is possible through the stacking of modules. With this idea it is also possible to divide the input voltage per module into any desired level; thus, enabling the utilization of devices with an even lower blocking voltage. Due to the triangular current,

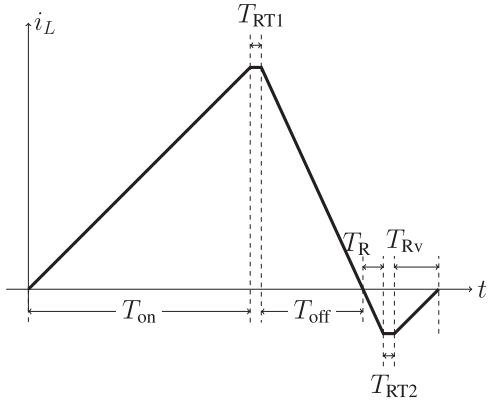

Fig. 5. Basic PFC triangular current waveform [9].

shown in Fig. 5, all fast switching MOSFETs (S_1 to S_6) in the PFC stage turn ON under zero voltage switching (ZVS) conditions, which results in zero turn-on losses.

The shown waveform for one phase starts with an on-time T_{on}, where the boost inductor is energized. After T_{on}, both switches of one phase are switched OFF; during this time the voltage across the switch which was OFF during T_{on} resonates to zero, which allows it to be switched OFF after T_{RT1} on under zero voltage, deenergizing the boost inductor during the time T_{off}. In order to extend the zero voltage range for input voltages higher than half the dc-link voltage, the switch is purposely conducting longer for the time T_R, reversing the current in the boost inductor which stores energy in the magnetic field for the second resonant transition during T_{RT2}, where again both switches are switched OFF. During that time, the voltage across the first switch resonates to zero, again allowing a turn-on under zero voltage and after the time T_{Rv} the inductor is deenergized and the shown period starts again. Depending on the load and the line voltage, the operating frequency varies in TCM operation. For the prototype, the switching frequency varies between 30 and 130 kHz.

For operation, the PFC requires multiple cascaded control loops consisting of a dc-link voltage control, a phase shedding control (which adds or drops active phases dependent on the current load for staying in a high efficient region), a phase-shift control (which controls the phase-shift between the active phases to minimize the input current ripple and therefore the requirements for the EMI filter) and, finally, at last a control to balance the voltages across the input capacitors, see Fig. 6. The output of these control loops is then used for the precalculation of the switch timings, which are calculated every 50 μs and then transmitted to the FPGA, which controls the actual switching. By measuring the zero current crossings for each of the three phases with the FPGA, the phase-shifts between phases one and two, namely ps_{12}, as well as phases one and three, or ps_{13}, are measured. Subtracting the desired phase-shifts ps_{ref1} and ps_{ref2} results in the phase-shift error signals ep_{12} and ep_{13}. These represent the input for a controller of which its output further modifies the switch timings together with required average current i_{avgBal} in order to balance the input capacitor voltages and

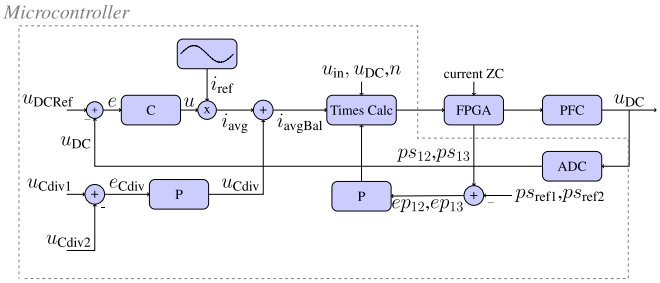

Fig. 6. Simplified block diagram of the PFC control.

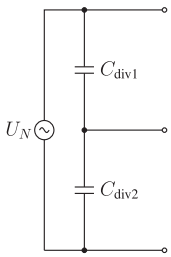

Fig. 7. Capacitive voltage divider for high line.

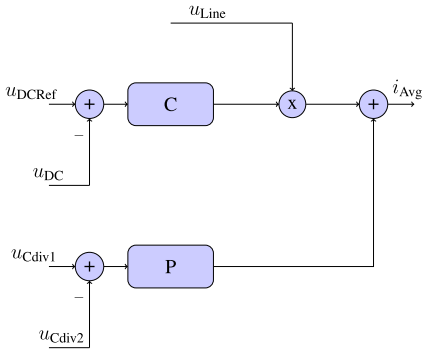

Fig. 8. Voltage balancing control.

to deliver the required power, the input voltage u_{in}, the dc-link voltage u_{DC}, and the amount of active phases n. A measurement demonstrating the phase-shift and dc-link control of the PFC is shown in Fig. 14 in Section VII where it is shown that the phase-shift between the inductor current has about 180°.

B. Capacitor Voltage Balancing

At high line, both stages are connected in series and the input voltage is divided capacitively. For the capacitive voltage divider, foil capacitors where chosen. To keep the volume and the phase-shift between the input voltage and current low, the capacitors C_{div1} and C_{div2} must remain small (around $5\mu F$) which also requires a control to equalize the voltages across each capacitor from Fig. 7. The control for the capacitor voltage equalization is depicted in Fig. 8 in which u_{DCref} is the reference dc-link voltage, u_{DC} is the actual measured dc-link voltage, u_{Line} is the line voltage, and u_{Cdiv1} and u_{Cdiv2} are the voltages across the input capacitors. In case of different input voltages, the average current i_{avg} is adjusted with a simple P-control to change the power intake for the module. If the input voltage of the first module is greater than that of the input voltage of the second module, the average input current i_{Avg} is increased to balance the voltages again. It suffices if only one module controls the voltages by adjusting its average current to balance the input voltages for each module.

V. PS-ZVS Bridge

The PS-ZVS bridge is well known and widely used in industry, due to its excellent and increasing efficiency achieved toward full load. The full bridge (S_{z1} to S_{z4}) converts the dc-link voltage down to 12 V dc with S_{s3} and S_{s4} as synchronous rectification MOSFETs in a center-tapped topology. For the primary MOSFETs, devices with a smaller chip area compared to the PFC (60 mΩ) were used to reduce the parasitic output capacitance C_{OSS}, which helps achieve ZVS turn-on conditions at low load conditions. As primary resonant inductance, the leakage inductance of the transformer is utilized; thus, saving cost and space for an additional inductor. The primary transformer windings consist of litz wire to reduce the ac losses (proximity and skin effect) and the secondary turns consist of 2×200 μm thick copper foil. To control the PS-ZVS bridge, both the microcontroller and the FPGA are utilized. Since the PS-ZVS bridge runs on a fixed frequency of 100 kHz, the control could also be carried out exclusively on either the microcontroller or the FPGA. Here, the duty cycle is calculated on the microcontroller and then transmitted via qSPI to the FPGA. The four required switching signals for each primary switch and the two synchronous rectifiers are then generated from the FPGA. The synchronous rectifier signals are generated from the FPGA with constant turn-on and turn-off delays which allow safe operation at very low loads; thus the body diode of the synchronous rectification MOSFETs conducts longer toward higher loads. Optimizing the synchronous rectification timings by an adaptive delay, which is already available in the form of integrated control solutions, could therefore improve the efficiency with increasing load. The control is located on the secondary side; therefore no isolation for the synchronous rectifier signals is required.

VI. Simulation of the Circuit

In order to optimize the components, accurate simulations of the circuits are required. Therefore, the simulations were carried out with MATLAB/Simulink coupled with Gecko [19] with an additional calculation of ac losses, core losses, gate losses, and off-switching losses in MATLAB. For the control of the PFC, a method similar to the one shown in [9] and in [4] was implemented in Simulink. The simulation also considered the parasitic elements like the ESR of the boost inductor, the on-resistances of the MOSFETs (R_{DSon}), the parasitic stray inductance of the MOSFET packages, the ESR of the dc-link capacitors and the output capacitances of the MOSFETs C_{OSS}. Furthermore, additional losses, such as the gate losses, ac losses of the magnetic components and leakage currents of the capacitors were later calculated in MATLAB with the simulation data.

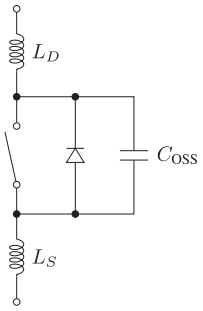

Fig. 9. Model of a MOSFET in Gecko.

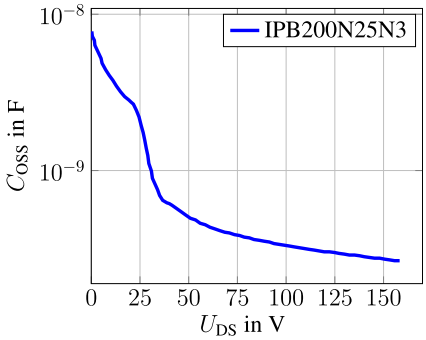

Fig. 10. Output capacity over U_{DS} from the MOSFETs on the primary side.

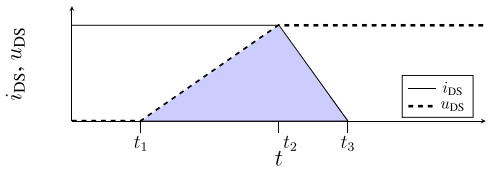

Fig. 11. Approximation for the off-switching loss of a MOSFET under current with a inductive load; the gray triangle where the current and the voltage overlap is the off-switching loss.

A. Modeling of the MOSFET

In Gecko, switches are assumed ideal (instantaneous switching) with a definable R_{DSon}. In order to model a MOSFETs additional components, as shown in Fig. 9, elements were added like the body diode, L_{d} and L_{s} for the parasitic drain and source inductivities, and C_{OSS} for the nonlinear output capacity of the MOSFET, see Fig. 10.

B. Off-Switching Losses

The on-switching losses are minimal and therefore assumed to be zero, since every MOSFET is turned ON under ZVS condition. The off-switching loss was calculated by an estimation of the switching time and information about the current and voltage around the switching event.

The off-switching loss can be calculated by integrating the drain–source current i_{DS} before the switching event and the voltage u_{DS} after the switching event, as shown in Fig. 11 with

$$P_{\mathrm{off-sw}} = \int_{t_1}^{t_3} u_{\mathrm{DS}}(t) i_{\mathrm{DS}}(t) dt = \frac{u_{\mathrm{DS}}(t_2) i_{\mathrm{DS}}(t_1) \cdot (t_3 - t_1)}{2} \quad (1)$$

where the switching timings mostly depend on the device characteristics as shown in

$$t_2 - t_1 = \frac{R_{\mathrm{G}} Q_{\mathrm{GD}}}{U_{\mathrm{th}} + \frac{i_{\mathrm{DS}}(t_2)}{g_{\mathrm{fs}}}}$$

$$t_3 - t_2 = R_{\mathrm{G}} C_{\mathrm{iss}}(u_{\mathrm{DS}}) ln \left(\frac{u_{\mathrm{th}} + \frac{i_{\mathrm{DS}}(t_2)}{g_{\mathrm{fs}}}}{U_{\mathrm{th}}} \right) \quad (2)$$

where R_{G} is the total gate resistance, $Q_{\mathrm{GD}}(on)$ the gate–drain charge, U_{th} the gate threshold voltage, g_{fs} the transconductance, and $C_{\mathrm{iss}}(u_{\mathrm{DS}})$ the input capacitance of the device at the voltage u_{DS}. All these parameters are obtainable from the datasheet [20], [21].

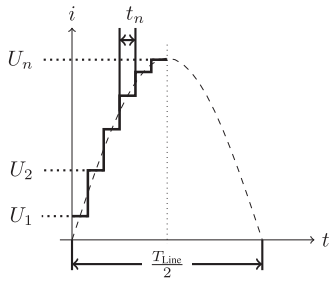

Fig. 12. Splitting of the input current sine for the PFC for a fast core loss estimation.

C. Gate Drive Losses

The gate drive losses were estimated by counting the turn-on events of every switch and were then calculated with (3) with Q_{Gate} as the gate charge and V_{G} as the gate driver supply voltage

$$P_{\mathrm{Gate}} = Q_{\mathrm{Gate}} \cdot V_{\mathrm{Gate}}. \quad (3)$$

D. Core Losses

The inductor core losses were calculated with the improved generalized Steinmetz equation (iGSE) formula [22]–[24], see

$$P_v = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt \quad (4)$$

where α and β can be used directly from the given Steinmetz parameters and k_i can be calculated from the Steinmetz parameters with

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}. \quad (5)$$

For the PFC stage, the sinusoidal mains voltage waveform was split into n parts [25], [26], see Fig. 12. For each part of

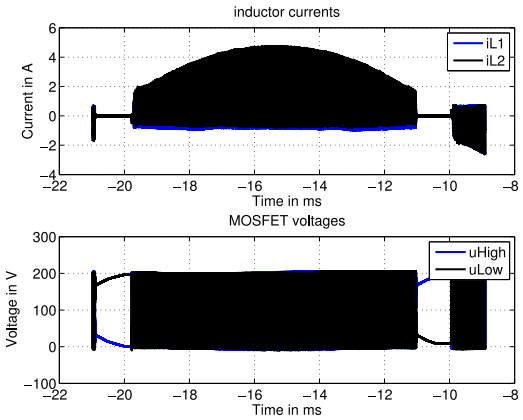

Fig. 13. Two phase interleaving (measured); (top) inductor currents i_{L1},i_{L2} (bottom) MOSFET voltages u_{High},u_{Low}.

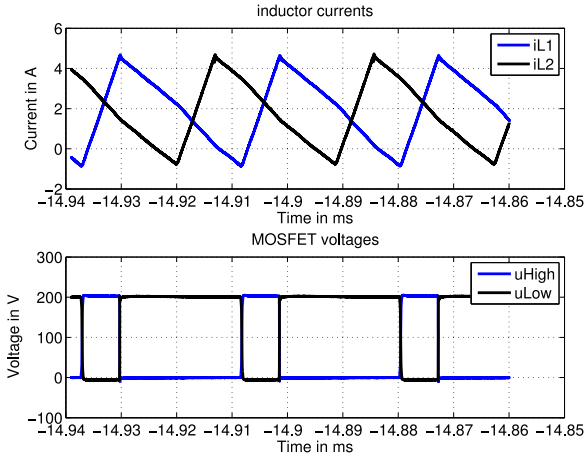

Fig. 14. Two phase interleaving (measured, zoomed); (top) inductor currents i_{L1},i_{L2} (bottom) MOSFET voltages u_{High},u_{Low}.

the sine, the triangular current-shape according to Fig. 5 for the specific dc input voltage is calculated. Then, for this triangular input current the magnetic field strength H was calculated and further with the material specific $B-H$ curve the magnetic flux density B was determined. Together with the Steinmetz parameters and (4), the core losses P_{cn}, for this specific part of the sine can be calculated. This has been done n times for every part of the first quarter of the line input voltage sine. Afterward the total core loss is equal the average of all P_{cn}.

E. AC Losses

The calculations for the ac losses are explained separately for foil conductors (which were used for the secondary turns of the transformer) and for round conductors (which were used for the output filter inductor). The boost inductors as well as the primary turns of the transformer are wound with litz wire, therefore the ac losses were neglected. For the simulation, only the dc resistance was used. Later the dc and ac losses were calculated separately for each frequency component with an FFT analysis. To keep this section short, the formulas will be given in the appendix.

1) Foil: The secondary side of the transformer consists of foil winding with a center tap with two 200 μm foils in parallel, isolated from each other with Kapton tape.

2) Round Conductor: The output filter consists of multiple round conductors in parallel (six strands in total).

F. Capacitor Losses

For the capacitor losses (dc-link capacitors and the capacitors for the 12-V output voltage), the ESR and the leakage current have been considered. The ESR resistance was calculated with

$$\mathrm{ESR} = \frac{DF}{2\pi f C} \tag{6}$$

where DF is the dissipation factor from the datasheet, f the frequency, and C the capacity of the capacitor. Another significant loss source, especially for electrolytic capacitors, is the leakage current, which was calculated with

$$I_L = K_c \cdot C \cdot V \tag{7}$$

which gives the leakage current I_L in μA; K_c is a constant from the datasheet (usually between 0.01 and 0.02 for electrolytic capacitors), V the rated voltage, and C the capacity in μF. With this formula the maximum leakage current after 5 min was calculated for a first approximation. Furthermore, the leakage current was measured and turned out to be much lower then the above approximation; therefore for more accurate loss-calculations the measured value was used.

VII. Experimental Verification

Fig. 14 shows the phase currents and voltages across the lower switches of each phase for the PFC for two active phases at 60% load. During the whole input voltage range, all turn-ons are under a zero voltage condition. This is demonstrated with the voltage across the switches for one leg in which u_{High} is the voltage across the high-side switch and u_{Low} the voltage across the low-side switch, since no overvoltage spikes can be seen. Furthermore, it is shown that the phase currents i_{L1} and i_{L2} are out of phase to each other due to the phase-shift control. The gap between the positive and negative half-wave, where every switch is OFF, is needed due to the ZCD measurement, which has a certain small nonlinear response delay over the input voltage range. With improvements to the ZCD detection circuit, this gap can be lowered, improving the total harmonic distortion (THD), which currently ranges from 34% (10% load) to 7% (100% load) without an EMI filter.

All the presented efficiency measurements have been carried out with a Norma 5000 power analyzer with a sampling rate of 1 MHz and a basic accuracy of 0.05% of the reading, 0.05% of the range and 10/1000 degrees for the phase for ac, and 0.1% of the reading and 0.1% of the range for dc. The efficiency measurements include the gate driver losses and the losses of the measurement circuits, but the control losses (FPGA and microcontroller) are excluded. The currents were measured

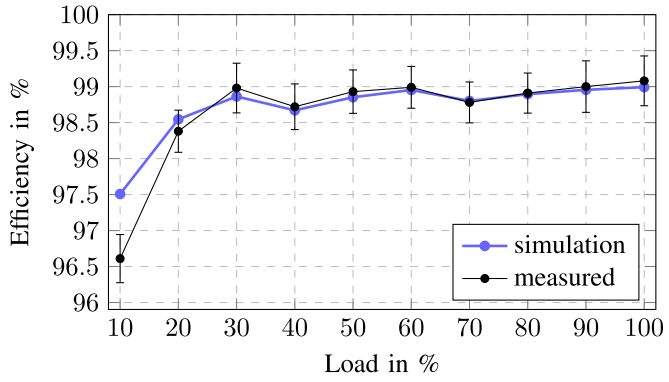

Fig. 15. PFC efficiency over the load measured from 10% up to 100% load (500 W) with measurement uncertainty compared with simulation, peaking at 99.07% at full load.

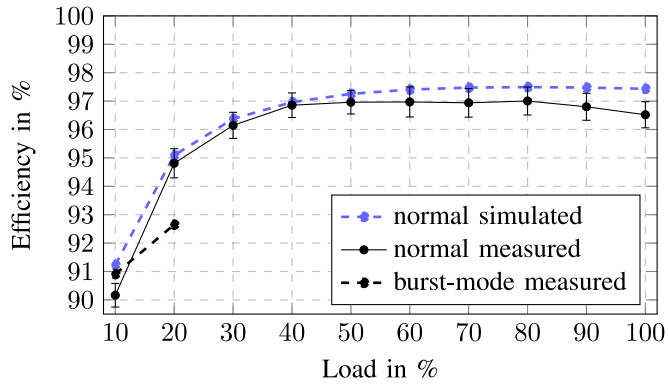

Fig. 17. Simulated and measured PS-ZVS bridge efficiency over the load for normal operation and burst-mode operation with measurement uncertainty.

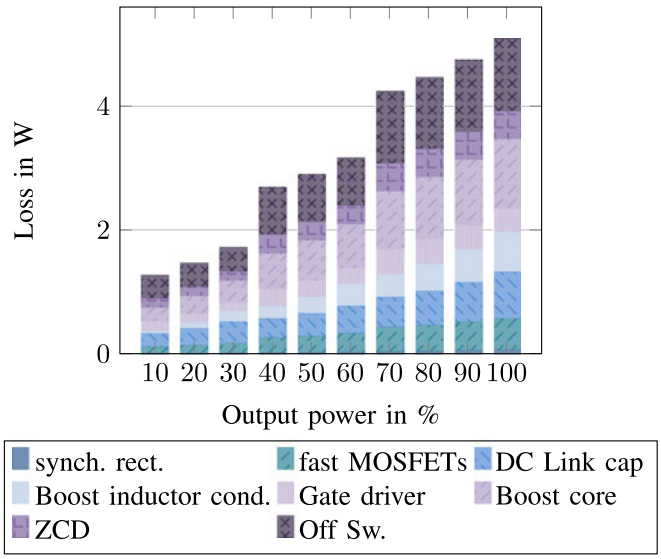

Fig. 16. PFC loss breakdown for a single stage with phase shedding over different load points (100% load correspond to 500 W).

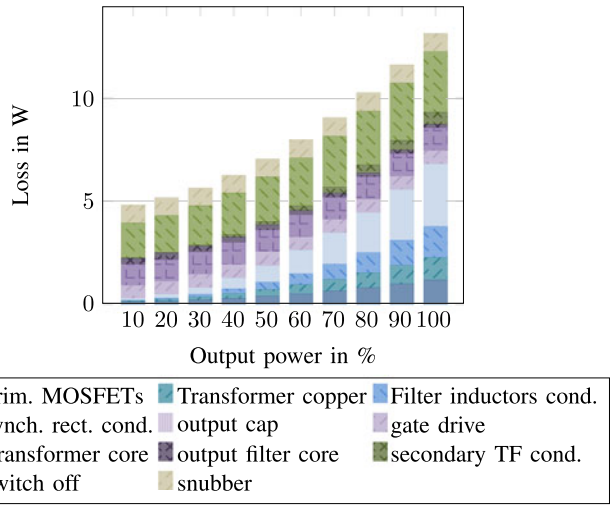

Fig. 18. PS-ZVS bridge loss breakdown over the load.

with external triaxial shunts with a stated accuracy of 0.03% of the reading and a phase error of less than 0.1° at 100 kHz. The calculation of the measurement errors is shown in detail in the appendix. The measured results are compared in the following with the results obtained from simulation. Additionally, the required efficiency for titanium certification is shown. In the following, the individual stages of a module have been measured and analyzed, like in Fig. 15 where the efficiency of the PFC over the load is shown and compared with results obtained from simulation. Drops in efficiency, which result from changing the number of active phases and with that additional gate, magnetic and ZCD losses can be seen. The simulation corresponds well with the measurement, except for light load (10% load). The PFC has its peak efficiency at 100% load with measured 99.07%. The loss breakdown of the PFC over the load is shown in Fig. 16.

Fig. 17 shows the efficiency of the PS-ZVS bridge over the load with the addition of the implemented burst-mode, where it is shown that burst-mode improves the efficiency for 10% load; however at higher loads like 20%, normal operation achieves again a higher efficiency. The increased output voltage ripple during burst-mode operation was measured at 10% load with 650 mV. Fig. 18 shows the corresponding loss breakdown. The ac loss for the output filter is minimal; therefore the dc and ac conduction loss of the output filter were combined.

The efficiency for a whole module is presented in Fig. 19. Fig. 19 shows that the measured efficiencies are high enough for the titanium criteria. Only at 10% load a modification to the PS-ZVS bridge control was necessary. In order to boost the light load efficiency, the control changes into burst mode. The slight drops in efficiency which can be seen between 30% and 40% load and as well between 60% and 70% result from changing the number of active phases of the PFC. The origin of the losses for the complete modules over the load is presented in Fig. 20.

A. *Parallel/Serial Operation*

Theoretically, for modular converter systems four different connection methods for the inputs and outputs are possible: input parallel output serial (IPOS), input parallel output parallel

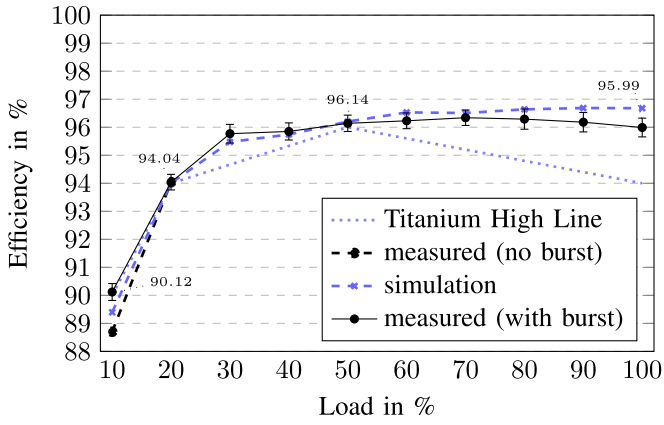

Fig. 19. Simulated efficiency of the whole SMPS; achieved efficiency with simulations (x, dashed); measured efficiency with measurement uncertainty (dot, solid); required efficiency for titanium grade (high line) (dotted).

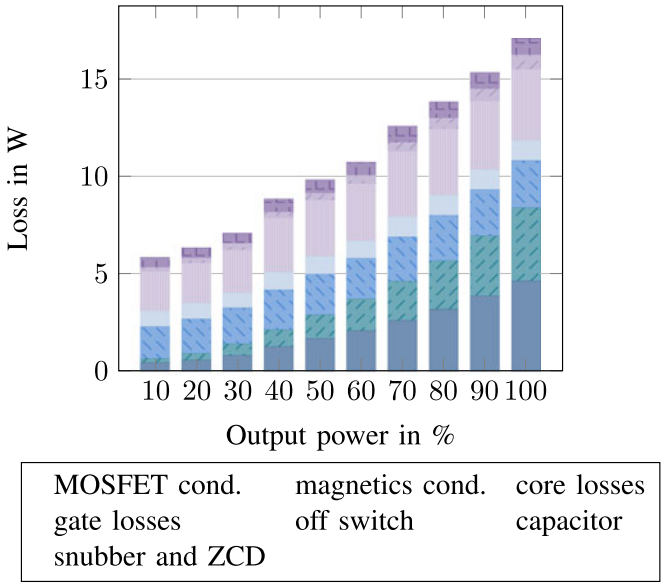

Fig. 20. Loss breakdown over the load for the complete module.

(IPOP), input serial output serial (ISOS), and input serial output parallel (ISOP), in which the ipop is today due to redundancy requirements in server power supplies the most common configuration [27]. All the modular converter concepts require for a stable operation that the input voltage is distributed equally among the modules. This always holds true for IPOS and IPOP systems and depending on the output configuration that either the output voltage or the output current is shared equally [28]. This often requires to measure either the output or the input current of the converter, [29]–[31]. The solution proposed here connects the outputs of the PS-ZVS-bridges in parallel, requiring the full output voltage of each PS-ZVS-bridge, but only half the output current, resulting in an ISOP or in an IPOP system. In order to obtain "output current sharing between the modules," one module always takes on the master role where the other has the slave role. For the master module, all feedback loops for the control are active, whereas certain feedback loops for the slave

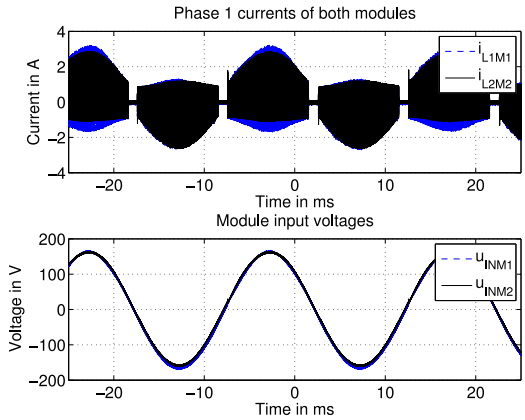

Fig. 21. Measurement of both modules running at 230 V in series connection; (top) currents of phase 1 of module 1 and 2; (bottom) module input voltages.

module, the output voltage control and the dc-link voltage control, are disabled. The slave module receives the required values from the master module which ensures that the output current is shared between the modules. During the ISOP operation at high line input, the voltage across the input capacitors can be balanced by either both or just one module. For the presented prototype, only the master module takes care of balancing the input voltages, which is experimentally verified in Fig. 21. A slight difference in the input voltages can be detected which is mainly due to the nonlinearity of the used error amplifiers to measure the input voltages of the modules.

VIII. Conclusion

The performance of the TCM PFC as well as of the PS-ZVS bridge with low-voltage MOSFETs was shown and has been experimentally verified. It clearly shows the advantages of using lower voltage MOSFETs with a better FOM like the OptiMOS for achieving high efficiencies even at low line input. Furthermore, it shows how a careful calculation of losses leads to the accurate evaluation of the efficiencies, which is required for the design of highly efficient circuits and the reduction of the time required to find optimal components by trial and error. It also points out the largest losses already during the design process, which helps from the start of the design to minimize them. A next step for further improvements could be to replace the PS-ZVS bridge with an *LLC* converter, which should boost light-load efficiency and reduce the turn-off losses, with the aim to achieve future efficiency certifications by the 80 PLUS organization.

Appendix

A. Electronic Components

The simulations are based on the electronic components shown in Table I. The synchronous rectifier switches S_{S1} and S_{S2} for the line rectification are paralleled three times each. The synchronous rectifier switches on the low voltage secondary S_{S3} and S_{S4} side are paralleled twice.

TABLE I
RELEVANT ELECTRONIC COMPONENTS

Part	Description	Details
1	PFC switches	OptiMOS 3, 250 V, 20 mΩ, IPB200N25N3G
2	PS-ZVS bridge switches	OptiMOS 3, 250 V, 60 mΩ, IPB600N25N3G
3	secondary switches	OptiMOS 5, 40 V, 1.45 mΩ, BSC014N04LSI
4	boost cores	Magnetics 55550A2, MPP, 180 uH, 81 turns
5	transformer core	Epcos PQ35/35, N95,26:2:2 turns
6	output filter core	Magnetics 55547A2, MPP, 7 turns
7	DC-link electrolytic cap	Rubycon BXF series, 7 × 120 μF paralleled
8	DC-link MLCC	TDK C5750 Series, 80 × 2.2 μF paralleled
9	output MLCC 12 V	AVX X7R 21 × 10 μF paralleled
10	output electrolytic 12 V	Nippon Chemicon LXV series 3 × 330 μF paralleled
11	isolated measurements	ADUM 3190 error amplifier
12	primary side gate driver	Si8235, 4 A version, dual isolated
13	secondary side gate driver	UCC27532, 5 A dual low-side driver

B. AC Losses

For the calculation of the ac losses, a distinction between a foil or a round inductor must be made.

1) Foil: For foil conductors the factor F_{Sf}, which defines the ratio of the skin resistance over the DC-resistance, can be calculated with

$$F_{Sf} = \frac{R_{\mathrm{skin}}}{R_{\mathrm{DC}}} = \left(\frac{h}{\delta}\right)\left(\frac{\sinh\left(\frac{2h}{\delta}\right) + \sin\left(\frac{2h}{\delta}\right)}{\cosh\left(\frac{2h}{\delta}\right) - \cos\left(\frac{2h}{\delta}\right)}\right) \tag{8}$$

with

$$\delta = \frac{1}{\sqrt{\pi f \sigma u_0}} \tag{9}$$

where δ is the skin depth, h the foil thickness, f the frequency, u_0 the free space permeability, and σ the electric conductivity of copper. The proximity effect is calculated individually for each layer where it is assumed to be zero for the first layer. For the second layer and second winding of the transformer, the proximity effect was calculated with

$$\begin{aligned} F_{Pf} &= \frac{R_{\mathrm{prox(n)}}}{R_{\mathrm{DC}}} \\ &= 2n\,(n-1)\left(\frac{h}{\delta}\right)\left(\frac{\sinh\left(\frac{h}{\delta}\right) - \sin\left(\frac{h}{\delta}\right)}{\cosh\left(\frac{h}{\delta}\right) + \cos\left(\frac{2h}{\delta}\right)}\right) \end{aligned} \tag{10}$$

where n is the layer with a total thickness of 400 μm for the second layer, [32], [33].

2) Round Conductor: For round conductors the factor F_{Sr} can be calculated with below equation, [33], [34]

$$\begin{aligned} F_{Sr} &= \frac{R_{\mathrm{skin}}}{R_{\mathrm{DC}}} \\ &= \frac{d}{2\delta\sqrt{2}} \frac{K_{\mathrm{ber}}(0,\xi)K'_{\mathrm{bei}}(0,\xi) - K_{\mathrm{bei}}(0,\xi)K'_{\mathrm{ber}}(0,\xi)}{K'_{\mathrm{ber}}(0,\xi)^2 + K'_{\mathrm{bei}}(0,\xi)^2} \end{aligned} \tag{11}$$

with

$$\xi = \frac{d}{\sqrt{2}\delta} \tag{12}$$

TABLE II
INTRINSIC UNCERTAINTY PARAMETERS OF THE POWER ANALYZER

Norma 5000 with PP50 modules		
max. uncertainty of reading AC (%)	$k_{d\,\mathrm{AC}}$	0.05
max. uncertainty of range AC (%)	$k_{g\,\mathrm{AC}}$	0.05
max. uncertainty of reading DC (%)	$k_{d\,\mathrm{DC}}$	0.1
max. uncertainty of range DC (%)	$k_{g\,\mathrm{DC}}$	0.1
phase uncertainty in degrees	k_a	0.01
max. uncertainty of shunt reading (%)	k_s	0.03

K_{ber} and K_{bei} are the Kelvin functions of the first kind for the order zero or two (first index). K'_{ber} and K'_{bei} are the derivatives of the original Kelvin functions. These equations are only valid for sinusoidal currents. To calculate the losses for nonsinusoidal currents, a Fourier analysis of the current waveform is needed. For each frequency component of the Fourier analysis, the skin and proximity effect losses are calculated and the sum is taken to obtain the total losses. For the proximity effect, the distance between the conductors (interwire distance ν) and the distance to the next layer (interlayer distance h) must also be considered [35]. Since d/δ is very large in this case, the Ferreira or Dowell Method show inaccuracies. The filter inductor consists only of one layer; therefore the interlayer distance h/d was used with the maximum distance available from the table, [35]. Equation (13) with the curve-fitting coefficients from the FEM calculation was used to calculate additional losses caused by the proximity effect afterward

$$\begin{aligned} F_{Pr} = (1-\omega)k_1\sqrt{(k_2)}\frac{d}{\delta} \\ \frac{\sinh\left(\sqrt{k_2}\frac{d}{\delta}\right) - \sin\left(\sqrt{k_2}\frac{d}{\delta}\right)}{\cosh\left(\sqrt{k_2}\frac{d}{\delta}\right) + \cos\left(\sqrt{k_2}\frac{d}{\delta}\right)} + \omega\hat{d}\left(\frac{d}{\delta}\right) \end{aligned} \tag{13}$$

with

$$\hat{d}\left(\frac{d}{\delta}\right) = \frac{K \cdot \frac{d}{\delta}}{\left(\left(\frac{d}{\delta}\right)^{-3n} + b^{3n}\right)^{\frac{1}{n}}} \tag{14}$$

where K is a constant of 0.096 and n, ω, k_1, k_2 are interpolated from the curve fitting coefficients given in [35].

C. Measurement Uncertainty

The measurement uncertainty of the power analyzer was calculated with the following equations and parameters given for the power analyzer from Table II.

The additional magnitude dependent factors k_v for the measured voltage and k_i for the current are calculated with

$$k_{v,i} = \frac{\text{Reading (V,I)}}{\text{Range(V,I)}} \tag{15}$$

in which the voltage and current uncertainty in percent of the reading can be calculated with

$$F_{v,i} = \overset{+}{-}\left(k_{\mathrm{dDC,AC}} + \frac{k_{g\mathrm{DC,AC}}}{k_{v,i}}\right). \tag{16}$$

Standard uncertainties are combined by the square root of the sum of their quadratures. With this the combined uncertainty for the current measurement with the shunt can be calculated, see

$$u_{i,c} = \sqrt{\sum_{i=1}^{n} \left(\frac{\partial f}{\partial x_i}\right)^2 u_{x,i}^2} = \sqrt{(F_i \cdot \text{Reading (I)})^2 + (k_\text{s} \cdot \text{Reading (I)})^2}. \quad (17)$$

The power uncertainty in percent of the reading is then calculated with (18) in which the last term is only needed in case of an ac measurement. In (18), PF stands for the measured power factor and k_p is the magnitude dependent phase error, which can be calculated with

$$F_p = \overset{+}{-} \left(F_\text{v} + \frac{u_{i,c}}{\text{Reading (I)}} + k_a \cdot k_p \frac{\pi}{1.8} \sqrt{\frac{1}{\text{PF}^2} - 1} \right) \quad (18)$$

$$k_p = \max \left[1; \sqrt{\frac{1}{k_v}}; \sqrt{\frac{1}{k_i}} \right]. \quad (19)$$

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