A Modular Multilevel Converter With DC Fault Handling Capability and Enhanced Efficiency for HVdc System Applications

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***Abstract*—This paper proposes a modular multilevel converter (MMC) topology for high-voltage dc (HVdc) system applications. The proposed MMC employs two half-bridge converters, a cascade of networks that consist of electronic switches, and multiple capacitors. Thus, charged capacitors are inserted in series with the arm current path, for a desired level of the output ac voltage. The switches that must be turned ON are judiciously selected for the most efficient current path. The proposed MMC also offers dc-side fault handling capability. The paper compares the proposed MMC with the half-bridge submodule-based MMC, full-bridge submodule-based MMC, and clamp-double submodule-based MMC technologies. It is shown that the proposed MMC is more efficient than the three aforementioned MMC technologies, while it offers the same fault handling capability as that of an equivalent full-bridge-based MMC. Time-domain simulation studies confirm the effectiveness of the proposed MMC under various normal and faulted operating scenarios, using detailed as well as reduced models.**

***Index Terms*—Fault handling capability, high-voltage dc, lattice modular multilevel converter (LMMC), modular multilevel converter.**

I. Introduction

THE modular multilevel converter (MMC) has become the converter of choice for high-voltage dc HVdc) systems, due to its modularity and low power losses [1]–[5]. These advantages have been tested in full in a project connecting Spain and France power grids through a 65-km-long dc link, using underground transmission lines [5]. However, many HVdc systems require long-distance overhead dc transmission lines, which are subject to atmospheric discharges and consequent temporary faults [5]–[7]. Therefore, widespread proliferation of MMC-based HVdc systems calls for configurations that are robust to dc-side faults.

To implement an MMC, the half-bridge submodule (HBSM) is the simplest and, therefore, the most common type of submodule. The HBSM inserts only one switch in series with the current path, for each ac voltage step and, therefore, the resultant MMC features low power losses [7]–[10]. The disadvantage of an HBSM-based MMC, however, is that in case of dc-side faults, the switches are disabled and the submodules become short circuits, allowing the ac grid to feed the dc fault [5]–[12]. Therefore, an MMC-based HVdc project using the HBSM relies heavily on the ac-side breakers [10], which do not have an operation time short enough to preclude damages to the converter during faults. The converter and the transmission line have to be designed to uphold this fault current for the time it takes for the ac breaker to operate, increasing the overall cost.

To address the aforementioned shortcoming, the full-bridge submodule (FBSM)-based configuration [5] and the clamp-double submodule (CDSM)-based configuration [9] have been proposed. An FBSM-based MMC is capable of driving the fault current down to zero, if its switches are disabled. Therefore, it isolates the ac and dc sides of the converter faster than an ac breaker. However, as compared to an HBSM-based MMC, an FBSM-based MMC has twice the number of series-connected switches in its current path and, consequently, features higher power losses. The CDSM, on the other hand, inserts, effectively, 1.5 switches per ac voltage step in its current path and, therefore, it features larger power losses than the HBSM-based configuration, but lower power losses than the FBSM-based configuration. A CDSM-based MMC is immune to dc-side faults, but the voltage that appears, effectively, under dc-side faults and opposes the ac grid voltage is half the total arm voltage [13]. Consequently, the fault current can flow if the grid voltage is adequately large. An in-depth analysis of faulted as well as normal operation of the aforementioned topologies can be found in [7].

To achieve both dc-side fault current handling capability and higher efficiency, a new MMC configuration is proposed in this paper. The proposed MMC, referred in this paper to as the *lattice modular multilevel converter* (LMMC) is implemented by two half-bridge converters, a cascade of networks that consist of electronic switches, and multiple capacitors, as discussed in Section II. It features lower power losses than equivalent an HBSM-based MMC, CDSM-based MMC, and FBSM-based MMC, while it offers the same fault handling capability as that offered by an FBSM-based MMC. The aforementioned objective is in line with the prior research efforts. For example, to reduce the cost and switching power losses of the FBSM, the *unipolar voltage FBSM* has been proposed in [14]. On the other hand, to enhance the dc fault handling capability of the CDSM, with the same conduction power losses, the *five-level cross-connected submodule* has been proposed in [15]. Further, the *three-level cross-connected submodule* proposed in [14] is an improved version of the five-level cross-connected submodule where the switching power losses are reduced. Moreover, various topologies for multilevel converters with reduced number

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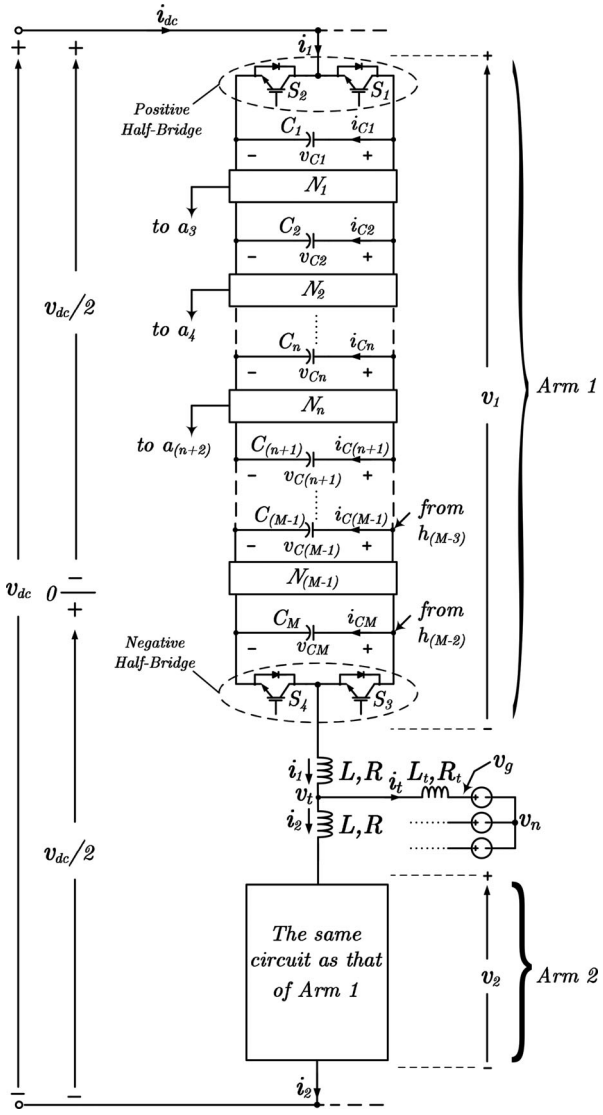

Fig. 1. Schematic diagram for one leg of the proposed MMC, the *LMMC*.

of dc sources and switching states, including topologies based on the packed *U-cell topology*, are discussed in [16]. However, since the HBSM is the most efficient configuration (regarding losses in the switches), the CDSM is no less efficient than all the other aforementioned configurations that feature the dc fault handling capability, and the FBSM, when subjected to a dc-side short circuit and disabled, requires the largest grid voltage before it allows the fault current to flow, this paper concentrates only on the HBSM, FBSM, and CDSM as its baselines. For ease of analysis, it is assumed in this paper that an MMC consists entirely of FBSMs, HBSMs, or CDSMs.

II. Proposed MMC: The LMMC

Fig. 1 shows a schematic diagram of the proposed MMC, i.e., the LMMC, based on the assumption that $M+1$ levels (M is assumed to be even) are to exist in the *ac-side terminal voltage*. As the figure shows, the upper arm of the converter, *Arm 1*, hosts $M-1$ identical five-terminal *networks*, M capacitors, and two half-bridge converters. Thus, starting from the top of an arm,

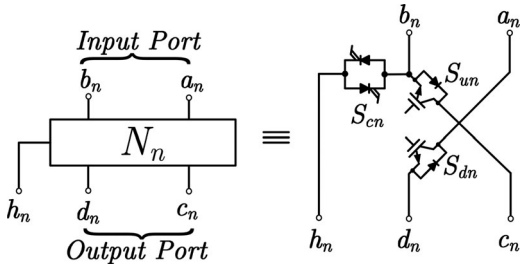

Fig. 2. Circuit of the *network*, the building block of the LMMC ($n = 1, 2, \ldots, M-1$).

Fig. 1 shows that, except for the first and last *networks*, the *input port* of each *network*, which is identified by respective terminals a and b of that *network*, is connected in parallel with the *output port* of the next *network*, which is identified by the corresponding terminals c and d of the *network*. However, terminals a and b of the first *network* are connected to, respectively, the positive and negative dc-side terminals of a half-bridge converter, the *positive half-bridge*, represented by switches S_1 and S_2. Also, terminals c and d of the last *network* are connected to the positive and negative dc-side terminals of another half-bridge converter, the *negative half-bridge*, which is constituted by switches S_3 and S_4. Fig. 1 also shows that, with the exception of the last two *networks*, terminal h of each *network* is connected to terminal a of the *network* after the next. Therefore, terminal h of the last *network* in each arm is not required. Fig. 1 further shows that the *input port* of the first network, the *output port* of the last network, and each pair of interconnected ports are connected in parallel with a capacitor whose voltage is represented by v_{Cj} ($j = 1, 2, \ldots, M$). The M capacitors are assumed to all have the same (nominal) capacitance. The lower arm, *Arm 2*, has the same structure and properties as the upper arm. All node voltages are expressed with reference to the *dc-side midpoint*, 0, which may be a physical or a virtual node.

Each *network* is a circuit of three fully controllable electronic switches, S_{un}, S_{dn}, and S_{cn}, as shown in Fig. 2 for the nth *network* ($n = 1, 2, \ldots, M-1$). The electrical connection associated with switch S_{un} and terminals b_n and c_n is referred in this paper to as a *positive regular link*, whereas the connection between terminals a_n and d_n through switch S_{dn} is called a *negative regular link*; they may simply be referred to as *regular links*. In addition, the connection associated with switch S_{cn} and terminals b_n and h_n is referred to as a *high-efficiency link*. Switches S_{un} and S_{dn} must be of the reverse-conducting type, e.g., IGBTs, whereas the switch for a *high-efficiency link*, S_{cn}, must be a bidirectional reverse-blocking switch. Thus, as indicated in Fig. 2, it is assumed in this paper that S_{cn} is implemented by antiparallel connection of two reverse-blocking IGCTs, such as those featured in [17]–[19]. Even though the IGCT is the preferred switch in applications with low switching frequencies, where the conduction power losses are dominant [20], [21], it is assumed to only be adopted for the *high-efficiency links* of the LMMC, due to its relatively high cost; the other switches are assumed to be of the IGBT type. Since terminal *h* is not used in the last network, switch $S_{c(M-1)}$ is not required.

It should be pointed out that, in each network only one switch at a time is permitted to be ON. Thus, for example, if S_{cn} is

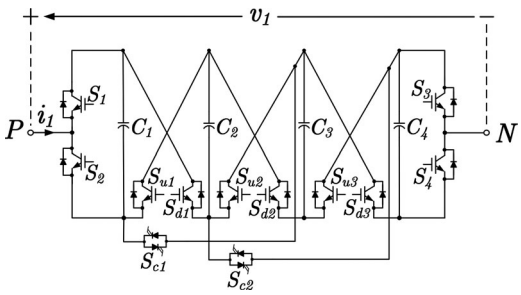

Fig. 3. Schematic diagram of the upper arm circuit of a five-level LMMC.

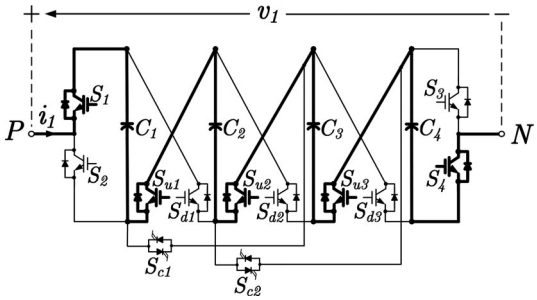

Fig. 4. The current path for the upper arm of the five-level LMMC of Fig. 3 if all capacitors must be inserted.

turned ON, S_{un} and S_{dn} are kept OFF, and so on. Also, the switches of each half-bridge converter are complementary, that is, only one of them is permitted to be ON at a time.

III. Principles of Operation

A. Normal Operation

Essentially, synthesis of the *ac-side terminal voltage*, v_t, and consequently the *ac-side terminal current*, i_t, boils down to the synthesis of *arm voltages*, v_1 and v_2 (see Fig. 1). In the LMMC, a particular *arm voltage* level is synthesized by *inserting* an appropriate number of capacitors in series with the path for the corresponding *arm current*, i_1 or i_2. Therefore, the capacitors that are not required are *withdrawn*, that is, they are left out of the *arm current* path, by diverting the current away from them, and by redirecting the current through alternative *regular links* and/or *high-efficiency links*. Whenever possible, *high-efficiency links* are preferred over the *regular links*, due to their lower conduction power losses, and are tuned *on* based on the algorithm described in Section IV. Since a desired *ac-side terminal voltage* level can almost always be synthesized by various combinations of a certain number of inserted capacitors, whether or not a capacitor is inserted also depends on the voltage across the capacitor (which must be maintained at about a nominal value). The LMMC assumes and requires the same nominal voltage for all capacitors.

For ease of visualization, and without loss of generality, the aforementioned principles of operation are illustrated for a five-level LMMC, that is, for an LMMC whose ac-side terminal voltage has five levels; one (the upper) arm of the LMMC is shown in Fig. 3, in which the internal circuitry of the constituting three networks are shown explicitly.

Fig. 4 illustrates a case where the maximum *arm voltage* is required and, therefore, the capacitors are all inserted (the thick line indicates the *arm current* path). In this case, no *high-efficiency link* can be tuned on and placed in series with the *arm current* path. By contrast, let us consider a situation in which half of the maximum *arm voltage* is to be synthesized, hence, two inserted capacitors. Let us then assume that the control has specifically required capacitors C_3 and C_4 to be inserted. Then, a *high-efficiency link* can be turned ON, as shown in Fig. 5, to withdraw capacitors C_1 and C_2 out of the current path. Alternatively, if the control requires C_2 and C_3 to be out of the current path, then no *high-efficiency link* can be used, but only *regular links* are employed, as Fig. 6 indicates.

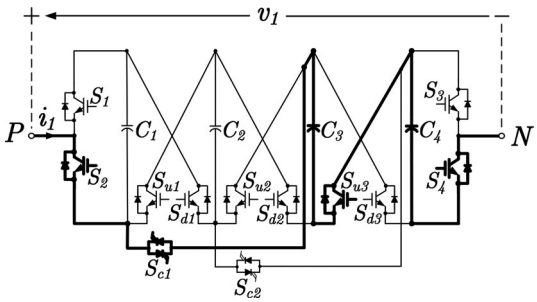

Fig. 5. Current path for the upper arm of the five-level LMMC of Fig. 3 if only capacitors C_3 and C_4 must be inserted.

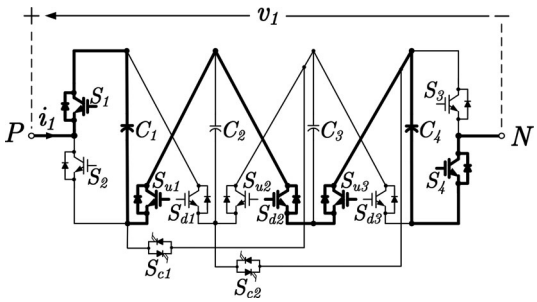

Fig. 6. Current path for the upper arm of the five-level LMMC of Fig. 3 if only capacitors C_1 and C_4 must be inserted.

For the circuit of Fig. 5, the number of switches in series with the arm current path is 4, due to the *high-efficiency link* that is ON. This is the same number of switches as that in an HBSM-based MMC featuring five levels in its *ac-side terminal voltage*. By contrast, in the cases represented by Figs. 4 and 6, the number of switches in series with the arm current path is 5, which is higher than that in the HBSM-based MMC. However, the situation where no *high-efficiency link* could be turned ON is less common. Therefore, the five-level LMMC is almost the same as the HBSM-based MMC, in terms of the number of switches in series with the arm current path. However, for an LMMC with a large M, which is typical in HVdc systems, the LMMC features a lower number of switches for each *ac-side terminal voltage* level than an equivalent HBSM-based MMC, due to the possibility of turning ON a large number of *high-efficiency links*, therefore, the LMMC, in general, offers a higher

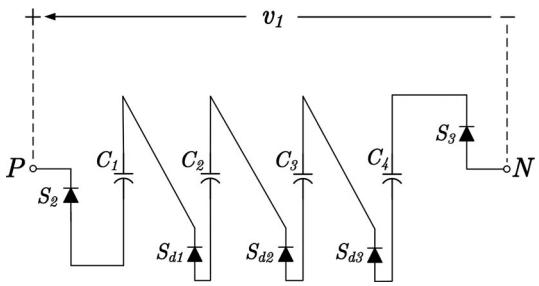

Fig. 7. Schematic diagram of the upper arm circuit of the five-level LMMC of Fig. 3 when the switches are OFF, e.g., subsequent to a dc-side fault.

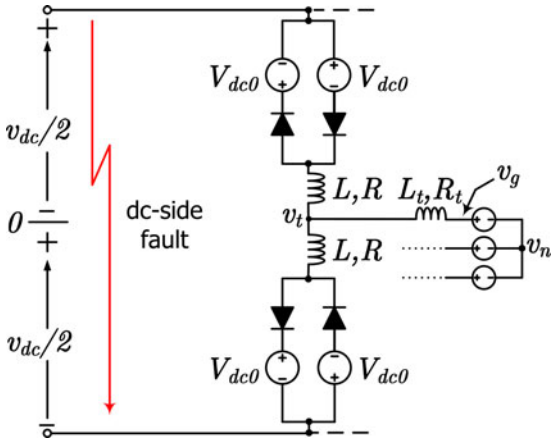

Fig. 8. Equivalent circuit of the LMMC when the switches are OFF, e.g., subsequent to a dc-side fault; only one leg is shown.

efficiency than an equivalent HBSM-based MMC, as Section VI explains.

B. Operation Under a DC-Side Fault

Subsequent to a dc-side fault, the switches are all turned OFF by the control. This, effectively, connects the capacitors in series with the antiparallel diodes of the reverse-conducting switches of the *negative regular links*, while the *high-efficiency link* are open, as shown in Fig. 7 for the LMMC of Fig. 3. The LMMC in this condition can therefore be represented by an equivalent circuit, Fig. 8, in which the capacitors of each arm are represented by a corresponding voltage source. Therefore, assuming that prior to the fault the capacitor voltages have reached the steady-state value V_{dc0}/M (where V_{dc0} signifies the prefault steady-state value of v_{dc}), the diodes turn OFF subsequent to the fault and the arm current drops to zero, unless the grid line-to-line voltage exceeds $2V_{dc0}$.

IV. Switching Scheme

The switching scheme of the LMMC adopts *near level control modulation* (NLC) strategy (a modulation strategy suitable for MMCs with a large number of submodules) [22], to determine the arm voltages that must be synthesized for a given ac-side terminal voltage. In turn, an arm voltage is used to determine the number of capacitors that must be inserted in the corresponding arm. The switching scheme also employs the sorting algorithm of [7], in its *voltage balancing algorithm* (VBA), to determine what specific capacitors must be inserted, to ensure that the capacitors all have voltages about the value $\overline{v}_c = v_{dc}/M$. Thus, the output of the switching scheme is an M-element vector of the form $\mathbf{x} = [x_1, x_2, x_3, \ldots, x_{(M-1)}, x_M]$, for each arm. In the vector, referred in this paper to as the *VBA array*, element x_j $(j = 1, 2, \ldots, M)$ represents the state, inserted or withdrawn, of the jth capacitor in the host arm. Thus, $x_j = 1$ corresponds to an inserted capacitor, whereas $x_j = 0$ indicates a withdrawn capacitor. The *VBA array* is then used to determine what switches must be turned ON in the corresponding arm, starting from capacitor C_1 to capacitor C_M. Thus, advancing the index j (corresponding to the jth capacitor) from 1 to $M-1$, the switching scheme determines the current path and the switches that must be turned ON. Five cases are faced, as explained below, depending upon what network a switch belongs to.

A. Capacitor Connected to Positive Half-Bridge: $j = 1$ Corresponding to C_1

The first capacitor, C_1, is connected to the LMMC arm through the *positive half bridge*. Therefore, the switching scheme must generate the state for the switches S_1 and S_2. If C_1 is to be inserted, then S_1 must be turned ON, whereas S_2 is turned OFF, and vice versa.

B. First Capacitor and Intermediate Capacitors: $1 \leq j \leq (M-3)$ Corresponding to $C_1, C_2, \ldots, C_{(M-3)}$

The first capacitor is also connected to a network, as are capacitors $C_2, C_3, \ldots, C_{(M-1)}$. Capacitors $C_{(M-2)}$ and $C_{(M-1)}$ are subject to different rules for their insertion into the arm and, therefore, are discussed separately in Sections IV-C and IV-D. The rules mentioned in this section apply only to capacitors $C_1, C_2, \ldots, C_{(M-3)}$.

If the jth capacitor is to be inserted, i.e., $x_j = 1$, the series connection to the $(j+1)$th capacitor can be established through switch S_{uj} (*positive regular link*). On the other hand, the series connection to the $(j+2)$th capacitor can be established through switch S_{cj} (*high-efficiency link*). As mentioned in Section III-A, the connection through switch S_{cj} is preferred, but it is subject to the two following constraints:

1) If capacitor $C_{(j+1)}$ is to be inserted (i.e., if $x_{(j+1)} = 1$ in the VBA array), then if S_{cj} is activated, C_j is connected directly to $C_{(j+2)}$. Consequently, $C_{(j+1)}$ is automatically withdrawn from the arm, and the VBA array state of $x_{(j+1)} = 1$ cannot be complied with.
2) If capacitors $C_{(j+2)}$ and $C_{(j+3)}$ are to be withdrawn and inserted, respectively (i.e., if $x_{(j+2)} = 0$ and $x_{(j+3)} = 1$), then if switch S_{cj} is ON while $C_{(j+2)}$ is withdrawn, the only available path for the current is through $S_{d(j+2)}$ (corresponding to a *negative regular link*). On the other hand, if $S_{d(j+2)}$ is ON, there is no connection available to $C_{(j+3)}$. Thus, $C_{(j+3)}$ is forced to be withdrawn from the arm, and the VBA array state of $x_{(j+3)} = 1$ cannot be complied with.

In both aforementioned situations, the VBA array states for $C_{(j+1)}$ and $C_{(j+3)}$ cannot be obeyed if S_{cj} is used. Therefore, in these two situations, S_{cj} must be kept OFF, and, instead, switch S_{uj} is turned ON.

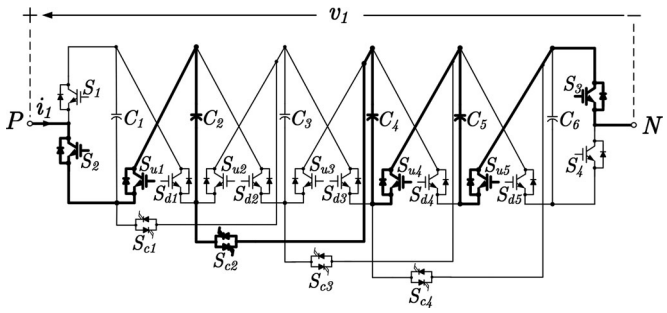

Fig. 9. Arm current path and ON switches in the upper arm of a seven-level LMMC, if $\mathbf{x} = [0, 1, 0, 1, 1, 0]$.

If the jth capacitor is to be withdrawn, that is, if $x_{(j)} = 0$, the only available connection to $C_{(j+1)}$ is through S_{dj}. Hence, S_{dj} must be turned ON.

C. Capacitor Connected to the Last High-Efficiency Link: $j = (M-2)$ Corresponding to $C_{(M-2)}$

If capacitor $C_{(M-2)}$ is to be inserted, then the activation of switch $S_{c(M-2)}$ is subject to only one of the two constraints described in Section IV-B; if $C_{(M-1)}$ is to be inserted, switch $S_{c(M-2)}$ must be kept OFF, and, instead, $S_{u(M-2)}$ is turned ON. If $C_{(M-1)}$ is to be withdrawn, then $S_{c(M-2)}$ must be turned ON.

If capacitor $C_{(M-2)}$ is to be withdrawn, then $S_{d(M-2)}$ must be turned ON.

D. Capacitor Before the Last: $j = (M-1)$ Corresponding to $C_{(M-1)}$

For capacitor $C_{(M-1)}$, there is no switch $S_{c(M-1)}$ in the $(M-1)$th network. Therefore, if $C_{(M-1)}$ is to be withdrawn, then $S_{d(M-1)}$ must be turned ON. Otherwise, $S_{u(M-1)}$ must be turned ON.

E. Capacitor Connected to Negative Half-Bridge: $j = M$ Corresponding to C_M

For capacitor C_M, i.e., the last capacitor, the only switches left are the switches that form the *negative half bridge*. Thus, if C_M is to be inserted, then S_4 must be turned ON. Otherwise, S_3 must be turned ON.

Fig. 9 shows the arm current path and the *on* switches of the upper arm of a seven-level LMMC, corresponding to a VBA array of $\mathbf{x} = [0, 1, 0, 1, 1, 0]$, based on the algorithm described in Sections IV-A through IV-E.

V. Comparison With the Conventional MMC

The structures of the LMMC and conventional MMC differ in two major respects, as described below.

A. Building Blocks

In HVdc applications, pulse-width modulation is avoided for its associated switching power losses. Rather, the right number of capacitors are inserted in series with the current path of the host arm, for a desired *ac-side terminal voltage*. This goal is achieved in the LMMC by the *networks*, whereas, as Fig. 10 illustrates, in the conventional MMC the submodules perform this task. Therefore, a *network*, together with the capacitor connected to its terminals a and b, constitute a building block of the LMMC, whereas the submodules are the building blocks of the conventional MMC.

In both the conventional MMC and the LMMC, the number of voltage levels in the produced *ac-side terminal voltage*, $M+1$, is one more than the number of capacitors in series with the current path of the host arm, M. The number of capacitors, in turn, determines the number of *networks* or submodules. As mentioned in Section II, in the LMMC the number of networks is one less than the number of capacitors, whereas in a conventional MMC, the number of submodules equals either the number of capacitors (in the HBSM- and FBSM-based MMCs) or half of the same (in the CDSM-based MMC). Consequently, in both the LMMC and a conventional MMC, the operation boils down to inserting the right number of capacitors in the arm current part.

Another difference between a conventional MMC and the LMMC is that, as explained in Section II, in the LMMC, the cascade of *networks* in each arm is interfaced with the rest of the converter through two half-bridge converters: the *positive half bridge* and the *negative half bridge*, whereas, in a conventional MMC, a submodule is directly interfaced at its ac-side terminals with the rests of the converter.

B. Interconnections

In the LMMC, the *networks* are interconnected through *regular links* and *high-efficiency links*. Therefore, a capacitor may be inserted in the current path of the host arm through various combinations of switches. This, in turn, means that the switches are switched less frequently, in comparison with those in a conventional MMC, thus reducing the switching stresses. In addition, as explained in Section II, a *network* can be connected not only to the next *network*, but also to the *network* after the next, through the shortcuts offered by the *high-efficiency links*, thus, reducing the conduction power losses.

VI. Analysis of Power Losses

A. Number of Series-Connected Switches in An Arm

In an MMC adopting the NLC modulation strategy, switching power losses are negligible, and the overall power loss of the converter can be assumed to consist only of conduction power losses. Calculation of conduction power losses, on the other hand, requires knowledge of the number of switches in series with the arm current paths. In the HBSM-based MMC, CDSM-based MMC, and FBSM-based MMC, the number of series-connected switches per arm is fixed by the number of capacitors, M. In the LMMC, however, the number of series-connected switches depends not only on the number of inserted capacitors (or, equivalently, the ac-side terminal voltage at the instant), but also on what specific capacitors are inserted, due, in turn, to the number of ON high-efficiency links that varies based on the (time varying) VBA array. For example, as illustrated in Section III-A, the number of series-connected switches required for an ac-side terminal voltage of $v_{dc}/2$ can be 4 (see Fig. 5) or 5 (see Fig. 6), whereas, independent from the ac-side terminal voltage level, it is 4 in an HBSM-based MMC, 6 in a

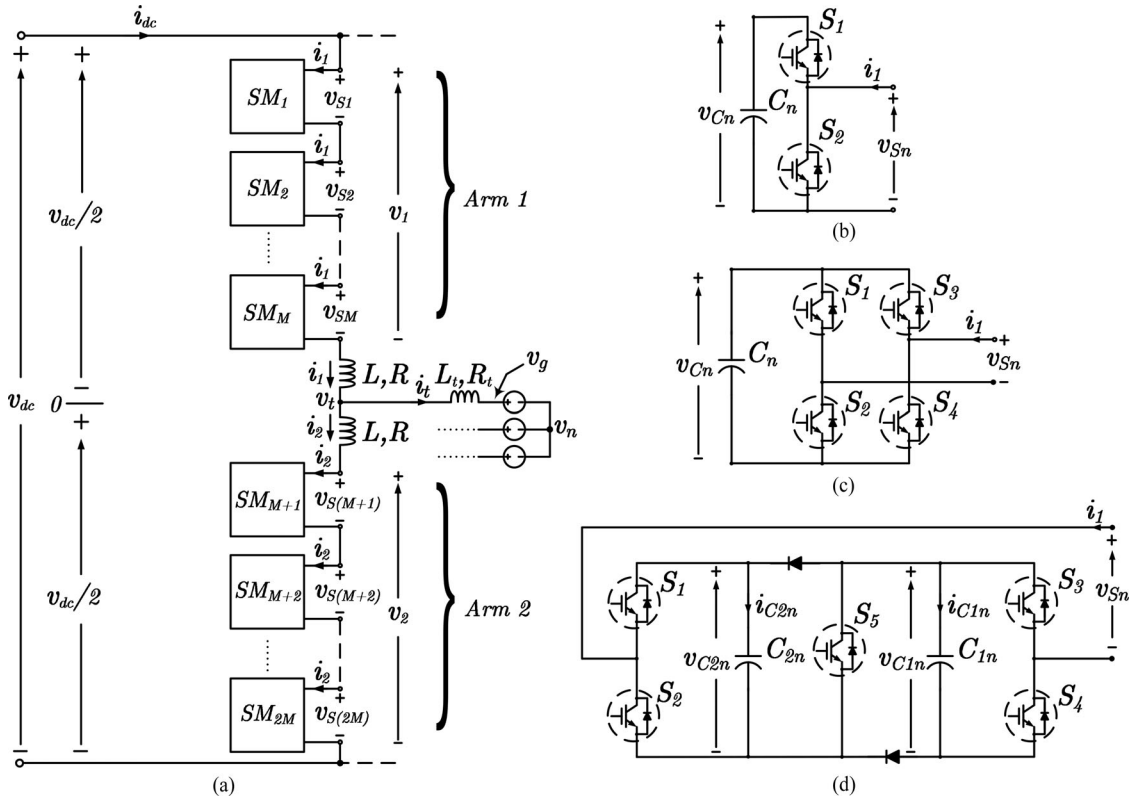

Fig. 10. Schematic diagrams of (a) one leg of a conventional three-phase MMC, (b) an HBSM in the upper arm, (b) a FBSM in the upper arm, and (c) a CDSM in the upper arm.

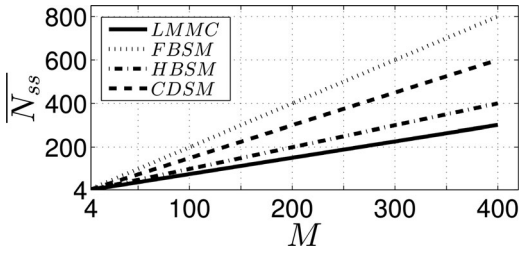

Fig. 11. Average number of series-connected switches per arm versus the number of capacitors, for different MMC technologies.

TABLE I
AVERAGE NUMBER OF SERIES-CONNECTED SWITCHES PER SRM

Converter	$\overline{N_{ss}}$
LMMC	$0.75M + 1.4$
HBSM-based MMC	M
CDSM-based MMC	$1.5M$
FBSM-based MMC	$2M$

CDSM-based MMC, and 8 in an FBSM-based MMC. Therefore, conduction power losses of the LMMC are computed based on the average number of series-connected switches and for a given ac-side terminal voltage swing (or, equivalently, for a given amplitude modulation index).

Fig. 11 shows the average number of series-connected switches, $\overline{N_{ss}}$, versus the number of capacitors, M, for the LMMC, assuming the maximum ac-side terminal voltage swing, i.e., a modulation index of unity. For the HBSM-based MMC, CDSM-based MMC, and FBSM-based MMC, $\overline{N_{ss}}$ is the same as the number of series-connected switches, which is independent of the modulation index, as mentioned earlier, and equal to M, $1.5M$, and $2M$, respectively. However, to determine $\overline{N_{ss}}$ in the LMMC, the switching state generation algorithm of Section IV was coded in MATLAB software environment, to count the number of series-connected switches and calculate its average for $M = 4$ through $M = 20$, in incremental steps of 2; the piece of the curve that corresponds to $M > 20$ is then drawn based on the assumption that $\overline{N_{ss}}$ rises linearly with M, a trend observed over the range $4 \leq M \leq 20$. Further, an inspection of the curve indicates that $\overline{N_{ss}}$ equals $0.75M + 1.4$ in the LMMC; Table I summarizes this conclusion. It is observed that the LMMC features a smaller average number of series-connected switches than the other topologies.

Fig. 12 shows the variation of $\overline{N_{ss}}$ versus the modulation index, $\widehat{m}$, for three different values of M in the LMMC.

B. Power Losses

Using the corresponding average number of series-connected switches, as reported in Table I, and the RMS values of the arm currents, Table II reports the power loss expressions for the LMMC and the three other MMC topologies for a large M.

VII. ANALYSIS OF VOLTAGE STRESS

The voltage stress on the switches of the LMMC can be characterized through the circuit of one sample *network*. The

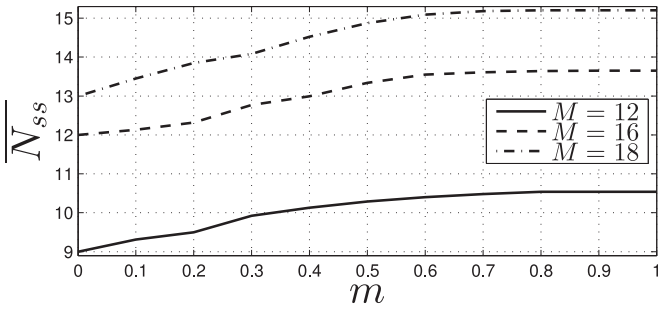

Fig. 12. Variation of $\overline{N_{ss}}$ with the modulation index, in the LMMC.

TABLE II
POWER LOSS EXPRESSIONS FOR LARGE M

Converter	Power Loss	Power loss relative to LMMC
LMMC	$\approx (I_1^2 + I_2^2)(0.75M)R_{\text{on}}$	1
HBSM-based	$(I_1^2 + I_2^2)MR_{\text{on}}$	1.33
CDSM-based	$(I_1^2 + I_2^2)(1.5M)R_{\text{on}}$	2
FBSM-based	$(I_1^2 + I_2^2)(2M)R_{\text{on}}$	2.66

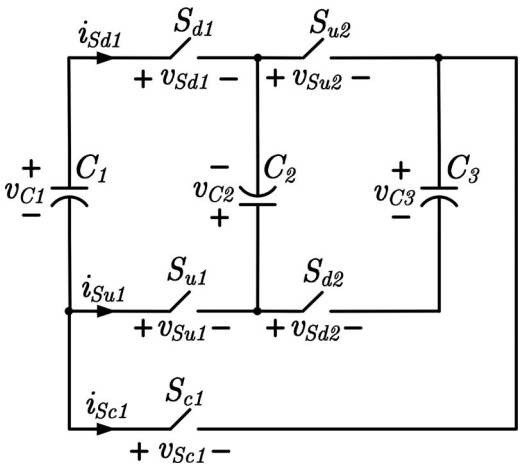

Fig. 13. Rearranged partial circuit for the voltage stress analysis in the switches connecting three capacitors in the LMMC arm.

network considered here, Fig. 13, is a subset of the upper arm circuit of a five-level LMMC, Fig. 3, in which the switches are considered ideal to enable one to concentrate on the essentials. It is further assumed that the switches have snubbers to ensure safe static and dynamic voltage sharing.

A. Switch S_{u1}

The voltage across switch S_{u1} must be characterized for three different cases:

1) If S_{u2} is ON, while all other switches are OFF, the voltage across S_{u1} can be found from the mesh formed by S_{u1}, C_2, and S_{c1}. As Fig. 13 illustrates, the voltage across capacitor C_2 is divided between S_{c1} and S_{u1}, such that $v_{Su1} = v_{C2}/2$.

TABLE III
VOLTAGE ACROSS THE SWITCHES IN THE LMMC ARM

Switch	Most frequent voltage	Less frequent voltage
S_{un}	$\approx \overline{v}_c/2$	$\approx 2\overline{v}_c$
S_{dn}	$\approx 2\overline{v}_c$	-
S_{cn}	$\approx \pm\overline{v}_c$	$\approx \overline{v}_c/2$

2) If S_{c1} is ON, while all other switches are OFF, the voltage of S_{u1} is governed by the mesh formed by S_{u1}, S_{d2}, and C_3, and $v_{Su1} = v_{C3}/2$.
3) If S_{d1} is ON, while the other switches are all OFF, the voltage across S_{u1} is governed by the mesh constituted by C_1, S_{u1}, and C_2. Thus, the sum of the voltages across C_1 and C_2 appears across S_{u1}, that is, $v_{Su1} = v_{C1} + v_{C2}$. This issue exists also in the *five-level cross-connected submodule* [15].

B. Switch S_{c1}

The voltage across switch S_{c1} is inspected for three different cases:

1) If S_{u1} and S_{u2} are ON, while all other switches are OFF, the voltage across S_{c1} is governed by the mesh represented by C_2 and S_{c1}. Therefore, $v_{Sc1} = -v_{C2}$.
2) If S_{u1} and S_{d2} are ON, while all other switches are OFF, the voltage across S_{c1} is governed by the mesh formed by C_3 and S_{c1}. Hence, $v_{Sc1} = v_{C3}$.
3) If S_{d1} and S_{u2} are ON, while all other switches are OFF, the voltage across S_{c1} is governed by the mesh formed by C_1 and S_{c1}. Therefore, $v_{Sc1} = v_{C1}$.
4) If S_{u2} is ON, while all other switches are OFF, the voltage across S_{c1} is governed by the mesh represented by S_{u1}, C_2, and S_{c1}, and $v_{Sc1} = v_{C2}/2$.

C. Switch S_{d1}

Switch S_{d1} is rarely turned ON. When OFF, it withstands a voltage of about $2\overline{v}_c$, based on the same analysis conducted under item 3 in Section VII-A, and assuming that the VBA regulates all capacitor voltages at about $\overline{v}_c$).

Switch S_{c1} constitutes the *high-efficiency link* and, therefore, closes the arm current path for most of the time. Thus, even though switches S_{u1} and S_{d1} experience two capacitor voltages, they are often bypassed by S_{c1} (when both S_{u1} and S_{d1} are OFF). This reduces the voltage across S_{u1} by a factor of two and, also, permits S_{d1} to be ON less frequently than otherwise. It should be pointed out that the switching scheme of the LMMC (see Section IV) does not permit any other combination of switching states for S_{u1}, S_{d1}, S_{c1}, S_{u2}, and S_{d2}. Hence, no switch in a *network* can assume a voltage different in value from $0.5\overline{v}_c$, $\overline{v}_c$, and $2\overline{v}_c$. Table III summarizes the conclusions.

The conclusions made through the aforementioned analysis hold also for all the other *networks* of the LMMC.

VIII. SIMULATION RESULTS

Similar to other MMC technologies that adopt the NLC switching strategy, the LMMC produces low-distortion ac-side terminal current waveforms only if its ac-side terminal voltage

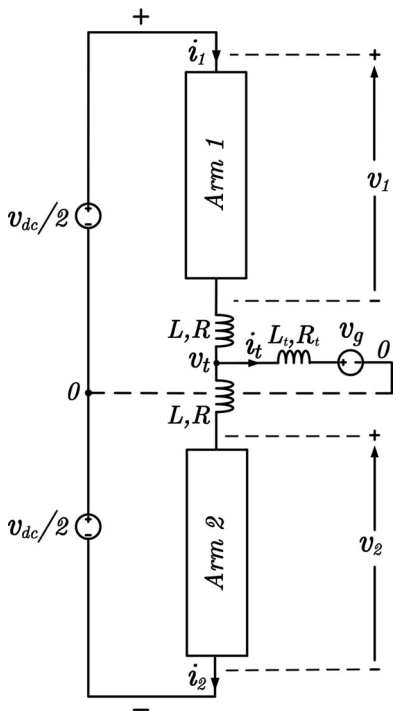

Fig. 14. Schematic diagram of the single-phase LMMC system for Case I.

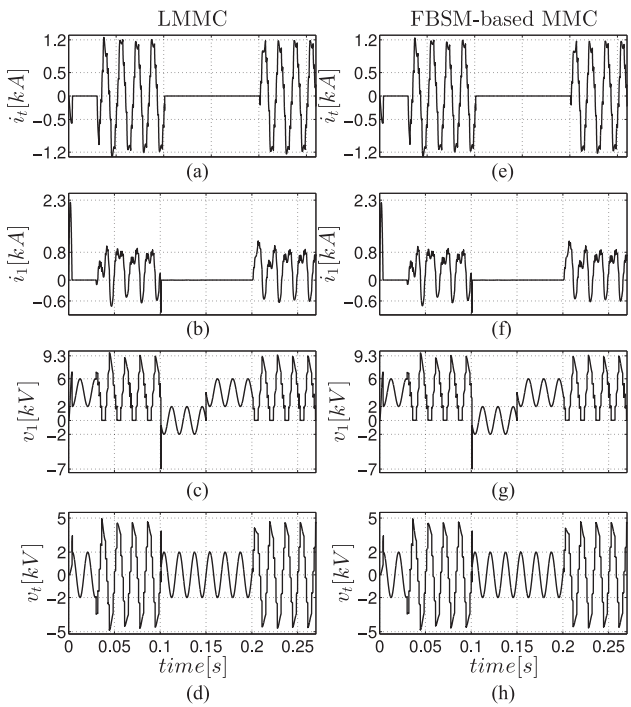

Fig. 15. Waveforms of selected variables in an open-loop controlled single-phase five-level LMMC (left column) and an equivalent FBSM-based MMC (right column), to various disturbances; Case I.

has an adequately large number of levels (e.g., corresponding to $M > 100$). Simulation models based on detailed models of the semiconductor switches are, however, difficult to develop and run for such an LMMC, due to excessive simulation runtime, limited number of nodes accommodated by the software packages, etc. Therefore, in this paper, *detailed models* were developed only for LMMCs with $M = 4$ and $M = 8$, for preliminary assessment of the principles of operation, salient features, and robustness to dc-side faults. The aforementioned detailed models were also used to verify the accuracy of the *equivalent-circuit-based model* that is used for simulating an LMMC with $M = 400$, in Section VIII-D, to further confirm the effectiveness of the control, the dc-side fault handling capability, and the quality of the synthesized voltages and currents, in a more realistic scenario. All simulations were conducted in the PSCAD/EMTDC software environment [23].

Due to space limitations, only a selection of the results are shown and discussed in the following sections. Moreover, if shown in a graph, only upper arm variables are displayed; the lower arm variables exhibit similar behaviors.

A. Case I

For this case, a detailed model of a single-phase five-level LMMC (i.e., with $M = 4$) was simulated. The LMMC, shown in Fig. 14 with its associated ac and dc systems, featured a *dc-side voltage*, v_{dc}, of 8 kV, which was impressed by two identical dc sources. The ac grid voltage and the modulating signal were represented by $v_g(t) = 2\sin(2\pi f_g t)$ kV and $m(t) = \sin(2\pi f_g t)$, respectively, where $f_g = 60$ Hz. The other parameters of the system were $C = 3.1$ mF, $R = 15$ mΩ, $L = 2$ mH, $R_t = 2\ \Omega$, and $L_t = 0$. The system also included a fault detection logics that compared the peak values of the arm currents, i_1 and i_2, with a threshold of 1.5 kA. Thus, the fault detection mechanism blocked the gating pulses of the switches, for 100-ms, if either of the two peak values exceeded the threshold.

Initially, the gating pulses of the switches were disabled and the capacitors precharged. Then, at $t = 0.03$ s, the gating pulses were unblocked and the LMMC functioned normally until $t = 0.1$ s. From $t = 0.1$ to $t = 0.15$ s, nodes "+" and "−" were connected through a short link, to simulate a 50-ms long dc-side fault. Almost immediately after the fault inception, the fault detection mechanism of the LMMC detected the fault and blocked the gating pulses, until $t = 0.2$ s. Thereafter, the gating pulses were unblocked to allow the LMMC to revert to its normal operation. Fig. 15 shows the responses of the LMMC and a detailed model of an equivalent five-level FBSM-based MMC.

As Fig. 15 shows, from $t = 0.1$ to $t = 0.15$ s, that is, during the fault, the arm current is zero and, consequently, the arm voltage is equal to the negative of the grid voltage, in both the LMMC and FBSM-based MMC. From $t = 0.15$ s onward, that is, from the fault clearance moment onward, the arm voltages assume a positive offset equal to half of the dc-side voltage, i.e., 4 kV, until the release of the gating pulses at $t = 0.2$ s, while the arm currents remains zero. From $t = 0.2$ s onward, i.e., from the instant at which the gating signals are released, the currents and voltages revert to their predisturbance forms and magnitudes. Fig. 15 demonstrates the similarity of the responses of the LMMC and FBSM-based MMC. Fig. 15 also shows that the arm currents exhibits harmonic distortion due to circulating current components. This, in turn, is due to the fact that the simulation was run in open loop, i.e., no circulating current suppression control was employed.

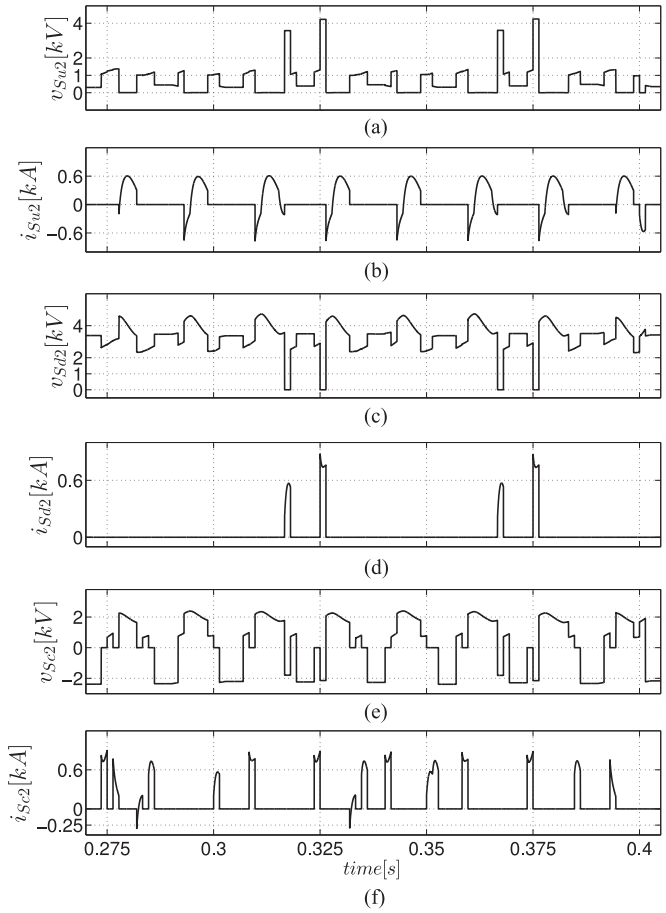

Fig. 16. Voltage and current waveforms for the switches of the second *network* of the upper arm; Case I.

Fig. 16 shows the voltage and current waveforms for the switches of the second *network* of the upper arm of the LMMC; the variables are labeled in accordance with the circuit of Fig. 13. It can be verified through the waveforms that the voltage magnitudes agree with the values predicted by the analysis of Section VII.

Fig. 17 depicts the gating pulses for the switches of the second *network* of the upper arm of the LMMC, as well as the gating pulses for switch S_3 of the first FBSM, Fig. 10(c), in the upper arm of the equivalent five-level FBSM-based MMC. The figure indicates that, as compared to the FBSM-based MMC, the switches of the LMMC are switched less frequently. This is due to the multiple possible switch state combinations in the LMMC, offered by the *high-efficiency links* and the *regular links*.

B. Case II

In this case, a detailed model of an open-loop controlled single-phase nine-level LMMC was simulated, in the same system as that of Fig. 14, assuming the same sequence of events as those in Case I, and with the same parameters as those in Case I, with the exception that $C = 6$ mF. The LMMC was also equipped with the same fault detection mechanism as that in the system of Case I. Fig. 18 depicts that responses of the LMMC and a detailed model of an equivalent HBSM-based MMC.

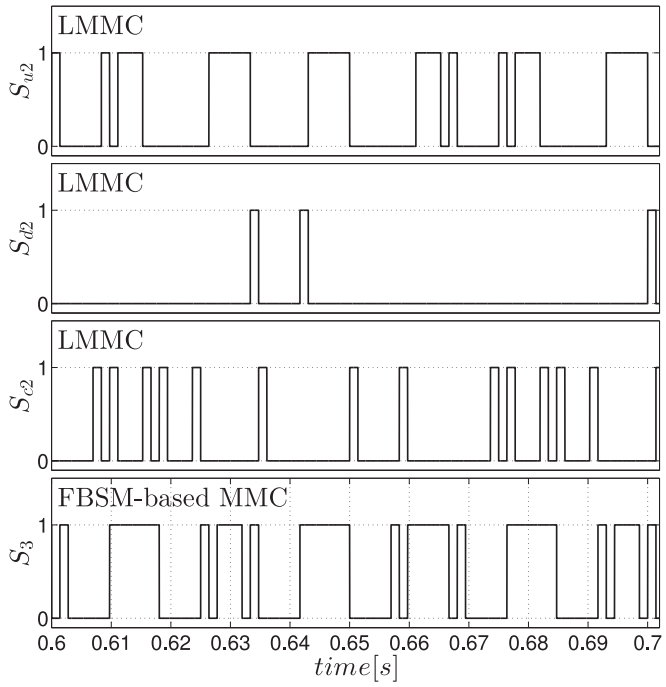

Fig. 17. Gating pulses for the switches of the second network in the upper arm of the LMMC, and for S_3 of the first submodule in the upper arm of the FBSM-based MMC; Case I.

As Fig. 18 shows, from $t = 0.1$ to $t = 0.15$ s, i.e., during the fault, in the LMMC the arm current is zero and the arm voltage is equal to the negative of the grid voltage. However, in the HBSM-based MMC, a large arm current develops, which cannot be interrupted and is only impeded by the inductance of the arm inductance. The figure also shows that the arm current is superimposed with a decaying negative dc offset. The dc offset depends on the fault inception instant, relative to the zero crossing instant of the grid voltage. In this case, the relationship happens to be such that the maximum possible negative offset develops subsequent to the fault inception. Therefore, the arm current remains negative for the entire duration of the fault, as Fig. 18 shows. Consequently, the arm voltage of the HBSM-based MMC is almost zero in this interval, due to the conduction of the antiparallel diode of the lower switches of the submodules. From the fault clearance moment, $t = 0.15$ s, the arm voltages of both the LMMC and HBSM-based MMC move up by half of the dc-side voltage, and the arm current of the HBSM-based MMC also becomes zero. After the gating pulses are released, that is, from $t = 0.2$ s onward, the two converters resume their normal operations.

C. Case III

In this case, a detailed model of a three-phase nine-level LMMC, operated as an inverter in a system such as shown in Fig. 1, was simulated under closed-loop control. The parameters were $C = 6$ mF, $R = 0.1\ \Omega$, $L = 4$ mH, $R_t = 0.8\ \Omega$, and $L_t = 10$ mH. The grid voltage had a peak value of 2 kV and its frequency was 50 Hz. The LMMC was current controlled in a dq frame synchronized to the grid voltage, [24]. The converter was also equipped with a fault detection mechanism that compared the peak value of the arm currents

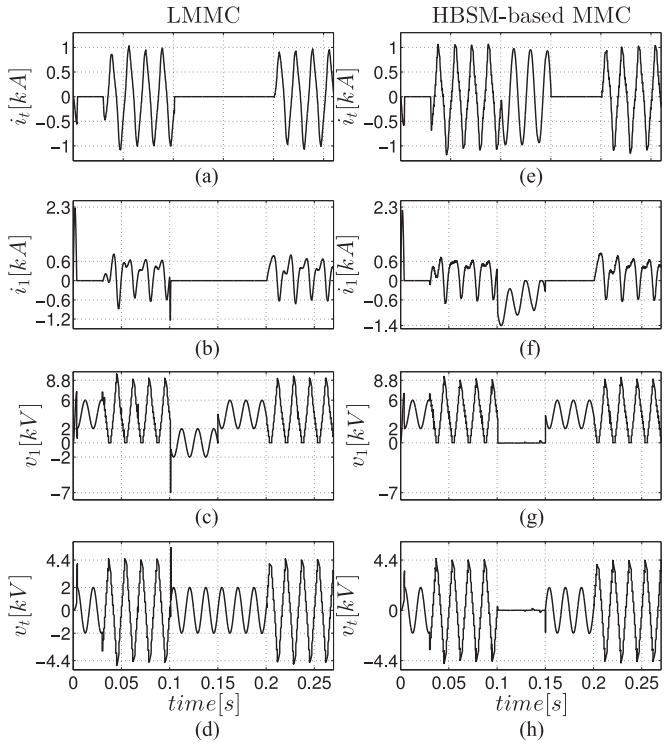

Fig. 18. Waveforms of selected variables in an open-loop controlled single-phase nine-level LMMC (left column) and an equivalent HBSM-based MMC (right column), to various disturbances; Case II.

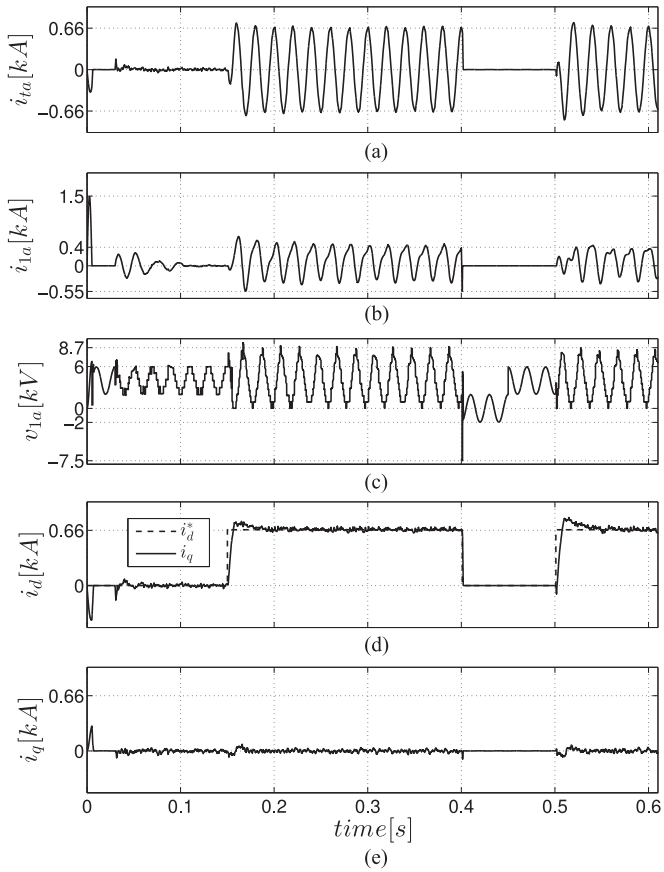

Fig. 19. Waveforms of selected variables in a closed-loop controlled three-phase nine-level LMMC, to various disturbances; Case III.

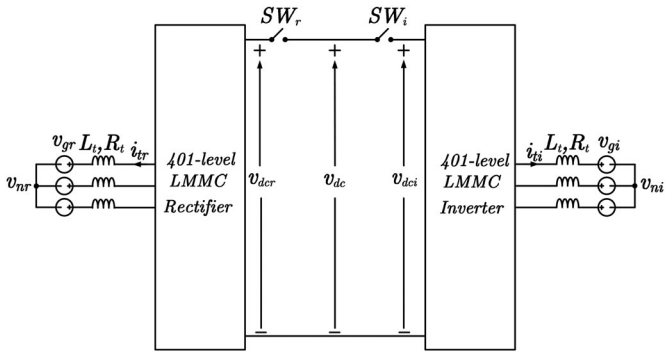

Fig. 20. Schematic diagram of the back-to-back LMMC system; Case IV.

with a threshold of 1.0 kA and disabled the current controller and the gating pulses for 100 ms, if any of the six arm current peak values exceeded the threshold. The fault detection mechanism also set the setpoint for the d-axis component of the ac-side terminal current to zero.

From the start to $t = 0.03$ s, the gating pulses and the current controller were disabled. At $t = 0.03$ s, the gating pulses were released and the current controller was activated, with the real- and reactive-power setpoints both set to zero. At $t = 0.15$ s, the real-power setpoint was stepped to 2 MW, thus raising the setpoint for the d-axis component of the ac-side terminal current to $i_d^* = 0.66$ kA. At $t = 0.4$ s, a short link was placed across the dc-side terminals of the LMMC, and was removed after 50 ms. The fault detection mechanism detected the fault, almost immediately, blocked the gating pulses, disabled the current controller, and set i_d^* to zero. At $t = 0.5$ s, the gating pulses were unblocked, the current controller was enabled, and i_d^* was reset to its predisturbance value of 0.66 kA.

Fig. 19 shows the waveforms of the ac-side terminal current, upper arm current, and upper arm voltage (all for phase-a). The figure also shows the waveforms of the d- and q-axis components of the ac-side terminal current. It is observed that, as expected, the arm current and the ac-side terminal current drop to zero once the fault is detected. It is also observed that the ac-side terminal current is noticeably distorted. The distortion, in turn, translates into considerable ripples in the d- and q-axis current components. The distortion is due to the small M for this simulation and, consequently, the low number of levels in the ac-side terminal voltage of the LMMC. The modulation strategy adopted for this paper, i.e., the NLC modulation strategy, produces quality ac-side voltage and current waveforms if M is large, as illustrated in the next case study, in Section VIII-D.

D. Case IV

In this case, a back-to-back system, similar to the system presented in [5] and [25], [26], was simulated. The system, whose simplified schematic diagram is shown in Fig. 20, was simulated by means of an *equivalent-circuit-based simulation model* [27], that is, by a model that employs dependent voltage sources to generate the arm voltages v_1 and v_2, for each LMMC. Thus, the mathematical equations that govern different variables of

the LMMCs were coded in a program and linked to the host circuit simulation software, i.e., PSCAD/EMTDC; the code, therefore, produced the control signals for the dependent voltage sources. The validity and accuracy of the equivalent-circuit-based simulation model were first confirmed by comparing its response with the response obtained from the detailed models used for simulation studies of Case I through Case III. For both LMMCs of the back-to-back system, the parameters were: $M = 400$, $C = 10$ mF, $R = 338$ mΩ, $R_t = 377$ mΩ, $L = 50$ mH, and $L_t = 60$ mH. The simulation model also included a scheme for circulating current suppression [28], and schemes for ac-side terminal current control and dc-side voltage regulation [24]. The grid voltages, v_{gi} and v_{gr} (i = inverter and r = rectifier), were balanced, 50 Hz, sinusoids with a peak value of 272 kV (corresponding to a line-to-line RMS voltage of 333 kV). Each LMMC was equipped with the same fault detection mechanism as that in the system of Case III, albeit with a threshold of 2.0 kA and a disablement period of 200 ms.

Initially, switches SW_r and SW_i were open to isolate the dc-side terminals of the two constituting LMMCs, and the gating pulses and the controllers were disabled. Thus, the capacitors of the two LMMC were precharged by the corresponding grids, to about 875 V each. At $t = 0.03$ s, the gating pulses were released and the controllers were enabled, while the reactive-power setpoints of both LMMCs were set to zero. However, the real-power setpoints were obtained from two corresponding dc-side voltage control loops, which raised the dc-side terminal voltages to 640 kV. At $t = 0.25$ s, SW_r and SW_i were closed and the real-power setpoint of the *rectifier LMMC* was switched OFF from the corresponding dc-side voltage control loop, to be regarded as the real-power setpoint for the back-to-back system. However, the real-power setpoint of the *inverter LMMC* was left in possession of the respective dc-side voltage regulation loop. Thus, the LMMC was delegated the task of dc-side voltage regulation, for the back-to-back system. At $t = 0.3$ s, the real-power setpoint was stepped down to -1000 MW, and stepped up to 1000 MW at $t = 0.55$ s. At $t = 0.85$ s, a short link was placed across the dc-side terminals of the LMMCs, and it was removed after 100 ms. Figs. 21 and 22 show the system response to the aforementioned sequence of events.

As Fig. 21 shows, the dc voltage of the system drops to zero due to the fault. The fault also results in large ac-side terminal currents in both LMMCs, until the fault is detected and the gating pulses are blocked (shortly after $t = 0.85$ s). The transient large ac-side terminal currents manifest themselves as current spikes, as Fig. 21 shows. The transient current growth is larger for the inverter LMMC, since the dc-side voltage regulation loop commands a large negative d-axis current for the inverter LMMC, in a futile attempt to maintain the dc-side voltage. Once the fault is detected, the gating pulses are blocked, the controllers are disabled, and the ac-side terminal currents drop to zero, in both MMCs (that is, i_d and i_q also become zero).

Fig. 22 shows the waveforms of the ac-side terminal currents and the line-to-line ac-side terminal voltages of the rectifier LMMC, zoomed around the moment of real-power flow reversal; the figure illustrates the smooth transition from the rectifying mode of operation to the inverting mode of operation, and vice versa, for the two LMMCs. The waveforms further demonstrate that the aforementioned waveforms are free from noticeable harmonic distortions, due to the large number of levels in the ac-side terminal voltage of the LMMCs.

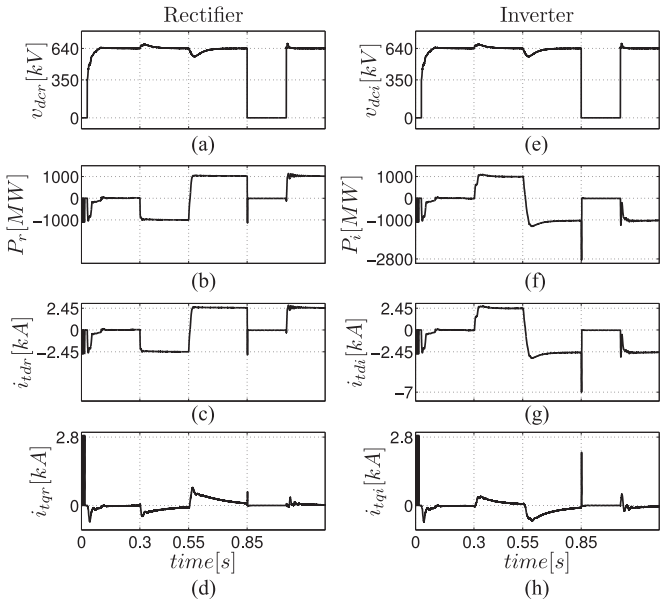

Fig. 21. Waveforms of selected variables in the rectifier LMMC (left column) and inverter MMC (right column); Case IV.

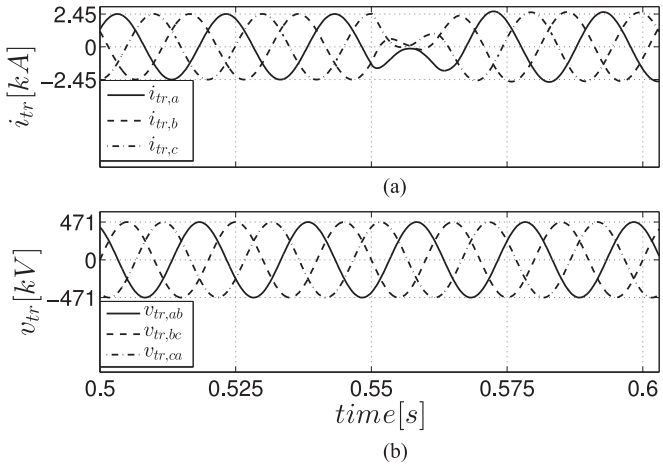

Fig. 22. Waveforms of (a) ac-side terminal current and (b) ac-side line-to-line terminal voltage, of the rectifier LMMC, zoomed around the Power-flow reversal instant; Case IV.

E. Simulated Power Losses

Cases I and II were also used to verify the predictions of Section VI of the power losses of the LMMC, with the results reported in Table IV; the power losses were computed as $P_{\text{loss}} = v_{dc}i_1 - v_t i_t$, using the simulated variables. A closer look at the results of Table IV reveals the fact that the predictions of Table II do not precisely hold. This is because the power loss expressions in Table II are derived, from those in Table I, based on the assumption of adequately large values of M. Further, the average number of series-connected switches, $\overline{N_{ss}}$, in the LMMC, exhibits deviations from the values predicted by the corresponding expression in Table I if M is small. Thus, in

TABLE IV
SIMULATED POWER LOSSES FOR CASES I AND II

Converter	Case I	Case II	Relative to LMMC
LMMC	0.0259 MW	0.026 MW	–
5-level FBSM-based MMC	0.038MW	–	1.5
9-level HBSM-based MMC	–	0.028 MW	1.08

Case I, where $M = 4$, the value of $\overline{N_{ss}}$ for the FBSM-based MMC is 1.8 times that for the LMMC, whereas, as shown in Table IV, the power loss of the FBSM-based MMC is 1.5 times that of the LMMC. However, for Case II, i.e., with $M = 8$, the ratio of the $\overline{N_{ss}}$ values is 1.08, which agrees with what Table IV reports from the simulations.

IX. CONCLUSION

In this paper, a new topology for MMC was proposed. The proposed MMC, referred in this paper to as the LMMC, offers the same fault handling capability of an equivalent FBSM-based MMC, while it features lower power losses than the HBSM-based MMC, the CDSM-based MMC, and the FBSM-based MMC. The effectiveness of the proposed MMC was demonstrated through time-domain simulation of single-phase, three-phase, and back-to-back systems, assuming various normal and faulted operating scenarios, using detailed as well as reduced models.

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