

A Dual-Mode Driver IC With Monolithic Negative Drive-Voltage Capability and Digital Current-Mode Controller for Depletion-Mode GaN HEMT

Yue Wen, *Member, IEEE*, Matthias Rose, Ryan Fernandes, Ralf Van Otten, Henk Jan Bergveld, and Olivier Trescases, *Senior Member, IEEE*

Abstract—This work presents a driver and controller integrated circuit (IC) for depletion-mode gallium nitride (GaN) high-electron-mobility transistors (HEMTs). The dual-mode driver can be configured for cascode-drive (CD) or HEMT-drive (HD) mode. In the CD mode, a cascode low-voltage DMOS is driven to achieve high-speed normally OFF operation. An active clamping circuit is proposed for the DMOS breakdown protection. In the HD mode, an HEMT gate driver with negative drive-voltage capability and programmable slope control is presented. A digital peak current-mode controller is also integrated with the dual-mode driver. The IC was implemented in a 140-nm automotive bipolar-CMOS-DMOS silicon-on-insulator process. The driver/controller IC is copackaged with an optimized 600-V GaN HEMT fabricated in a GaN-on-Si process. The solution was verified to operate at up to 1 MHz in a 35-W boost converter prototype and achieves a programmable switching-node dv/dt of up to 20 V/ns. To the best of the author's knowledge, this is the first monolithic integration of a cascode MOSFET, device driver, and digital current-mode controller that is designed specifically for high-voltage GaN devices.

Index Terms—Current-mode control, device driver, gallium nitride, high electron mobility transistor, integrated boost converter.

I. INTRODUCTION

GALLIUM nitride (GaN) power devices are leading to a technological revolution in power electronics by offering higher power density through increased switching frequency and reduced switching losses. It is projected that GaN devices will have significant growth in applications such as electric vehicles and renewable energy [1]. Depletion-mode (normally ON) GaN high-electron-mobility transistors (HEMTs) have been widely used with a series-connected low-voltage (LV) Silicon (Si) MOSFET to achieve normally OFF behavior in a cascode structure. The attractive benefits of the depletion-mode GaN HEMT are motivating numerous research

Manuscript received June 27, 2015; revised January 5, 2016; accepted February 16, 2016. Date of publication March 1, 2016; date of current version September 16, 2016. This work was supported by NXP Semiconductors, the Natural Sciences and Engineering Research Council of Canada, and the Canada Foundation for Innovation. Recommended for publication by Associate Editor K. Sheng.

Y. Wen, R. Fernandes, and O. Trescases are with the University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: wenyue@ele.utoronto.ca; ryan.fernandes@mail.utoronto.ca; ot@ece.utoronto.ca).

M. Rose, R. V. Otten, and H. J. Bergveld are with NXP Semiconductors, Eindhoven 5656 AE, The Netherlands (e-mail: matthias.rose@nxp.com; ralf.van.otten@nxp.com; henkjan.bergveld@nxp.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2016.2537002

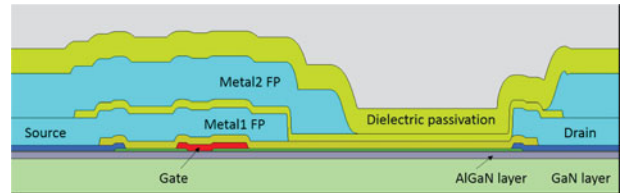


Fig. 1. Cross section of a depletion-mode GaN HEMT.

efforts in high-frequency dc–dc boost converters [2], [3], power-factor-correction boost converter [4], dc–dc buck, and *LLC* resonant converters [5]. While high-voltage (HV) enhancement-mode (normally OFF) GaN devices have been demonstrated [6], [7], depletion-mode GaN HEMTs are typically superior in intrinsic performance. Additional process steps such as the recessed-gate technique and fluorine-based plasma treatment are required to obtain enhancement-mode GaN HEMTs [8], which increase the cost of the fabrication and impact the device performance.

The depletion-mode GaN HEMT used in this work was manufactured in NXP's standard Si production fab, the cross section is shown in Fig. 1. The device has a measured leakage current of 1 $\mu\text{A}/\text{mm}$ and an $R_{\text{on}} \cdot A$ of 2.5 $\text{m}\Omega \cdot \text{cm}^2$ [9], as shown in Fig. 2(a) and (b), respectively. While the $R_{\text{on}} \cdot A$ of existing Si and silicon-carbide (SiC) power devices have almost reached their theoretical limits, the $R_{\text{on}} \cdot A$ of GaN devices can still be further improved.

The most popular driving scheme for a normally ON device is the cascode-drive (CD) structure, as shown in Fig. 3(a). An LV Si MOSFET is connected in series with the HV GaN HEMT, and the gate of the HEMT is tied to the source of the MOSFET. The LV MOSFET only adds a small R_{on} penalty due to the relatively low $R_{\text{on}} \cdot A$ product of the LV MOSFETs compared to HV devices. A conventional MOSFET driver can be used to drive the LV MOSFET at high speeds. The cascode device has a normally OFF characteristic, as shown in Fig. 4, where the drain-to-source current, I_{ds} , is plotted versus the gate-to-source voltage, V_{gs} , when $V_{\text{ds}} = 5$ V. The threshold voltage of the cascode device is essentially the threshold voltage of the LV MOSFET. The HV GaN HEMT does not have an intrinsic body diode; however, the body diode of the cascode LV MOSFET serves as the body diode for the whole cascode device. During dead-time when the body diode of the LV MOSFET conducts, the HV GaN HEMT is turned ON since its V_{gs} is now positive and equal to the voltage drop of the body diode. This

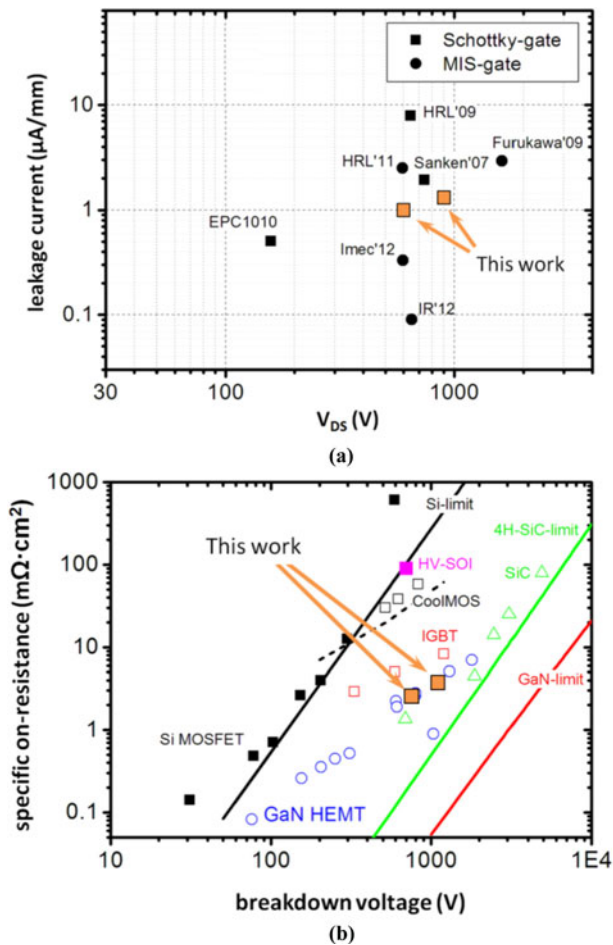


Fig. 2. Measured (a) leakage current and (b) $R_{\text{on}} \cdot A$ of the depletion-mode GaN HEMTs [9].

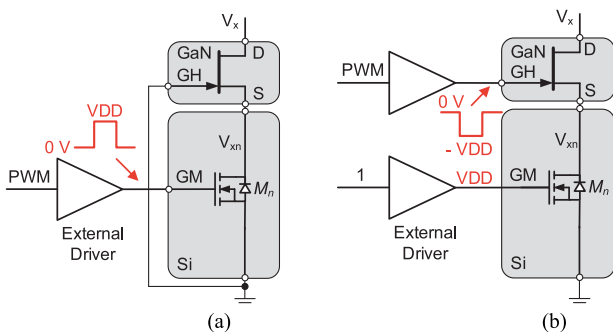


Fig. 3. Normally ON device driver. (a) CD and (b) HD schemes.

third-quadrant operation with the LV MOSFET being off has been shown in [5].

The normally ON device can also be driven directly with a negative gate voltage to turn it OFF, as shown in Fig. 3(b). This scheme is referred as HEMT drive (HD) or direct drive. A cascode MOSFET is still required since if the negative supply voltage is not available during start-up or fault conditions, the MOSFET can be turned OFF to switch OFF the HEMT. During normal operation, the MOSFET is kept on. The $I_{\text{ds}}-V_{\text{gs}}$

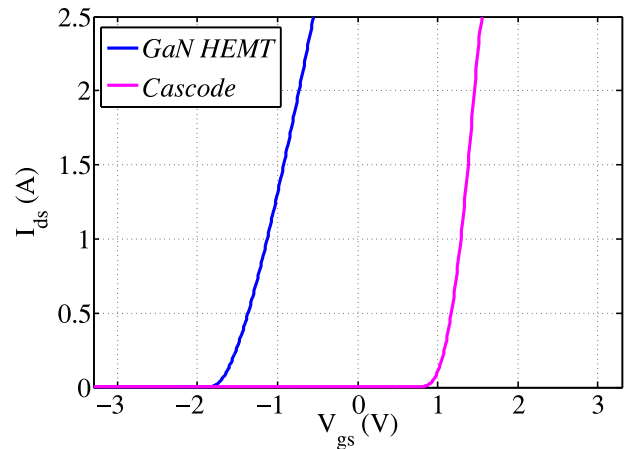


Fig. 4. GaN HEMT and cascode device I_{ds} versus V_{gs} plots ($V_{\text{ds}} = 5$ V).

relationship of the GaN HEMT device used in this work is shown in Fig. 4, where the threshold voltage of the GaN HEMT is -1.8 V.

The cascode and direct drive schemes were previously demonstrated for SiC junction field-effect transistors (JFETs), which are also normally ON devices. It was concluded that the CD scheme has larger switching losses, due to the driving of the cascode LV MOSFET [10], [11]. The CD is also an indirect driving scheme, which offers less controllability over the device switching behavior [10], [11]. The direct drive requires a negative driver supply to be present to keep the SiC JFET OFF; therefore, start-up and supply fault conditions have to be studied. In [12], the power-up protection was investigated to ensure the safety of SiC JFET-based inverters. The direct drive scheme was also implemented in an integrated circuit (IC) with an on-chip negative voltage regulator for SiC JFET, and the operations of start-up and power-down were demonstrated; a cascode PMOS is used to reduce the stray inductances of the driver loop for reduced switching losses [11]. In [13], a self-powered gate driver was proposed for a SiC JFET without the need for any dedicated driver power supply; however, it requires a number of components including two transformers, which are not suitable for IC implementation.

In this work, the focus is the implementation of a driver/controller IC for GaN HEMTs, in low-power applications (≤ 100 W), where compact and low-cost solutions are more desirable. Both the CD [2]–[5] and HD [14], [15] schemes have been previously reported for GaN HEMTs. In [2]–[5], an external driver IC is used to drive a copackaged cascode device. The driver in this work is integrated with an LV DMOS to form the cascode configuration with an HV GaN HEMT. Existing HD solutions require either a negative driver supply [14] or external bootstrap circuits [15]. The proposed HD mode driver has a fully integrated inverted bootstrap circuit to generate the negative gate voltage, digital programmable slope-control capability for fulfilling electromagnetic interference (EMI) requirements, and an integrated charge pump to handle the gate leakage of the HEMT. A digital peak current-mode controller is also integrated by using the cascode DMOS as a sensing resistor.

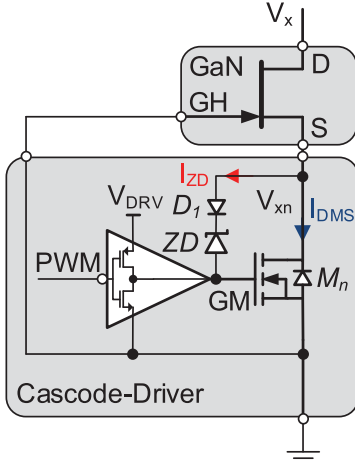


Fig. 5. Proposed CD mode architecture with active clamping to protect the LV MOSFET.

The driver/controller IC was implemented in a 140-nm bipolar-CMOS-DMOS (BCD) silicon-on-insulator (SOI) process. The BCD IC was copackaged with the GaN HEMT to form a single-package solution for a high level of integration, and was verified in a 35-W boost converter prototype.

This work is an extension of [16], with additions of implementation details, integrated current-mode operation, and entirely new experimental results. This paper is organized as follows. Section II presents the implementations of the dual-mode driver and integrated digital peak current-mode controller. The experimental results are reported in Section III.

II. DRIVER/CONTROLLER IC ARCHITECTURE

A. CD Mode With Active Clamping

The integrated cascode DMOS, M_n , is a 130-m Ω and 20-V device, driven by a high-speed CMOS driver, as shown in Fig. 5. In the CD mode, the gate of the HEMT, GH , is shorted to the source of M_n . It has been shown that the drain of M_n , V_{xn} , can reach the breakdown voltage of the LV device. This reliability concern was previously addressed by an additional off-chip capacitor in [17], which increases cost and packaging complexity.

In this work, a 10-V Zener diode, ZD , is connected from V_{xn} to the output of the driver, as shown in Fig. 5. When the driver output is low, V_{xn} is clamped by ZD . When the driver output is high, the diode D_1 blocks the path to V_{xn} , which is pulled low. This clamping circuit actively prevents the breakdown of M_n , and the operation is simulated, as shown in Fig. 6, where the CD mode architecture is used as a low-side switch in a boost converter. After the turn-off of the DMOS, M_n , I_{DMOS} goes to 0 A. ZD is ON and conducts current I_{ZD} , and V_{xn} is clamped to 10 V. When there is excessive charge on the V_{xn} node during the turn-off, M_n can be turned ON slightly by the combination of the high current in ZD and the finite pull-down resistance in the CMOS driver. This helps the clamping circuit to discharge the V_{xn} node.

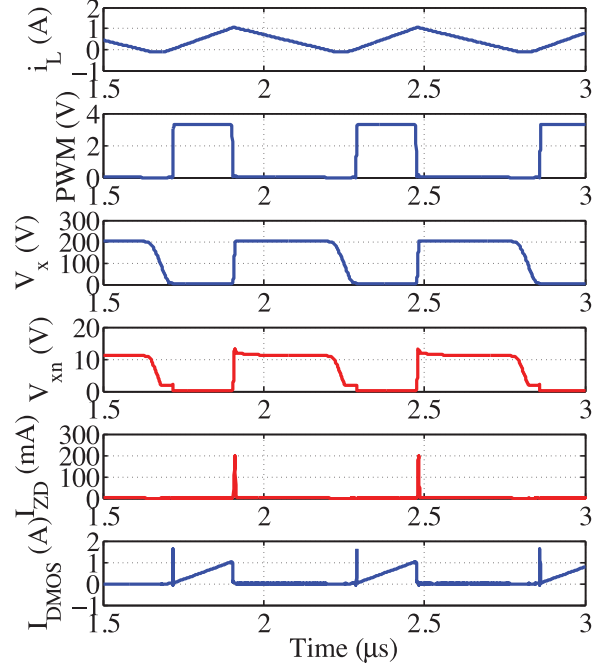


Fig. 6. Simulated CD mode operation showing V_{xn} node is actively clamped below 11 V when M_n is switched OFF.

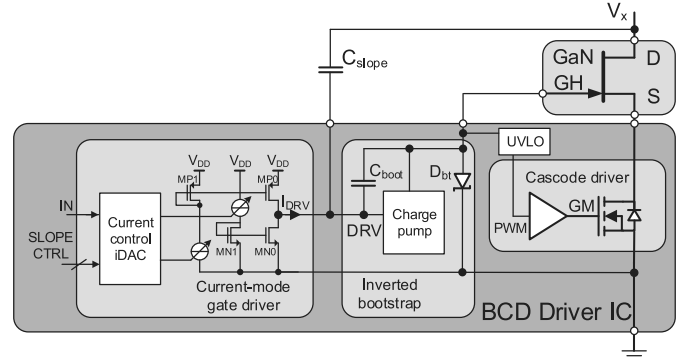


Fig. 7. Proposed HD mode architecture with inverted bootstrap circuit.

B. HD Mode With Programmable Slope Control

HD mode was also implemented to take advantage of its direct gate control of the GaN HEMT. The HD mode architecture is shown in Fig. 7, which consists of a current-mode driver and an inverted bootstrap circuit. Unlike the push-pull-type CMOS driver in the CD mode, the current-mode driver operates at a controlled current level, I_{DRV} . With a small external capacitor, C_{slope} , the current-mode driver can control the rising and falling slopes of the switching node, V_x . This slope control can be used to fulfill any specific EMI requirement [18]. A similar method was also used for SiC JFET in a cascode configuration for EMI control in [19]. With the proposed HD mode architecture, the dV_x/dt slope is given by

$$\frac{dV_x}{dt} = \frac{I_{DRV}}{C_{slope}} \quad (1)$$

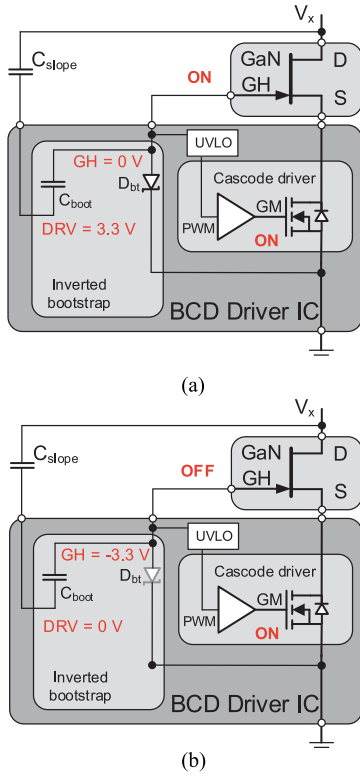


Fig. 8. Inverted bootstrap circuit operation in HEMT. (a) ON and (b) OFF states.

and I_{DRV} is programmable through a serial peripheral interface (SPI). C_{slope} is an HV capacitor and is, therefore, implemented off-chip. The value of C_{slope} should be chosen to be a few times larger than the gate-to-drain capacitance, C_{gd} , of the GaN HEMT, such that the nonlinearity of C_{gd} does not impact the overall dV_x/dt slope. I_{DRV} should be chosen to achieve the desired dV_x/dt slope, which needs to be fast enough for the target switching frequency. The value of C_{slope} used in this work is in the range of a few picofarads, and I_{DRV} can be programmed from 10 to 100 mA.

As discussed in Section I, HD mode requires a negative gate voltage to turn OFF the HEMT. This is accomplished by using a fully integrated inverted bootstrap scheme without the need of a negative driver supply, as shown in Fig. 8. A discrete version of the inverted bootstrap technique was previously demonstrated in [15], with external components and without slope control capability. The operation of the proposed bootstrap circuit is described as follows:

- 1) *HEMT on-state*: When the output of the current-mode driver, DRV, is driven to 3.3 V, the bootstrap diode, D_{bt} , conducts and the gate of the HEMT, GH, is 0 V, which turns the HEMT ON.
- 2) *HEMT off-state*: When DRV is driven to 0 V, D_{bt} turns OFF. GH becomes -3.3 V, which is maintained by the bootstrap capacitor, C_{boot} , and the HEMT, which has a threshold voltage of -1.8 V, is turned OFF.

The simulation results in the HD mode with I_{DRV} of 25 and 100 mA, and C_{slope} of 1 pF are shown in Fig. 9. The negative

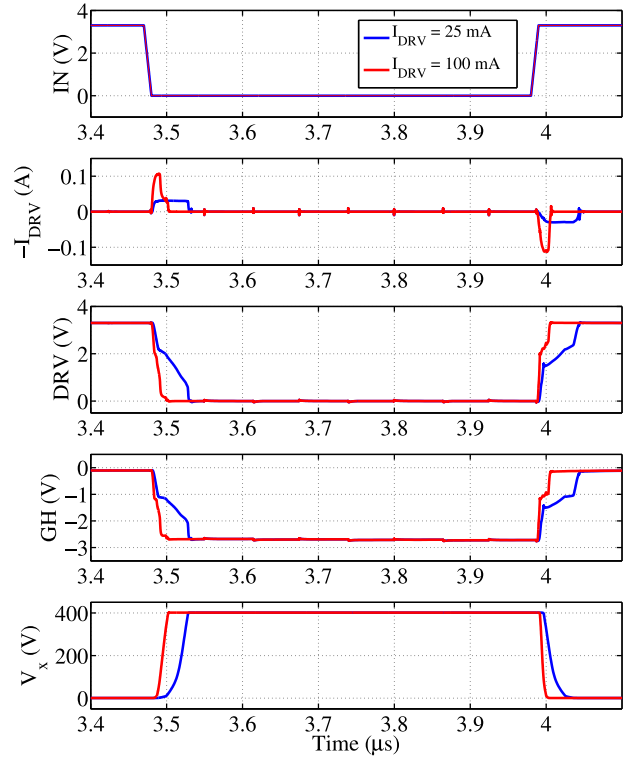


Fig. 9. Simulated HD mode operation showing the negative gate switching achieved by the inverted bootstrap circuit.

gate switching is achieved at the gate of the HEMT, GH, and the slope of switching node, V_x , is controlled. The bootstrap capacitor, $C_{boot} = 2$ nF, is fully integrated. This is only possible due to the low gate charge of the GaN HEMT. The bootstrap diode, D_{bt} , is implemented with an active transistor for the LV of 3.3-V operation. In the HD mode, M_n is always ON. For added reliability, M_n can be turned OFF by an under-voltage-lock-out (UVLO) block if C_{boot} gets discharged in fault conditions. During start-up, M_n is kept OFF until the driver supply of 3.3 V has been reached, to ensure normally OFF operation. The proposed current-mode driver and inverted bootstrap circuit can then be enabled for operation. Since the driver supply was not integrated and an external power supply was used, the start-up function was performed manually during the experiments.

The GaN HEMT has a Schottky gate structure with a leakage current in the range of tens of microamperes. Although the leakage current has been reduced by device improvements, it remains a challenge for gate driver designs. In this work, a high-frequency charge-pump circuit is used to replenish C_{boot} , as shown in Fig. 7. The charge pump operates in two phases when the HEMT is OFF, at a programmable high frequency of 8 and 16 MHz, as shown in Fig. 10(a). The addition of the charge pump circuit guarantees the turn-off of the HEMT under static conditions. The transistor-level implementation of the inverted bootstrap circuit and the charge pump is shown in Fig. 10(b). The integrated charge pump capacitor, C_{charge} , is 100 pF, which is minimized by the high-frequency operation.

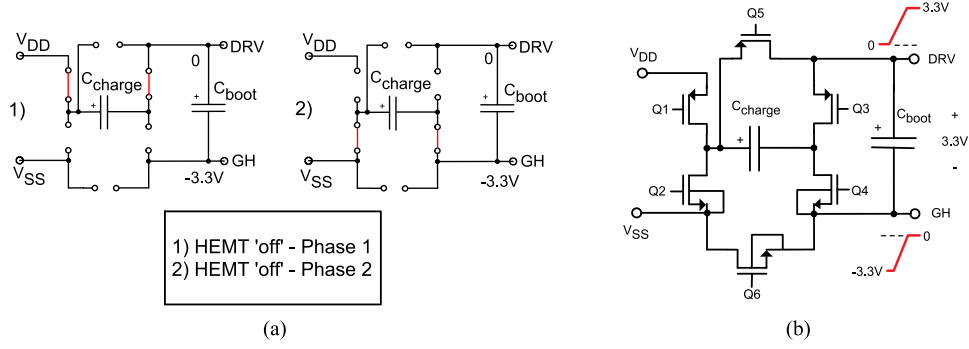


Fig. 10. (a) Charge pump operation in the HD mode. (b) Transistor-level implementation of the inverted bootstrap circuit with charge pump.

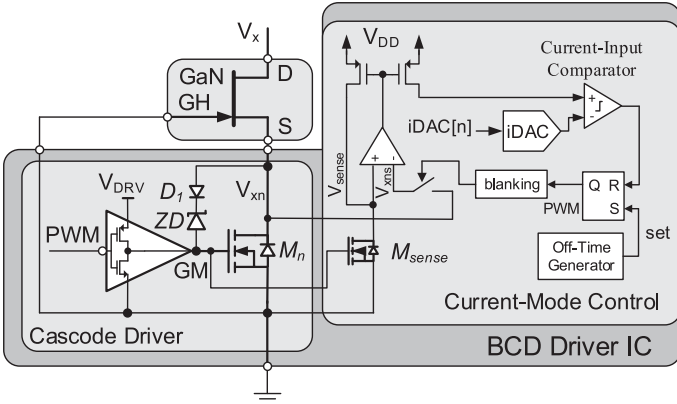


Fig. 11. Architecture of the digital peak current-mode controller.

C. Integrated Current-Mode Controller With Off-Time Generator

Integrating the driver and controller on the same IC can achieve a more compact solution. Although GaN-based pulse width modulation (PWM) circuits have been demonstrated in [20], Si-based controller ICs can deliver more advanced control features and are much more cost effective. The proposed current-mode controller is shown in Fig. 11. The peak of the inductor current, $i_L(t)$, can be digitally controlled using a combination of the on-chip 10-bit digital-to-analog converter (DAC) and the high-bandwidth closed-loop senseFET-based (M_{sense}) current sensor. A high-speed amplifier is used to equalize the drain voltage of M_{sense} , V_{sense} , with the sampled drain voltage V_{xns} . The sensed current in M_{sense} is mirrored into a current-mode comparator. The reference for the comparator is set by a flash-based current-mirror DAC, whose input is derived from the SPI. The current-sensor output was designed to track $i_L(t)$ within 40 ns of the turn-on transient. The use of the cascode structure is inherently useful for current-mode operation, as the LV cascode device shields the sensor from the HV switching node.

The conventional fixed-frequency peak current-mode controller requires slope compensation in continuous-conduction mode (CCM), when the duty ratio D is greater than 0.5 [21]. Slope compensation can limit the control bandwidth and needs

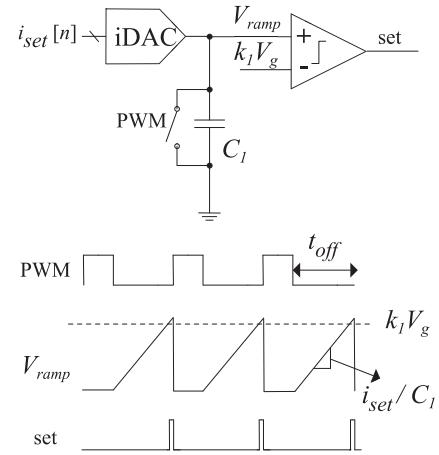


Fig. 12. Architecture and operation of the OTG.

to be adaptive for converters with a wide operating voltage range [22]. An adaptive off-time control method can be used to achieve fixed switching frequency without slope compensation [23]. The off-time generator (OTG) in this work consists of a programmable current-DAC, a capacitor, C_1 , and a comparator, as shown in Fig. 12. C_1 is reset to 0 V during on-time. The off-time t_{off} is determined by the OTG and is given by

$$t_{off} = \frac{k_1 V_g C_1}{i_{set}} \quad (2)$$

where $k_1 V_g$ is the scaled converter input voltage and i_{set} can be programmed to achieve the targeted t_{off} . Since

$$D = \frac{t_{on}}{t_{on} + t_{off}} \quad (3)$$

and

$$f_s = \frac{1}{T_s} = \frac{1}{t_{on} + t_{off}} = \frac{D}{t_{on}} = \frac{1-D}{t_{off}} \quad (4)$$

by setting a proper t_{off} , the desired switching frequency f_s can be achieved for a given converter topology. By programming t_{off} digitally, variable-frequency operation can be achieved for efficiency optimization, as demonstrated by [24] for a flyback converter at light loads.

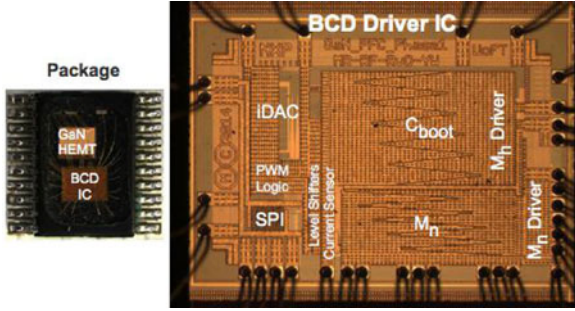


Fig. 13. Packaged GaN HEMT with driver/controller IC and its micrograph.

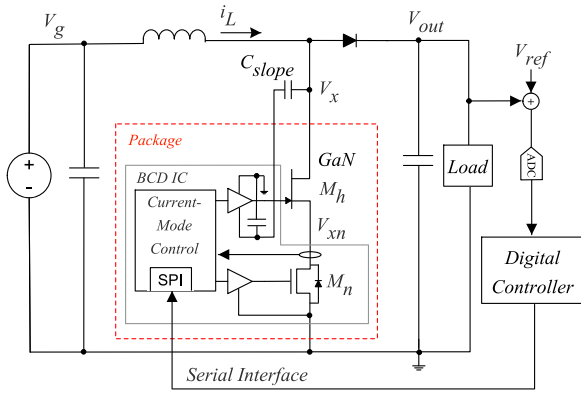


Fig. 14. Experimental boost converter that utilizes the copackaged solution.

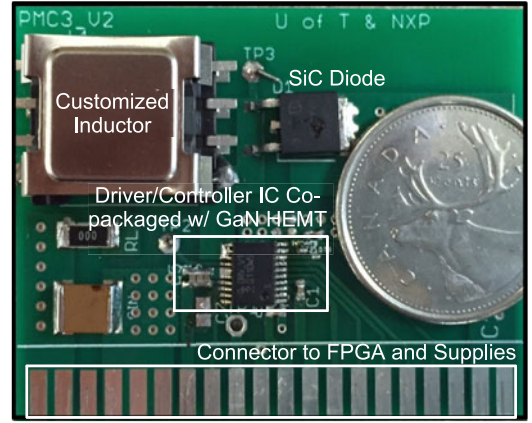
TABLE I
PROTOTYPE SPECIFICATIONS

Specifications	Value	Unit
Input Voltage, V_g	50–150	V
Output Voltage, V_{out}	200	V
Sw. Freq., f_s	up to 1	MHz
Rated Power, P_{rated}	35	W
Inductor, L	200	μ H

III. EXPERIMENTAL RESULTS

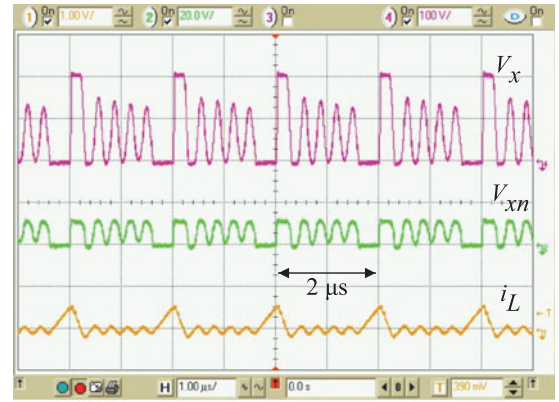
The driver/controller IC was implemented in a 140-nm automotive BCD SOI process. The BCD IC was copackaged with a 570-m Ω depletion-mode GaN HEMT to minimize the interconnect parasitics. The package and the IC layout are shown in Fig. 13. The BCD die measures 1.4×2 mm², and the GaN HEMT die measures 1.4×1.6 mm².

The driver/controller IC requires a 3.3-V supply for the analog and driver circuits and a 1.8-V supply for the digital circuits. To improve the noise immunity of the low driver supply in an HV application, multiple bonding wires are used for the driver supply and ground connections to reduce parasitic resistance and inductance. The copackaged solution was tested in a boost converter, as shown in Fig. 14, with specifications listed in Table I. The boost converter prototype PCB is shown in Fig. 15, with a customized inductor and a SiC diode. An external analog-to-digital converter (ADC) and a digital voltage-loop

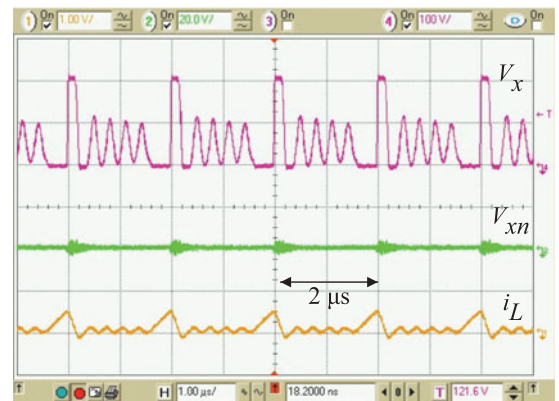


Prototype PCB

Fig. 15. Experimental boost converter prototype PCB.



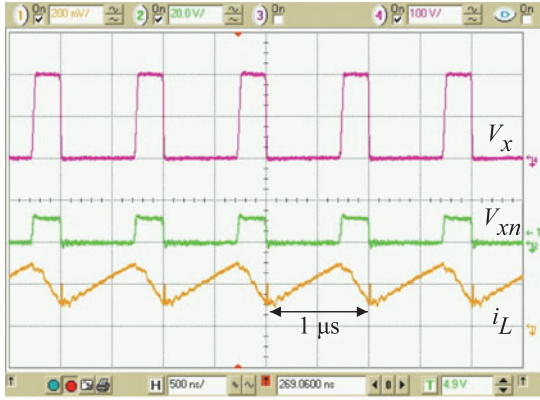
(a)



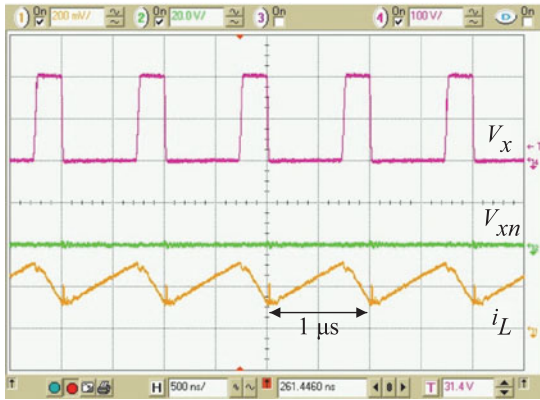
(b)

Fig. 16. Measured switching waveforms at 500 kHz in DCM in (a) CD and (b) HD modes (CH1: 1 A/div, $V_g = 50$ V, $V_{out} = 200$ V).

controller are required for full closed-loop regulation. Since the driver/controller IC was implemented in a deep submicrometer process, the complete control loop can easily be integrated in the future. The copackaged solution can be used as a driver/controller IC with an integrated LS HV switch for boost and flyback converters.



(a)



(b)

Fig. 17. Measured switching waveforms at 1 MHz in CCM in (a) CD and (b) HD modes (CH1: 0.2 A/div, $V_g = 50$ V, $V_{out} = 200$ V).

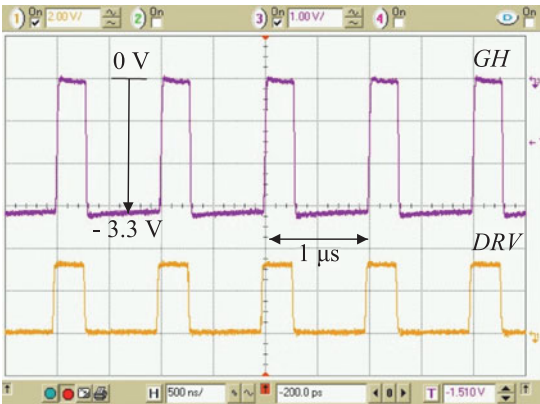


Fig. 18. Measured HD mode switching waveforms demonstrating the 0 to -3.3 V gate swing.

The switching waveforms for CD and HD modes in discontinuous conduction mode (DCM) at 500 kHz are shown in Fig. 16(a) and (b), respectively. The switching waveforms for CD and HD modes in CCM at 1 MHz are shown in Fig. 17(a) and (b), respectively. In the CD mode, the drain of M_n , V_{xn} , is clamped to 11 V when M_n is turned OFF, as designed. In the HD mode, M_n remains ON and V_{xn} remains zero. The GaN HEMT is actively switched by the inverted bootstrap circuit in

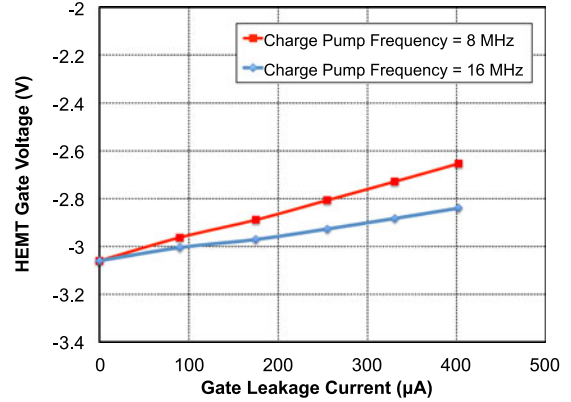
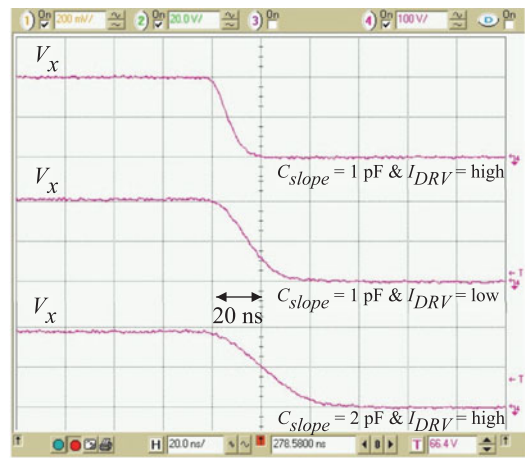
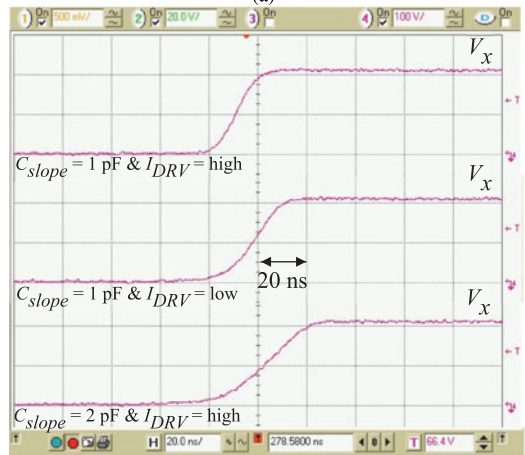


Fig. 19. Measured bootstrap capacitor voltage at different leakage current with charge pump operating at 8 and 16 MHz.



(a)



(b)

Fig. 20. (a) Falling and (b) rising slope control of the switching node, V_x , in the HD mode.

the HEMT driver. The 0 to -3.3 V swing of the GaN HEMT gate, GH, is shown in Fig. 18.

The measured bootstrap capacitor voltage when the HEMT is OFF is shown in Fig. 19. The charge pump was loaded externally to emulate different leakage currents in the HEMT. As expected, the amplitude of the bootstrap capacitor voltage decreases as

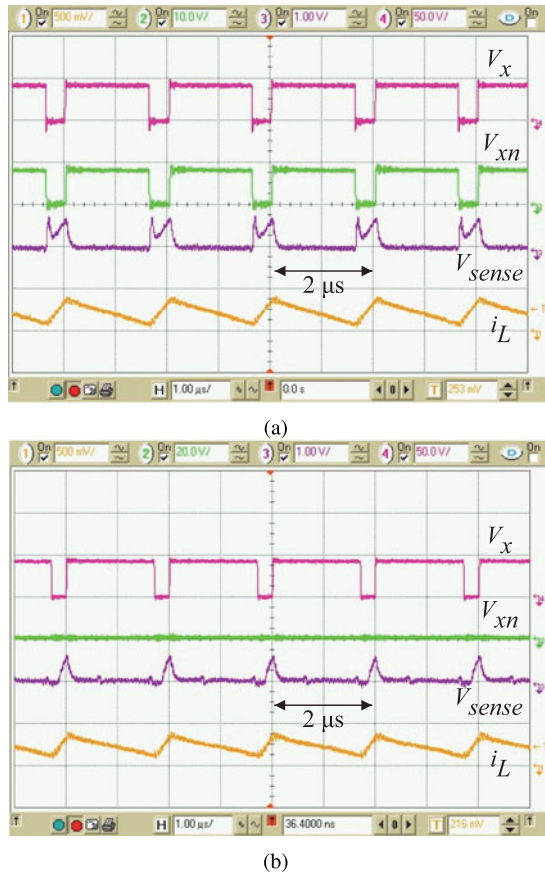


Fig. 21. Measured current sensor output, V_{sense} , in (a) CD and (b) HD modes.

the HEMT gate leakage current increases. By operating the charge pump at higher switching frequency, a higher amplitude of the gating voltage can be achieved. The programmable slope control capability in the HD mode is also demonstrated in Fig. 20(a) and (b), for the falling and rising slopes of V_x node, respectively. With $C_{slope} = 1$ pF, variable slopes from 7 to 20 V/ns can be achieved with different settings of I_{DRV} , which is configurable through SPI. The slope control range can be further extended by changing the value of C_{slope} .

The boost converter prototype was also tested in closed current-loop operation. The current sensor output waveforms are shown in Fig. 21(a) and (b), for CD and HD modes, respectively. The current sensor output, V_{sense} , tracks the rising slope of i_L , as designed. In the CD mode, since M_n is switched, the current sensor tracks the current pulse that charges the drain-to-source capacitance of M_n , as shown in Fig. 21(a). That pulse is ignored by the blanking circuit, and the blanking time limits the minimum duty cycle. In the HD mode, M_n is always ON; no pulsed sensing current is observed; therefore, a smaller blanking time is used.

As discussed in Section II, fixed-frequency peak current-mode control suffers from current oscillation when $D > 0.5$ without slope compensation. This was also experimentally verified, as shown in Fig. 22(a). The switching cycle is initiated by a 500-kHz clock. In Fig. 22(b), the OTG is used instead

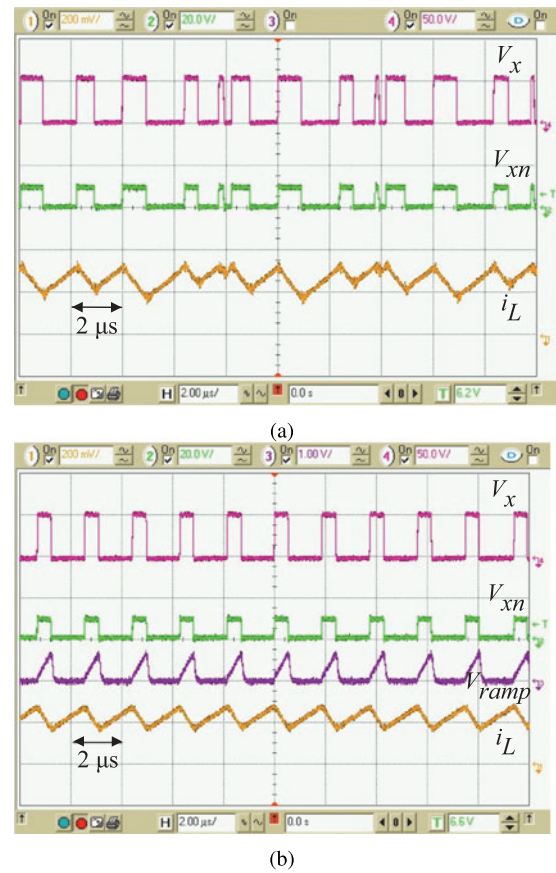


Fig. 22. (a) Measured closed current-loop operation when $D > 0.5$ showing unstable current oscillation without slope compensation. (b) Current oscillation is avoided using the OTG.

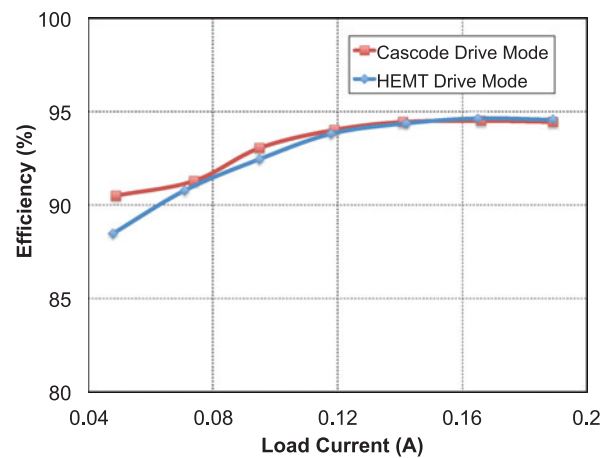


Fig. 23. Measured boost converter efficiencies in both driving modes ($V_g = 150$ V, $V_{out} = 200$ V, and $f_s = 1$ MHz).

and the current oscillation is eliminated. The V_{ramp} signal in the OTG is reset to 0 V during on-time. The switching frequency is controlled to be approximately 500 kHz.

The efficiency of the boost converter was measured in the CD and HD modes, as shown in Fig. 23. Peak efficiency of 94.5% is achieved with switching frequency of 1 MHz. Since

TABLE II
COMPARISON OF CD AND HD SCHEMES

	CD	HD
Direct Gate Control	×	✓
Cascode MOSFET Required	✓	✓
Driver Requirement	Conventional MOSFET driver	Negative gate swing and ability to supply leakage current
Suitable Application	Soft-switching	Hard-switching

the CD has the fastest switching speed which reduces switching losses, its light-load efficiency is slightly higher. At heavy load, conduction losses dominate; therefore, CD and HD modes have similar efficiencies. The measured driver current are 2.1 and 2.6 mA in CD and HD modes, respectively. The higher driver current in HD mode is mainly due to the current consumptions in slope control and charge-pump circuits. Since the driver supply is only 3.3 V, the driver power is insignificant compared to other losses.

The CD and HD schemes are compared in Table II. The cascode MOSFET with inherent body diode not only provides driving and safety functions in CD and HD schemes, but also eliminates the need to have a dedicated body diode in the GaN HEMT. The CD scheme is based on indirect gate control, and a conventional MOSFET driver can be used. The CD scheme is more suitable for soft-switching applications in which the cascode MOSFET can be switched at high speed. In contrast, the HD scheme is based on direct gate control and requires the HEMT driver to provide negative gate swing and ability to supply leakage current. The HD scheme is more suitable for hard-switching applications where programmable drive strength is required to fulfill EMI requirements.

IV. CONCLUSION

The dual-mode driver IC presented in this work offers the flexibility needed for a wide variety of high-frequency hard- and soft-switching power converter applications. The HD mode is particularly important in hard-switching applications where digitally programmable slope control is important for EMI considerations. The monolithic HEMT driver with negative gate swing was successfully demonstrated. The charge pump can replenish the bootstrap capacitor to prevent undesired discharging caused by the leakage of the HEMT Schottky gate. The integrated driver and controller allow fast switching, in excess of 20 V/ns, for up to 1MHz operation. The cascode DMOS allows for accurate digital peak current-mode control using the senseFET approach. Advanced digital control schemes can be easily implemented in the same process technology in the future. To the best of the author's knowledge, this is the first monolithic integration of a cascode MOSFET, device driver, and digital current-mode controller that is designed specifically for HV GaN devices. Future work includes the integration of the voltage-loop controller and ADC and full closed-loop demonstration.

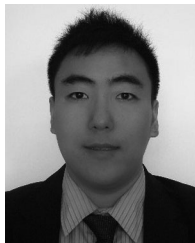
ACKNOWLEDGMENT

The authors would like to acknowledge F. Schoofs at NXP Semiconductors for the stimulating discussions.

REFERENCES

- [1] A. Bindra, "Wide-bandgap-based power devices: Reshaping the power electronics landscape," *IEEE Power Electron. Mag.*, vol. 2, no. 1, pp. 42–47, Mar. 2015.
- [2] Y. Wu, M. Jacob-Mitos, M. Moore, and S. Heikman, "A 97.8% efficient GaN HEMT boost converter with 300-W output power at 1 MHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 824–826, Aug. 2008.
- [3] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "A 120-W boost converter operation using a high-voltage GaN-HEMT," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 8–10, Jan. 2008.
- [4] Z. Liu, X. Huang, M. Mu, Y. Yang, F. Lee, and Q. Li, "Design and evaluation of GaN-based dual-phase interleaved MHz critical mode PFC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2014, pp. 611–616.
- [5] X. Huang, Z. Liu, Q. Li, and F. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014.
- [6] L.-Y. Su, F. Lee, and J. J. Huang, "Enhancement-Mode GaN-based high-electron mobility transistors on the Si substrate with a P-type GaN cap layer," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 460–465, Feb. 2014.
- [7] J. Das, J. Everts, J. Van den Keybus, M. Van Hove, D. Visalli, P. Srivastava, D. Marcon, K. Cheng, M. Leys, S. Decoutere, J. Driesen, and G. Borghs, "A 96% efficient high-frequency DC-DC converter using E-mode GaN DHFETs on Si," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1370–1372, Oct. 2011.
- [8] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.
- [9] J. Donkers, S. Heil, G. Hurkx, H. Broekman, R. Delhougne, J. Croon, D. Gravesteijn, and J. Šonský, "600V-900V GaN-on-Si process technology for Schottky barrier diodes and power switches fabricated in a standard Si-production fab," in *Proc. Int. Conf. Compound Semicond. Manuf. Technol.*, May. 2013, pp. 259–262.
- [10] R. Siemienieć and U. Kirchner, "The 1200V direct-driven SiC JFET power switch," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.
- [11] K. Norling, C. Lindholm, and D. Draxelmayr, "An optimized driver for SiC JFET-based switches enabling converter operation with more than 99% efficiency," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3095–3104, Dec. 2012.
- [12] D. Risaletto, D. Bergogne, F. Dubois, H. Morel, B. Allard, and R. Meuret, "A 200 °C safety system at power-up of normally on SiC JFETs inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2338–2344, May 2014.
- [13] D. Pefitsis, J. Rabkowski, and H.-P. Nee, "Self-powered gate driver for normally ON silicon carbide junction field-effect transistors without external power supply," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1488–1501, Mar. 2013.
- [14] B. Wang, M. Riva, J. Bakos, and A. Monti, "Integrated circuit implementation for a GaN HFET driver circuit," *IEEE Trans. Ind. Appl.*, vol. 46, no. 5, pp. 2056–2067, Sep. 2010.
- [15] T. Ishibashi, M. Okamoto, E. Hiraki, T. Tanaka, T. Hashizume, D. Kikuta, and T. Kachi, "Experimental validation of normally-on GaN HEMT and its gate drive circuit," *IEEE Trans. Ind. Appl.*, vol. 51, no. 3, pp. 2415–2422, May 2015.
- [16] M. Rose, Y. Wen, R. Fernandes, R. Van Otten, H. Bergveld, and O. Trescases, "A GaN HEMT driver IC with programmable slew rate and monolithic negative gate-drive supply and digital current-mode control," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices ICs*, May. 2015, pp. 361–364.
- [17] X. Huang, W. Du, F. Lee, Q. Li, and Z. Liu, "Avoiding Si MOSFET Avalanche and achieving zero-voltage-switching for cascode GaN devices," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 593–600, Jan. 2016.
- [18] B. Wittig and F. Fuchs, "Analysis and comparison of Turn-off active gate control methods for low-voltage power MOSFETs with high current ratings," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1632–1640, Mar. 2012.

- [19] D. Aggeler, F. Canales, J. Biela, and J. Kolar, "Dv/Dt-control methods for the SiC JFET/Si MOSFET Cascade," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4074–4082, Aug. 2013.
- [20] H. Wang, A. Kwan, Q. Jiang, and K. Chen, "A GaN pulse width modulation integrated circuit for GaN power converters," *IEEE Trans. Electron Devices*, vol. 62, no. 4, pp. 1143–1149, Apr. 2015.
- [21] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.
- [22] Y. Wen and O. Trescases, "Analysis and comparison of frequency stabilization loops in self-oscillating current mode DC-DC converters," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4753–4766, Oct. 2013.
- [23] L. Cheng, J. Ni, Y. Qian, M. Zhou, W.-H. Ki, B. Y. Liu, G. Li, and Z. Hong, "On-chip compensated wide output range boost converter with fixed-frequency adaptive off-time control for LED driver applications," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2096–2107, Apr. 2015.
- [24] Y. Panov and M. Jovanovic, "Adaptive off-time control for variable-frequency, soft-switched flyback converter at light loads," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 596–603, Jul. 2002.



Yue Wen received the B.A.Sc., M.A.Sc., and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2009, 2011, and 2015, respectively.

From 2007 to 2014, he was an Intern with Advanced Micro Devices, NXP Semiconductors, Apple, Inc., and Qualcomm, Inc. He has experience in the design of voltage regulator modules, integrated switched-capacitor power converters, integrated switched-mode power supplies, and linear voltage regulators. He is currently at Apple, Inc., Cupertino, CA, USA, as an Analog Circuit Designer. His research interests include high-frequency/high-efficiency power management ICs and mixed-signal control techniques.

Dr. Wen received the Ontario Graduate Scholarship from 2011 to 2015.



Matthias Rose was born in Dresden, Germany, in 1981. He received the M.Sc. degree (*cum laude*) and the Ph.D. degree (*cum laude*) in electrical engineering in 2011 from the Dresden University of Technology, Dresden.

He has expertise in the design of gate drivers, inductive and switched-capacitor power converters, as well as linear voltage regulators. He is currently a Research Principal in the Technology and Operations Department at NXP Semiconductors, Eindhoven, The Netherlands. His main research interests include integrated circuit design for high-voltage power converters and low-voltage power management systems, especially for applications that require new developments in silicon BCD and widebandgap technologies.

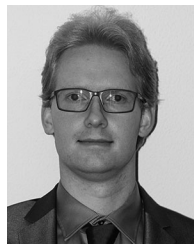
Dr. Rose received the Ontario Graduate Scholarship from 2011 to 2015.



Ryan Fernandes received the B.A.Sc. degree in electrical engineering and the M.A.Sc. degree, both from the University of Toronto, Toronto, ON, Canada, in 2012 and 2015, respectively.

From 2010 to 2011, he was an Intern with Advanced Micro Devices, Markham, ON, where he was involved in printed circuit board design and testing and debugging for graphics cards. From 2013 to 2014, he was a Researcher with NXP Semiconductors, Eindhoven, The Netherlands, where he was involved in the research of a high-frequency PFC

boost rectifier using a GaN HEMT. His current research interests include non-linear digitally controlled switch mode converters and mixed-signal integrated circuits for power converters.



R. van Otten was born in Eersel, the Netherlands, in 1984. He received the B.Eng. degree in electrical engineering from the Fontys University of Applied Sciences, Eindhoven, the Netherlands, in 2005, and the M.Sc. degree in electrical engineering from the Eindhoven University of Technology, Eindhoven, in 2009.

He joined TMC, Eindhoven, in 2009. During with TMC, he was hired by NXP Semiconductors, Eindhoven, on the topic of power converters for photovoltaic systems. He joined NXP Semiconductors in 2012 as a Research Scientist working on integrated drivers for GaN HEMT and later on integrated circuits for automotive magnetic sensors. He is currently an Analog Mixed Signal Designer in the Automotive Sensors Department of NXP Semiconductors.



H. J. Bergveld was born in Enschede, the Netherlands, in 1970. He received the M.Sc. degree (*cum laude*) and the Ph.D. degree (*cum laude*) in electrical engineering from the University of Twente, Enschede, in 1994 and 2001, respectively.

He joined Philips Research Laboratories, Eindhoven, the Netherlands, in 1994. His research interest was modeling of rechargeable batteries to design better battery management systems. This work resulted in his Ph.D. degree and the book *Battery Management Systems: Design by Modeling* (Boston, MA, USA: Kluwer, 2002).

He is currently a Power Management Architect in the Technology and Operations Department at NXP Semiconductors, Eindhoven, as well as a Part time Professor of embedded control in energy management at the Eindhoven University of Technology, Eindhoven. His main research interests include electronics for PV systems, (fully integrated) dc/dc converters, and battery management systems.

Dr. Bergveld served on the technical program committee of the IEEE VLSI Symposium on VLSI Circuits from 2012 to 2015.



Olivier Trescases received the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, in 2007.

From 2007 to 2008, he was a Concept Engineer and Mixed-Signal IC Designer with Infineon Technologies in Austria, focusing on safety-critical automotive applications. He is currently an Associate Professor in the E. S. Rogers, Sr., Department of Electrical and Computer Engineering at the University of Toronto. His group conducts research on advanced power electronic converters. Since 2015, he has been an Associate Editor of the IEEE TRANSACTIONS ON

POWER ELECTRONICS. While on sabbatical in 2016, he was with the Texas Instruments Kilby Labs in Santa Clara, CA, USA. Since 2016, he has been the Vice Chair of the IEEE Toronto Section and has served on various IEEE conferences technical committees, including the Applied Power Electronics Conference, the Custom Integrated Circuits Conference, and the International Symposium on Power Semiconductors and ICs.