A 300-V Ultra-Low-Specific On-Resistance High-Side p-LDMOS With Auto-Biased n-LDMOS for SPIC

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***Abstract*—In this paper, a high-side p-channel LDMOS (p-LDMOS) with an auto-biased n-channel LDMOS (n-LDMOS) based on Triple-RESURF technology is proposed. The p-LDMOS utilizes both carriers to conduct the on-state current; therefore, the specific on-resistance ($R_{\rm on,sp}$) can be much reduced because of much higher electron mobility. The simulation result shows that the proposed 300-V p-LDMOS obtains a $R_{\rm on,sp}$ of 16.97 mΩ/cm^2, which is about 65% reduced compared with the Triple-RESURF *silicon limit* and is comparable to an optimized n-LDMOS (BV = 340 V, $R_{\rm on,sp} = 18$ mΩ/cm^2). In addition, due to larger current capability, the active area of the proposed p-LDMOS is only about one third of an optimized Triple-RESURF p-LDMOS. The turn-on (t_r) and turn-off time (t_f) are reduced by 51.2% and 40.0%, compared to the optimized Triple-RESURF p-LDMOS, respectively.**

***Index Terms*—High-voltage p-LDMOS, specific on-resistance, transmission gate.**

I. Introduction

LATERAL diffused metal oxide semiconductor (LDMOS) is suitable for smart power integrated circuit (SPIC) [1]–[8]. Normally, in comparison with the n-LDMOS, p-LDMOS is used less frequently in high-voltage applications due to much larger specific on-resistance ($R_{\rm on,sp}$). However, in a full-complementary IC consisting of p-LDMOS and n-LDMOS, the driving circuit can be simplified [6], [9]–[14]. And a high-side p-LDMOS transistor is used with an n-LDMOS transistor for a symmetrical bipolar output waveform, which affects the harmonic performance in transmitter ICs in medical ultrasound imaging applications [5], [6]. To have the same current capability, p-LDMOS usually takes up an active area of about three times that of an n-LDMOS, which not only increases the cost but also degrades the impedance matching [6]. The key issue when designing a high-voltage LDMOS is the trade-off between $R_{\rm on,sp}$ and breakdown voltage (BV). Many technologies have been proposed to improve this trade-off of p-LDMOS [3], [6], [8], [15], [16], but the $R_{\rm on,sp}$ is still much larger than that of an n-LDMOS. In [17], a new type of high-voltage LDMOS with two kinds of carriers for conduction is proposed, and the control problem for the gate in the tub region is solved in [18]. But the solution in [18] is quite complex. It includes an amplifier, a comparator, a buffer, and even a voltage regulator to generate the control signal in the low-voltage circuit. Moreover, the trigger signal is detected at the rated current. When the load current decreases, the value of the trigger signal decreases and may become too small to be detected, or even be merged by the noise in the high-voltage system. Thus, the control circuit may not work functionally.

In this paper, a novel and simple method to overcome the earlier problems based on Triple-RESURF technology [19] is proposed.

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II. Proposed p-LDMOS and Its Performance

A. Device Structure and Mechanism

Fig. 1(a) shows a block diagram of the proposed device. There are three main parts in the device, including a modified high-voltage transmission gate, an integrated inverter, and a low-voltage power supply.

Fig. 1(b) shows the equivalent circuit of Fig. 1(a), where a resistive load $R_{\rm load}$ is connected to electrode D of the device for the transient simulation, which will be discussed in Section II-F and Section II-G. Apart from $R_{\rm load}$, there are three parts shown in Fig. 1(b) and are as follows:

Part 1: The high-voltage transmission gate consists of an intrinsic PMOS1 (M_{P1}) of a p-LDMOS and an intrinsic NMOS1 (M_{N1}) of an n-LDMOS which are in parallel connection. Each of M_{P1} and M_{N1} is in series connection with its own drift region (L_d) resistance R_P and R_N, as shown in Fig. 1(b). After both the M_{P1} and M_{N1} are turned on, the drift region resistance is reduced from R_P to $R_P R_N/(R_P + R_N)$. Thus, the specific on-resistance ($R_{\rm on,sp}$) will be much reduced.

In the modified transmission gate, there is a clamping device consisting of a gate-drain-shorted PMOS2 (M_{P2}), as shown in Fig. 1(b). This part is used to clamp the source to drain voltage of the intrinsic M_{P1} of the p-LDMOS to prevent prebreakdown.

Part 2: The integrated inverter consists of a high-side PMOS3 (M_{P3}) and a low-side NMOS2 (M_{N2}), as shown in Fig. 1(b).

Part 3: The low-voltage power supply part ($V_{\rm CD}$) consists of a diode (D_0), a capacitor (C_0), and a self-adjusted resistance under the p-base region, which is presented as R_s, as shown in Fig. 1(c). The value of R_s will be

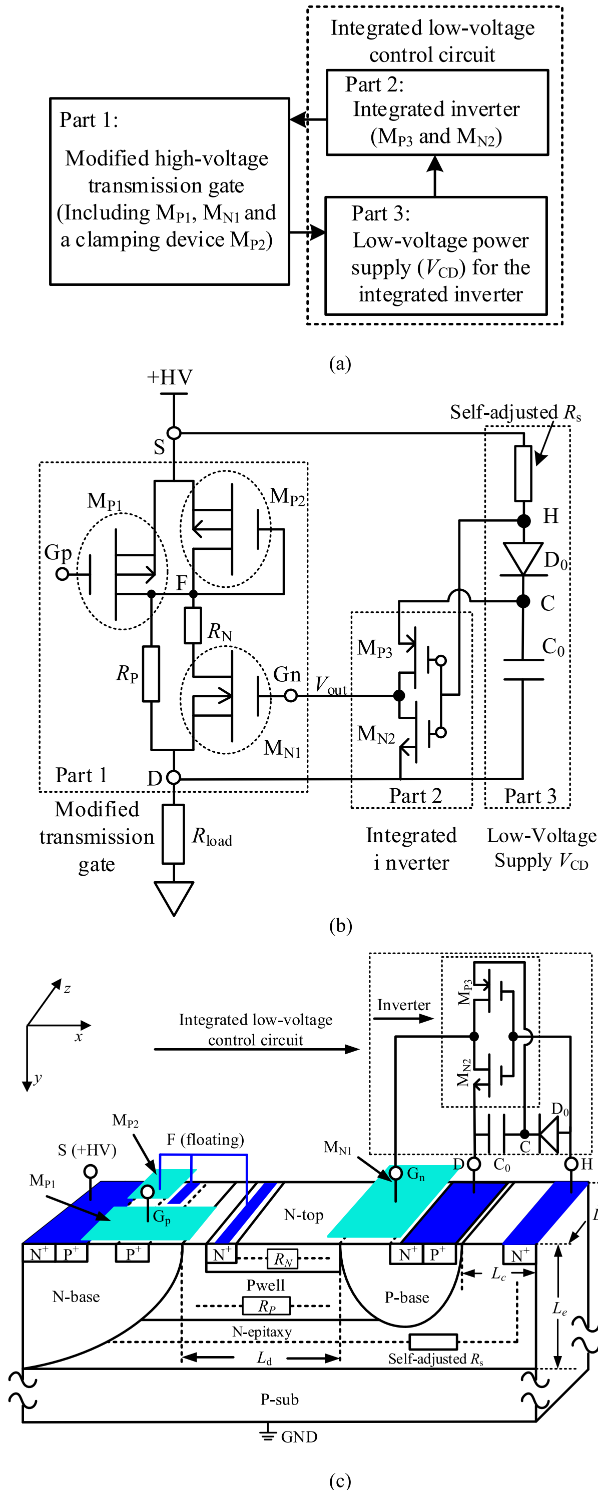


Fig. 1. (a) Block diagram of proposed p-LDMOS, (b) equivalent circuit of the proposed p-LDMOS with resistive load R_{load}, and (c) proposed p-LDMOS structure.

self-adjusted according to the depletion degree of the drift region under p-base region.

The inverter and the low-voltage power supply part constitute the low-voltage control circuit to generate the auto-control signal for the gate (G_n) of M_{N1} in the floating tub region.

TABLE I
KEY PARAMETERS IN SIMULATION

Parameters	Peak Position (μm)	Peak Value (cm^{-3})	Diffusion Length (μm)
n-Epitaxy	–	4×10^{15}	–
n-Base	0	5×10^{16}	2.5
p-Base	0	2×10^{17}	2.6
p-Well	0	2.7×10^{16}	2.8
n-Top	0	5.3×10^{16}	1
p-Sub	–	1.5×10^{14}	–
L_d (μm)		22	
L_e (μm)		9	
L_c (μm)		1	
L_Z (μm)		1	

The basic mechanism of the proposed p-LDMOS can be explained by using Fig. 1(b). When M_{P1} is off, the low-voltage power supply, i.e., the capacitor C_0 is charged to a maximum value. After M_{P1} is turned on, the voltage V_{SD} decreases to a negligible value and can be taken as 0 V. And the diode D_0 is reverse biased; thus, $V_{\mathrm{HC}} = V_{\mathrm{SC}} = V_{\mathrm{SD}} - V_{\mathrm{CD}} = -V_{\mathrm{CD}}$. As long as $-V_{\mathrm{CD}}$ is less than the threshold voltage of M_{P3} ($V_{\mathrm{th}M_{P3}}$), M_{P3} will be turned on and begins to charge G_n to turn on M_{N1}.

To turn off the device, M_{P1} is turned off, then V_{SD} increases. When V_{SD} is larger than the threshold voltage of $M_{N2}(V_{\mathrm{th}M_{N2}})$ and $V_{\mathrm{HD}} \approx V_{\mathrm{SD}}$, M_{N2} is turned on to discharge the gate voltage of G_n to 0 V. Thus, M_{N1} is turned off and the whole device is turned off. The detailed mechanism will be discussed in the following sections.

Fig. 1(c) shows the detailed 3-dimensional structure of proposed p-LDMOS which will be used for simulation in the following sections.

B. TCAD Tool and the Calibrated Models

In this paper, TCAD tool Sentaurus [20] is used to investigate the performances of the proposed p-LDMOS. When simulating an LDMOS, the key models, which should be used, are as follows: Avalanche, SRH(DopingDep), Mobility(DopingDep), and Mobility(HighFieldsaturation). Avalanche model is used to model the BV and determines the leakage current of the device. SRH(DopingDep) model is used to model the influence of doping concentration on carrier lifetime (τ), which will also influence the leakage current because the leakage current is proportional to $1/\tau$ [21]. Mobility(DopingDep) is used to model the influence of doping concentration on carrier mobility, and Mobility(HighFieldsaturation) is used to model the influence of high electric field in the inversion layer on carrier mobility. The mobility models will determine the $R_{\mathrm{on,sp}}$ of the LDMOS. All the earlier models are calibrated according to experimental data [20], and by applying these kind of models, the simulated results of modern TCAD tool has been proved to have a very good agreement with experimental results [22]–[30].

Table I lists the key simulation parameters of the device in Fig. 1(c). In Fig. 1(c), due to the symmetry in the z-axis, the width in the direction of z-axis is set to be only 1 μm to save the time of the numerical simulation. Thus, the channel width of M_{P1} is set to 0.8 μm, and the channel width of M_{P2} is set to

0.1 μm. In practice, these dimensions can be magnified according to the process dimension at the same proportion. The doping concentration of N-epitaxy and p-sub are available according to the previous works [31]–[35].

All the doping concentrations in Table I are Gaussian distribution. Since multiple thickness of gate oxide ($t_{\rm ox}$) can be employed in the SPIC platform, $t_{\rm ox}$ for M_{P1} and M_{N1} is set to 30 nm, corresponding to a threshold voltage $(V_{\rm th})V_{{\rm th}M_{N1}} = |V_{{\rm th}M_{P1}}| = 2\,{\rm V}$. $t_{\rm ox}$ for M_{P2}, M_{P3}, and M_{N2} is set to 80 nm, corresponding to $V_{{\rm th}M_{N2}} = |V_{{\rm th}M_{P3}}| = 5\,{\rm V}$, and $|V_{{\rm th}M_{P2}}| = 5.5\,{\rm V}$. $|V_{{\rm th}M_{P2}}|$ is a little larger than $|V_{{\rm th}M_{P3}}|$, because the channel width of M_{P2} is only 0.1 μm as being set earlier, which is 1/10th of that of M_{P3} when simulating $V_{\rm th}$. The reason why higher $V_{\rm th}$ for M_{P2}, M_{P3}, and M_{N2} is needed will be discussed in Section II-F and Section II-G. M_{N2} and M_{P3} of the inverter having a BV of more than 20 V can be integrated with the modified transmission gate in the right-side region of electrode *H*. The capacitor C_0 can be an integrated MIS or an external one, which is a commonly used component in SPIC application system [36]–[39].

C. Voltage-Sustaining Mechanism and Low-Voltage Supply

As shown in Fig. 1(c), there is an n-base/p$^+$/n-top/p-base structure in the device. Usually, this structure does not sustain high voltage. This is because, in a reverse-biased pn junction of silicon, the main leakage current is caused by the generation–recombination current, which is expressed as $J_{\rm ge} = (qn_i/\tau)\sqrt{2\varepsilon_s(\varphi_{bi} - V)/qN}$ [21], where n_i is the intrinsic carrier of silicon, τ is generated carrier lifetime, φ_{bi} is the build-in voltage of a pn junction, *V* is the applied voltage drop, *N* is the doping concentration of a pn junction at the lighter doped side, and *q* is the elementary charge. Since n-base/p$^+$ and n-top/p-base junctions conduct the same current and the doping concentration of n-base is heavier than that of n-top, from the earlier equation, for the same leakage current, the reverse voltage drop across n-base/p$^+$ will be larger than that across the n-top/p-base junction.

That is to say, the applied voltage will be mainly sustained by the heavier doped n-base/p$^+$ junction and the BV is usually tens of volts for the doping concentration of the n-base. In order to sustain high BV, a gate-drain-shorted M_{P2} in Fig. 1(c) is employed. When the source to drain voltage of M_{P2} is beyond the subthreshold voltage, the leakage current flows through M_{P2} instead of n-base/p$^+$ junction. Thus, the voltage across n-base/p$^+$ junction is clamped and the n-top/p$^+$ junction starts to sustain the main voltage.

Fig. 2 shows the simulated potential contour of the proposed p-LDMOS. Due to the clamping effect of M_{P2}, the main voltage is successfully sustained by the drift region. Fig. 3 can be used to further explain the voltage sustaining mechanism. As it shows, at the beginning of the source voltage ($V_{\rm SD}$) rising stage (0–4 V), the applied voltage is sustained by the reverse-biased n-base/p$^+$ junction due to its heavier doping concentration and the reverse voltage across n-base/p$^+$ junction ($V_{\rm SF}$) increases with $V_{\rm SD}$. Fig. 4 shows the leakage current around M_{P2}. In Fig. 4(a), the source to drain voltage $V_{\rm SD} = 2$ V. Under this value, the gate to

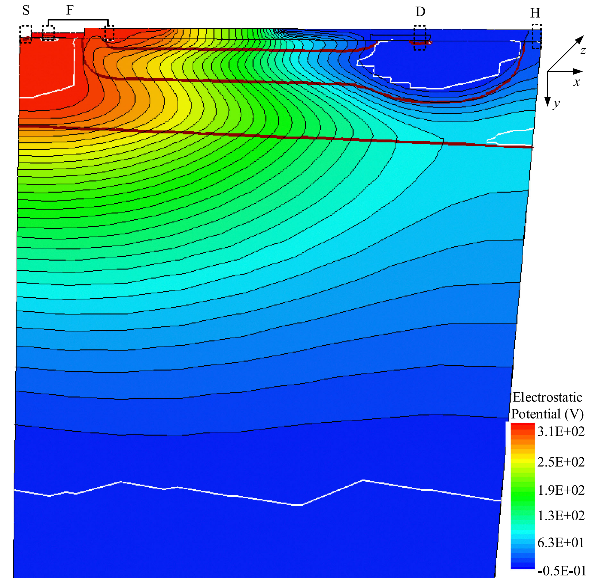


Fig. 2. Potential contour of the proposed p-LDMOS, $\Delta V = 10$ V.

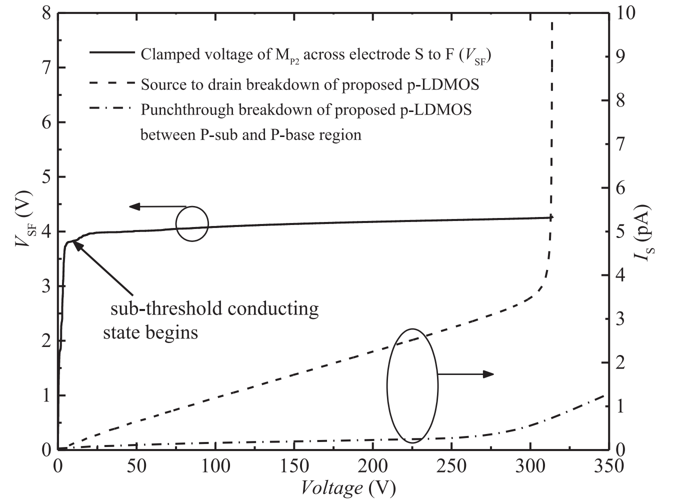


Fig. 3. Breakdown characteristic and the clamping figure of the gate-drain-shorted M_{P2}.

source voltage of M_{P2} is below the subthreshold voltage. Thus, part of the leakage current flows directly through n-base/p$^+$ junction into electrode *F*. With the increasing of $V_{\rm SD}$, the leakage current through n-base/p$^+$ junction increases, which will lead to the increasing of $V_{\rm SF}$, as shown in Fig. 3. But, with further increasing of the applied voltage, M_{P2} goes into the subthreshold conducting state, and the increased leakage current causing the voltage drop on n-base/p$^+$ junction to increase will not flow through the reverse-biased n-base/p$^+$ junction but will flow through the channel of M_{P2} due to its larger current capability than the reverse-biased n-base/p$^+$ junction, as shown in Fig. 4(b). Fig. 4(b) shows the leakage current around M_{P2} at $V_{\rm SD} = 5$ V. It shows that M_{P2} starts to conduct the leakage current in its subthreshold conducting state. Thus, the voltage across n-base/p$^+$ junction ($V_{\rm SF}$) is clamped at about 4.2 V as

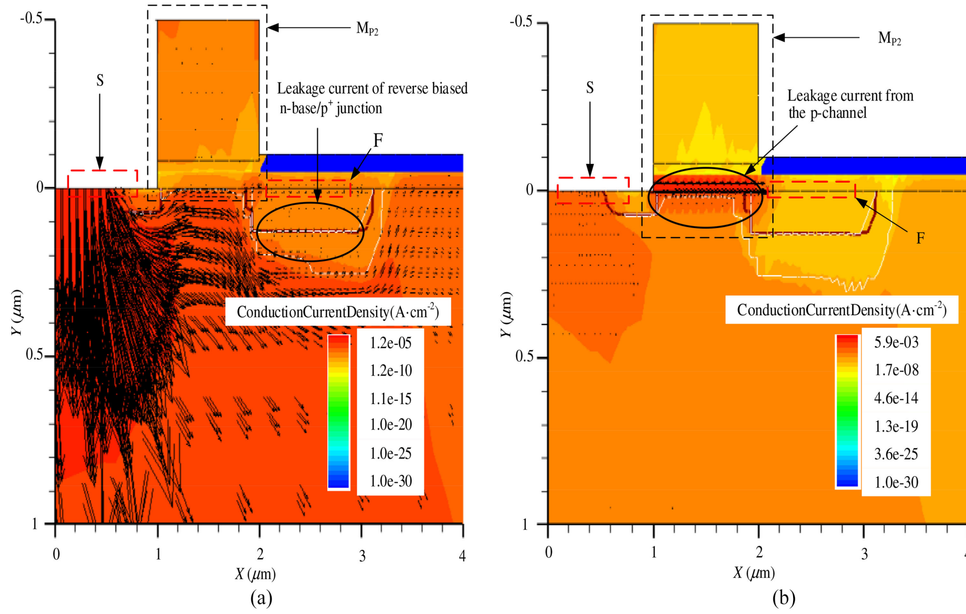


Fig. 4. Cross-section of M_{P2} across z-axis (a) vector of leakage current at $V_{\rm SD} = 2$ V and (b) vector of leakage current at $V_{\rm SD} = 5$ V.

shown in Fig. 3. Then, any further increase in voltage will be sustained by the drift region.

Since p-LDMOS is used as a high-side switch, the source electrode (*S*) in Fig. 1(c) is connected to the highest voltage (+HV) and the p-sub region is connected to the lowest voltage (GND). Both the source and drain voltages will be high after the p-LDMOS is turned on. Then, the n-epitaxy/p-sub junction in Fig. 1(c) will be reverse biased. Punch-through breakdown between p-base region and p-sub region should be avoided. In Fig. 3, the punch-through breakdown is also simulated, which shows that a punch-through BV of more than 300 V is obtained. Thus, punch-through breakdown will not be a problem.

Fig. 5 shows the voltage at electrode *H* [shown in Fig. 1(c)] with respect to electrode *D*, named $V_{\rm HD}$ [40]. The voltage $V_{\rm HD}$ is used to generate a low-voltage power supply ($V_{\rm CD}$) for G_n of M_{N1}. There are three different regions of $V_{\rm HD}$ versus the value of $V_{\rm SD}$ as shown in Fig. 5. The first one is the linear region (line *OA* in Fig. 5) in which the $V_{\rm HD}$ increases linearly with the applied source voltage ($V_{\rm SD}$) up to about 7 V, at which point the n-epitaxy region under electrode *H* is almost fully depleted. The second one is quasi-saturated region (line *A*–*B* in Fig. 5). In this region, the increase in $V_{\rm HD}$ is slowed down compared to $V_{\rm SD}$. Further, when $V_{\rm SD}$ is up to or more than about 40 V (point *B* in Fig. 5), the JFET region under p-base is fully depleted and the self-adjusted R_s becomes very large. The further increase in voltage will be sustained by R_s. Then, the generated low-voltage $V_{\rm HD}$ becomes stable, which is the saturated region [41]. As shown in Fig. 1(c), a diode D_0 and a capacitor C_0 are used to obtain the needed low-voltage power supply $V_{\rm CD}$ through electrode *H*. The capacitor C_0 is used to store the charge during the off-state and D_0 is used to prevent the discharge of C_0 during the on-state of the p-LDMOS. The simulated result in

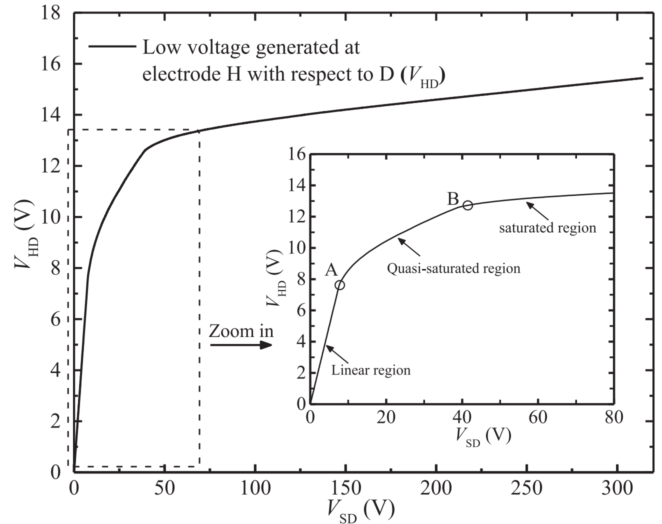


Fig. 5. Relationship between applied voltage and the generated voltage at electrode *H*.

Fig. 5 shows that a stable low voltage ($V_{\rm HD}$), which varies from 13 to 15 V, can be obtained over a wide voltage range of $V_{\rm SD}$ from 40 to 310 V.

To further explain the formation of the low-voltage $V_{\rm HD}$, the process of depletion region formation near electrode *H* at different values of $V_{\rm SD}$ is presented in Fig. 6. Fig. 6(a) shows the depletion region near electrode *H* at $V_{\rm SD} = 5.5$ V. This is in the linear region (0 V< $V_{\rm SD}$ <7 V), and it clearly shows that the n-epitaxy layer under electrode *H* is not fully depleted. Then the voltage on electrode *H* is equal to the voltage on electrode *S*. Fig. 6(b) shows the depletion region near electrode *H* at $V_{\rm SD} = 30$ V. This is in the quasi-saturated

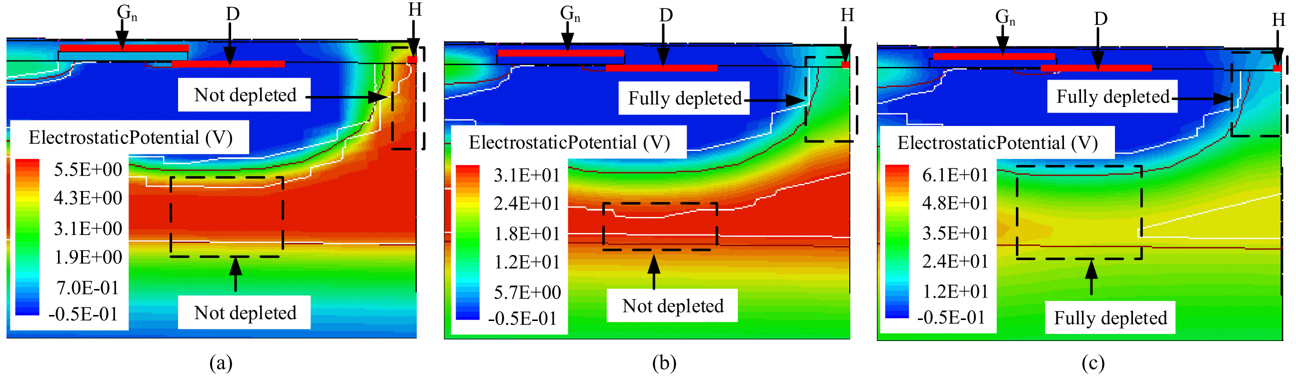


Fig. 6. Process of depletion region near electrode *H* of proposed p-LDMOS (a) $V_{\rm SD} = 5.5$ V, (b) $V_{\rm SD} = 30$ V, and (c) $V_{\rm SD} = 60$ V (white curves represent depletion boundaries).

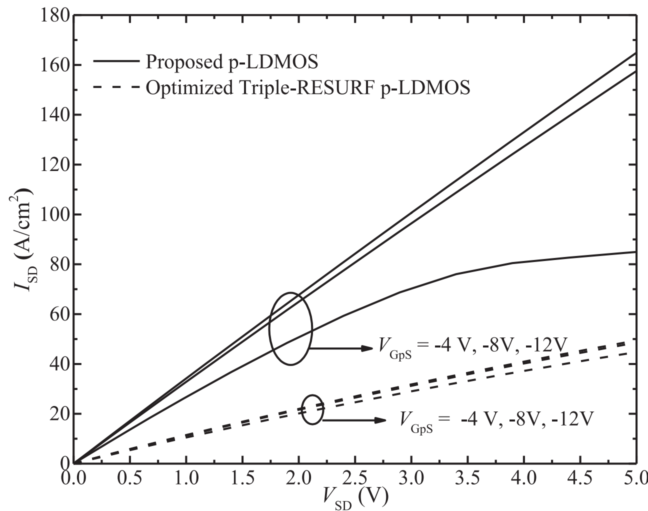


Fig. 7. Comparison of the current capabilities between the proposed p-LDMOS and an optimized Triple-RESURF p-LDMOS.

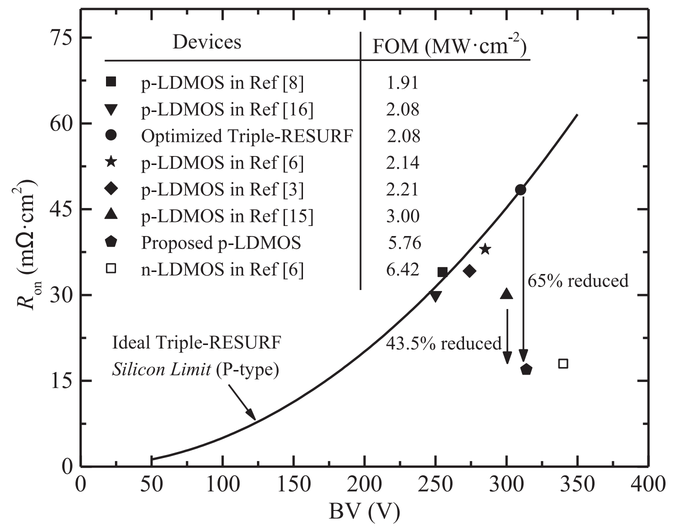


Fig. 8. $R_{\rm on,sp}$ vs. BV and FOM of different p-LDMOSs, $\mathrm{FOM} = \mathrm{BV}^2/R_{\rm on,sp}$.

region (7 V< $V_{\rm SD}$ <40 V), and it clearly shows that the n-epitaxy layer under electrode *H* is fully depleted while the n-epitaxy region under p-base is not fully depleted. The depleted region under electrode *H* acts like a resistor, the voltage at electrode *H* will increase slowly with the increasing of $V_{\rm SD}$. Fig. 6(c) shows the depletion region near electrode *H* at $V_{\rm SD} = 60$ V. This is in the saturated region (40 V< $V_{\rm SD}$). The n-epitaxy layer under electrode *H* and the n-epitaxy region under p-base are both fully depleted. The depleted region under electrode *H* and the depleted region under p-base both act like a resistor having a total self-adjusted value of R_s, which is very large; the further increase in $V_{\rm SD}$ is sustained by R_s and the low-voltage $V_{\rm HD}$ becomes stable.

D. Comparison of Proposed p-LDMOS and Triple-RESURF p-LDMOS

Fig. 7 shows the *I–V* characteristics of the proposed p-LDMOS and an optimized Triple-RESURF p-LDMOS. As can be seen that for the proposed p-LDMOS, the current capability is about 3.4 times of the optimized Triple-RESURF p-LDMOS. Thus, the SPIC chip area can be much reduced since the power devices in SPIC chip occupy most of the chip area [23].

Fig. 8 compares the $R_{\rm on,sp}$ and figure of merit ($\mathrm{FOM} = \mathrm{BV}^2/R_{\rm on,sp}$) of different p-LDMOSs [3], [6], [8], [15], [16]. It shows that the proposed p-LDMOS not only breaks the *silicon limit* and shows a very high FOM among all the state-of-the-art, but also the FOM of proposed p-LDMOS is very close to an optimized n-LDMOS having the same rated BV as shown in Fig. 8.

E. Start-Up Stage

As shown in Fig. 1(c), the total hole current through electrode S is divided into two parts. The first part flows directly from p-channel to electrode *D* through the p-well region. The second part is transformed into electron current through a floating electrode *F* and then flows to electrode *D* through n-top region and n-channel. Therefore, the total device current can be controlled by a single gate G_p with an autogenerated control signal on G_n, which will be discussed in detail in the following section.

Fig. 1(b) shows the equivalent circuit connection of the mixed-mode transient simulation for the switching application.

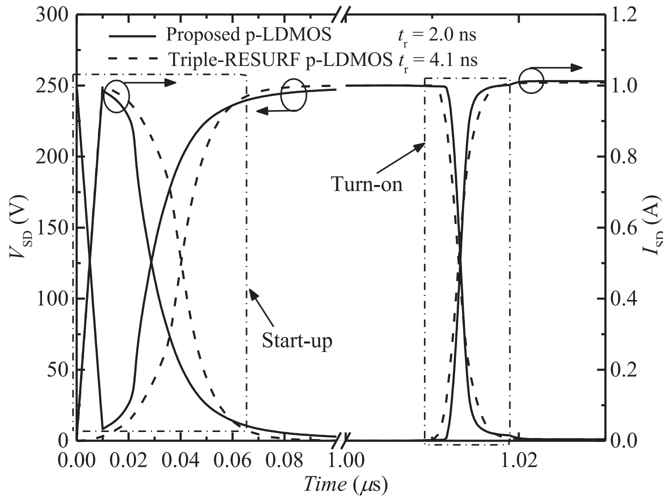


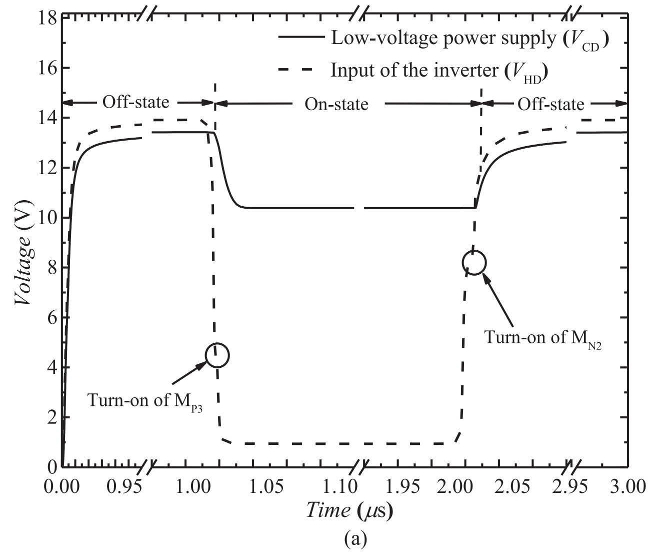
Fig. 9. Start-up and turning-on process of the proposed p-LDMOS and the optimized Triple-RESURF p-LDMOS.

The modified transmission gate is set to have an area of 3.3 mm^2 and the working current is 1 A. The load resistance $R_{\text{load}} = 247\ \Omega$, and the bus voltage is 250 V. An external diode model D_0 and a capacitor C_0 having a value of 1.5 nF is used in the simulation to supply the low voltage. The active area of the integrated inverter is set to 0.015 mm^2, which is only 0.45% of the modified transmission gate. Since the area of the integrated inverter is much smaller than that of the modified transmission gate, two separated *mesh* files for them are used in the mixed-mode transient simulation. Meanwhile, an optimized Triple-RESURF p-LDMOS is also simulated for comparison. Since the Triple-RESURF p-LDMOS has a low-current capability for the same area, as shown in Fig. 7, the device area is set to 10.8 mm^2 to have the same current capability, which is about three times than that of the proposed p-LDMOS.

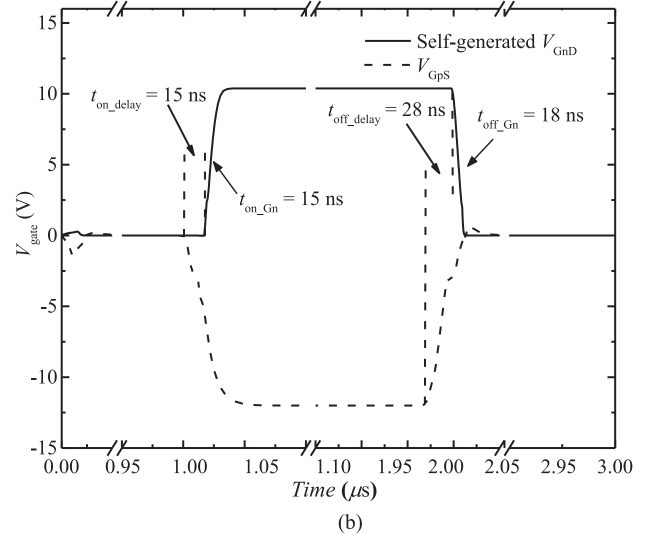
In the start-up stage, the bus voltage is ramped from 0 to 250 V in 10 ns. Fig. 9 shows the start-up stage of the switching circuit. After the bus voltage at electrode *S* has ramped to 250 V, the drain voltage (V_D) is automatically ramped to 250 V due to the intrinsic capacitor of the p-LDMOS device because the voltage across the capacitor cannot change abruptly. This means that $V_{\text{SD}} \approx 0$ V. Then, the intrinsic capacitor starts to be charged and V_{SD} increases. The bus voltage is gradually sustained by the p-LDMOS, and the electrode *H* begins to charge the capacitor C_0 through D_0 for the proposed p-LDMOS. C_0 is fully charged within 1 μs, as shown in Fig. 10(a).

F. Turn-On Process

At time $t_1 = 1\ \mu$s, the gate G_p is ramped from 0 to -12 V (with respect to electrode *S*) in 10 ns, as shown in Fig. 10(b). After the p-channel is turned on, V_D of the p-LDMOS increases to about the bus voltage, as shown in Fig. 9. When the drain voltage reaches more than 245 V, the voltage $V_{\text{HD}} = V_{\text{SD}}$ <5 V, since $V_S = V_H$ (as shown in Fig. 5). Then $V_{\text{HC}} < -8$ V, since $V_{\text{CD}} \approx 13$ V. So the input of the inverter becomes low, as shown in Fig. 10(a), and the upside M_{P3} is turned on to charge G_n as shown in Fig. 10(b). Therefore, M_{N1} is turned on. After



(a)



(b)

Fig. 10. (a) Autogenerated input wave of the integrated inverter and obtained low-voltage power supply (V_{CD}) and (b) applied gate wave of G_p and the self-generated gate wave on G_n of the proposed p-LDMOS in transient simulation.

charging the G_n, the voltage on C_0 decreases a little due to a part of its charge having transferred to G_n, as shown in Fig. 10(a).

The current capability of the inverter decides the charging delay time of G_n. Using the earlier device area (0.015 mm^2), the turn-on delaying time for G_n is only about 15 ns to the voltage of G_p, as shown in Fig. 10(b). Although, there is a gate voltage delay for G_n, the turn-on time (from 90% V_{SD} to 10% V_{SD}) of the proposed p-LDMOS is still faster than the optimized Triple-RESURF p-LDMOS. This is because that the Triple-RESURF p-LDMOS has an intrinsic capacitor about three times larger than that of the proposed p-LDMOS. The simulated results in Fig. 9 show that the turn-on time for proposed p-LDMOS and optimized Triple-RESURF p-LDMOS is 2.0 and 4.1 ns, respectively.

G. Turn-Off Process

Fig. 11 shows the turn-off process of the proposed p-LDMOS. After the p-channel is turned off, V_{SD} starts to increase, and

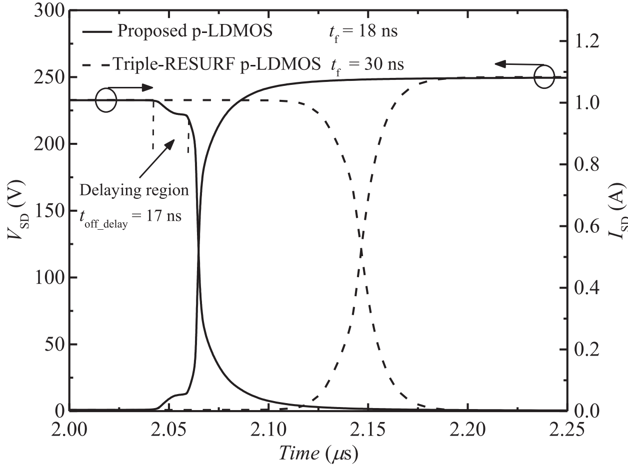


Fig. 11. Turn-off process of the proposed p-LDMOS and the optimized Triple-RESURF p-LDMOS.

TABLE II
COMPARISON OF PROPOSED AND TRIPLE-RESURF p-LDMOS

	Area (mm^2)	t_r (ns)	t_f (ns)	$E_{\mathrm{turn-on}}$ (μJ)	$E_{\mathrm{turn-off}}$ (μJ)
Triple-RESURF	10.8	4.1	30	0.21	1.7
This paper	3.3	2.0	18	0.13	1.3
Reduced percentage	69.4%	51.2%	40.0%	38.1%	23.5%

the increased voltage is mainly sustained by the gate-drain-shorted M_{P2}, resulting in the turn-on of the M_{P2}. Then, the total current through *S* electrode is transferred into electron current by electrode *F*. The electron current continues to flow through M_{P2} and M_{N1} to the load R_{load}, and V_{SD} stops to increase. This stage is shown as the delaying region in Fig. 11. At this stage, $V_{\mathrm{SF}} > 5.5$ V (because $|V_{\mathrm{th}M_{P2}}| = 5.5$ V). Thus, $V_{\mathrm{HD}} > 5.5$ V since $V_H = V_S$ from 0 to 7 V, as shown in Fig. 5. Therefore, M_{N2} of the inverter is turned on to discharge the charges on G_n, and G_n decreases to 0 V, as shown in Fig. 10(b). Thus, the total device is turned off, and the device starts to charge the capacitor C_0 to compensate the lost charges, as shown in Fig. 10(a). The p-LDMOS is successfully turned off, as shown in Fig. 11. Although, there is a delay time of about 17 ns before the further decrease of voltage at electrode *D* caused by the turn-off delay of G_n, as shown in Fig. 10(b), the turn-off time of proposed p-LDMOS is still faster than that of the optimized Triple-RESURF p-LDMOS since the optimized Triple-RESURF p-LDMOS has a larger intrinsic capacitor than the proposed one due to its larger device area. The turn-off time (from 10% V_{SD} to 90% V_{SD}) of proposed p-LDMOS and optimized p-LDMOS is 18 and 30 ns, respectively, as shown in Fig. 11.

The fast turn-on and turn-off speed ensures the symmetrical bipolar output waveform with n-LDMOS [6] and the switching loss is also reduced.

Table II compares the device area and power loss of different p-LDMOSs during switch on and off process. The device area of proposed p-LDMOS is reduced by 69.4%, and the total switching loss (including the delaying region in Fig. 11) of proposed p-LDMOS is reduced by 25.1% compared to that of the optimized Triple-RESURF p-LDMOS.

III. PROCESS SIMULATION AND DISCUSSION FOR PROPOSED p-LDMOS

Process simulator Tsuprem-4 [42] is used to verify the compatibility with present planar silicon technology of proposed p-LDMOS. Fig. 12 shows the key steps of the process flow. In Fig. 12(a), an 8 μm n-type epitaxial layer (arsenic) with a concentration of 4×10^{15} cm^{-3} is introduced on the p-substrate, which has a concentration of 1.5×10^{14} cm^{-3}. Then, the p-well layer (boron) having a dose of 1.1×10^{13} cm^{-2} is implanted with 130 keV energy and driven in for 200 min at 1150 °C, as shown in Fig. 12(b). In Fig. 12(c), the n-top layer (arsenic) having a dose of 1.1×10^{13} cm^{-2} is implanted at 130 keV energy and annealed in oxygen for 250 min at 1050 °C. The field oxide is finished at the same time. In Fig. 12(d), after the active region is opened, gate oxide is thermally grown, followed by n$^+$ polysilicon deposition. In Fig. 12(e), the n-base (phosphorus) and p-base (boron) are implanted at 50 and 120 keV energy, respectively, and driven in for 250 min at 1150 °C. The following steps include BPSG deposition and reflowing, contact etch, metal deposition and etch, and passivation layer deposition. The last structure is shown in Fig. 12(f).

After the process simulation, the process file is loaded in MEDICI [43] for electrical characteristic simulation. The simulated BV is 328 V and the $R_{\mathrm{on,sp}} = 16.9$ mΩ/cm^2, which is in good agreement with the device simulation results in Fig. 8.

Usually, the effective dose deviation of the drift region will influence the BV of the RESURF LDMOS. For the proposed p-LDMOS, the dose of p-base will also influence the performance of the p-LDMOS. The effective dose of p-base may influence the low-voltage power supply and the punch-through breakdown between p-base and p-sub. Therefore, the process window of the drift region (n-top and p-well) and the p-base for the proposed p-LDMOS is discussed.

The influence on BV and $R_{\mathrm{on,sp}}$ of the deviation of n-top and p-well is simulated within a reasonable process window of $\pm 10\%$ [44], [45]. Fig. 13 shows the influence of n-top and p-well on BV and $R_{\mathrm{on,sp}}$, It shows that within $\pm 10\%$ deviation for both n-top and p-well, all the BV reaches above 88.6% of the maximum BV ($\mathrm{BV_{max}}$), which is very close to the value about 93% of a robust RESURF LDMOS [44], [45]. The worst condition is that the dose deviation of p-well and n-top is -10% and $+10\%$, respectively. But under this condition, the $R_{\mathrm{on,sp}}$ still has a reduction of 64% compared to the ideal Triple-RESURF p-LDMOS ($R_{\mathrm{on,sp}} \approx 44.5$ mΩ/cm^2 at BV = 298 V).

Fig. 14 shows the simulated process results of low-voltage supply and BV depending on different deviation of p-base within a reasonable process window of $\pm 10\%$ [44], [45]. As can be seen from the figure, both the BV of source to drain and the punch-through BV between the p-sub region and p-base region is above 320 V. For each dose of the p-base, a stable low voltage can be obtained when V_{SD} changes from 40 to 320 V. This is in good agreement with the device simulation results shown in Fig. 5.

Fig. 12. Key process steps for proposed p-LDMOS.

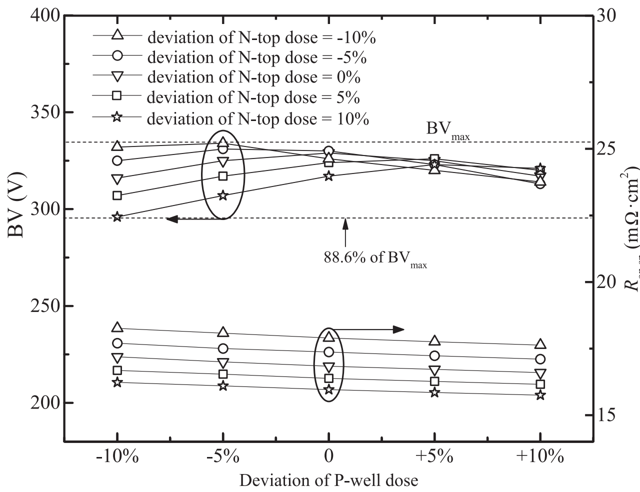


Fig. 13. Influence of n-top and p-well on BV and $R_{\mathrm{on,sp}}$ of proposed p-LDMOS.

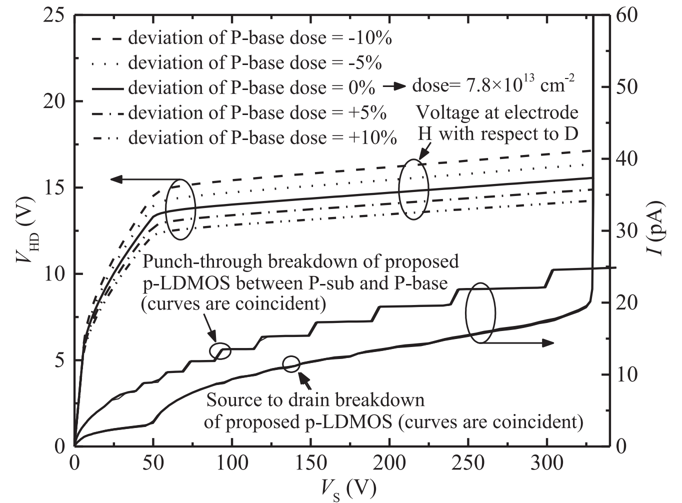


Fig. 14. Simulated process result of low-voltage supply and BV,depending on injected dose deviation of p-base; the injected dose of n-top and p-well is 1.1 × 10^{13} cm^{-2}.

As discussed in Section II, the obtained low voltage can ensure the normal operation of the proposed p-LDMOS.

When the deviation is -10%, the stable low voltage (V_{HD}) is only about 2 V higher than the designed one. This will only increase a little discharge time of G_n, which may increase a little of the device's turn-off time. For different dose deviations of p-base, the curves of leakage current of source to drain and p-base to p-sub are coincident, respectively. This means the dose deviation of p-base within $\pm 10\%$ has little influence on the BV and punch-through of the proposed p-LDMOS.

The earlier process simulation is based on two dimensions; thus, the gate-drain-shorted M_{P2} is not shown in Fig. 12. But it is obvious that the M_{P2} can be easily implemented in a three-dimensional layout. After the growing of gate oxide for M_{P1}, re-growing of gate oxide for M_{P2} can be completed before deposition of n^{+} poly. Then the following steps are the same as shown in Fig. 12(e) and (f).

IV. Conclusion

In this paper, a 300-V novel high-voltage p-LDMOS is proposed. The proposed p-LDMOS utilizes two kinds of carriers to conduct the on-state current. Thus, the specific on-resistance is reduced by 65% compared to the Triple-RESURF *silicon limit.* Also, since the current capability is improved, the device area is reduced, leading to a lower input and output capacitor of the p-LDMOS, which helps improve the switching speed and reduce the switching loss, and can obtain a symmetrical bipolar output waveform with an n-LDMOS. Process window is simulated by process simulator to verify that the proposed p-LDMOS can tolerate a reasonable process window within $\pm 10\%$.

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References

[1] Y. Fu-Jen, G. Jeng, S. Ru-Yi, H. Ker-Hsiao, T. Chun-Lin, C. Chih-Chang, L. Ruey-Hsin, T. Hsiao-Chin, and H. Chih-Fang, “A 700-V device in high-voltage power ICs with low on-state resistance and enhanced SOA,” *IEEE Trans. Electron. Devices*, vol. 60, no. 9, pp. 2847–2853, Sep. 2013.

[2] Q. Ming, L. Yanfei, Z. Xin, L. Zhaoji, and Z. Bo, “A 700-V junction-isolated triple RESURF LDMOS with N-type top layer,” *IEEE Electron. Device Lett.*, vol. 35, no. 7, pp. 774–776, Jul. 2014.

[3] T. Miyoshi, T. Tominari, H. Fujiwara, T. Oshima, and J. Noguchi, “Design of a reliable P-channel LDMOS FET with RESURF technology,” *IEEE Trans. Electron. Devices*, vol. 61, no. 5, pp. 1451–1456, May 2014.

[4] S. G. Nassif-Khalil and C. A. T. Salama, “170V super junction—LDMOST in a 0.5 μm commercial CMOS/SOS technology,” in *Proc. 2003 IEEE 15th Int. Symp. Power Semicond. Devices ICs*, pp. 228–231.

[5] S. Shimamoto, Y. Yanagida, S. Shirakawa, K. Miyakoshi, T. Imai, T. Oshima, J. Sakano, and S. Wada, “High performance Pch-LDMOS transistors in wide range voltage from 35V to 200V SOI LDMOS platform technology,” in *Proc. 2011 IEEE 23rd Int. Symp. Power Semicond. Devices ICs*, 2011, pp. 44–47.

[6] S. Shimamoto, Y. Yanagida, S. Shirakawa, K. Miyakoshi, T. Oshima, J. Sakano, S. Wada, and J. Noguchi, “High-performance P-channel LDMOS transistors and wide-range voltage platform technology using novel P-channel structure,” *IEEE Trans. Electron. Devices*, vol. 60, no. 1, pp. 360–365, Jan. 2013.

[7] S. L. Kim, C. K. Jeon, M. H. Kim, and J. J. Kim, “Realization of robust 600V high side gate drive IC with a new isolated self-shielding structure,” in *Proc. 17th Int. Symp. Power Semicond. Devices ICs*, 2005, pp. 143–146.

[8] M. Sambi, D. Merlini, P. Galbiati, E. Bonera, and F. Belletti, “A novel 0.16um-300 V SOIBCD for ultrasound medical applications,” in *Proc. 2011 IEEE 23rd Int. Symp. Power Semicond. Devices ICs*, pp. 36–39.

[9] M. Qiao, X. Zhou, Y. T. He, H. J. Wen, Y. Y. Zhao, B. Zhang, and Z. J. Li, “300-V high-side thin-layer-SOI field pLDMOS with multiple field plates based on field implant technology,” *IEEE Electron. Device Lett.*, vol. 33, no. 10, pp. 1438–1440, Oct. 2012.

[10] C. Yuhui, F. C. Lee, L. Amoroso, and W. Ho-Pu, “A resonant MOSFET gate driver with efficient energy recovery,” *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 470–477, Mar. 2004.

[11] X. Zhou, Z. G. Liang and A. Huang, “A high-dynamic range current source gate driver for switching-loss reduction of high-side switch in buck converter,” *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1439–1443, Jun. 2010.

[12] A. W. Ludikhuize, “A versatile 700–1200-V IC process for analog and switching applications,” *IEEE Trans. Electron. Devices*, vol. 38, no. 7, pp. 1582–1589, Jul. 1991.

[13] M. Nakano, K. Takahashi, A. Tanaka, A. Osawa, and H. Yoshida, “Full-complementary high-voltage driver ICs for flat display panels,” in *Proc. 1989 Int. Symp. VLSI Technol. Syst. Appl. Tech. Papers*, pp. 55–58.

[14] R. Bondade, W. Yikai, and M. Dongsheng, “Design of integrated bipolar symmetric output DC–DC power converter for digital pulse generators in ultrasound medical imaging systems,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1821–1829, Apr. 2014.

[15] X. Zhou, M. Qiao, Y. T. He, Z. Wang, Z. J. Li, and B. Zhang, “Back-gate effect on Ron,sp and BV for thin layer SOI field P-channel LDMOS,” *IEEE Trans. Electron. Devices*, vol. 62, no. 4, pp. 1098–1104, Apr. 2015.

[16] B. Luo, M. Qiao, Y. C. Wang, M. L. K, J. Ye, B. Zhang, and Z. J. Li, “High voltage SJ-pLDMOS with variation lateral doping drift layer,” in *Proc. 2010 Int. Conf. Commun. Circuits Syst.*, pp. 503–506.

[17] X. Chen, “Lateral high-voltage semiconductor devices with majorities of both types for conduction,” U.S. Patent 8 159 026, Apr. 17, 2012.

[18] M. F. Kong, W. F. Du, and X. B. Chen, “Study on dual channel n-P-LDMOS power devices with three terminals,” *IEEE Trans. Electron. Devices*, vol. 60, no. 10, pp. 3508–3514, Oct. 2013.

[19] M. M.-H. Iqbal, F. Udrea, and E. Napoli, “On the static performance of the RESURF LDMOSFETS for power ICs,” in *Proc. 21st Int. Symp. Power Semicond. Devices IC’s*, 2009, pp. 247–250.

[20] Synopsys Inc., CA, USA, *Sentaurus Device User Guide*, 2010.

[21] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, pp. 83–96.

[22] M. Qiao, Y. R. Wang, X. Zhou, F. Jin, H. H. Wang, Z. Wang, Z. J. Li, and B. Zhang, “Analytical modeling for a novel triple RESURF LDMOS with N-top layer,” *IEEE Trans. Electron. Devices*, vol. 62, no. 9, pp. 2933–2939, Sep. 2015.

[23] J. J. Cheng and X. B. Chen, “A novel low-side structure for OPTVLD-SPIC technologically compatible with BiCMOS,” in *Proc. 2013 25th Int. Symp. Power Semicond. Devices ICs*, pp. 123–126.

[24] Y. Wei, G. Gildenblat, C. C. McAndrew, and A. Cassagnes, “Compact model of impact ionization in LDMOS transistors,” *IEEE Trans. Electron. Devices*, vol. 59, no. 7, pp. 1863–1869, Jul. 2012.

[25] X. R. Luo, B. Zhang, T. F. Lei, Z. J. Li, Z. Q. Xiao, W. C. W. Hsu, and F. Udrea, “Numerical and experimental investigation on a novel high-voltage (>600-V) SOI LDMOS in a self-isolation HVIC,” *IEEE Trans. Electron. Devices*, vol. 57, no. 11, pp. 3033–3043, Nov. 2010.

[26] L. X. Theolier, H. Mahfoz-Kotb, K. Isoird, F. Morancho, S. Assie-Souleille, and N. Mauran, “A new junction termination using a deep trench filled with benzo cyclo butene,” *IEEE Electron. Device Lett.*, vol. 30, no. 6, pp. 687–689, Jun. 2009.

[27] S. Reggiani, G. Barone, S. Poli, E. Gnani, A. Gnudi, G. Baccarani, C. Ming-Yeh, T. Weidong, and R. Wise, “TCAD simulation of hot-carrier and thermal degradation in STI-LDMOS transistors,” *IEEE Trans. Electron. Devices*, vol. 60, no. 2, pp. 691–698, Feb. 2013.

[28] S. Poli, S. Reggiani, G. Baccarani, E. Gnani, A. Gnudi, M. Denison, S. Pendharkar, R. Wise, and S. Seetharaman, “Investigation on the temperature dependence of the HCI effects in the rugged STI-based LDMOS transistor,” in *Proc. 2010 22nd Int. Symp. Power Semicond. Devices IC’s*, pp. 311–314.

[29] S. F. Frre, J. Rhayem, H. O. Adawe, R. Gillon, M. Tack, and A. J. Walton, “LDMOS capacitance analysis versus gate and drain biases, based on comparison between TCAD simulations and measurements,” in *Proc. 31st Eur. Solid-State Device Res. Conf.*, 2001, pp. 219–222.

[30] Y. S. Chung and B. Baird, “Electrical-thermal coupling mechanism on operating limit of LDMOS transistor,” in *Proc. Tech. Dig. Int. Electron. Devices Meeting*, 2000, pp. 83–86.

[31] B. Zhang, W. L Wang, W. J. Chen, Z. J. Li, and Z. J. Li, “High-voltage LDMOS with charge-balanced surface low on-resistance path layer,” *IEEE Electron. Device Lett.*, vol. 30, no. 8, pp. 849–851, Aug. 2009.

[32] Y. Ota, “Si molecular beam epitaxy (n on n+) with wide range doping control,” *J. Electrochem. Soc.*, vol. 124, pp. 1795–1802, 1977.

[33] R. Young, J. Cleland, R. Wood, and M. Abraham, “Radiation damage in neutron transmutation doped silicon: Electrical property studies,” *J. Appl. Phys.*, vol. 49, pp. 4752–4760, 1978.

[34] R. Tadikonda, S. Hardikar, D. W. Green, M. Sweet, and E. M. S. Narayanan, “Analysis of lateral IGBT with a variation in lateral doping drift region in junction isolation technology,” *IEEE Trans. Electron. Devices*, vol. 53, no. 7, pp. 1740–1744, Jul. 2006.

[35] B. Duan, Y. Yang, and B. Zhang, “High voltage REBULF LDMOS with N+ buried layer,” *Solid-State Electron.*, vol. 54, pp. 685–688, 2010.

[36] A. Moazenzadeh, F. Suarez Sandoval, N. Spengler, V. Badilita, and U. Wallrabe, “3-D microtransformers for DC-DC on-chip power conversion,” *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5088–5102, Sep. 2015.

[37] C. Lin, N. Jinhua, Q. Yao, Z. Minchao, K. Wing-Hung, L. Bill Yang, G. Li, and H. Zhiliang, “On-chip compensated wide output range boost converter with fixed-frequency adaptive off-time control for LED driver applications,” *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2096–2107, Apr. 2015.

[38] K. Yeong-Chau, L. Yung-Jie, and L. Li-Jen, “Synthesizable integrated circuit and system design for solar chargers,” *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4260–4266, Sep. 2013.

[39] X. Zhang, L. Jiang, J. Deng, S. Li, and Z. Chen, “Analysis and design of a new soft-switching boost converter with a coupled inductor,” *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4270–4277, Aug. 2014.

[40] X. Chen, “Method of producing a low-voltage power supply in a power integrated circuit,” U.S. Patents 7 701 006, Apr. 20, 2010.

[41] W. F. Du, X. J. L. Wai Tung, N. Wai Tung, and X. B. Chen, “An ultra-low specific ON-resistance LDMOST with self-driven split gate,” *IEEE Trans. Electron. Devices*, vol. 62, no. 4, pp. 1230–1234, Apr. 2015.

[42] Synopsys Inc., CA, USA, *Tsuprem-4, Two Dimensional Process Simulation Program*, 2010.

[43] *MEDICI, Two Dimensional Device Simulation Program*, Synopsys Inc., Fremont, CA, 2002.

[44] J. J. Cheng and X. B. Chen, “A practical approach to enhance yield of OPTVLD products,” *IEEE Electron. Device Lett.*, vol. 34, no. 2, pp. 289–291, Feb. 2013.

[45] Z. Hossain, “Determination of manufacturing RESURF process window for a robust 700V double RESURF LDMOS transistor,” in *Proc. 20th Int. Symp. Power Semicond. Devices IC’s*, 2008, pp. 133–136.

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