Unified Digital Current Mode Control Tuning With Near Optimal Recovery in a CCM Buck Converter

V. Inder Kumar, *Student Member, IEEE*, and Santanu Kapat, *Member, IEEE*

***Abstract*—Linear small-signal models of a dc–dc converter often ignore switching dynamics; thus such models are insufficient to fully explore the performance objective under large signal transients. Linear/nonlinear hybrid controllers are promising alternatives; however, they require structurally different hardware resources along with extra antiwindup arrangements. This paper proposes a geometric tuning method in a digitally current-mode-controlled buck converter under continuous-conduction mode. This considers a proportional-integral voltage controller along with a load current feedforward in the digital domain, while the inductor current has a traditional analog implementation. This resembles a first-order switching surface with near load-invariant regulation; thus a (fixed) small integral gain is sufficient to minimize the steady-state error. Using phase-plane geometry, the objective is to tune the controller gain in a way to achieve proximate time optimal recovery using a fixed-frequency pulse-width modulator and also to retain the large-signal stability. The effects of parameter variation and finite sampling are analyzed. The proposed tuning is implemented using an FPGA device.**

***Index Terms*—Buck converter, current-mode control (CMC), digital pulse-width-modulator (DPWM) controller tuning, geometric approach, time-optimal recovery.**

I. Introduction

DIGITAL power management has been growing at a rapid pace due to their ease of integration with other digital systems, ability to implement high-performance control schemes [1]–[4], immunity to noise and analog component variations, compact size, real-time energy optimization [5], [6], and faster time-to-market. This paper considers a digitally current-mode-controlled (CMC) buck converter and attempts to develop a unified tuning method to achieve proximate time optimal (large-signal) recovery using a fixed-frequency modulator.

A proportional-integral-derivative (PID) controller finds wide spread applications, because of its simplicity, ease of use, and clear functionality [7]. This is a special form of a phase lead-lag compensator with one pole at the origin and the other at infinity. Difficulties of offline PID controller tuning are because of unknown load characteristics, as well as parameter uncertainties of the converter. This necessitates real-time controller tuning for sake of a more optimal design over a wide operating range [8]. PID controller tuning based on model reference adaptive control were successfully applied to a continuous-conduction mode (CCM) buck converter in [9] and [10]. Any adaptive control should ensure stability of the adaptive loop for the controller parameters to converge. Tuning methods based on online identification of the converter control-to-output frequency response can overcome these limitations, which have been successfully applied to CCM buck converters in [11] and [12]. Relay feedback based autotuning of a digitally controlled dc–dc converter is proposed in [13]. An autotuning method of a PID controller based on online frequency response measurement is presented in [14]. A robust tuning method based on desired phase margin was proposed in [15]. A nonlinear PID controller can achieve improved performance [16]. However, because of ignoring the switching dynamics using linear small-signal models, the performance and stability objectives cannot be fully explored.

Time-optimal control algorithms have been reported in the context of dc–dc converters [17]–[27]. These include boundary control methods [19]–[21], which use first order, second, or higher order, including natural switching surfaces, with the objective to achieve time-optimal recovery. A higher order is expected to provide a better proximity; however, sensing requirements and the controller complexity increase significantly. Moreover, majority of the above methods suffer from switching frequency variation at a steady state. Linear/nonlinear hybrid controllers are alternative approaches, in which a linear pulse-width-modulation (PWM) technique is interfaced to operate when the trajectory moves toward the target operating point [22]–[24]. However, these require separate hardware resources and additional antiwindup arrangements. The objectives of this paper are 1) to frame a first-order switching surface in [24] to a current-mode digital PWM controller, and 2) to tune the proportional voltage controller under finite analog-to-digital converter (ADC) sampling 3) to achieve proximate time-optimal (large-signal) recovery, which would reduce the hardware resources and (real-time) computational requirements.

This paper proposes a geometric tuning method in a digitally CMC buck converter with a load current feedforward using a PI voltage controller. Using phase-plane geometry, an optimal proportional gain k_p is analytically derived using the operating point information. This can achieve proximate time-optimal recovery using a fixed-frequency modulator by varying k_p in real time. The effects of parameter variation and finite sampling are analyzed. The proposed method is implemented using an FPGA device.

The paper is organized as follows: Section II introduces a geometric tuning approach in a digitally CMC buck converter, including various practical aspects. Section III discusses

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The authors are with the Department of Electrical Engineering, Indian Institute of Technology, Kharagpur 721302, India (e-mail: indervedula@gmail.com; santanu.kapat@ieee.org).

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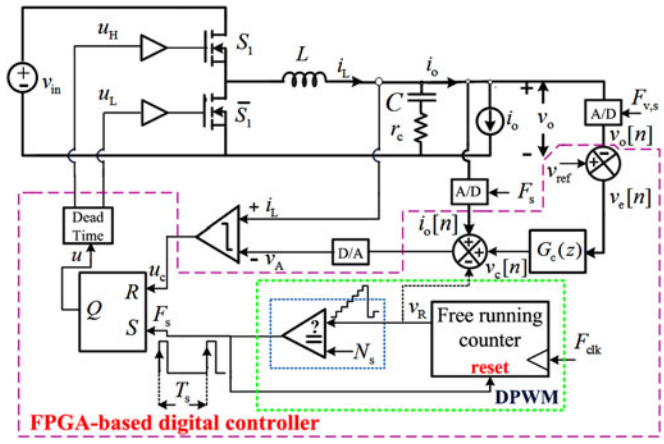

Fig. 1. A synchronous buck converter under mixed-signal current mode control (MCMC) with load current feed-forward.

robustness against parameter variation and large-signal stability analysis. Section IV presents hardware implementation and experimentally justifies the merits of the proposed tuning. Section V concludes the paper.

II. Proposed Geometric Tuning Approach

A. Switching Surface Formulation Using PWM Control

Consider a CMC buck converter with a load current feedforward and a PI voltage controller. The overall control can be framed into a switching surface as [17]

$$\sigma = k_p(v_{\rm ref} - v_o) + k_i \int (v_{\rm ref} - v_o)d\tau - (i_L - i_o) \qquad (1)$$

where k_p and k_i are the proportional and integral gains; $v_{\rm ref}$ is the reference voltage; i_L and i_o indicate the inductor current and load current; the error current $(i_L - i_o)$ indicates the capacitor current i_c for a CCM buck converter. The control mechanism in Fig. 1 is similar to fixed frequency 1) CMC with load current feedforward as well as 2) current injection control in [25]. For $k_i = 0$, (1) resembles a first-order switching surface, in which the current error $(i_L - i_o)$ can be used for the derivative purpose [26]. This can replace a direct voltage derivative and minimize the high-frequency noise injection. This can also improve the (load) transient response using the load current feedforward. It significantly improves the output impedance [25] and achieves near load-invariant regulation even in absence of an integral action. Thus, a small (fixed) integral gain is sufficient to minimize the steady-state error.

B. Mixed-Signal CMC (MCMC) With Load Current Feedforward

Fig. 1 shows the schematic of a MCMC buck converter, in which the fast-changing inductor current i_L is considered in the analog domain. A variety of power-efficient current sensing methods are available in the literature [28] as well as in various commercial products [29], such as LM3075, FSL4110LR, RC5057, etc. An ADC along with an analog multiplexer (MUX) can be used for sampling v_o and i_o. This utilizes the real-time tuning flexibility of the digital voltage controller $G_c(z)$ and allows one to implement high-performance control algorithms.

A counter-based digital pulse-width-modulator (DPWM) is considered, which is incremented using the rising edge of the controller clock $F_{\rm clk}$ with the time period $t_{\rm clk}$. A set value N_s is used to generate a fixed-frequency switching clock F_s with the time period $T_s = (N_s + 1) \times t_{\rm clk}$. The output voltage is sampled with a rate $F_{v,s}$ which is also used for computation of the digital voltage controller $G_c(z)$. The controller output $v_c[n]$ is then added to the sampled load current $i_o[n]$ which is sampled at the rate of the switching clock F_s. The DPWM output v_R can be added for an optional discrete-time ramp compensation. Thereafter, the result is converted into an equivalent analog voltage v_A using a D/A converter and directly compared with the inductor current i_L in the analog domain. The comparator output u_c is then latched using an RS flip/flop. The dead-time circuit uses the output u to generate gate signals u_H and u_L for the respective high-side and low-side MOSFETs as shown in Fig. 1.

C. Indirect Methods for Extracting Load Current Information

The proposed tuning method in Section II-B requires load current information, and direct sensing may not be possible, not even practically recommended for high-current applications.

Incidentally direct sensing is not required for modern digital devices, consisting of smart processors, of which the task schedulers can provide detailed information of the sequence of tasks along with the estimated start and end times, energy requirements, etc., [30], [31]. These can be directly used for extracting the desired time-domain current and voltage profile of a task. Thus, load current information can be obtained in a digital form, which can be used in the proposed scheme.

Additionally, load current information can be obtained from 1) the current regulators in LED driving applications and 2) the data bus in PMBus for dc distribution systems. Also the method of load current estimation in [32] can be used. The load step-size information which is required for the proposed tuning can be obtained using any of the above indirect methods. However, a certain degree of inaccuracy can be expected, even using a direct sensing method, and its effect on the optimal gain formulation should be investigated. This issue is thoroughly discussed in the subsequent section.

D. Capacitor Current Control: Indirect Sensing and Estimation

The proposed scheme in Fig. 1 can also be framed as current injection control using the feedback capacitor current $(i_L - i_o)$ in the inner current-loop. However, the outer voltage controller $G_c(z)$ and the objective of optimal gain formulation remain the same as that of the other configuration. Here an undershoot/overshoot in the capacitor current represents the load step-size after a load step-up/down transient is imposed.

Various capacitor current sensing techniques are proposed, such as the use of current transformers [33], non-invasive sensor for indirect capacitor current measurement in [34]–[36]. These methods are useful, which rely on impedance matching.

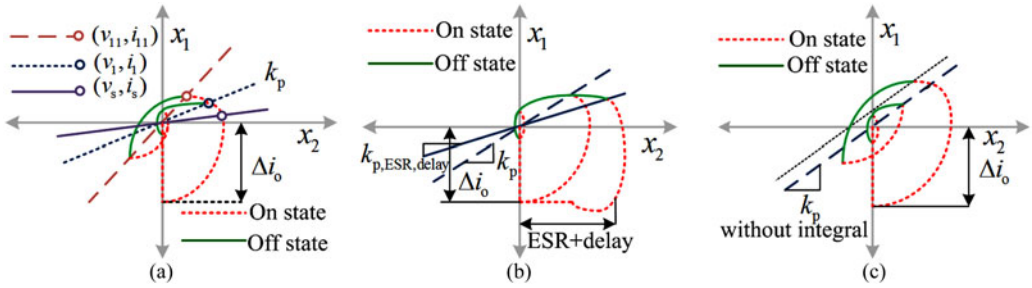

Fig. 2. Phase-plane plots under step load transients with (a) finite sampling effect, (b) ESR and detection delay, and (c) using integral gain throughout.

However, the sensed current may considerably deviate during the initial phase of a large-signal recovery. Capacitor current estimation techniques in [22], [24], [26] can enable high frequency implementation, which require a higher ADC sampling rate and a finite convergence time.

The proposed tuning method can be applied to any of the above configurations to tune the digital voltage controller. However, the use of indirect sensing or estimation methods may lead to inaccuracy in load step-size information, the effects of which are discussed later. The rest of this paper develops a geometric controller tuning approach in a synchronous buck converter under finite hardware resources.

E. Proximate Time Optimal Gain Formulation

Consider the state variables in (1) as $x_1 = i_L - i_o = i_c$ and $x_2 = v_{\rm ref} - v_c$, where i_c is the capacitor current and v_c is the voltage across the capacitor. The output voltage v_o would be the same as the voltage across the capacitor, v_c if the effective-series-resistance (ESR) is ignored; thus the state-space model of a CCM buck converter becomes

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} \\ \frac{-1}{C} & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \frac{u}{L} & 0 & \frac{-1}{L} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{\rm in} \\ i_o \\ v_{\rm ref} \end{bmatrix}. \tag{2}$$

If the control signal u is set to "logic 1," the high-side MOSFET is turned ON; otherwise, the switch is turned OFF. The state-space solutions for the former and the latter represent the ON- and the OFF-state trajectories, and a general form becomes

$$Z_c^2 \int_{i_i}^{i_f} x_1 dx_1 + \int_{v_i}^{v_f} (x_2 + u v_{\rm in} - v_{\rm ref}) dx_2 = 0 \tag{3}$$

where i_k and v_k are initial/final conditions of x_1 and x_2, respectively; $Z_c = \sqrt{L/C}$ is the characteristic impedance. The index "k" corresponds to either an initial condition index "i" or a final condition index "f". Using (3), the general solution can thus be obtained as

$$\begin{aligned} F_i(v_i, i_i) &= F_f(v_f, i_f), \\ F_k(v_k, i_k) &= \frac{{i_k}^2}{2} + \frac{v_k^2}{2Z_c^2} + \left[\frac{u v_{\rm in}}{Z_c^2} v_k - \frac{v_{\rm ref}}{Z_c^2} v_k \right]. \end{aligned} \tag{4}$$

1) Step-Up Transient: Consider a load step-up transient in Fig. 2(a). The trajectory moves along the on-state trajectory starting from an initial vector $(0, -\Delta i_o)$. After intersecting σ in (1) at (v_1, i_1), it follows the off-state trajectory to reach the final condition $(0, 0)$. After a step-up transient is imposed, instantaneous load current becomes $i_o = i_{o1} + \Delta i_o$. Thereafter, using (4), the on-state and the off-state trajectories can be obtained [1], which are simplified as

$$\begin{aligned} i_1 &= \frac{\Delta i_o}{2v_{\rm in}} \lambda_{\rm up}, \quad v_1 = \frac{\Delta i_o^2 {Z_c}^2}{2v_{\rm in}} \\ \text{where} \quad \lambda_{\rm up} &= \sqrt{4 v_{\rm in} v_{\rm ref} - \Delta i_o^2 {Z_c}^2}. \end{aligned} \tag{5}$$

The effects due to the finite voltage-loop sampling and the transient detection delay need to be considered. After the on-state trajectory intersects σ in (1) at (v_1, i_1), the finite voltage loop sampling may introduce a delay before the off-state trajectory becomes active. Considering $T_{v,s}$ to be the worst-case delay, the initial conditions for the off-state trajectory are derived as

$$i_{11} = i_1 + m_1 T_{v,s}, \quad v_{11} = v_1 - \frac{T_{v,s}}{C} \left(\frac{\Delta i_o \lambda_{\rm up}}{2v_{\rm in}} + \frac{m_1 T_{v,s}}{2} \right) \tag{6}$$

where m_1 is the rising slope of i_c. It is apparent from Fig. 2(a) that a delay would result in extra overshoot and undershoot, and this would deviate from the optimal recovery condition. However, this can be adjusted by decreasing the slope of σ such that the on-state trajectory will intersect at (v_s, i_s) as

$$i_s = i_1 - m_1 T_{v,s}; \; v_s = v_1 + \frac{T_{v,s}}{C} \left(\frac{\Delta i_o \lambda_{\rm up}}{2v_{\rm in}} - \frac{m_1 T_{v,s}}{2} \right). \tag{7}$$

Above expression implies a conservative choice, which would avoid any additional overshoot/undershoot. During a large-signal recovery, the integral action can be disabled, i.e., $k_i = 0$; thus using (7), $\sigma = 0$ in (1) gives rise to

$$\sigma = -i_s + k_p v_s = 0. \tag{8}$$

From (7) and (8), the optimal gain k_p can be derived as

$$k_p = \frac{\left(\frac{\Delta i_o}{2v_{\rm in}} \lambda_{\rm up} - m_1 T_{v,s} \right)}{\frac{\Delta i_o^2 Z_c^2}{2v_{\rm in}} + \frac{T_{v,s}}{C} \left(\frac{\Delta i_o}{2v_{\rm in}} \lambda_{\rm up} - \frac{m_1 T_{v,s}}{2} \right)}. \tag{9}$$

Thus, the optimal gain k_p is a function of the input/output voltage, the sampling time, and Z_c. This can be computed offline and stored using lookup tables (LUTs) along with the other necessary parameter information.

The current overshoot $i_{\rm os}$ and the voltage undershoot $v_{\rm us}$ during load step-up transient can be derived using (5)–(8) as

$$i_{\rm os} = \Delta i_o \lambda_{\rm up}/2v_{\rm in}; \quad v_{\rm us} = v_{\rm ref} - v_{\rm in} + \gamma$$
$$\gamma = \sqrt{(v_{\rm in} - v_{\rm ref})^2 + \Delta i_o^2 Z_c^2}. \tag{10}$$

2) Step-Down Transient: In a pulse-width modulated dc–dc converter under trailing edge modulation, a turn-off to turn-on transition occurs in synchronism with the rising edge of the switching clock. This makes it difficult to directly optimize the (load) step-down transient response. However, an attempt to optimize k_p would certainly improve the performance over the previously optimized k_p during a load step-up transient. Consider a load step-down transient with an initial load current of $i_{o1} + \Delta i_o$ and a step size of Δi_o. Then, the optimal gain can be derived using the similar methodology. After detecting a (step-down) transient, the converter trajectory moves along the off-state path from the initial vector $(0,\ \Delta i_o)$, and then, changes to the on-state trajectory after intersecting σ to reach the final condition $(0,\ 0)$. After a load step-down transient is imposed, instantaneous load current becomes $i_{o1} - \Delta i_o$. Thereafter, considering the finite (voltage-loop) sampling effect, the on-state and off-state trajectories can be obtained using (4), which are simplified as

$$i_{22} = i_2 - m_2 T_{v,s}, \quad v_{22} = v_2 + \frac{T_{v,s}}{C}\left(\frac{\Delta i_o \lambda_d}{2v_{\rm in}} + \frac{m_2 T_{v,s}}{2}\right)$$
$$\text{where} \quad i_2 = -\frac{\Delta i_o}{2v_{\rm in}}\lambda_d; \quad v_2 = -\frac{\Delta {i_o}^2 {Z_c}^2}{2v_{in}},$$
$$\lambda_{\rm d} = \sqrt{4v_{\rm in}(v_{\rm in} - v_{\rm ref}) - \Delta i_o^2 Z_c^2} \tag{11}$$

m_2 is the falling slope of i_c. Similar to a load step-up transient, a delay due to the finite voltage-loop sampling can be compensated by decreasing the slope of σ; thus the intersecting point (v_{s1}, i_{s1}) of the off-state trajectory will be modified as

$$i_{s1} = i_2 + m_2 T_{v,s};\ v_{s1} = v_2 - \frac{T_{v,s}}{C}\left(\frac{\Delta i_o \lambda_d}{2v_{\rm in}} - \frac{m_2 T_{v,s}}{2}\right). \tag{12}$$

If the integral action is disabled during a large-signal recovery, using $\sigma = 0$, (1) can be rearranged as follows:

$$\sigma = -i_{s1} + k_p v_{s1} = 0. \tag{13}$$

From (12) and (13), the optimal gain k_p can be derived as

$$k_p = \frac{\left(\frac{\Delta i_o}{2v_{\rm in}}\lambda_d - m_2 T_{v,s}\right)}{\frac{\Delta i_o^2 {Z_c}^2}{2v_{\rm in}} + \frac{T_{v,s}}{C}\left(\frac{\Delta i_o}{2v_{\rm in}}\lambda_d - \frac{m_2 T_{v,s}}{2}\right)}. \tag{14}$$

The current undershoot and output voltage overshoot during a load step-down transient can be derived using (11)–(14) as

$$i_{\rm us} = \frac{\Delta i_o}{2v_{\rm in}}\lambda_d; \quad v_{\rm os} = \sqrt{{v_{\rm ref}}^2 + \Delta i_o^2 Z_c^2} - v_{\rm ref}. \tag{15}$$

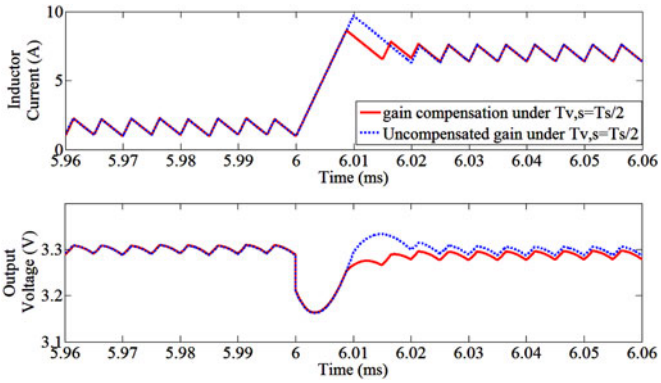

Fig. 3. Load transient response of a synchronous buck converter using the proposed scheme, highlighting the finite voltage-loop sampling effects.

F. Effects of Finite Sampling and Transient Detection Delay

Consider the nominal parameter set for the synchronous buck converter as: $T_s = 5\,\mu$s, i.e., $f_s = 200$ kHz, $i_o \in [1\,A,\ 7\,A]$, $v_{\rm in} \in [8\,{\rm V},\ 12\,{\rm V}]$, $v_{\rm ref} = 3.3$ V, $L = 10\,\mu$H, $C = 570\,\mu$F, the capacitor ESR $r_c \cong 10\,{\rm m}\Omega$, and the inductor dc resistance $r_L \cong 2.2\,{\rm m}\Omega$. The same parameter set has been considered for simulation as well as experimental studies.

It can be found from (9) and (14) that beside the operating point dependency, the voltage-loop sampling has a strong influence on k_p, which can be accounted by a conservative choice of gain. The use of uniform sampling at the same rate of the switching frequency would introduce a delay. This cannot be longer than the switching period in worst case, which can be compensated by a conservative gain choice using (9) and (14) by setting $T_{v,s} = T_s$. Thus, a high-sampling A/D converter is not needed. Interestingly, an existing high-frequency DPWM architecture would further reduce the worst-case delay because of a smaller switching period, and the proposed tuning method will be useful. A comparative (simulation) study in Fig. 3 demonstrates near time-optimal recovery under finite voltage-loop sampling, which can be achieved by a suitable gain choice using (9) in comparison with ideal gain choice using (16).

A similar delay may be expected while detecting a (step) transient, as the load current is uniformly sampled. Also the pulse-width-modulator can introduce a delay due to the modulation mechanism, which would result in extra voltage and current overshoots/undershoots. The effects due to this detection delay can be compensated by modifying the initial conditions in Fig. 2(a) during step-up and step-down transients as $[(\Delta i_o T_s/C), -\Delta i_o]$, $[-(\Delta i_o T_s/C),\ \Delta i_o]$, respectively. Then, the similar methodology in Section II-E1 can be extended to accordingly modify the optimal value of k_p. The effect of delay in transient detection is shown in Fig. 2(b) on phase plane, with gain $k_{\rm p,ESR,delay}$ derived based on above initial conditions. If the sampling-induced delay and transient detection are neglected, the overall optimal value of k_p can be written using (9) and (14) as

$$k_p = \frac{\lambda}{\Delta i_o Z_c^2}; \quad \lambda = \left\{\begin{array}{ll} \lambda_{\rm up}, & \text{for step-up} \\ \lambda_d, & \text{for step-down} \end{array}\right\}. \tag{16}$$

Conventional small-signal model-based tuning methods require to initiate certain online steps to compute tuning parameters for a given operating point. This takes considerable amount of time, and such tuning parameters may not be readily applicable for a large load disturbance. The proposed method analytically computes the optimal gain k_p using instantaneous values of $v_{\rm in}$, $v_{\rm ref}$, Δi_o, Z_c, and F_s. This helps to reduce computational resource requirements and time overhead. Also the performance optimization can be extended much beyond the local neighborhood of an operating point.

III. Robustness and Stability Analysis

A. Effect of Offset in Load Current Information

In practice, a certain degree of inaccuracy exists, while extracting the load-step information using direct load current sensing or indirect methods as discussed in Section II-C. Similarly, indirect capacitor current sensing or estimation methods (in Section II-D) may lead to inaccuracy. Thus, it is important to analyze the robustness of the optimal gain computation by adding an offset current $i_{\rm off}$ with the load current i_o. The switching surface in (1), with $k_i = 0$ is modified as

$$k_p(v_{\rm ref} - v_o) - i_c \pm i_{\rm off} = 0. \tag{17}$$

The instantaneous load current after the transient is $i_o \pm i_{\rm off}$; thus the load step size can be modified to $\Delta i_o \pm i_{\rm off}$, and the optimal gain in (16) will be modified as

$$\begin{aligned} k_p &= \frac{\lambda}{(\Delta i_o \pm i_{\rm off})Z_c^2}; \quad \lambda = \left\{ \begin{array}{ll} \lambda_{\rm up}, & \text{for step up} \\ \lambda_d, & \text{for step down} \end{array} \right\} \\ \lambda_{\rm up} &= \sqrt{4v_{\rm in}v_{\rm ref} - (\Delta i_o \pm i_{\rm off})^2 Z_c^2} \\ \lambda_d &= \sqrt{4v_{\rm in}(v_{\rm in} - v_{\rm ref}) - (\Delta i_o \pm i_{\rm off})^2 Z_c^2}. \end{aligned} \tag{18}$$

Thereafter, the effect of sampling and delay in transient detection can also be included, by replacing Δi_o with $\Delta i_o \pm i_{\rm off}$ in (9) and (14) for step-up and step-down transients, respectively. The variation in the optimal gain for a given variation in the offset load current is computed as

$$\frac{\partial k_p}{\partial i_{\rm off}} = \frac{\mp 1}{\lambda} + \frac{\mp \lambda}{(\Delta i_o \pm i_{\rm off})^2 Z_c^2}. \tag{19}$$

For the nominal parameter set as given in Section II-F, the above analysis shows that the optimal gain deviates by 0.2% from its nominal value for a 10% deviation in the offset load current. Thus, the proposed method closely retains the proximate time optimality in presence of errors in load current information. Further, the integral gain is enabled during steady state to minimize the steady-state error.

B. Effect of Integral Gain During Transient

The magnitude of the discrete time integral gain of a practical design is generally much smaller than that of the proportional gain; thus the latter primarily drives the large signal recovery. The job of the integral action is to rather minimize the steady-state error, and to keep it within the zero-error bin. The use of an integral gain during a transient recovery would make the switching surface in (1) to be nonlinear and introduce an explicit time-dependent memory element. Thus, it is difficult to analytically derive the optimal gain k_i using phase-plane geometry. The switching surface in (1) with $k_i \neq 0$ is written in mixed-signal representation as

$$k_p(v_{\rm ref} - v_o[n]) + u_{\rm int}[n] - i_c = 0 \tag{20}$$

where the integral term $u_{\rm int}[n]$ can be implemented as

$$u_{\rm int}[n] = u_{\rm int}[n-1] + k_i T_s(v_{\rm ref} - v_o[n]). \tag{21}$$

From (20) and (21), it can be found that

$$(k_p + k_i T_s)(v_{\rm ref} - v_o[n]) + u_{\rm int}[n-1] - i_c = 0. \tag{22}$$

From (22), the time varying offset term $u_{\rm int}[n-1]$ would introduce extra overshoots/undershoots [also evident from Fig. 2(c)], which can be compensated by reducing the optimal proportional gain, as discussed in Section II-E1. A switching surface implemented in (20) and (21) will provide an antiwindup arrangement by setting a saturation limit on $u_{\rm int}$. In this proposed scheme, the integral action is disabled during a large-signal recovery, which needs to be reinitiated close to the new operating point. Thus, an additional activation/deactivation arrangement is considered as follows:

$$\sigma = k_p\,(v_{\rm ref} - v_o[n]) + q u_{\rm int}[n] - i_c. \tag{23}$$

This provides an extra flexibility to completely disable the integral action, and also to store the value of $u_{\rm int}[n-1]$ in the memory for future use. This can be used as the initial condition after reinitiating the integral action, which attempts to prevent an integrator wind up. A voltage hysteresis band $\Delta v_{\rm th}$ can be used to detect a small-signal and/or a large-signal transient for the activation and/or the deactivation of the integral action.

C. Effect of Resistive Load

Prior analysis was limited to a constant current load. However, it is important to extend the analysis for a resistive load, considering R_1 and R_2 as the load resistances before and after the transient. Here, the output-voltage undershoot/overshoot during a large-signal recovery results in a change δi_o in instantaneous load current, which can be derived using the voltage undershoot $v_{\rm us}$ in (10) as

$$\delta i_o = v_{\rm us}/R_2 = (v_{\rm ref} - v_{\rm in} + \gamma)/R_2 \tag{24}$$

$$\delta i_o/\Delta i_o = (v_{\rm ref} - v_{\rm in} + \gamma)R_1/v_{\rm ref}(R_1 - R_2) << 1 \tag{25}$$

where $\gamma = \sqrt{(v_{\rm in} - v_{\rm ref})^2 + \Delta i_o^2 Z_c^2}$. The above analysis shows that in a well-designed converter, the deviation in load current is insignificant with respect to the load step size; thus the time optimality conditions for a constant current load will be preserved for a constant resistive load. This argument will also be consistent for a load step-down transient.

D. Effect of Capacitor ESR on Time Optimality

In a practical converter, the capacitor ESR r_c plays a crucial role in performance and stability of the converter, particularly at a higher frequency range. Thus, it is important to analyze

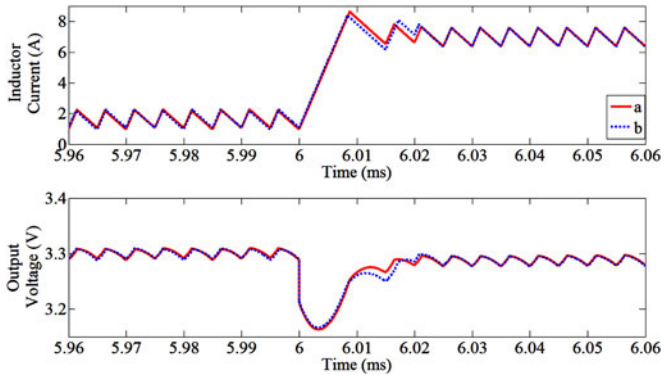

Fig. 4. Simulation results highlighting the ESR effects: (a) and (b) are related to gains computed with and without considering the ESR.

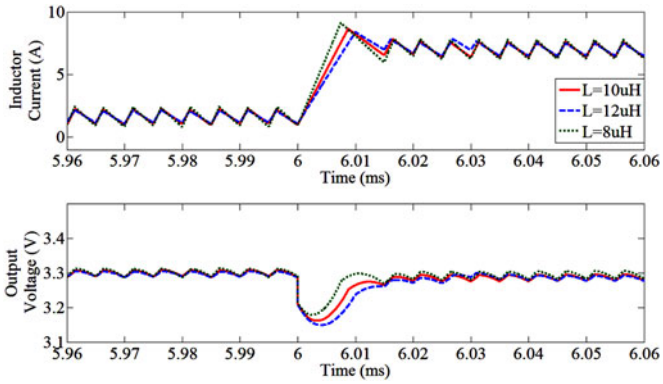

Fig. 5. Load transient response of a synchronous buck converter, highlighting the effects of inductor variation using the proposed tuning scheme.

its effects on time optimality and to modify (16) for improving robustness. Considering the same state vector in (2), the output voltage v_o can be written in terms of x_2 as

$$v_o = v_{\rm ref} - x_2 + r_C x_1. \tag{26}$$

During a step-up transient, the on-time trajectory can be formulated using the same equation (3). Because of the ESR-induced voltage jump, the initial conditions in (26) need to be accordingly modified, which can be written as

$$x_{i,1} = -\Delta i_o,\ x_{i,2} = r_C \Delta i_o. \tag{27}$$

However, the final conditions will remain unaltered. Now incorporating both the effects due to the ESR and the finite (voltage-loop) sampling, the modified state vector $(v_{1,c}, i_{1,c})$, at point of intersection of the on-time trajectory and the switching surface σ, can be derived using (4) as follows:

$$i_{1,c} = i_s;\ v_{1,c} = v_s - r_C x_1 \tag{28}$$

where the expression of i_s and v_s can be found in (7). The state vector in (28) can be further simplified as follows:

$$i_{1,c} = i_s;\ v_{1,c} = v_s - r_C[(\Delta i_o/2v_{\rm in})\,\lambda_{\rm up} - m_1 T_{v,s}]. \tag{29}$$

At the intersecting point, the switching surface in (1) becomes

$$\sigma = -i_{1,c} + k_{\rm p,ESR} v_{1,c} = 0. \tag{30}$$

Using (26)–(30), the modified optimal gain can derived as

$$\frac{1}{k_{\rm p,ESR}} = \frac{1}{k_p} - r_c. \tag{31}$$

This shows that the optimal gain $k_{\rm p,ESR}$ is sensitive to the capacitor ESR. Moreover, the gain needs to be increased with the ESR; otherwise, it would result in the slower transient performance as shown in Fig. 4. This is mainly because of the fact that the ESR would introduce an additional damping in the closed-loop system. It is also important to note that

$$r_C < r_{C,\rm crit} = \frac{1}{k_p} \tag{32}$$

where the critical ESR value $r_{C,\rm crit}$ is linked with the worst-case jump $(r_{C,\rm crit} \times \Delta i_o)$ in the output voltage during a load-transient event. Thus, it is desirable that $r_{C,\rm crit} \times \Delta i_o$ should be smaller in magnitude than Δv (voltage undershoot/overshoot) during load step up/down transients with a step-size Δi_o.

Similarly, the optimal gain $k_{p,\rm ESR}$ can be derived for a load step-down transient and Fig. 4 shows the robustness of the optimal gain against the variation in r_C. This shows that proximate time optimal recovery can be achieved by incorporating the ESR effect in the gain computation in (31).

E. Robustness Against System Parameters

The proposed tuning method requires system parameter information. Thus, it is necessary to analyze its effectiveness under parameter uncertainty. Nominal parameter values in Section II-F are considered for gain formulation in (31) during both load step-up and step-down transients. However, the system parameter of a practical converter are expected to vary. If the actual inductance is 20% smaller than the calculated or the rated value, the overshoot/undershoot in the output voltage decreases in the order of 15 mV, but the time-optimal recovery is closely retained as shown in Fig. 5. Similarly, for the actual inductance with a 20% larger magnitude, the voltage overshoot/undershoot increases in the order of 20 mV. A smaller inductance increases the current overshoot, which may saturate the inductor core. An upper limit can be easily set in digital CMC to limit the peak inductor current. However, this would increase the settling time [3], and a tradeoff can be made using an upper current limit and the settling time.

Consider a $\pm 20\%$ variation in the actual capacitance of the buck converter; however, the nominal capacitance value is used for the gain computation. Fig. 6 shows that for a (load) step size of 5.34 A, the voltage overshoot/undershoot increases or decreases in the order of 15 mV for a 20% decrease or increase in the actual output capacitance. Moreover, the proposed tuning closely retains proximate time optimal recovery for a considerable variation of system parameters.

F. Large Signal Stability Analysis

The switching surface in (1) with $k_i = 0$ divides the state space in such a way that the equilibrium points of either of the on-state or the off-state trajectories are located in the other sides of the switching surface. This satisfies the necessary condition

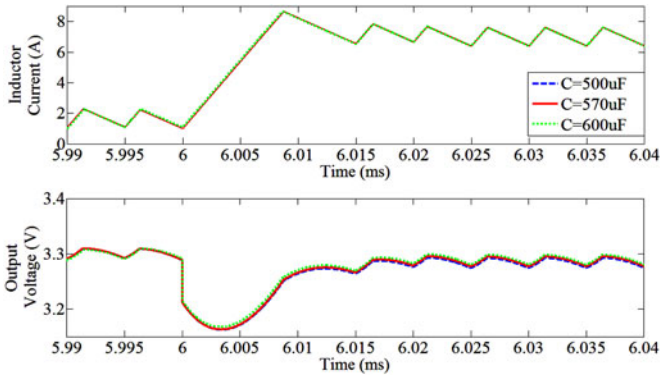

Fig. 6. Load transient response of a synchronous buck converter, highlighting the effects of output capacitor variation using the proposed tuning scheme.

[37]–[40] for large signal stability. Referring Fig. 2, a horizontal switching surface in a buck converter would be in the reflective region and acts as sliding mode control with a slower response time. A vertical surface will be in the refractive region, which would also be stable. Only the surface with a negative slope in Fig. 2 would, however, make a positive feedback system and result in an unstable operation. In the proposed tuning with transformed state variables, the slope was positive over the entire operating range, even considering all the practical aspects. This would remain in the refractive region and ensure large-signal stability [41]. The stability condition for the trajectory to hit the switching surface is $\sigma \frac{d\sigma}{dt} < 0$, and the on-state trajectory needs to satisfy

$$v_{\rm in} - v_{\rm ref} + x_2 > -k_p \frac{L}{C} x_1. \tag{33}$$

For the off-state trajectory, $\sigma \frac{d\sigma}{dt} > 0$ ensures a refractive boundary, while the condition $\sigma \frac{d\sigma}{dt} < 0$ is responsible for a sliding mode operation. Because of time-optimal recovery, the proposed scheme considers the former condition (evident from Fig. 2), and the off-state trajectory should satisfy

$$v_{\rm ref} - x_2 < k_p \frac{L}{C} x_1. \tag{34}$$

Large signal stability can also be ensured for the refractive and reflective modes using direct Lyapunov approach [37]. A transition from the refractive to the reflective or the rejective region will occur, when either the on- or the off-state trajectory is tangential to the boundary, and the condition becomes

$$k_p \frac{dx_2}{dt} - \frac{dx_1}{dt} = 0. \tag{35}$$

The locus of transition points around the operating point $(0, 0)$ can be obtained using (36) and (37) in the on- and the off-states, respectively, as

$$C\left(v_{\rm in} - v_{\rm ref} + x_2\right)\left(v_{\rm ref} - x_2\right) = Lx_1\left(x_1 + i_o\right) \tag{36}$$

$$C(x_2 - v_{\rm ref})(v_{\rm ref} - x_2) = Lx_1(x_1 + i_o). \tag{37}$$

Based on the aforementioned analysis, large-signal stability was found to be satisfied for a wide deviation of the optimal gain, to accommodate the effects due to all practical limitations, for the entire operating region.

IV. Hardware Implementation

A buck converter prototype has been made, and the proposed control is implemented using an (Vertex-5) FPGA device. The nominal parameter set in Section II-F is considered for the experimental investigation. The time period of the FPGA controller clock is taken as $t_{\rm clk} = 10$ ns. For the prototype signal conditioning circuits, two 10-bit differential pipeline A/D converters (AD-9215) are considered for sampling both the output voltage and the load current. However, one ADC would be enough for a stand-alone digital controller which would require an extra analog MUX. The ADC uses a differential amplifier (AD-8138) to convert the single ended output voltage into differential form for the reduction of common-mode noise. The output of the digital compensator $v_c[n]$ is added with the digitized load current $i_o[n]$ (shown in Fig. 1). The output is then converted into an equivalent analog voltage v_A by using a 12-bit D/A converter (AD-9762) followed by a differential amplifier (AD-8130). A high-speed comparator (TLV-3501) is used to compare v_A with the sensed inductor current i_L. The comparator output is then latched, and the dead-time circuit generates the respective gate signals. A $10\,{\rm m}\Omega$ current sense resistor is used to sense i_L followed by a current sense amplifier (ADM-4073). Although over-rated discrete components are used for the hardware implementation, the design can be substantially optimized for stand-alone (system and IC level) implementation.

The voltage loop is sampled at the rate of twice the switching frequency during large-signal recovery, when the integral action is disabled. Even with $D < 0.5$, sub-harmonic instability was found at steady state, due to the effects of finite sampling, capacitor ESR, and computation delay. At steady state, beside the activation of the integral action, an additional ramp compensation is found to be sufficient to ensure fast-scale stability. In the experimental setup, all the load transient events and the switching frequency clocks are synchronized with respect to the FPGA clock.

For the input voltage range of 8–12 V, the variation of the optimal gain in (31) was found to be insignificant. Thus, k_p has been computed offline for different load step sizes, and the computed gains with respective step sizes are stored using LUTs in the FPGA device.

A. Load Transient Performance: A Comparative Study

1) Relay-Based Tuning: Fig. 7(a) shows the load step-up transient of a buck converter using the relay-based tuning [13]. This results in 100-μs (or 20 cycles) settling time, 260-mV (output) voltage undershoot, and 1.5-A current overshoot.

2) Proposed Tuning: Under the test conditions as in Fig. 7(a), the load transient performance using the proposed tuning is shown in Fig. 7(b). This demonstrates fast transient recovery with 20 μs (or four cycles) settling time, 160-mV voltage undershoot, and 2.5-A current overshoot for a step-up transient. The proposed scheme improves the settling time by nearly five

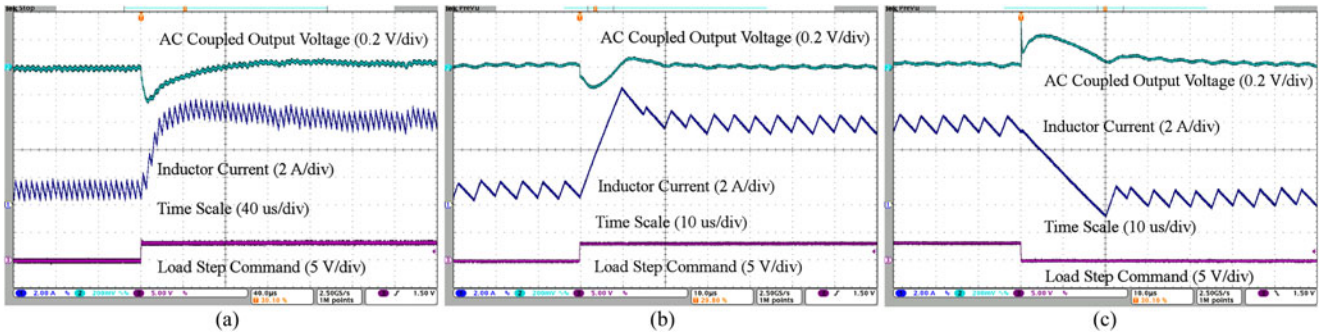

Fig. 7. Load transient response of a synchronous buck converter from 1 to 6 A, and vice-versa at 12 V input: (a) Step-up response using the relay-based tuning; (b) Step-up response using the proposed tuning; (c) Step-down response using the proposed tuning.

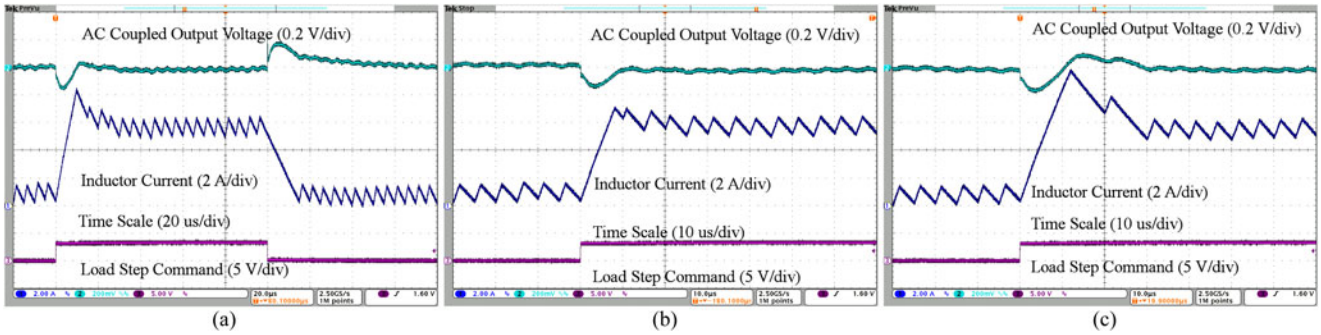

Fig. 8. Load transient response of a synchronous buck converter using the proposed scheme: (a) Considering optimal gain for step-up throughout; (b) Step-up response highlighting the effect for a 20% reduction in optimal gain; (c) Step-up response highlighting the effect for a 20% increase in optimal gain.

fold compared to the relay-based tuning approach [in Fig. 7(a)]. However, the current overshoot increases using the proposed scheme. For a load step-down transient, Fig. 7(c) shows that the proposed tuning results in 20-μs settling time, 220-mV voltage overshoot, and 1.6-A current undershoot. Moreover, the proposed tuning achieves proximate time optimal recovery for both load step-up and step-down transients using respective optimal gains in (9) and (14).

B. Effect of Optimal Gain Variation

It is apparent from (9) and (14) that the optimal value of k_p is sensitive to power circuit parameters which are subject to vary within a tolerable range. For example, the nominal inductance value may decrease as the current flowing through it increases. Thus, k_p which is computed using the nominal parameter set is expected to deviate from its optimal value. It is, therefore, important to investigate the performance using the proposed tuning for a deviation in k_p from its optimal value. Fig. 8(a) shows the load transient response using the optimal gain for step up (9) used throughout. It results in a longer settling time of 30 μs for a step-down transient, as $v_{\rm ref} < (v_{\rm in} - v_{\rm ref})$. Thus, a higher gain is needed for further improvement. Fig. 8(b) shows the load (step-up) transient with a 20% reduction in k_p from its computed value. The performance is more or less optimal. However, a further reduction in k_p would slow down the performance. Similarly Fig. 8(c) shows the load (step-up) transient response for 20% increase in k_p from its computed value. The current and voltage overshoot increases significantly as seen in Fig. 8(c). It is reasonable to consider the gain deviation up to ± 10 % of its computed value, and the proposed tuning was found to retain the proximate time optimal recovery.

C. Effect of Finite Voltage Loop Sampling and Detection Delay

Fig. 9(a) shows the effect of finite voltage loop sampling with $F_{v,s} = 2F_s$ using ideal gain computation in (17). This results in 3.5-A current overshoot and 160-mV voltage undershoot followed by an additional 100-mV voltage overshoot. Compared to Fig. 7(b), the settling time also increases to 30 μs. This is primarily because of ignoring the finite sampling effect in the gain computation in (16). Similarly, Fig. 9(b) shows the effect of delay in transient detection along with sampling effect, where the delay is approximately one switching cycle. Gain computation based on (16) results in 4-A current overshoot, 250-mV voltage undershoot followed by an additional 120-mV voltage overshoot. Incorporating the worst-case switching delay in (9), time-optimal recovery is almost achieved in Fig. 9(c). Fig. 10 shows the load transient performance in a buck converter using the proposed scheme, considering different load steps from 1 to 3.75 to 6 A. Based on the load step size, the optimal values of k_p are selected from the LUTs. The figure justifies that the proposed tuning achieves proximate time-optimal recovery under frequent load-transient events.

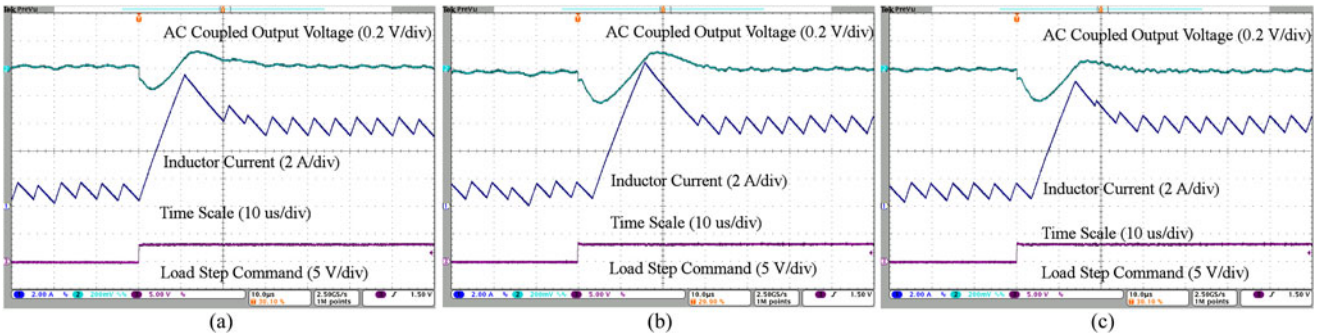

Fig. 9. Load step-up response of a synchronous buck converter using the proposed scheme with $F_{v,s}=2F_s$: (a) Effect of finite voltage-loop sampling using ideal gain computation in (16); (b) Effect of finite sampling and delay in detection using ideal gain computation in (16); (c) Compensating the effects due to sampling and delay by conservative gain choice in (9), considering a worst case delay equal to the switching period.

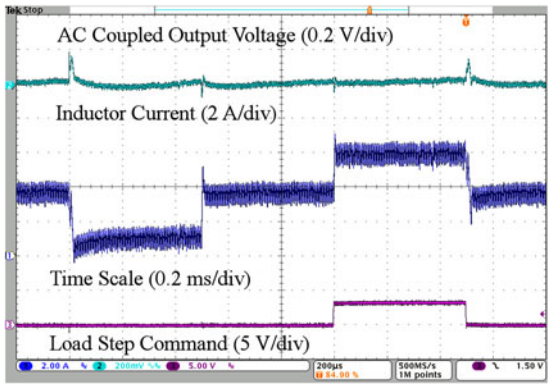

Fig. 10. Load transient response of a synchronous buck converter using the proposed scheme, considering different load steps from 1 to 3.75 to 6 A, and vice-versa at 12 V input.

Above experimental results clearly demonstrate that the proposed tuning can achieve ultrafast recovery using a fixed-frequency modulator, even under the finite voltage-loop sampling, a delay in transient detection, and also in presence of the model uncertainty within an acceptable range.

D. Efficiency

The efficiency of a dc–dc converter is generally considered at steady-state conditions; however, frequent transients can considerably affect the overall efficiency. This is particularly important when the transient step-size increases. Thus, it is important to minimize the switching events during a large-signal recovery. The time-optimal recovery involves one switching action which can drastically reduce the switching and the driver losses. Multiple switching actions using a conventional (small-signal based) tuning method can reduce the overall efficiency. For $v_{\rm in} = 12$ V, $i_o = 5$ A, and the load-step frequency of 1 kHz, the measured efficiency using the proposed tuning was found to be 90.6%, whereas 86.70% efficiency was achieved using the relay-based tuning. The (efficiency) improvement fold using the proposed scheme is expected to further increase with the load-step frequency.

In summary, the proposed approach considers a simple first-order switching surface in [24], which resembles a digitally CMC buck converter with a proportional voltage controller. The objective is to analytically derive the optimal proportional gain which is aimed to achieve near time-optimal recovery using a fixed-frequency PWM controller only. Compared to existing hybrid controllers, the proposed method eliminates the need for additional controllers and extra antiwindup arrangements. The derived gain is a function of load step size, input and output voltages, characteristics impedance, and sampling period. This provides design insights and guidelines for a conservative gain choice under finite hardware resources, time delays, and the capacitor ESR.

V. Conclusion

A geometric tuning method was proposed in a digitally CMC buck converter which uses a PI voltage controller. The proportional gain was analytically derived using the phase-plane geometry, which was able to achieve proximate time optimal load transient recovery. The effects of the finite voltage-loop sampling, the transient-detection delay, and the capacitor ESR were analyzed. A buck converter prototype was made, and the proposed tuning was implemented using an FPGA device. Test results demonstrate significant performance improvement using the proposed tuning over the conventional small-signal-based tuning approach. The proposed method can be extended for other dc–dc converter topologies to achieve proximate time optimal recovery using a fixed-frequency modulator.

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V. Inder Kumar (SM'15) received the B.Tech. degree in electrical engineering from Jawaharlal Nehru Technological University College of Engineering, Hyderabad, India, in 2012, and the M.Tech. thesis work in electrical engineering from IIT Kharagpur, Kharagpur, India, in 2014, where he is currently working toward the Ph.D. degree.

His research interests includes analysis, modeling and nonlinear digital control of dc–dc power converters, and applications to dynamic voltage scaling and RF power amplifier.

Santanu Kapat (M'10) received the M.Tech. and the Ph.D. degrees in electrical engineering from the IIT Kharagpur, Kharagpur, India, in 2006 and 2010, respectively.

From 2009 to 2010, he was a Visiting Scholar with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign. From 2010 to 2011, he was a Research Engineer at GE Global Research, Bangalore, India. Since 2011, he has been with the Department of Electrical Engineering, IIT Kharagpur, where he is an Assistant Professor. His research interests include analysis and design of digital and nonlinear control in switching power converters, and applications to dynamic voltage scaling, RF power amplifier, LED drivers, and dc nanogrid.

Dr. Kapat has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2015.