Letters

Failure Modes of 15-kV SiC SGTO Thyristors During Repetitive Extreme Pulsed Overcurrent Conditions

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***Abstract*—SiC SGTO thyristors are an advanced solution for increasing the power density of medium voltage power electronics. However, for these devices to replace Si thyristor technology in industrial applications their characteristics and failure modes must be understood. This letter presents the failure modes of two 15-kV SiC SGTO thyristors during repetitive overcurrent conditions. The devices were evaluated with 2-kA (3.85 kA/cm^2) square pulses of 100 μs duration using a pulse forming network. Throughout testing, each devices' static characteristics were analyzed for signs of degradation; upon degradation, testing was ceased and the physical failure mode was determined through imaging with a scanning electron microscope (SEM) in conjunction with a focused ion beam. The electrical results demonstrate the failure modes of both SiC SGTO thyristors during pulsed overcurrents electrically manifested themselves as a conductive path through the gate-anode junction and an increased device on-state voltage. SEM imaging revealed one SiC thyristor formed an approximately 10-μm wide cylindrical void, and the second SiC thyristor formed an approximately 200-μm long crack. However, the experimental results demonstrate these 15-kV SiC SGTO thyristors' robust ability to repetitively switch at extreme high current density for tens of thousands of cycles.**

***Index Terms*—Failure modes, pulsed overcurrent, scanning electron microscope (SEM), SiC, thyristor.**

I. Introduction

SiC MOSFETs are well established as a leading option for increasing the power density and maximum thermal operating regime of power electronics [1]–[4]; however, SiC MOSFETs lack conductivity modulation and, therefore, still have significant shortcomings in blocking voltage and conduction current for power electronic applications such as high-voltage dc (HVdc) [5]–[11], medium voltage industrial drives [12], [13], and advanced renewable energy applications such as medium voltage wind turbines [14]–[17]. Modern HVdc back-to-back converters, static var converters, and thyristor-controlled series capacitors currently utilize Si thyristor valves [7], [18]. Advanced HVdc fault protection methods utilize silicon controlled rectifiers (SCRs) or integrated gate-commutated thyristors [5], [19]–[21]. Medium voltage industrial drives (e.g., belt conveyors [12]) and megawatt industrial loads (e.g., dc arc furnaces [22]) are implemented with Si insulated-gate bipolar transistors or thyristor technology [12], [13], [22], [23]. In addition, bidirectional medium and high-power resonant LCL dc–dc converters are being developed with Si thyristors for wide ranging applications [15]. The power density and efficiency of the aforementioned power electronic systems are currently bounded by the inherent material properties of Si. The fundamental limitations of Si result in series stacks or multilevel topologies and a large number of paralleled devices required for adequate blocking voltage and conduction current. SiC super gate turn-OFF (SGTO) thyristors are an advanced solution for increasing the power density and efficiency of medium voltage or megawatt power electronics because of SiC's characteristic wide energy bandgap enabling high-temperature operation, high critical electric field yielding approximately one-tenth the drift region width compared to a Si thyristor for a given blocking voltage, and three times higher thermal conductivity enabling rapid heat extraction. The substitution of established Si thyristor technology with SiC SGTOs would result in significantly fewer devices being required for meeting the previously described blocking voltage and conduction current specifications. Moreover, the devices could be operated at significantly higher junction temperatures with reduced thermal management overhead. Combined the benefits of the SiC SGTO over the current Si technology would result in an increased power density for medium voltage power electronics and high-power industrial applications.

In this letter, two distinct failure modes of SiC SGTO thyristors during pulsed overcurrent conditions are presented for two research grade devices. The devices evaluated are rated for 15 kV/52 A (using 100 A/cm^2 guideline) and labeled devices 1 and 2. The failure modes were determined by individually pulsing each of the devices with approximately 2 kA (3.85 kA/cm^2) 100-µs square pulses at 0.5 Hz in sets of 1000 pulses. The devices' transient characteristics were monitored for signs of degradation during each pulse switching set; between switching sets the devices' static characteristics were measured and analyzed for signs of degradation. After degradation was observed, the devices were imaged using a scanning electron microscope

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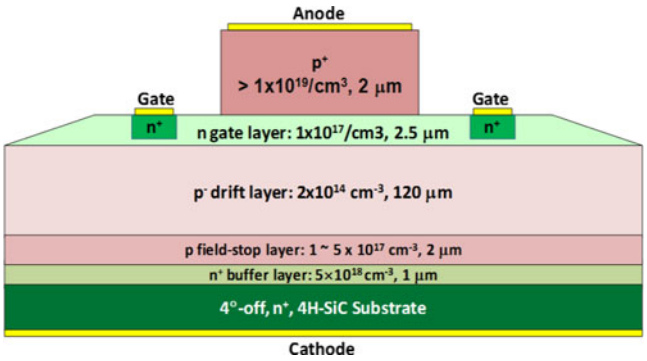

Fig. 1. 15-kV SiC SGTO simplified cross-sectional device structure. Note that the gate is anode referenced in the SiC SGTO as opposed to the gate-cathode reference of Si thyristors.

(SEM) in conjunction with a focused ion beam (FIB) to determine how the failures physically manifested. The experimental data indicated that both SiC SGTOs failed due to the formation of a conductive path through their gate-anode junction, and an increase in on-state voltage. However, the SiC SGTO labeled device 1 failed at 72 000 pulses with a gradual increase in on-state voltage of approximately 4.7% over the last 22 000 pulses, while device 2 failed with a rapid on-state voltage change of 12% during the middle of pulse number 42 898. SEM imaging revealed that device 1 failed because of the formation of a 10-μm wide void that extended down into the p-epitaxy layer at the edge of an anode mesa, and device 2 failed because of the formation of a crack that penetrated down into the p-epitaxy layer under an anode boding wire. However, these results demonstrate the SiC SGTOs' robust ability to withstand pulse overcurrent conditions common in commercial applications.

II. Device Structure and Fabrication

The SiC SGTO thyristors were fabricated by Cree (now Wolfspeed) with a chip size of 1.05 cm^2 and an active conducting area normalized to the anode mesa of 0.52 cm^2. The "S" refers to the highly interdigitated gate-anode regions that enable high turn-on di/dt, and the "GTO" refers to the ability to turn the device off by control of the gate and not strictly by line commutation of the anode–cathode current. Additional information about the SiC SGTO fabrication and switching characteristic versus the silicon SCR can be found in [24] and [25]. A simplified cross-sectional device structure of the 15-kV SiC SGTO is shown in Fig. 1.

III. Test Setup and Procedure

A ten stage 0.5-Ω pulse forming network (PFN) was designed and built for determining the long-term reliability and failure modes of advanced power semiconductor switches during pulse overcurrent conditions [26]. The PFN generates a 100 μs, 2 kA (3.85 kA/cm^2) current pulse that simulates various overcurrent fault conditions of medium voltage converters or high-power industrial loads, where fault resilience and long-term reliability are requirements [12]. An overview of the tests performed is shown in Table I. The pulses were applied at

TABLE I
OVERVIEW OF TESTS PERFORMED

Device ID	Pulses	Freq. (Hz)	Current (kA)	Failure
Device 1	72 000	0.5	2	Gate
Total: 72 000 pulses				
Device 2	42,898	0.5	2	Gate
Total: 42 898 pulses				

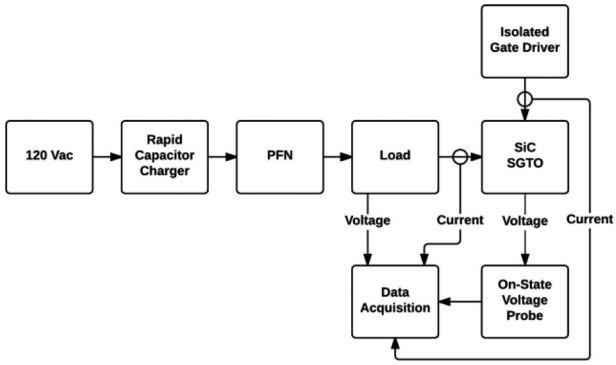

Fig. 2. Simplified block diagram of the system used for determining the failure modes of 15-kV SiC SGTO thyristors during pulsed overcurrent conditions. A detailed description of the system can be found in [26].

0.5 Hz to allow the device to return to room temperature after each pulse by minimizing the average power dissipation. The current amplitude was chosen to be approximately 2 kA based off of prior work that determined the pulsed overcurrent safe operating area of a prior generation of SiC SGTOs [27]. The devices were trigger with a gate-anode current of 0.5 A. The transient waveforms gathered during the current pulses include the anode–cathode voltage, anode–cathode current, gate-anode current (device triggering current), and on-state voltage. The anode–cathode voltage is measured with an Agilent Technologies N2891A 70 MHz differential probe; the anode-cathode current is measured with a Power Electronic Measurements Rogowski type CWT 15B with a sensitivity of 2.00 mV/A; the gate-anode current is measured with a Pearson Current Monitor model 2877 with an output of 1.0 V/A; the on-state voltage of the device is accurately measured with an active high-voltage saturation probe as described in [28]. Specifics about this unique system can be found in [26], and [29] and a simplified block diagram of the power stage and data acquisition is shown in Fig. 2. Throughout testing, the device under test is removed from the high energy testbed and its static characteristics are measured with an Agilent Technologies B1505A Power Device Analyzer/Curve Tracer. The static characteristics measured include device forward conduction, gate-anode forward conduction, and gate-anode reverse leakage. The procedure of switching the device with approximately 2 kA, and then measuring the devices' static characteristics allows for subtle degradation to be captured. After degradation occurred, the die was removed from the package using CEE BEE C-105NC and then imaged with a Carl Zeiss Crossbeam 540 FIB-SEM Microscope.

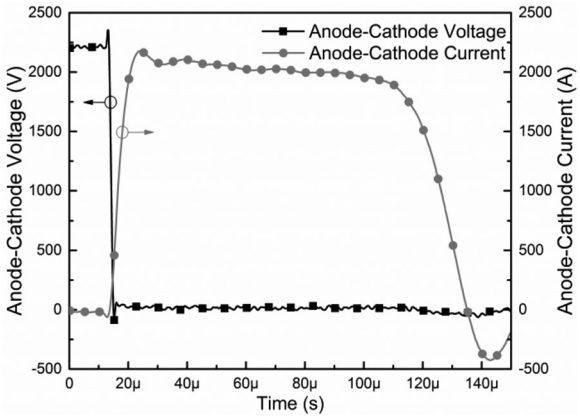

Fig. 3. Example 2 kA PFN discharge through the SiC SGTO labeled device 1.

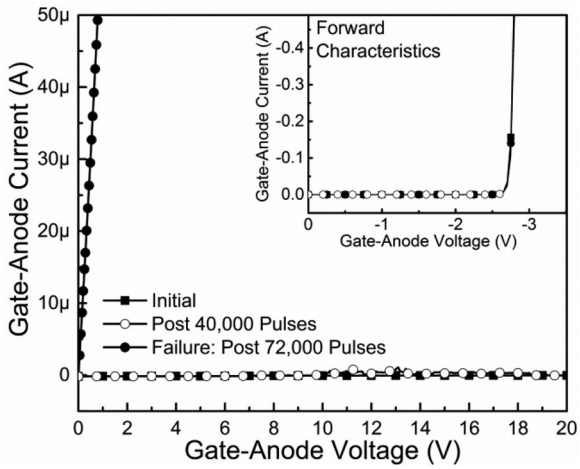

Fig. 4. Gate-anode static characteristics of device 1 measured throughout testing. The main plot displays the reverse characteristics and the subplot displays the forward characteristics. The reverse characteristics show that a resistive path formed through the anode-gate junction after pulse number 72 000; the subplot shows that the forward characteristics remained consistent.

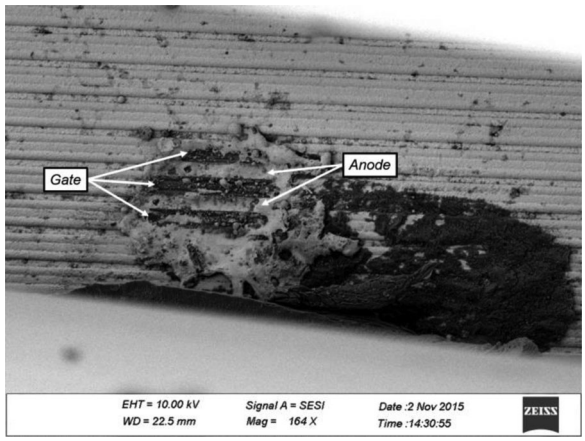

Fig. 5. SEM image of the surface of device 1 at the failure location. The metal overlayer melted back leaving the gate-anode regions exposed. The failure location is directly next to an anode bonding wire seen slightly out of focus across the bottom of the image. The exact dimension scale is proprietary to the manufacturer and not displayed in this image.

IV. Results and Discussion

The previously described electrical system, SEM, and FIB were utilized to determine the electrical and physical failure modes of 0.52 cm^2 15 kV SiC SGTO thyristors during pulsed overcurrent condition. An overview of the tests performed is shown in Table I, and an example 2-kA PFN discharge through device 1 is presented in Fig. 3. The overview provided in Table I shows that device 1 was pulsed 72 000 times with the electrical failure occurring in the gate-anode junction while device 2 failed after 42,898 pulses with the failure again occurring in the gate-anode junction. This section will overview the electrical and physical failure mode for each of the SiC SGTO thyristors, starting with device 1.

The SiC SGTO labeled device 1 failed after 72 000 pulses with a gradual increase in on-state voltage and the formation of a conductive path through the gate-anode junction. The on-state voltage of device 1 during the 2-kA pulses increased by 4.7% from a nominal value of 17.2 V measured at 50 μs into pulse 50 000 to 18 V during pulse number 72 000. The on-state voltage change of only 4.7% is not a significant problem from a system perspective; however, it is indicative of a physical change occurring within the semiconductor material or packaging. Fig. 4 shows the static characteristics of the gate-anode junction during reverse and forward bias measured initially, after 40 000 pulses, and after 72 000 pulses. The reverse bias characteristics shown in Fig. 4 demonstrate that a resistive path formed through the gate-anode junction after 72 000 pulses, but the forward characteristics shown in the subplot remained constant throughout testing.

Testing was ceased after measuring the degradation seen in the reverse bias characteristics of device 1 shown in Fig. 4. After removing the die from the package, the physical failure point was located using SEM analysis of the device surface. Fig. 5. shows an SEM image of the device surface at the point of failure directly next to an anode bonding wire; the metal overlayer is melted back in a "crater like" manner leaving the gate-anode regions exposed. After pinpointing the degradation location, the FIB was utilized to cut into the interior of the device to reveal the physical failure mode. Fig. 6. displays the cylindrical void that was uncovered by the FIB in the middle of the crater. The void starts at the top of an anode mesa, next to a gate bonding region, and extends down through the gate n layer into the p-epitaxy layer. It is hypothesized that current crowding at this location caused extreme localized high current density which melted the SiC material. Upon cooling, the SiC resolidified creating a hollow void. The walls of the void consist of damaged SiC crystal bonds, or dangling bonds, that supported the charge transport seen in the reverse bias characteristics of the gate-anode junction as shown in Fig. 4.

The SiC SGTO labeled device 2 failed after 42 898 pulses because of the formation of a conductive path through the gate-anode junction and an abrupt increase in device on-state voltage. The on-state voltage of device 2 increased by 12% from the nominal value of 18.3–20.5 V over a time period of 11.8 μs during the middle of pulse 42 898. Fig. 7 shows the static characteristics of the gate-anode junction during reverse and forward bias measured initially, after 30 000 pulses, and after the failure

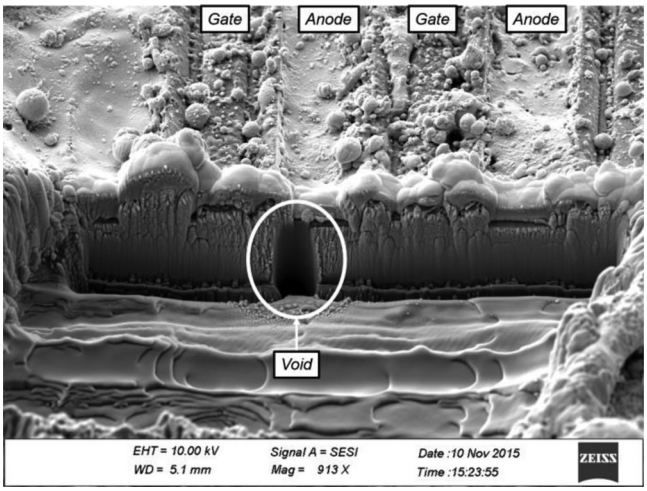

Fig. 6. SEM image of device 1 taken after the FIB uncovered a hollow void at the edge of an anode mesa. The void punches through the gate-anode pn junction and the dangling bonds at the edges of the void supported the charge transport seen in the reverse bias characteristics shown in Fig. 4. It should be noted that the light colored material at the top of the FIB wall is a palladium layer deposited for obtaining a cleaner FIB cut. The exact dimension scale is proprietary to the manufacturer and not displayed in this image.

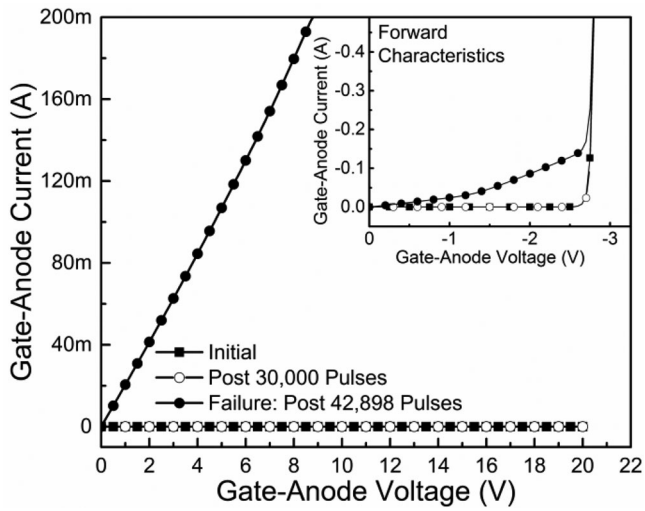

Fig. 7. Gate-anode static characteristics of device 2 measured throughout device testing. The main plot displays the reverse characteristics and the subplot displays the forward characteristics. The reverse and forward characteristics show that a resistive path formed through the anode-gate junction after pulse number 42,898.

pulse, number 42 898. The forward and reverse bias characteristics, shown in Fig. 7, demonstrate that a resistive path formed through the gate-anode junction after pulse number 42 898. The resistive path resulted in significant leakage current during both reverse bias and forward bias prior to pn junction turn-on.

Testing of device 2 was ceased after pulse number 42 898 because of the abrupt increase in on-state voltage and degradation to the device's gate-anode junction characteristics as previously discussed. After removing the die from the package, SEM imaging revealed that the metal overlayer around one of the anode bonding wires had melted. The anode bonding wire pad was

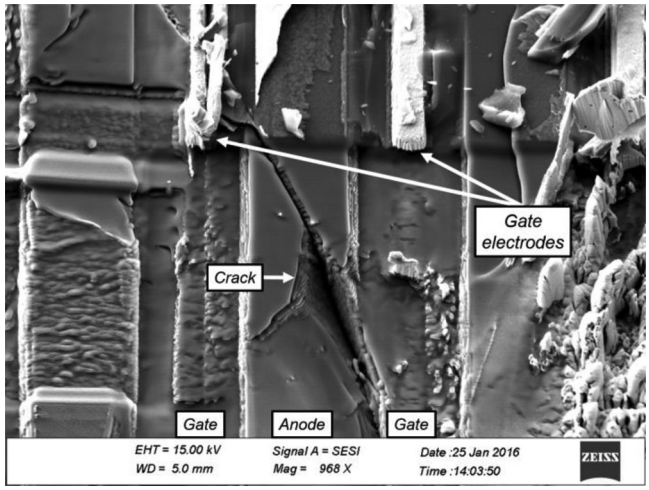

Fig. 8. SEM image of the middle of the crack that occurred under an anode bonding wire pad of device 2. Further FIB and SEM imaging revealed that the crack penetrated through the gate n layer and into the p- epitaxy layer. The exact dimension scale is proprietary to the manufacturer and not displayed in this image.

then removed and the top several micrometers of the device surface in the entire region of where the pad had been located were removed using the FIB to uncover the physical failure mode. Removing the top several micrometers of material exposed a large crack that spread approximately 200 μm across the region, where the anode bonding pad had been located. An SEM image of the middle of the crack is shown in Fig. 8. This figure shows that the crack spread across several gate-anode regions, and disrupted the gate electrodes. Further imaging revealed that the crack penetrated through the gate n layer and into the p-epitaxy layer. The broken bonds of the cracked SiC in this region supported the charge transport seen in the gate-anode characteristics.

Detailed analysis of the underlining mechanisms that resulted in the on-state voltage increase and physical failure modes presented here are outside the scope of this Letter; however, these results serve as a reference for the electrical and physical failure modes of advanced SiC SGTOs during pulsed overcurrents common during power electronic fault conditions. The succinct experimental results and SEM analysis presented here demonstrate that subtle increases ($<$10%) in the on-state voltage of SiC SGTOs indicate physical changes (void or crack formation) within the semiconductor material and foreshadow catastrophic device failure. In addition, these results point to the need for SiC SGTOs to be packaged with bonding wireless techniques because both device failures occurred at anode bonding wire locations. It is hypothesized that advanced packaging techniques may circumvent the failure modes presented here.

V. Conclusion

The failure modes of two SiC SGTO thyristors rated for 15 kV/52 A during extreme pulsed overcurrent conditions were presented. The electrical failure modes were determined through analysis of the devices' transient and static

characteristics, and the physical failure modes were determined through SEM analysis in conjunction with a FIB. Results presented show that both SiC SGTO thyristors lasted through tens of thousands of approximately 2 kA (3.85 kA/cm^2) 100-μs square pulses performed at 0.5 Hz with degradation eventually occurring to the gate-anode junction and device on-state voltage. SEM and FIB analysis revealed that device 1 failed after 72 000 cycles because of the formation of a hollow void directly next to an anode bonding wire that started at the top of an anode mesa and extended through the n gate layer into the p- epitaxy layer; device 2 failed after 42 898 cycles because of the formation of a crack under an anode bonding wire that spread approximately 200 μm across the surface of the device and penetrated through the n gate layer into the p-epitaxy layer. These electrical and physical results serve as a reference for the failure modes of advanced SiC SGTO thyristors, and demonstrate that increases in device on-state voltage foreshadow device failure. Although it is important for power electronic engineers to identify and understand the safe operating area and failure modes of SiC SGTO thyristors, the exceptionally high current density and number of pulses required to induce the failure modes presented here demonstrate that SiC SGTO thyristors offer a robust alternative to the established Si thyristor technology for increasing the power density of medium voltage converters, HVdc applications, and high-power industrial loads.

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