Combined Phase-Shift and Frequency Modulation of a Dual-Active-Bridge AC–DC Converter With PFC

Felix Jauch, *Student Member, IEEE*, and Jürgen Biela, *Member, IEEE*

***Abstract*—This paper presents a combined phase-shift and frequency modulation scheme of a dual–active-bridge (DAB) ac–dc converter with power factor correction (PFC) to achieve zero voltage switching (ZVS) over the full range of the ac mains voltage. The DAB consists of a half bridge with bidirectional switches on the ac side and a full bridge on the dc side of the isolation transformer to accomplish single-stage power conversion. The modulation scheme is described by means of analytical formulas, which are used in an optimization procedure to determine the optimal control variables for minimum switch commutation currents. Furthermore, an ac current controller suitable for the proposed modulation scheme is described. A loss model and measurements on a 3.3-kW electric vehicle battery charger to connect to the 230 V_{rms} / 50-Hz mains considering a battery voltage range of 280–420 V validate the theoretical analysis.**

***Index Terms*—AC–DC Converter, bidirectional, isolated, power factor correction, zero voltage switching.**

I. Introduction

THE power conversion from ac to dc or vice versa has become a fundamental part of the electricity infrastructure since many applications demand either a dc source or a dc sink. Even for electrical machines, ac frontend rectifiers are in place with subsequent inverters driving the machines. In some cases, also galvanic isolation between ac and dc side is needed or even mandatory to be compliant with standards. Isolated ac–dc converters are used for instance for charging electric vehicles, interfacing storage batteries for uninterruptible power supplies or supplying energy from photovoltaic systems to the grid. In order to keep the conducted electromagnetic interference low, the harmonic content of the ac current has to be limited. Furthermore, to reduce losses in distribution grids, a converter equipment should draw mainly active power with a power factor (PF) close to unity.

For isolated power conversion from ac to dc, the conventional approach is a two-stage solution with a boost power factor correction (PFC) rectifier and a subsequent high-frequency isolated dc–dc converter such as a dual-active-bridge (DAB) [1] or a resonant dc–dc converter [2]. Besides this two-stage conversion, several single-stage isolated ac–dc PFC converter topologies have been proposed. A review of state-of-the-art single-phase power quality ac–dc converters is given in [3], whereas [4] summarizes single-phase nonisolated PFC topologies based on the boost converter approach.

A DAB converter topology with a rectified ac line voltage as input is presented in [5]–[7], where modulation schemes for the ac–dc operation under zero voltage switching (ZVS) conditions are derived. Approaches where the DAB is connected directly to the ac line voltage by applying bidirectional switches are given in [8]–[10]. In [10], a modulation scheme that guarantees ac-side zero current switching (ZCS) and dc-side ZVS is presented. The main drawbacks of the modulation are the high transformer peak currents that substantially limit the efficiency of the converter. The operation proposed in [9] allows a three-level pulsewidth modulation on the ac side while achieving either ZVS or ZCS conditions for all switching devices in all points of operation. Nevertheless, through the applied commutation control, the switching frequency and in turn the power density of the converter is rather limited.

In general, several modulation methods like phase-shift modulation, triangular, and trapezoidal current mode modulation [1], [11], [12] have been investigated for the operation of a DAB. Besides the commonly used control variables like phase-shifts and clamping intervals, also the switching frequency is considered to control a DAB in [7] and [13] to boost the efficiency in light-load operation as well as to maintain ZVS conditions in full ac–dc operation.

This paper focuses on the DAB ac–dc converter presented in [14], where bidirectional switches are applied on the ac side. The discussed combined phase-shift and frequency modulation strategy is generalized in this paper so that the control variables are found by an optimization to achieve ZVS over the whole ac mains voltage for minimum commutation currents. Especially with the use of silicon power MOSFETs, hard switching conditions in terms of forced body diode commutations lead to relatively high switching losses (high reverse recovery losses), and therefore, to a reduced efficiency of the converter system. Furthermore, hard switching can lead in the worst case to the destruction of the semiconductor devices. For these reasons, this paper focuses on developing a modulation scheme to allow ZVS for all switches of the DAB at every time instant of the ac mains voltage.

First, in Section II, the DAB ac–dc converter topology is explained. The operating principle in ac-to-dc and dc-to-ac operation including the mathematical analysis of the modulation scheme is discussed in Section III. There, also the derivation of the optimal control variables and the design of an ac input current controller is given. Finally, Section IV shows a hardware prototype system including a detailed loss model and experimental results for validating the theoretical analysis.

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The authors are with the Laboratory for High Power Electronic Systems, ETH Zurich, Zurich 8092, Switzerland (e-mail: jauchf@ethz.ch; jbiela@ethz.ch).

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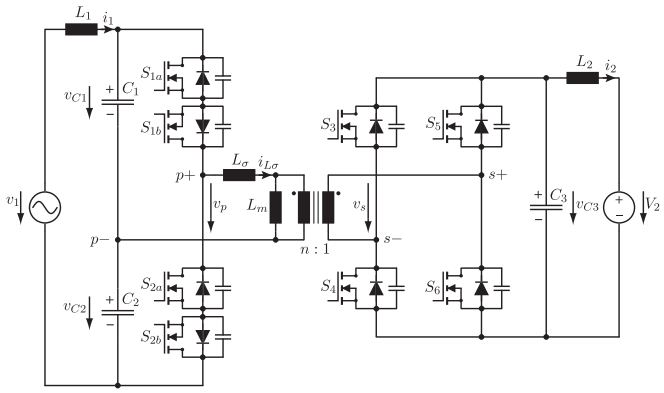

Fig. 1. DAB ac–dc converter with PFC, which applies a combined phase-shift and frequency modulation to guarantee ZVS over the whole ac line period.

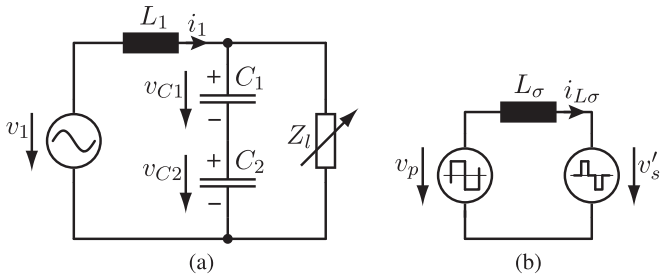

Fig. 2. Equivalent circuits of the DAB converter: (a) with variable impedance load Z_l for representing the behavior of the DAB seen from the mains and (b) for representing phase-shift modulation for controlling the power transfer from the ac to the dc side and vice versa.

II. DAB AC–DC Converter

The schematic of the DAB ac–dc converter is shown in Fig. 1 and has been introduced in [14]. Due to the alternating line voltage, bidirectional switches on the ac side have to be used. These can be realized by an antiserial connection of two MOSFETs/IGBTs as shown in Fig. 1 or by reverse blocking IGBTs.

Compared to the conventional boost PFC approach, the proposed converter filters high-frequency harmonic distortions on the mains due to the inherently integrated *LC* input filter stage. The capacitors C_1 and C_2 absorb the high-frequency switched currents. Nevertheless, the remaining ac voltage ripple on the capacitors leads to a certain degree of high-frequency input-current distortions.

In either power flow direction, the converter can operate in buck or boost mode depending on the transformer turns ratio. For the considered ac-to-dc operation in boost mode in the following, the turns ratio n is chosen such that the primary referred dc voltage $V_2' = nV_2$ is higher than half of the maximum peak voltage of the ac line voltage in every operating point according to

$$nV_2 > \frac{\hat{V}_1}{2}. \tag{1}$$

The boost mode condition has to be fulfilled for the whole battery voltage range and leads to a minimal turns ratio n at the lowest battery voltage V_2. Based on the induced relation of the winding voltages referred to the ac side of the transformer, the transformer leakage inductance current $i_{L\sigma}$ is shaped according to the modulation scheme described in the following to allow ZVS at every switching instant.

III. Modulation and Control

The converter is operated with a combined phase-shift and frequency modulation [14] based on a general trapezoidal current mode modulation of the well-known DAB dc–dc converter [12]. This modulation method is suitable for high power transfer at relatively low peak currents and can be adjusted to achieve ZVS in every switching point as shown later.

A simple equivalent circuit is given in Fig. 2(a), which consists of the *LC* input filter stage and a parallel connected variable impedance load Z_l. The impedance load represents the behavior of the DAB seen from the mains.

By adjusting the control variables of the modulation, and therefore, controlling the power drawn from the mains the impedance load is changing. The converter is operated in such a way, that the reactive power consumed by the filter capacitors is compensated by the variable impedance load in order to achieve PFC.

Fig. 2(b) shows a simplified representation of the converter for phase-shift control. The magnetizing inductance L_m of the transformer is assumed to be much larger than the leakage inductance L_σ and is, therefore, neglected in the following.

The ac-side half bridge is switched with a constant duty cycle of 50%, which leads to equally distributed capacitor voltages v_{C1} and v_{C2}. Neglecting the input inductor L_1, the average value over one switching cycle of v_{C1}, v_{C2} follows the ac line voltage according to

$$v_{C1}(t) = v_{C2}(t) = \frac{\hat{V}_1}{2} \sin(\omega t). \tag{2}$$

Assuming further a negligible small capacitor voltage ripple, the dc-link voltage is $v_{C3} = V_2$ (see Fig. 1) for the following mathematical considerations.

During one half cycle of the ac line voltage, only two of the ac-side switches are switched at high frequency. These are S_{1a} and S_{2a} for the positive and S_{1b} and S_{2b} for the negative half wave. The switches switched at low frequency are turned ON/OFF at nearly zero voltage and zero current at the zero crossing of the ac voltage.

As indicated in Fig. 2(b), on the primary side of the transformer, a square-wave voltage v_p with the time-dependent amplitude $|v_1(t)|/2$ is applied. The voltage v_s on the transformer secondary side consists of positive and negative voltage pulses including a clamping interval with an amplitude of V_2, which allows shaping the transformer leakage inductance current $i_{L\sigma}$ to transfer the desired instantaneous power and to achieve ZVS. The voltage amplitudes of v_p and v_s are assumed to be constant over one switching cycle because the switching frequency is chosen to be well above the mains frequency.

A. AC-to-DC Operation

In ac-to-dc operation, power flows from the mains to the dc side. To describe the combined phase-shift and frequency modulation analytically, the control variables g and w normalized to

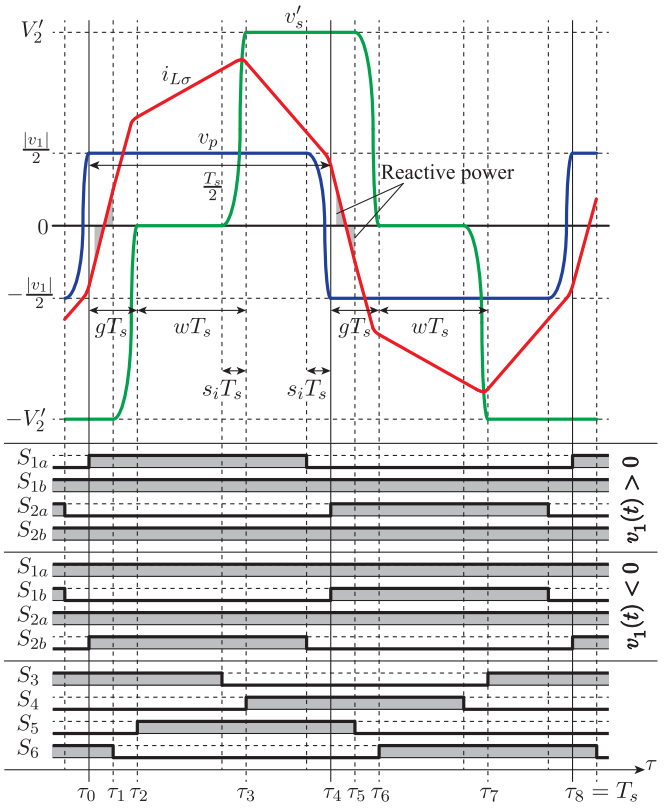

Fig. 3. Primary and secondary transformer voltages v_p, v_s' and transformer leakage inductance current $i_{L\sigma}$ over one switching period T_s in ac-to-dc operation. The gate signals of the ac-side switches differ for a positive and a negative ac line voltage.

the switching period $T_s = 1/f_s$ are introduced. g is the phase shift between the ac side applied square-wave voltage v_p and the dc side applied square-wave voltage v_s' as shown in Fig. 3. w represents the length of the dc-side clamping interval. Moreover, the interlocking interval $t_i = s_i T_s$ is considered, which corresponds to the dead time between the turn-off and the turn-on of a switch in a half bridge. This time interval is taken into account since it leads to a substantial contribution to the power transfer especially at high switching frequencies. In a state machine realization for generating the gate signals for the switches, this interval is usually kept constant so that no external control possibilities exist to adjust it. Therefore, the derivation of the power flow equation incorporates the dead time to improve the converter model from which the control variables g and w are derived for a given reference power.

It is assumed that the resonant transition for a minimum commutation current takes place rather slowly. This means that the voltage change on the transformer winding occurs near the end of the interlocking interval. The assumption coincides with the measurements shown in [15], where the charging behavior of a MOSFETs output capacitance is observed to be not time reciprocal to its discharging behavior.

In Fig. 3, the resulting transformer leakage inductance current $i_{L\sigma}$ and the gate signals of the switches for a positive and a negative mains voltage are given. For the following mathematical analysis, the voltages applied to the transformer windings are assumed to be changing instantaneously (step function) at the end of the interlocking interval and the leakage inductance current is simplified to a linear waveform during that interval.

With the points in time τ_0 up to τ_8 defined according to Fig. 3, the transformer leakage inductance current $i_{L\sigma}$ in ac-to-dc operation is in general modeled by

$$i_{L\sigma}(\tau) = \begin{cases} \frac{\frac{|v_1|}{2}+nV_2}{L_\sigma}(\tau-\tau_0)+i_{L\sigma}(\tau_0) & \tau_0 \le \tau \le \tau_1 \\ \frac{\frac{|v_1|}{2}+nV_2}{L_\sigma}(\tau-\tau_1)+i_{L\sigma}(\tau_1) & \tau_1 \le \tau \le \tau_2 \\ \frac{\frac{|v_1|}{2}}{L_\sigma}(\tau-\tau_2)+i_{L\sigma}(\tau_2) & \tau_2 \le \tau \le \tau_3 \\ \frac{\frac{|v_1|}{2}-nV_2}{L_\sigma}(\tau-\tau_3)+i_{L\sigma}(\tau_3) & \tau_3 \le \tau \le \tau_4 \\ \frac{-\frac{|v_1|}{2}-nV_2}{L_\sigma}(\tau-\tau_4)+i_{L\sigma}(\tau_4) & \tau_4 \le \tau \le \tau_5 \\ \frac{-\frac{|v_1|}{2}-nV_2}{L_\sigma}(\tau-\tau_5)+i_{L\sigma}(\tau_5) & \tau_5 \le \tau \le \tau_6 \\ \frac{-\frac{|v_1|}{2}}{L_\sigma}(\tau-\tau_6)+i_{L\sigma}(\tau_6) & \tau_6 \le \tau \le \tau_7 \\ \frac{-\frac{|v_1|}{2}+nV_2}{L_\sigma}(\tau-\tau_7)+i_{L\sigma}(\tau_7) & \tau_7 \le \tau \le \tau_8 \end{cases} \tag{3}$$

with the values at the points in time

$$i_{L\sigma}(\tau_0) = -\frac{\frac{1}{2}|v_1| + (4g+2w-1)nV_2}{4f_sL_\sigma} \tag{4}$$

$$i_{L\sigma}(\tau_1) = \frac{(2g-2s_i-\frac{1}{2})|v_1| - (2w+4s_i-1)nV_2}{4f_sL_\sigma} \tag{5}$$

$$i_{L\sigma}(\tau_2) = \frac{(2g-\frac{1}{2})|v_1| - (2w-1)nV_2}{4f_sL_\sigma} \tag{6}$$

$$i_{L\sigma}(\tau_3) = \frac{(2g+2w-\frac{1}{2})|v_1| - (2w-1)nV_2}{4f_sL_\sigma} \tag{7}$$

$$i_{L\sigma}(\tau_4) = \frac{\frac{1}{2}|v_1| + (4g+2w-1)nV_2}{4f_sL_\sigma} \tag{8}$$

$$i_{L\sigma}(\tau_5) = -\frac{(2g-2s_i-\frac{1}{2})|v_1| - (2w+4s_i-1)nV_2}{4f_sL_\sigma} \tag{9}$$

$$i_{L\sigma}(\tau_6) = -\frac{(2g-\frac{1}{2})|v_1| - (2w-1)nV_2}{4f_sL_\sigma} \tag{10}$$

$$i_{L\sigma}(\tau_7) = -\frac{(2g+2w-\frac{1}{2})|v_1| - (2w-1)nV_2}{4f_sL_\sigma}. \tag{11}$$

The points in time τ_1 and τ_5 are not necessary for the analytical determination of the power-flow equation. Nevertheless, they are required for calculating the turn-off currents for stating the ZVS conditions as shown later. The allowed intervals of the control variables g and w are given by

$$s_i \le g \le \frac{1}{2} \tag{12}$$

$$0 \le w \le \frac{1}{2} - g. \tag{13}$$

The boundaries for the control variables g and w arise from the applied general trapezoidal current mode modulation [12]

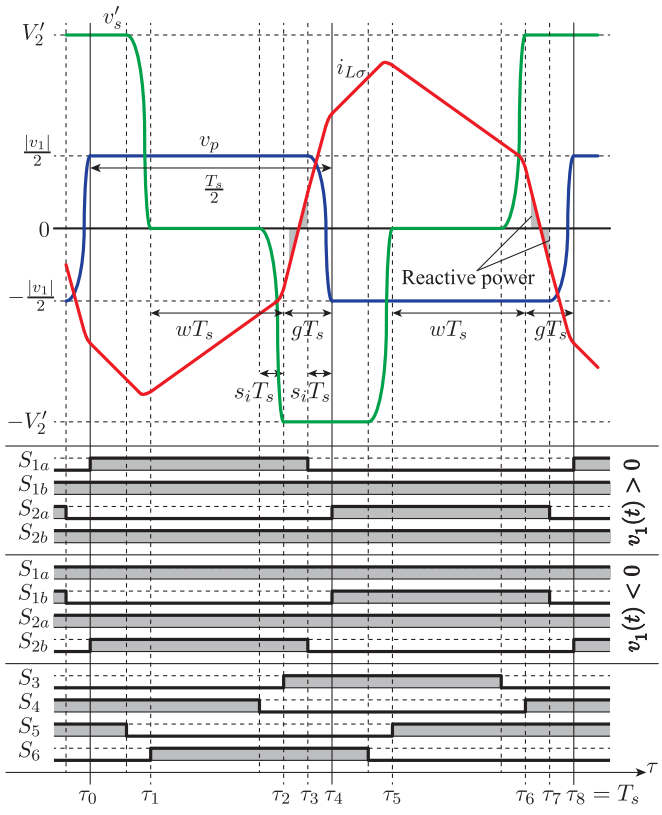

Fig. 4. Primary and secondary transformer voltages v_p, v_s' and transformer leakage inductance current $i_{L\sigma}$ over one switching period T_s in dc-to-ac operation. The gate signals of the ac-side switches differ for a positive and a negative ac line voltage.

and the defined time intervals between the points in time τ_0 up to τ_8 depicted in Fig. 3. With the aforementioned assumption that the applied voltages to the transformer windings change at the near end of the interlocking interval, the lower limit of the phase shift g is given by the constant interval s_i. This limit is reached for $\tau_1 = \tau_0$. The upper limit for g is reached at $1/2$ when the clamping interval w gets zero. This means that the intervals $[\tau_2, \tau_3]$ and $[\tau_3, \tau_4]$ become zero with $\tau_4 = \tau_3 = \tau_2$. Depending on the phase shift g, the length of the clamping interval w reaches its upper limit where the time interval $[\tau_3, \tau_4]$ becomes zero with $\tau_4 = \tau_3$.

Besides the phase shift g and the clamping interval w, also the switching period T_s is considered as a control variable with its limits

$$T_{s,\min} \leq T_s \leq T_{s,\max}. \tag{14}$$

Varying the switching frequency $f_s = 1/T_s$ can lead to substantial improvements of the efficiency of a DAB converter in light-load operation [13]. From a practical point of view, the control variable T_s should be limited within reasonable boundaries. The lower limit of the switching period $T_{s,\min}$ (upper limit of the switching frequency $f_{s,\max}$) is mainly restricted by the switching speed and the switching losses under ZVS conditions of the applied MOSFET device. The upper limit of the switching period $T_{s,\max}$ (lower limit of the switching frequency $f_{s,\min}$) determines the size of the passive components and in turn limits the power density of the converter system. The required core cross section of the transformer is given by the flux excitation at the lowest switching frequency. Moreover, the ac- and dc-side capacitors as well as the filter inductors have to be designed for $f_{s,\min}$ since the current and voltage ripples become substantially greater compared to the operation at $f_{s,\max}$.

The power transferred over one switching cycle T_s from the ac to the dc side can be calculated with the integral $\frac{1}{T_s}\int_0^{T_s} v_p(\tau)\, i_{L\sigma}(\tau)d\tau$ and is given by

$$p_t = \frac{|v_1|\, nV_2\left(2g - 4g^2 + w - 2w^2 - 4\mathrm{gw}\right)}{4f_s L_\sigma}. \tag{15}$$

Setting the derivatives of p_t with respect to g and w to zero, leads to the maximum transferrable power of

$$p_{t,\max} = \frac{|v_1|\, nV_2}{16 f_s L_\sigma} \tag{16}$$

at $g = 1/4$ and $w = 0$.

During the intervals $[\tau_0, \tau_1]$ and $[\tau_4, \tau_5]$, only reactive power is transferred in the shaded areas shown in Fig. 3, which is required for the resonant transition to achieve ZVS. For a positive voltage v_p and as well for a negative voltage v_p, the shaded areas highlight two time intervals where the leakage inductance current $i_{L\sigma}$ exhibits once a negative and once a positive polarity so that the power derived by the integral $\frac{1}{T_1+T_2}\int v_p(\tau) i_{L\sigma}(\tau)d\tau$ over these two time intervals T_1, T_2 gets zero. This means that no active power is transferred during these intervals. The derivation of the control variables by keeping these areas small will be shown later.

B. DC-to-AC Operation

In dc-to-ac operation, power flows from the dc side to the ac side of the transformer, which demands an unequal sign of the applied transformer voltages v_p, v_s and the transformer leakage inductance current $i_{L\sigma}$. Fig. 4 shows the transformer voltages v_p, v_s', the leakage inductance current $i_{L\sigma}$ and the gate signals of the switches for a positive and a negative mains voltage.

The analytical expression of the transformer leakage inductance current $i_{L\sigma}$ in dc-to-ac operation can be determined the same way as in the ac-to-dc operation considering the switching instants from Fig. 4. The power transferred from the dc to the ac side is given by (15) by setting $-p_t$. The same holds for the maximum transferrable power, which is defined by (16) by means of $-p_{t,\max}$.

Again, only reactive power is transferred during the intervals $[\tau_2, \tau_3]$ and $[\tau_6, \tau_7]$ in the shaded areas given in Fig. 4 that is required for ZVS.

C. ZVS Conditions

To achieve ZVS for all switching devices during one half cycle of the mains, the turn-off currents have to be large enough to charge/discharge the drain–source capacitances of the switching devices in a bridge leg. The ZVS conditions for the general trapezoidal modulation scheme described previously and depicted in

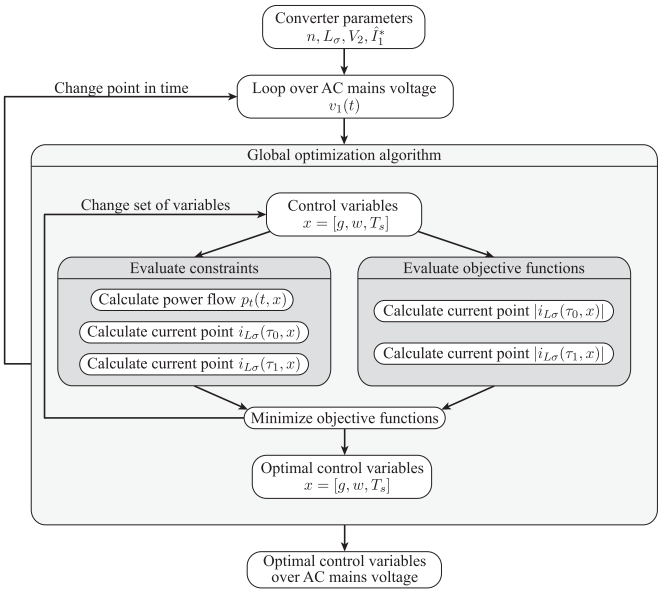

Fig. 5. Flow chart of the optimization algorithm to derive optimal control variables g, w, T_s for ZVS conditions for a given set of converter parameters n, L_σ, V_2 and a reference current amplitude $\hat{I}_1^*$.

Fig. 3 for ac-to-dc operation are given by

$$i_{L\sigma}(\tau_0) < -I_s \tag{17}$$

$$i_{L\sigma}(\tau_1) > I_s \tag{18}$$

$$i_{L\sigma}(\tau_4) > I_s \tag{19}$$

$$i_{L\sigma}(\tau_5) < -I_s \tag{20}$$

where I_s is the minimum commutation current required for the resonant transition during the interlocking interval. With these conditions, ZVS is inherently guaranteed also for the switching instants $\tau_2, \tau_3, \tau_6, \tau_7$ in Fig. 3. In the same way, the ZVS conditions in dc-to-ac operation can be derived. Introducing energy equivalent capacitances $C_{\text{eq},p}$, $C_{\text{eq},s}$ for the parallel connection of the drain–source capacitances of the ac-/dc-side bridge leg, the minimum commutation current can be determined as

$$I_s = \max\left\{\frac{v_1}{\sqrt{\frac{L_\sigma}{C_{\text{eq},p}}}}, \frac{V_2}{\sqrt{\frac{L_\sigma}{C_{\text{eq},s}}}}\right\}. \tag{21}$$

Compared to [14], where the current points have been fixed to the minimum commutation current, a general approach to derive the control variables for ZVS conditions using an optimization is described. This is presented in the next section.

D. Optimal Control Variables

For the combined phase-shift and frequency modulation, there are three degrees of freedom in the modulation scheme. These are the phase shift g, the length of the clamping interval w, and the switching period T_s. At each point of the ac mains voltage, these control variables are derived by minimizing the absolute value of the transformer leakage inductance current $i_{L\sigma}$ at the time instants τ_0 and τ_1 for a minimal commutation current as shown in Fig. 5. In this way, the reactive power (shaded areas in Figs. 3 and 4) that is required for ZVS is kept minimal what in turn results in minimal transformer leakage inductance peak currents.

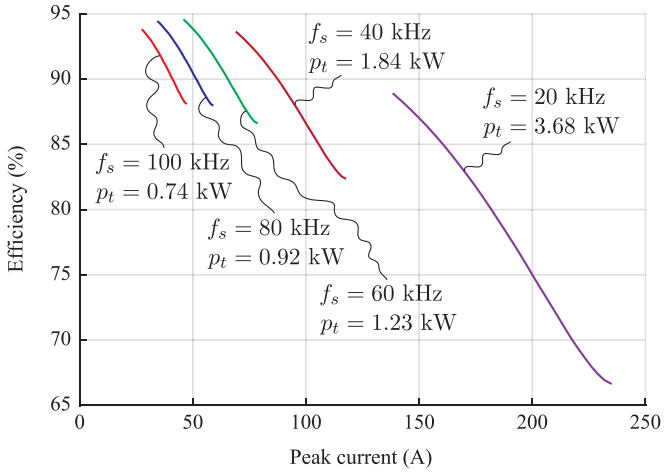

Fig. 6. Converter efficiencies for the prototype system depending on the transformer leakage inductance peak current $i_{L\sigma}(\tau_2)$ for different parameterizations with the switching frequency f_s and the power p_t. The efficiencies are given at the ac voltage amplitude $v_1 = 325$ V and the dc voltage $V_2 = 350$ V at a given dc power operating point p_t.

The minimization of the peak current in every switching cycle leads to the maximum converter efficiency as shown in Fig. 6 for different parameterizations with the switching frequency f_s and the power p_t. There, the efficiencies at the ac voltage amplitude $v_1 = 325$ V and the dc voltage $V_2 = 350$ V are evaluated by iterating over the phase shift $g \in [s_i, 1/2]$ for a constant switching frequency f_s and a given dc power operating point p_t for the prototype system described later. With increasing phase shift g the clamping interval w is decreased to keep the power p_t constant. As the phase shift increases also the leakage inductance peak current $i_{L\sigma}(\tau_2)$ (see Fig. 3) increases and the converter efficiency drops. The starting point of the phase shift where the efficiency exhibits its maximum guarantees that $i_{L\sigma}(\tau_0) < 0$ as well as $i_{L\sigma}(\tau_1) > 0$.

The optimization problem is formulated as

$$\min_x \left(|i_{L\sigma}(\tau_0, x)|, |i_{L\sigma}(\tau_1, x)|\right) \tag{22}$$

with respect to

$$x = \begin{bmatrix} g \\ w \\ T_s \end{bmatrix} \text{ with } x_{\text{lb}} = \begin{bmatrix} s_i \\ 0 \\ T_{s,\min} \end{bmatrix}, \; x_{\text{ub}} = \begin{bmatrix} \frac{1}{2} \\ \frac{1}{2} - g \\ T_{s,\max} \end{bmatrix} \tag{23}$$

where x denotes the vector of control variables, which is restricted to lower and upper bounds $x_{\text{lb}}, x_{\text{ub}}$ respectively. The first constraint is given by the power equality constraint

$$p_t(t, x) = p_t^*(t) \tag{24}$$

with the reference of the instantaneous power $p_t^*(t)$ for a given input current amplitude $\hat{I}_1^*$

$$p_t^*(t) = \hat{V}_1 \hat{I}_1^* \sin^2(\omega t) - \frac{\omega\,(C_1 + C_2)}{4} \hat{V}_1^2 \sin(\omega t)\cos(\omega t). \tag{25}$$

TABLE I
PARAMETERS OF THE HARDWARE PROTOTYPE SYSTEM

Mains voltage	V_1	230 V_{rms} ± 10 %
Mains frequency	$f_g = 1/T_g$	50 Hz
Battery voltage	V_2	280 V...420 V
Output power	P_2	3.3 kW
Switching frequency	f_s	20 kHz...120 kHz
Transformer turns ratio	n	$10/13$
Transformer leakage inductance	L_σ	20 μH
Transformer magnetizing inductance	L_m	11 mH
Inductors	L_1, L_2	100 μH
Capacitors	C_1, C_2	10 μF
Capacitor	C_3	20 μF

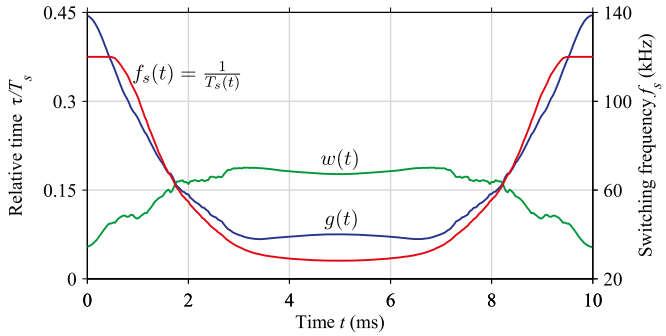

Fig. 7. Optimal control variables $g(t), w(t)$, and $f_s(t) = 1/T_s(t)$ over a half cycle of the mains period in ac-to-dc operation for a mains voltage of 230 V_{rms}, an input current of 16 A_{rms}, and an output voltage of 350 V. The control variables are derived by using the optimization algorithm depicted in Fig. 5 and stored in the lookup table shown in Fig. 8.

There, also the compensation of the reactive power of the input capacitors C_1, C_2 is taken into account. Further constraints are given by the minimum commutation current I_s for ZVS as

$$|i_{L\sigma}(\tau_0, x)| \geq I_s \tag{26}$$

$$|i_{L\sigma}(\tau_1, x)| \geq I_s. \tag{27}$$

The optimization results for a mains voltage of 230 V_{rms}, an input current of 16 A_{rms}, and an output voltage of 350 V by using the parameters from Table I is shown in Fig. 7. Around the zero crossing of the mains voltage, the switching frequency $f_s(t)$ is increased to lower the output power and reaches its maximum that is set to 120 kHz. Similar, the phase shift $g(t)$ is increased with lower output power that guarantees a triangular-like transformer leakage inductance current that is required to maintain ZVS also around the zero crossing of the mains voltage. For high power transfer at $t = 2$ ms up to $t = 8$ ms (see Fig. 7), $w(t)$ stays rather constant and the power is controlled mainly by the phase shift $g(t)$ and the switching frequency $f_s(t)$.

E. Converter Control

The control of the DAB converter is based on a phase-locked loop (PLL) for synchronization to the ac mains voltage v_1, a lookup table to store the optimal control variables g, w, T_s as well as a PI controller for adjusting the switching period T_s to shape the ac input current i_1. An overview of the control is depicted in Fig. 8.

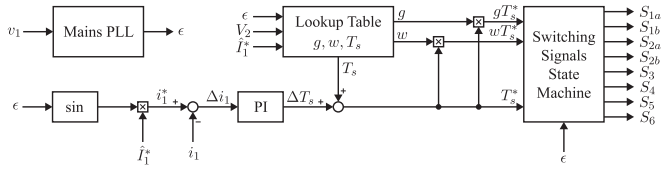

Fig. 8. Overview of the DAB converter control including the mains PLL to determine the mains angle ϵ, a lookup table to store the optimal control variables g, w, T_s as well as a PI controller for adjusting the switching period T_s to shape the ac input current i_1.

1) Mains PLL: The mains PLL includes an orthogonal system generator (OSG) implemented with a second-order generalized integrator (SOGI) structure as proposed in [16], [17]. With the OSG–SOGI structure, two clean orthogonal voltage waveforms v_α, v_β are constructed. These are then transformed into rotating dq-coordinates and v_d is controlled to zero (synchronization to a sinusoidal waveform) to derive the mains angle ϵ.

2) Lookup Table: The lookup table stores the optimal control variables g, w, T_s for an ac mains half-wave dependent on the mains angle ϵ and parameterized with the dc output voltage V_2 and the reference current amplitude $\hat{I}_1^*$. The output of the switching period T_s serves as feed-forward value for the PI controller that adds a ΔT_s to it as shown in Fig. 8. The resulting T_s^* gets then multiplied by g and w. The switching signals state machine finally generates the gate signals for the switches from gT_s^*, wT_s^*, T_s^* according to Figs. 3 and 4, respectively.

3) PI Controller: For the PI controller design, the small-signal transfer function from ΔT_s to Δi_1 is derived from (15) and given as

$$G_p = \frac{\Delta i_1}{\Delta T_s} = \frac{nV_2\left(2g - 4g^2 + w - 2w^2 - 4gw\right)}{4L_\sigma}. \tag{28}$$

Since the DAB converter is not operated near the resonant frequency of the resonant tank formed by C_1, C_2, C_3, and L_σ, the dynamics of these passive elements can be neglected what has been also a prerequisite previously for describing $i_{L\sigma}$ with linear equations. The transfer function G_p is mainly dependent on the mains angle ϵ (indirectly via the control variables $g(\epsilon), w(\epsilon)$) and the output voltage V_2. To compensate the voltage dependences, the proportional and integral gain of the PI controller are scaled by

$$K = \frac{1}{G_p} = \frac{4L_\sigma}{nV_2\left(2g - 4g^2 + w - 2w^2 - 4gw\right)} \tag{29}$$

such that

$$K_P = K\widetilde{K}_P \tag{30}$$

$$K_I = K\widetilde{K}_I \tag{31}$$

where $\widetilde{K}_P, \widetilde{K}_I$ are the constant gains and K_P, K_I the effective and adaptive ones. The closed-loop transfer function can be written as

$$G_{\text{cl}} = \frac{G_{\text{PI}}G_p}{1 + G_{\text{PI}}G_p} = \frac{\widetilde{K}_I + \widetilde{K}_P s}{\widetilde{K}_I + (1 + \widetilde{K}_P)s} \tag{32}$$

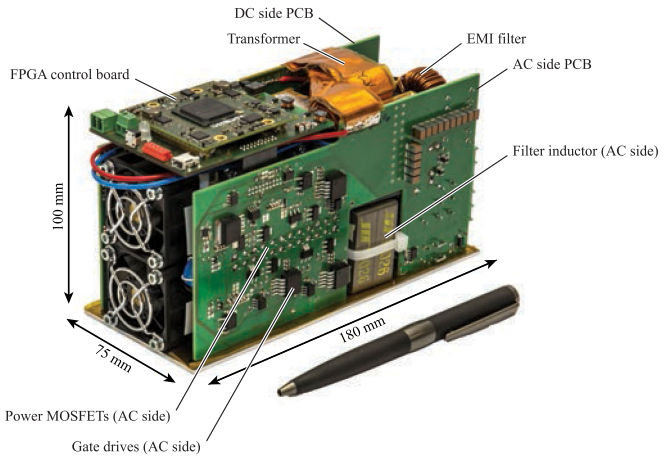

Fig. 9. Photograph of the hardware prototype system for experimental verification of the proposed combined phase-shift and frequency modulation.

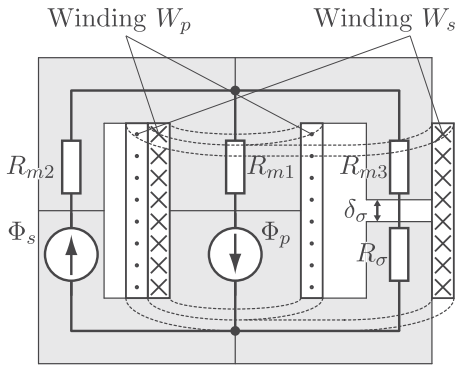

Fig. 10. 2-D drawing of the transformer including its reluctance model consisting of C-cores forming an E-core with the ac-side winding W_p wound around the inner leg and the dc-side winding W_s around the inner and the right-hand sided stray leg. By inserting an air gap of length δ_σ in the stray leg, the leakage inductance L_σ can be set.

with G_{PI} being the transfer function of the PI controller

$$G_{\mathrm{PI}} = K_P + \frac{K_I}{s} = K\left(\widetilde{K}_P + \frac{\widetilde{K}_I}{s}\right). \tag{33}$$

By setting $\widetilde{K}_P = 0$, the closed-loop transfer function can be simplified to a first-order system

$$G_{\mathrm{cl}} = \frac{1}{1 + \frac{1}{\widetilde{K}_I}s} \tag{34}$$

where the rise time from 10% to 90% of the steady-state value in the step response is given by

$$t_r = \frac{2.2}{\widetilde{K}_I}. \tag{35}$$

Since the controller tracks a sinusoidal waveform, the rise time should be kept small in the magnitude of a few switching periods $T_{s,\max}$ at the lowest switching frequency. With a rise time of $t_r = 100\ \mu$s, the controller gains are determined to be $\widetilde{K}_P = 0$ and $\widetilde{K}_I = 22\,000$.

TABLE II
COMPONENTS OF THE HARDWARE PROTOTYPE SYSTEM

MOSFETs $S_{1a}, S_{1b}, S_{2a}, S_{2b}$	2x STY139N65M5, 650 V, 14 mΩ
MOSFETs S_3, S_4, S_5, S_6	2x STY139N65M5, 650 V, 14 mΩ
Transformer	2x 2x AMCC-4 VITROPERM 500
	10 primary turns, 120 μm copper foil
	13 secondary turns, 120 μm copper foil
Inductor L_1	2x Kool Mu E 4317 26u, 27 turns
	Litz wire, 20 strands, 0.355 mm
Inductor L_2	2x Kool Mu E 4317 26u, 27 turns
	Litz wire, 20 strands, 0.355 mm
Capacitors C_1, C_2	18x Syfer 1825J500564KX, 560 nF
Capacitor C_3	36x Syfer 1825J500564KX, 560 nF

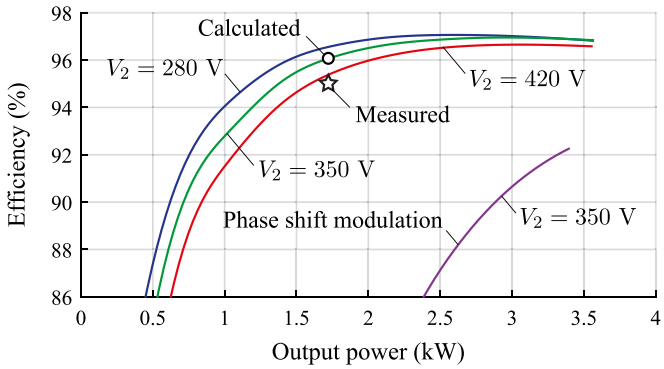

Fig. 11. Calculated efficiencies of the DAB ac–dc converter applying the proposed combined phase-shift and frequency modulation over the output power range for battery voltages 280, 350, and 420 V. Additionally, the calculated efficiency curve for the converter operated with the standard phase-shift modulation and the measured efficiency of the hardware prototype both at a battery voltage of 350 V are shown.

IV. HARDWARE PROTOTYPE

For validating the combined phase-shift and frequency modulation, an electric vehicle battery charger for Lithium-ion batteries with 3.3-kW output power to connect to the single-phase ac mains has been built and is shown in Fig. 9. The parameters of the hardware prototype are given in Table I.

A. Converter Components and Loss Model

In the following, the converter components with their loss models are presented for evaluating the converter efficiencies at different operating points. Table II summarizes the components of the hardware prototype, whereas Fig. 11 shows the calculated efficiencies over the output power range for battery voltages of 280, 350, and 420 V. For low output power, the efficiency curves diverge because of the high transformer leakage inductance peak currents occurring at high output voltages. In low power mode, mainly a triangular-like leakage inductance current occurs at the maximum switching frequency where the peak current is directly proportional to the output voltage.

Additionally, the efficiency of the converter applying the standard phase-shift modulation without the use of the dc-side clamping interval ($w = 0$) is depicted in Fig. 11. The switching frequency is fixed at 60 kHz, which corresponds to the average of the control variable f_s depicted in Fig. 7 for an input current of 16 A_{rms} and an output voltage of 350 V. The leakage inductance of the transformer is slightly adjusted to 12 μH to allow

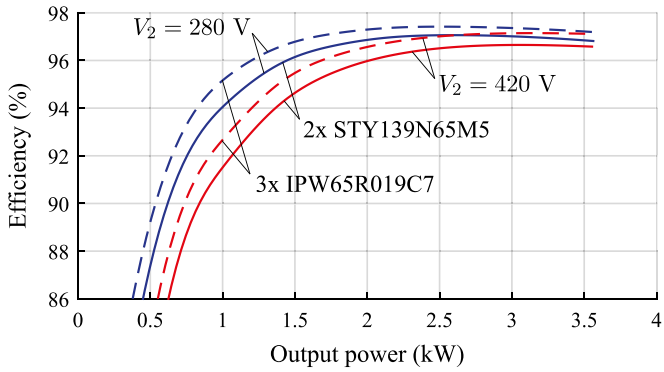

Fig. 12. Calculated efficiencies of the DAB ac–dc converter over the output power range for battery voltages 280 and 420 V applying two parallel STY139N65M5 MOSFETs ($R_{\mathrm{ds,on}} = 23.8$ mΩ at $T_j = 100$ °C) from STMicroelectronics [18] (solid lines) and three parallel IPW65R019C7 MOSFETs ($R_{\mathrm{ds,on}} = 32.5$ mΩ at $T_j = 100$ °C) from Infineon [19] (dashed lines).

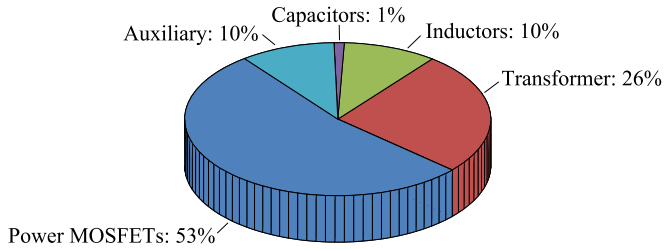

Fig. 13. Calculated loss distribution between the converter components at the maximum output power of 3.56 kW and a battery voltage of 350 V.

the maximum power to be transferred in case of the phase-shift modulation. Especially the ac-side MOSFETs are operated under hard switching conditions in the region of low output power so that the efficiency drastically drops what in turn can lead in the worst case to the destruction of the semiconductor devices.

The loss distribution between the components at the maximum output power of 3.56 kW and a battery voltage of 350 V is depicted in Fig. 13.

Fig. 12 shows the calculated efficiencies of the DAB ac–dc converter for battery voltages 280 and 420 V for the considered prototype system applying two parallel STY139N65M5 MOSFETs from STMicroelectronics [18] (solid lines) and for a converter solution applying three parallel IPW65R019C7 MOSFETs from Infineon [19] (dashed lines).

1) Power MOSFETs: Since the proposed modulation scheme guarantees ZVS at every switching instant, MOSFET devices with a comparable low on-state resistance are chosen. The used device is a 650-V MOSFET with an on-state resistance of 14 mΩ from STMicroelectronics [18]. The losses of the power MOSFETs are mainly determined by conduction losses. The switching loss energy $E_{\mathrm{Si,sw}}$ per MOSFET depending on the drain–source current is approximated by the turn-off loss curves given in the datasheet as well as measurement data and linearly scaled with the drain–source voltage v_{Si}. To reduce conduction losses, N_s number of MOSFETs are paralleled so that the power loss per switch is then approximated by

$$P_{\mathrm{Si}} = \frac{R_{\mathrm{ds,on}}}{N_s} I_{\mathrm{Si}}^2 + N_s f_s E_{\mathrm{Si,sw}} \frac{v_{\mathrm{Si}}}{400\ \mathrm{V}} \tag{36}$$

with $i = \{1a, 1b, 2a, 2b, 3, 4, 5, 6\}$. The hardware prototype applies two MOSFETs in parallel for all switches ($N_s = 2$). For conduction loss calculations, a worst-case junction temperature of 100 °C is assumed.

2) Transformer: For the proposed modulation to work properly, the transformer turns ratio has to guarantee $v'_{C3} > \hat{V}_1/2$ (with v'_{C3} referred to the ac side of the transformer), also at the lowest battery voltage of 280 V. Furthermore, the leakage inductance L_σ is designed such that the peak of the instantaneous power $\hat{P}_1$ [neglecting the reactive power term in (25)] at full input power of 3.68 kW can be transferred at the lowest switching frequency of 20 kHz and the lowest battery voltage of 280 V. This can be done by using (16) and solving for L_σ.

The transformer is built of two AMCC-4 C-cores [20] made of VITROPERM 500 [21] material forming an E-core. To increase the core area, two of them are stacked. The ac-side winding is wound around the center leg and the dc-side winding around the center and an outer stray leg [22]. Fig. 10 depicts a 2-D drawing of the transformer including its reluctance model with the flux sources Φ_p, Φ_s (driven by the applied winding voltages v_p, v_s) and the magnetic core reluctances R_{m1}, R_{m2}, R_{m3}. An air gap δ_σ is inserted in the stray leg to get the desired leakage inductance which is modeled by the leakage reluctance R_σ. In the loss model, the core losses per volume are calculated by applying the improved generalized Steinmetz equation (iGSE) [23].

For the ac- and dc-side windings, copper foil is used where the optimal foil thickness is calculated according to [24], which gives a minimum value of effective ac resistance. These values are 132 and 116 μm. For the hardware prototype, 120-μm copper foil is chosen, with 10 primary and 13 secondary turns. The skin and proximity effect losses per unit length in foil conductors for each current harmonic are then calculated according to [25]. The external magnetic field strength for calculating proximity losses is derived by a 1-D approximation based on the Dowell method [26] as the air gap in the stray leg is relatively small and losses caused by the fringing field can be neglected.

3) Inductors: For the ac- and dc-side inductors L_1, L_2 two stacked E-cores of type Kool Mu 4317 with material 26u from Magnetics [27] are used. Powder cores are ideally suited for the hardware prototype because they offer a distributed air gap and a high saturation flux density. This is advantageous over a ferrite core with a large air gap exhibiting considerable fringing magnetic field. Both inductors are wound with the litz wire with 20 strands of diameter 0.355 mm and a turns number of 27 so that a minimum inductance value of 100 μH is guaranteed at the highest peak current.

Again, the core losses per volume are calculated by using the iGSE, the Steinmetz parameters are obtained from [27]. The skin and proximity effect losses per unit length in the litz wire for each current harmonic are calculated according to [25]. Also for the inductors, the external magnetic field strength is derived by a 1-D approximation [26].

4) Capacitors: For the ac- and dc-side capacitors C_1, C_2, C_3, paralleled 560-nF ceramic capacitors with dielectric X7R from Syfer [28] are used. For achieving high power densities, multilayer ceramic capacitors are ideally suited because they

offer comparable high energy densities and allow high current ripples. Since the voltage ripple on the capacitors is relatively small at high switching frequencies, dielectric losses are not accounted for in the loss model. Therefore, only the ohmic losses according to

$$P_{\mathrm{Ci}} = \frac{R_{\mathrm{esr}}}{N_c} I_{\mathrm{Ci}}^2 \quad i = \{1, 2, 3\} \tag{37}$$

where R_{esr} denotes the equivalent series resistance obtained from datasheet and N_c the number of parallel capacitors are considered.

5) Auxiliary Losses: Besides the load-dependent losses shown in the previous sections, a constant loss share for precharging relay, FPGA control board, sensing and fans of 6 W is considered. The gate drive losses per switch are approximated by

$$P_{\mathrm{Gi}} = N_s V_{\mathrm{gs}} Q_g f_s \tag{38}$$

with $i = \{1a, 1b, 2a, 2b, 3, 4, 5, 6\}$, V_{gs} the gate–source voltage, and Q_g the gate charge from the datasheet. Furthermore, losses caused by an EMI filter are approximated by an equivalent resistance of 4 mΩ.

6) Cooling System: The number of semiconductors basically defines the base plate size of the heat sink as 80 × 65 mm for ac- and dc-side switching devices so that a double-sided heat sink can be used. Two 40 × 40 mm fans of type San Ace 40 are applied for forced convection cooling. After optimizing the cooling system as described in [29] considering a minimum fin thickness of 1 mm and a minimum fin spacing of 2 mm, a thermal heat sink to ambient resistance of $R_{\mathrm{th},s-a} = 0.32$ K/W results which in turn leads to a cooling system performance index of 9.86.

B. Experimental Verification

For validating the proposed modulation scheme on the hardware prototype, the control shown in Fig. 8 is implemented in VHDL on an FPGA device. The optimization of the control variables is done offline with the results stored in lookup tables on the FPGA. The interlocking for the used switching devices is set to 500 ns. For each parallel connection of two MOSFETs, a 10-nF ceramic capacitor is placed in parallel in order to limit the di_{ds}/dt, and therefore, the ringing of the drain–source voltage v_{ds} at the end of the resonant transition. Under these circumstances, a minimum commutation current I_s of 5 A per device is found to be sufficient for achieving ZVS over the whole ac mains cycle.

The experiments are conducted by using an ac source capable of delivering 8 A_{rms} at 230 V_{rms} connected to the input of the hardware prototype and a 10-kW dc source connected to the output of the hardware prototype to simulate a battery voltage of 350 V. Additionally, a resistive load draws 15 A from the dc source so that power can flow from the ac input of the converter to the dc output.

For the measurements, the ac current controller described earlier is enabled and its reference set to 8 A_{rms}. Fig. 14 shows the measured ac input current i_1 together with the ac input voltage v_1, whereas Fig. 15 depicts the measured dc output current i_2 and the dc output voltage v_{C3}. During the zero crossing of the ac voltage, all MOSFETs are opened for a short time period so that i_1 starts to ring when the switching operation is started again. Oscillations can also be seen in the dc output current i_2 when it touches the zero line.

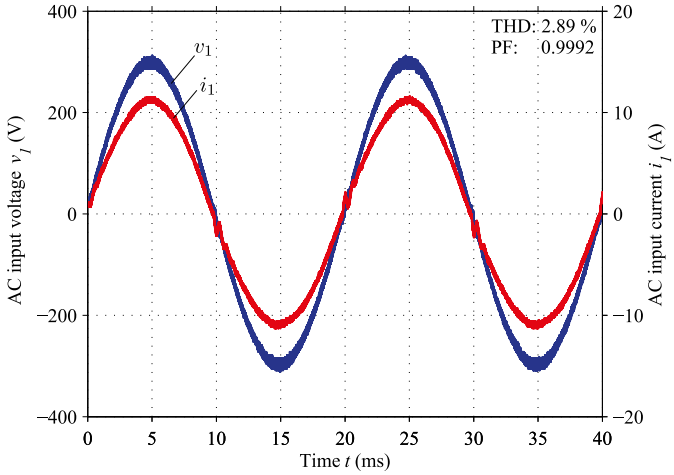

Fig. 14. Measured ac input current i_1 and ac input voltage v_1 for an input current reference $\hat{I}_1^* = \sqrt{2} \cdot 8$ A_{rms} and an output voltage of 350 V in ac-to-dc operation for a mains voltage of 230 V_{rms}.

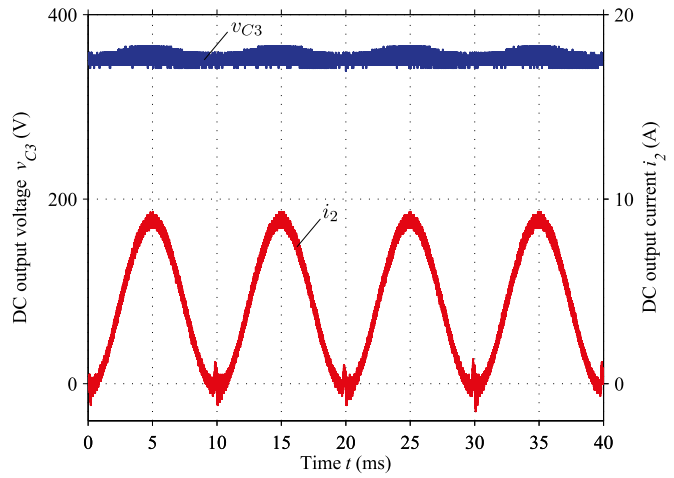

Fig. 15. Measured dc output current i_2 and dc output voltage v_{C3} for an input current reference $\hat{I}_1^* = \sqrt{2} \cdot 8$ A_{rms} and an output voltage of 350 V in ac-to-dc operation for a mains voltage of 230 V_{rms}.

The measurements of voltages and currents at the transformer are given in Figs. 16 and 17. The transformer leakage inductance current $i_{L\sigma}$ exhibits the typical envelope with twice the ac input voltage frequency. The transformer voltage v_{p+} measured from point $p+$ to the negative ac input rail shows square-wave voltages with amplitudes following the ac input voltage. During the first half wave of the input voltage, the amplitudes are positive, during the second half wave, they are negative. The transformer voltages v_{s+}, v_{s-} are measured from points $s+, s-$ to the negative dc output rail and show square-wave voltages with a constant amplitude of the dc output voltage.

Postprocessing of the waveforms i_1, v_1 from Fig. 14 leads to a total harmonic distortion (THD) of 2.89% and a PF of 0.9992 at the given operating point. The ac input current harmonics

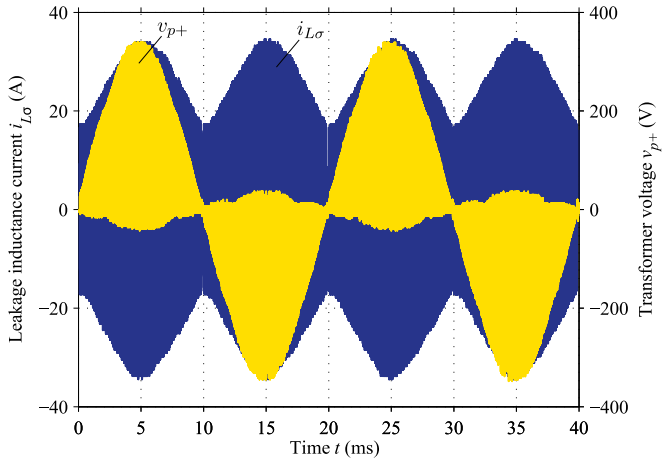

Fig. 16. Measured transformer leakage inductance current $i_{L\sigma}$ and transformer voltage v_{p+} (transformer connection $p+$ to negative ac input rail) for an input current reference $\hat{I}_1^* = \sqrt{2} \cdot 8$ A_{rms} and an output voltage of 350 V in ac-to-dc operation for a mains voltage of 230 V_{rms}.

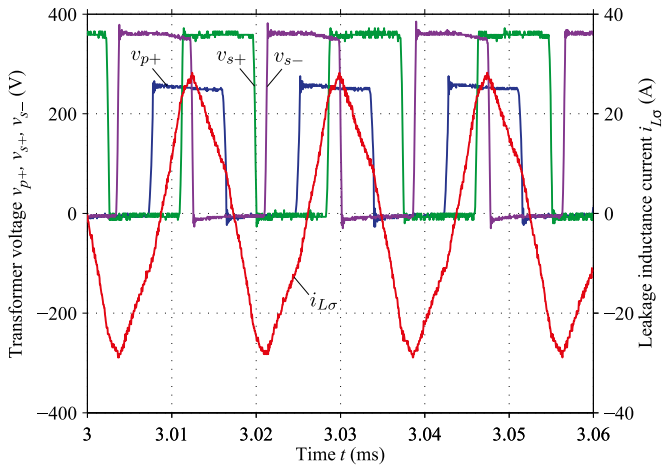

Fig. 17. Measured transformer leakage inductance current $i_{L\sigma}$ and transformer voltages v_{p+}, v_{s+}, v_{s-} (transformer connection $p+$ to negative ac input rail, transformer connections $s+, s-$ to negative dc output rail) for an input current reference $\hat{I}_1^* = \sqrt{2} \cdot 8$ A_{rms} and an output voltage of 350 V in ac-to-dc operation for a mains voltage of 230 V_{rms}.

compared to the IEC 61000-3-2 class A standard are given in Fig. 18. It can be seen, that the proposed modulation scheme of the DAB ac–dc converter guarantees full compliance with the IEC standard.

The measured efficiency is determined to be 95% for an ac mains voltage of 230 V_{rms}, a dc output voltage of 350 V and an input current reference of 8 A_{rms}. The power density is around 2.5 kW/L. The measurement at 1.7-kW output power is compared to the calculated efficiency curves in Fig. 11. From the calculation with the applied loss models presented previously, an efficiency of around 96% is obtained. The difference in losses is mainly due to the assumption of relatively small switching losses of the MOSFETs under ZVS conditions. The applied device STY139N65M5 [18] exhibits a relatively small on-state resistance but a large output capacitance, which demands a corresponding commutation current for the resonant transition during the interlocking interval. Having increased minimal currents

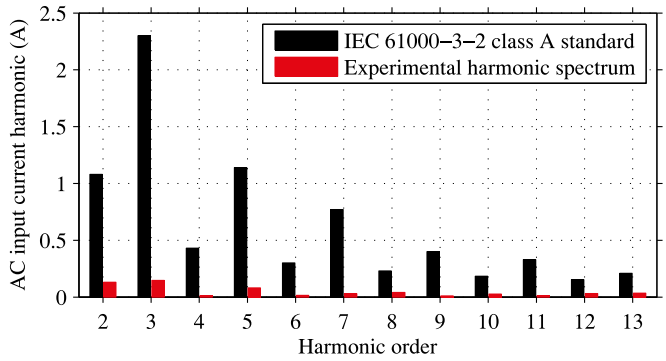

Fig. 18. Experimental ac input current harmonics compared to the IEC 61000-3-2 class A standard for an input current reference $\hat{I}_1^* = \sqrt{2} \cdot 8$ A_{rms} and an output voltage of 350 V in ac-to-dc operation for a mains voltage of 230 V_{rms}.

at the switching instants in combination with a slow turn-off of the MOSFET has a substantial impact on the semiconductor losses. By using devices with an improved switching behavior, the efficiency of the hardware prototype could be further increased.

V. Conclusion

A combined phase-shift and frequency modulation for a DAB ac–dc converter with PFC is presented to achieve ZVS over the whole ac mains voltage period. The modulation is described by analytical formulas and the control variables for minimum switch commutation currents are derived by an optimization procedure. A 3.3-kW electric vehicle battery charger with a 230-V_{rms}/50-Hz ac mains input for a battery voltage range of 280–420 V is built. The evaluation of the losses predict efficiencies of 96% up to 97% for an output power between 50% and 100% and a power density of 2.5 kW/L. The theoretical analysis of the modulation is validated by measurements, which show a THD of 2.89% and a PF of 0.9992 at 8 A_{rms} ac input current. Furthermore, the harmonic spectrum of the ac input current fully complies with the IEC 61000-3-2 class A standard.

Acknowledgment

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Felix Jauch (S'11) received the Bachelor's degree in electrical engineering and information technology from the Swiss Federal Institute of Technology (ETH) in Zurich, Switzerland, in August 2008, and the master's degree in October 2010, from ETH Zurich. His master thesis dealt with developing a test environment for high frequency converter for ultra-high-speed electrical drive systems and was carried out with the ETH spin-off company Celeroton. Since January 2011, he has been working toward the Ph.D. degree with the Laboratory for High Power Electronic Systems, ETH, focusing on fast charging stations for electric vehicles.

During his studies, he focused on power electronics, electrical drives, and electric power systems. After he had received his bachelor's degree, he worked at Bombardier Transportation, Switzerland as an Intern, where he developed electronic equipment for a test environment for traction converters.

Jürgen Biela (S'04–M'06) received the Diploma (Hons.) degree from Friedrich-Alexander Universität Erlangen-Nürnberg, Nuremberg, Germany, in 1999, and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 2006.

He joined the Research Department, Siemens A&D, Erlangen, Germany, in 2000, where he has been involved in inverters with very high switching frequencies, SiC components, and EMC. In 2002, he joined the Power Electronic Systems Laboratory, ETH Zurich, focusing on optimized electromagnetically integrated resonant converters. From 2006 to 2007, he was a Postdoctoral Fellow with the Power Electronic Systems Laboratory, and a Guest Researcher with the Tokyo Institute of Technology, Tokyo, Japan. From 2007 to 2010, he was a Senior Research Associate with the Power Electronic Systems Laboratory. Since 2010, he has been an Associate Professor of high-power electronic systems with ETH Zurich. His current research interests include the design, modeling, and optimization of PFC, dc–dc and multilevel converters with an emphasis on passive components, the design of pulsed-power systems, and power electronic systems for future energy distribution.