Letters

An Enhanced Single-Phase Step-Up Five-Level Inverter

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***Abstract*—In this letter, an enhanced step-up five-level inverter is proposed for photovoltaic systems. Compared with conventional five-level inverters, the proposed topology can realize the multilevel inversion with high step-up output voltage, simple structure, and reduced number of power switches. The operating principle of the proposed inverter has been analyzed and the output voltage expression has been derived. In addition, the comparison with existing topologies of single-phase five-level inverters is presented. Finally, experimental results validate the performance of the proposed topology.**

***Index Terms*—Multilevel inverter, single phase, step up, switch-diode-capacitor cell.**

I. Introduction

In the past decade, renewable energy sources such as photovoltaic (PV)-based systems have attracted much more attention due to the advantages such as less environmental impact and improved economic benefits. With the rapid growth of power electronics technology, various converters topologies have been developed for PV systems. Among these topologies, multilevel inverters have been receiving significant interest due to the reduced total harmonic distortion (THD) and improved quality of output waveform. As the output voltage level increases, the output harmonic content of such inverters decreases, allowing the use of smaller output filters.

For single-phase multilevel inverters, the most common topologies are the neutral-point clamped (NPC), flying capacitor (FC) and the cascaded H-bridges (CHB) types [2]–[5]. Some extended topologies for NPC have been further discussed in [6]–[8] and new topologies for the cascaded-type-based multilevel inverter have been proposed in [9]–[11]. In recent years, modular multilevel converter (MMC) has become an attractive topology due to its modularity, inherent redundancy, improved power quality, and ease of expansion [12]. Nevertheless, the number of component MMC used is not reduced and two inductors are added. Alternatively, some multilevel topologies with coupled inductors are proposed in [13]–[16] and they increase the number of output voltage levels without the need for a number of dc sources and bulky capacitors. The drawback is that coupled inductors need to be carefully designed.

Overall, the aforementioned multilevel topologies only can realize the voltage step-down inversion, i.e., the ac voltage amplitude cannot exceed the input dc voltage. A "transformerless" architecture is competent since it reduces the system cost and weight and realizes the voltage step up [17], [18]. However, two dc sources and corresponding split of dc bus capacitors are required as well as more switches and diodes in [17]. The step-up ratio of the boost converter has some limitations which restrict the step-up capability [18]. A high step-up inverter is proposed in [19] using the diode–capacitor cell and couple inductor. It uses less switches but just implements the two-level inversion.

In this letter, a novel single-phase step-up five-level inverter is proposed using the switch-diode-capacitor cell [20]. Compared to the conventional five-level topologies, the proposed inverter has the following advantages: 1) reduced number of power switches, diodes, and a single dc source are used; 2) multilevel inversion with step-up output voltage is obtained; 3) only four switches work at high frequency while two switches work at low frequency (50 Hz), which helps to reduce the switching losses; 4) simple topology and easy control are achieved.

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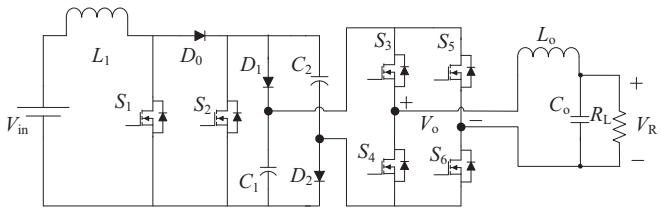

Fig. 1. Topology of the proposed single-phase step-up five-level inverter.

II. Proposed Single-Phase Step-Up Five-Level Inverter

Fig. 1 shows the topology of the proposed single phase step-up five-level inverter. As shown in Fig. 1, it consists of a single dc source, a conventional boost converter, a switch-diode-capacitor cell, and an H-bridge. The diode–capacitor cell (C_1–D_1, C_2–D_2) and the inductor L_1 are used to boost the dc-link voltage. The multilevel signal is generated by switch S_2 and the diode–capacitor cell. The proposed topology can implement the multilevel inversion with high step-up output voltage.

A. Modulation Method

As shown in Fig. 2, this proposed topology uses the level-shift multicarrier-based pulse width modulation method. Assuming that the capacitors C_1 and C_2 are equal and the diode–capacitor cell (C_1–D_1, C_2–D_2) is symmetrical and balanced, one can obtain

$$C_1 = C_2 = C,\ u_{C1} = u_{C2} = U_C \tag{1}$$

where u_{C1} and u_{C2} are the voltage across the capacitors C_1 and C_2. The following analysis is also based on the

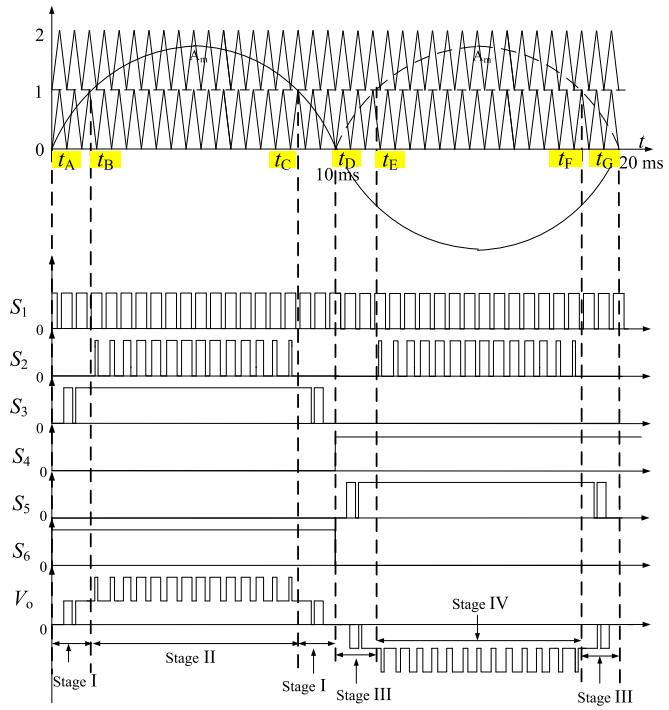

Fig. 2. Modulation method of the proposed step-up five-level inverter.

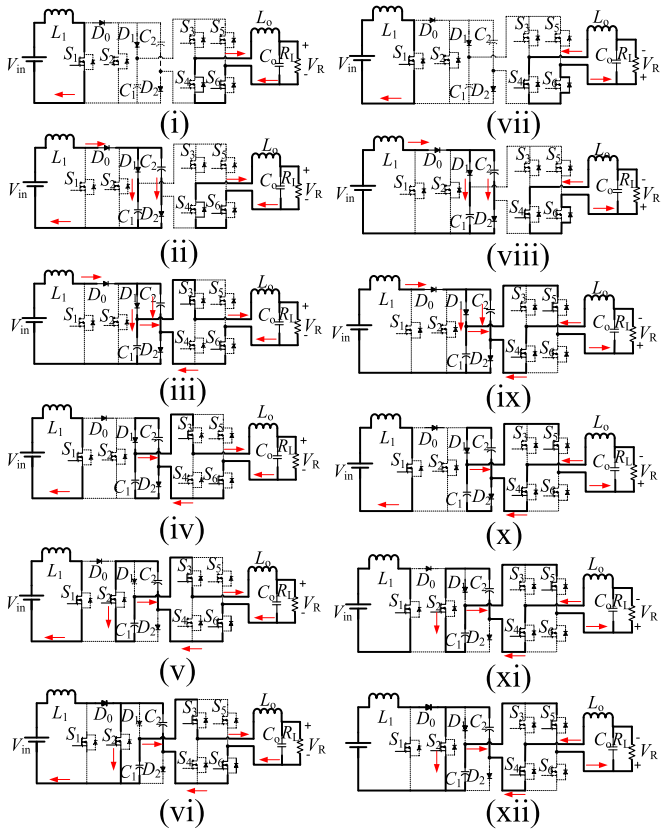

Fig. 3. Equivalent circuits of the proposed five-level inverter, (i)—(xii) modes 1–12.

assumption that the capacitor voltage is constant. Depending on the intersections between the reference and carrier, it can be seen that two stages exist in positive reference wave (Stages I and II) and negative reference wave (Stages III and IV).

1) Positive Output Voltage $(t_A < t < t_D)$*:* Switches S_4 and S_5 are maintained OFF state in the positive output voltage period.

Stage I $(t_A < t < t_B, t_C < t < t_D)$: the switch S_3 is switching due to the intersection between the sinusoidal reference waveform and the lower carrier waveform. In this stage, S_2 is OFF while S_6 is maintained ON state. The modes 1–4 shown in Fig. 3(i)–(iv) work alternately and the output voltage of the inverter V_o is 0 or U_c.

Stage II $(t_B < t < t_C)$: the switch S_2 is switching due to the intersection between the sinusoidal reference waveform and the upper carrier waveform. S_3 is maintained ON state during this period. In Stage II, the modes 3–6 shown in Fig. 3(iii) and (vi) operate alternately and the output voltage of the inverter V_o is u_c or $2U_c$.

2) Negative Output Voltage $(t_D < t < t_G)$*:* When the output voltage is negative, switches S_3 and S_6 are maintained OFF state. Stages III and IV are the counterpart of Stages I and II in the negative output of the ac voltage, respectively.

The switching states and corresponding modes are summarized in Table I. Generally, the switches in the H-bridge $(S_3$–$S_6)$ work to determine the polarity of the output voltage and switch S_2 operates to determine the output voltage level.

TABLE I
SWITCHING STATES AND WORKING MODES

Stage	Switching states	Possible modes
I	S_1, S_3: switching, S_2, S_4, S_5: OFF, S_6: ON	Modes 1, 2, 3, 4
II	S_1, S_2: switching, S_4, S_5: OFF, S_3, S_6: ON	Modes 3, 4, 5, 6
III	S_1, S_5: switching, S_2, S_3, S_6: OFF, S_4: ON	Modes 7, 8, 9, 10
IV	S_1, S_2: switching, S_3, S_6: OFF, S_4, S_5: ON	Modes 9, 10, 11,12

B. Operating Principle

Fig. 3 shows the working mode of the proposed five-level inverter. The red arrows in the figures show the current path. Overall, it can be seen that there are six switching states in each half-cycle. The operating modes of the positive half sinusoidal cycle (modes 1–6) are discussed in detail as follows.

Mode 1 (*see Fig. 3*(*i*)): S_1 is turned ON in this mode. The inductor L_1 is charged by the input dc source and the inductor current is increasing linearly. Meanwhile, the load current flows through S_6 and antiparallel diode of S_4.

Mode 2 (*see Fig. 3*(*ii*)): S_1 is turned OFF in this mode. Diodes D_0, D_1, and D_2 are all conducting. The inductor L_1 is discharging and the input source is charging the diode–capacitor network. In this mode, the ac load current still flows through S_6 and antiparallel diode of S_4.

Mode 3 (*see Fig. 3*(*iii*)): S_1 is maintained OFF and S_3 is ON in this mode. Diodes D_0, D_1, and D_2 are maintained

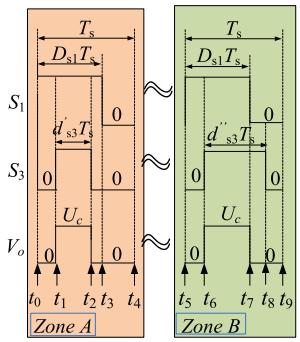

Fig. 4. Switching states in Stage I.

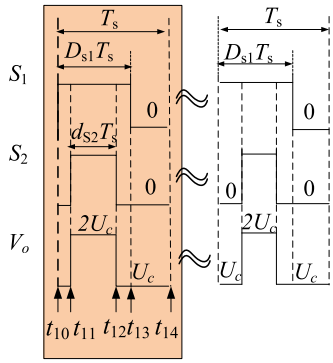

Fig. 5. Switching states in Stage II.

ON. The input dc source charges the diode–capacitor cell and simultaneously provides the power to the load.

Mode 4 (*see Fig. 3*(*iv*)): S_1 is turned ON again while D_0 is turned OFF in this mode. L_1 is charged by the input source and capacitors C_1 and C_2 are working in parallel to feed the load.

Mode 5 (*see Fig. 3*(*v*)): S_1 stays ON state and S_2 is turned ON in this mode. The input inductor L_1 is charged again and the capacitors C_1 and C_2 are connected in series supplying power to the ac load.

Mode 6 (*see Fig. 3*(*vi*)): S_2 stays ON state and S_1 is turned OFF in this mode. Similar as mode 5, the capacitors C_1 and C_2 are connected in series supplying power to the ac load.

Similarly, there are six working modes when the inverter outputs negative voltage and the equivalent working modes 7–12 are shown in Fig. 3(vii)–(xii).

III. Performance Analysis

The output voltage expression of the proposed converter and the comparison with other five-level inverters is performed in this section.

A. Output Voltage Derivation

In Stage I, since the sinusoidal modulating waveform does not intersect with the upper carrier waveform, S_2 is maintained OFF and S_3 is switching, as shown in Table I. Fig. 4 shows the possible switching states in Stage I. Depending on the duty cycle of $S_3(d_{s3})$, two conditions could exist in the switching process in Stage I, i.e., $d_{S3} < D_{S1}$ and $d_{S3} > D_{S1}$ (shown in Zone A and Zone B, respectively, in Fig. 4). D_{s1} is the duty cycle of switch S_1. In Stage II, S_3 is maintained ON and S_2 is switching since the modulating waveform intersects with the upper carrier waveform.

It is worth noting that the maximum duty cycle of S_2 is set to be less than the duty cycle of S_1, i.e., S_1 is definitely ON when S_2 is ON, as shown in Fig. 5. Under this condition, modes 6 and 12 do not appear. Thus, the following inequality is satisfied:

$$A_m - 1 < D_{s1} \tag{2}$$

where A_m is the amplitude of the reference wave. The total current ripple of inductors L_1 and L_o during one switching cycle of S_1 ($[t_0, t_4]$, $[t_5, t_9]$ – Stage I, $[t_{10}, t_{14}]$ – Stage II) can be derived as follows:

$$\begin{cases} \Delta i_{L1[t_0,t_4]or[t_5,t_9]} = \dfrac{1}{L_1}[V_{\text{in}} - U_C(1-D_{s1})]T_s \\ \Delta i_{L1[t_0,t_4]or[t_5,t_9]} = \dfrac{1}{L_o}(U_C d_{s3} - v_R)T_s \end{cases},$$

$$\begin{cases} \Delta i_{L1[t_{10},t_{14}]} = \dfrac{1}{L_1}[V_{in} - U_C(1-D_{s1})]T_s \\ \Delta i_{Lo[t_{10},t_{14}]} = \dfrac{1}{L_o}(U_C(1+d_{s2}) - v_R)T_s \end{cases} \tag{3}$$

where v_R is the output voltage of the resistive load R_L and T_s is the switching cycle of S_1.

By applying the principle of voltage–second balance on the inductor L_1, i.e., the inductor current ripple during one switching cycle is zero ($\Delta i_{L1[t0,t4]} = \Delta i_{L1[t10,t14]} = 0$), the mean capacitor voltage U_C can be derived as

$$U_C = \frac{V_{\text{in}}}{1 - D_{s1}}. \tag{4}$$

Considering the current ripple of the output inductor L_o in (3), $1 + d_{S2}$ and d_{S3} are determined by the intersection of the reference waveform $A_m sin\omega t$ with the upper and lower carrier, respectively. Hence, using (4), the output voltage of the resistor R_L can be expressed as follows:

$$v_R = U_C \times A_m \sin\omega t = \frac{A_m \sin\omega t}{1 - D_{s1}} V_{\text{in}}. \tag{5}$$

The voltage gain (ratio between amplitude of load resistor voltage V_{Rm} and input voltage V_{in}) can be defined as follows:

$$\frac{V_{Rm}}{V_{\text{in}}} = \frac{A_m}{1 - D_{s1}}. \tag{6}$$

It can be seen that the voltage gain is dependent on amplitude of reference wave A_m and duty cycle of S_1. Once (2) is not satisfied, the output voltage is also dependent on the working time of modes 6 and 12 in one switching cycle.

B. Comparison With Other Five-Level Inverters

Table II provided to summarize comparisons of the popular five-level inverter topologies and the proposed inverter. It is seen that the proposed topology can implement the five-level

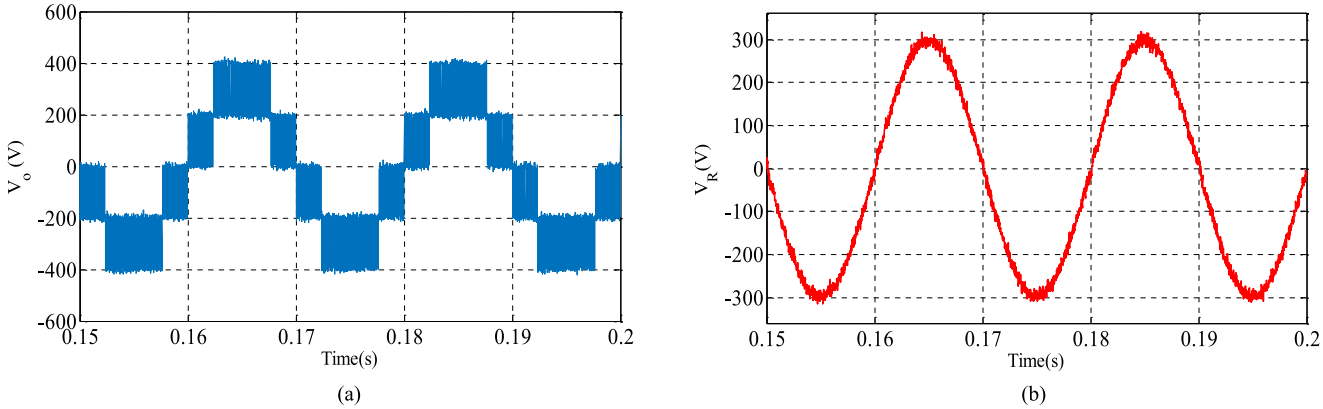

Fig. 6. Experimental result of the proposed inverter when $D_{S1} = 70\%$, (a) output voltage V_o, (b) load resistor voltage V_R.

TABLE II
COMPARISON OF THE COMPONENT NUMBERS IN THE FIVE-LEVEL INVERTERS

Topology	Main switches	Diodes	Capacitors	DC sources	Inductors	Step-up voltage
NPC	8	20	4	1	0	No
FC	8	8	10	1	0	No
CHB	8	8	2	2	0	No
MMC [12]	8	8	0	1	2	No
Topology proposed in [8]	7	12	0	2	0	No
Topology proposed in [10]	6	14	0	2	0	No
Topology proposed in [13] and [14]	6	6	0	1	2	No
Topology proposed in [15]	4	8	0	1	4	No
Topology proposed in [17]	8	14	7	2	5	Yes
Proposed topology	6	9	3	1	2	Yes

TABLE III
EXPERIMENTAL PARAMETERS

Parameter	Symbol	Value
Power switches	S_1–S_6	IRF830
Diodes	D_0, D_1, D_2	BYR29-600
Capacitor/filter capacitor	C_1, C_2 / C_o	330 μF/3 μF
Input inductor/filter inductor	L_1/L_o	2 mH/1 mH
Load resistor	R_L	200 Ω
Input dc voltage	V_{in}	60 V
Switching frequency	f_s	15 kHz

inversion and high step-up output with less number of power switches, diodes, and dc sources.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

In order to verify the performance of the proposed single-phase step-up five-level inverter, a 600 W prototype has been built in the lab. The parameters are listed in Table III.

Fig. 6 shows the experimental result of the proposed inverter when $A_m = 1.5$, $D_{S1} = 70\%$. As seen from Fig. 6(a), the maximum positive output $(2U_c)$ is 400.22 V and the half-level positive output (U_c) is 200.11 V. This is consistent with (4). In addition, it is clearly seen in Fig. 6(b) that the amplitude of resistor voltage is 300 V, which agrees with the derivation in (5).

As discussed in Section III-A, the output voltage can be regulated by D_{S1} or A_m. When $A_m = 1.5$, the experimental waveforms under $D_{s1} = 0.5$, 0.4 are shown in Figs. 7 and 8, respectively. It can be calculated from Fig. 7 that the measured voltage gain is 3.17 and this is slightly different from the analytical result. Also, it is shown in Fig. 8 that when $D_{s1} = 40\%$, the measured amplitude of resistor voltage is 220 V. Consequently, the measured voltage gain is 3.67 and it deviates the analytical result in (6). This is because in these two cases the output voltage also depends on the operating time of modes 6 and 12, which could change the output voltage. When A_m is set to 1.3, Figs. 9–11 show the experimental results under $D_{s1} = 0.3$, 0.4, 0.5, respectively. When the critical condition of (2) occurs, i.e., $A_m - 1 = D_{s1}$, it can be calculated from Fig. 9 that the measured voltage gain is 2.75. Again, this does not match the derivation in (6) since the inequality (2) is not satisfied. In contrast, the calculated voltage gain from Figs. 10 and 11 is 2.17 and 2.5, respectively, which is in alignment with the analytical gain in (6).

Based on the experimental results, the relationship between the voltage gain and the duty cycle of S_1 is plotted in Fig. 12. When the amplitude of reference wave A_m is set to 1.5, discrepancy between the theoretical and experimental result appears if D_{S1} is 0.4 or less. In contrast, when D_{S1} is higher than 0.5, a good agreement can be observed between the measured voltage gain and the theoretical derivation in (6). Similarly, when A_m is set to 1.3, the experimentally measured voltage gain is consistent with the analytical result if D_{S1} is larger than 0.3.

The measured voltage gain with respect to amplitude of reference wave A_m is shown in Fig. 13 and the analytical result derived from (6) is also given for comparison. It can be seen that when D_{S1} is set to 80%, the experimental result matches with the analytical derivation when A_m is less than 1.8. When $D_{S1} = 60\%$, it is seen that the measured voltage gain shows

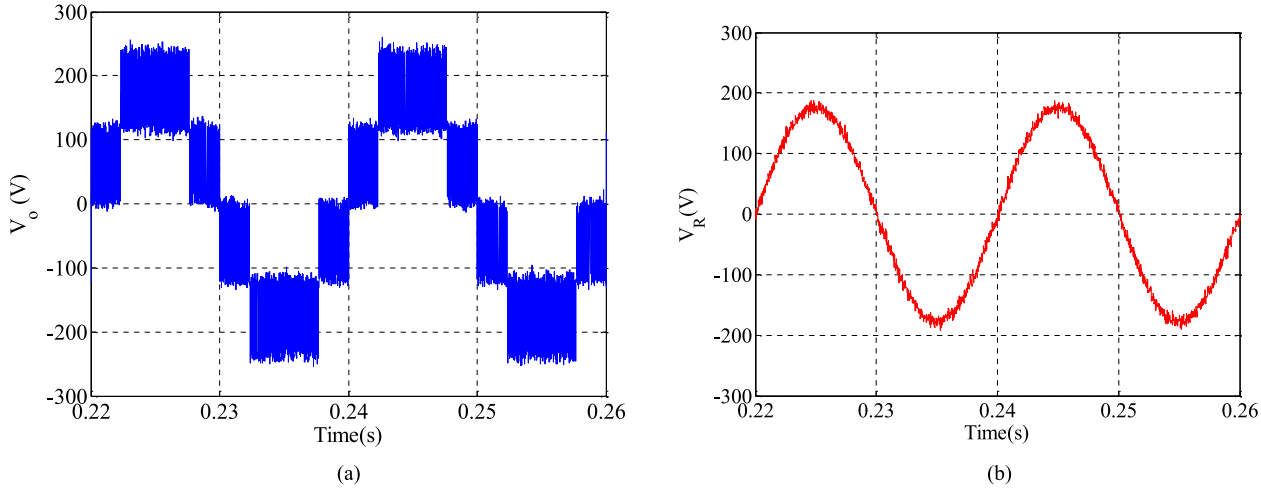

Fig. 7. Experimental result of the proposed inverter when $A_m = 1.5$, $D_{s1} = 50\%$, (a) output voltage V_o, (b) load resistor voltage V_R.

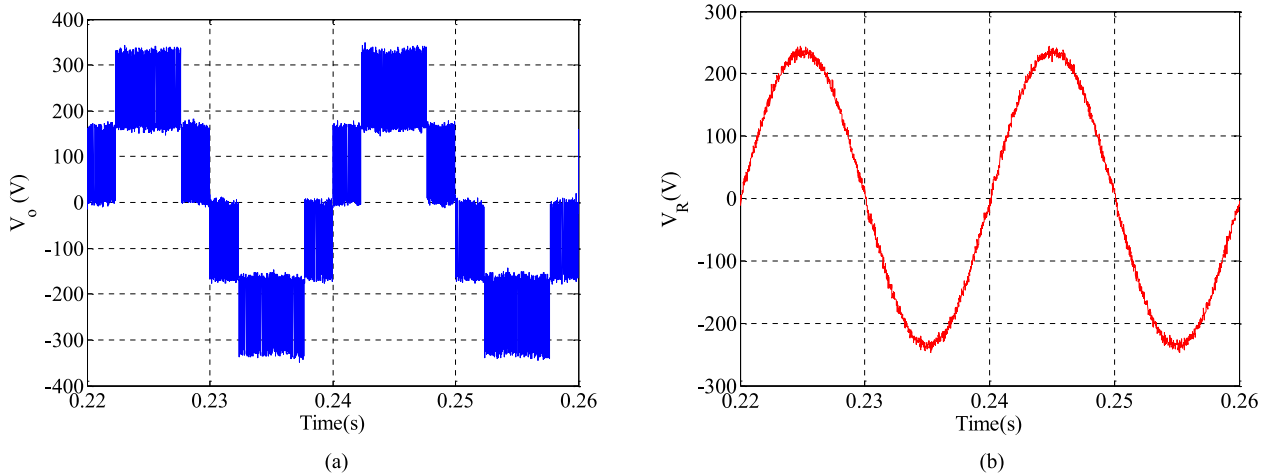

Fig. 8. Experimental result of the proposed inverter when $A_m = 1.5$, $D_{s1} = 40\%$, (a) output voltage V_o, (b) load resistor voltage V_R.

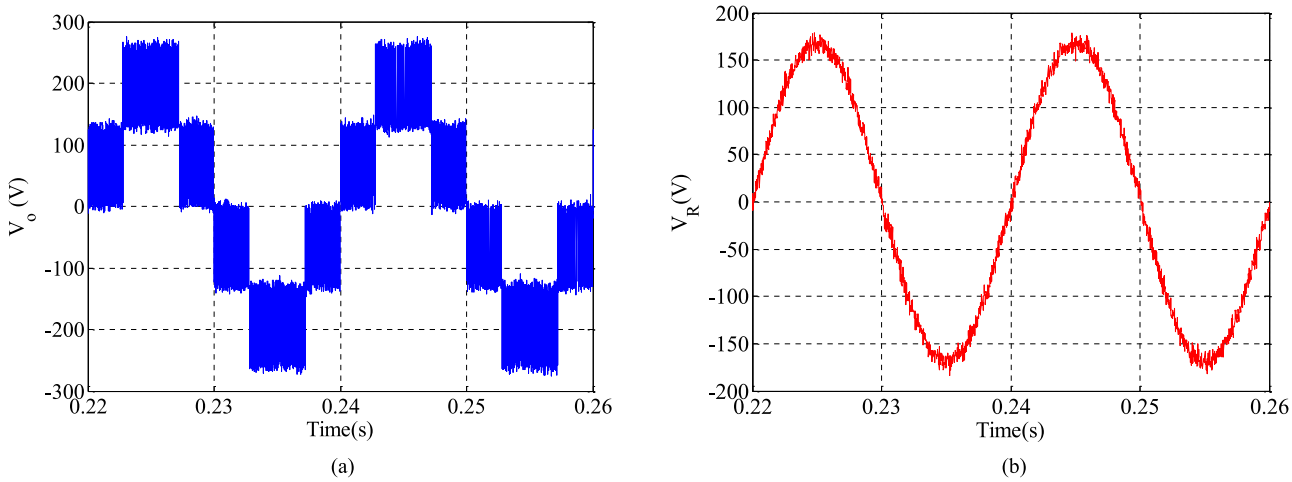

Fig. 9. Experimental result of the proposed inverter when $A_m = 1.3$, $D_{s1} = 30\%$, (a) output voltage V_o, (b) load resistor voltage V_R.

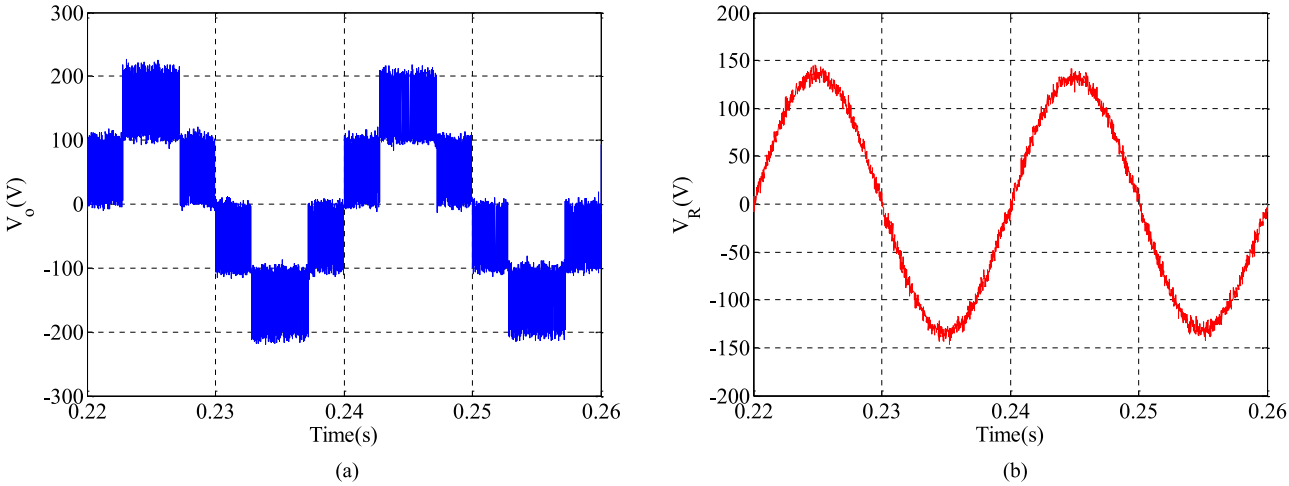

Fig. 10. Experimental result of the proposed inverter when $A_m = 1.3$, $D_{s1} = 40\%$, (a) output voltage V_o, (b) load resistor voltage V_R.

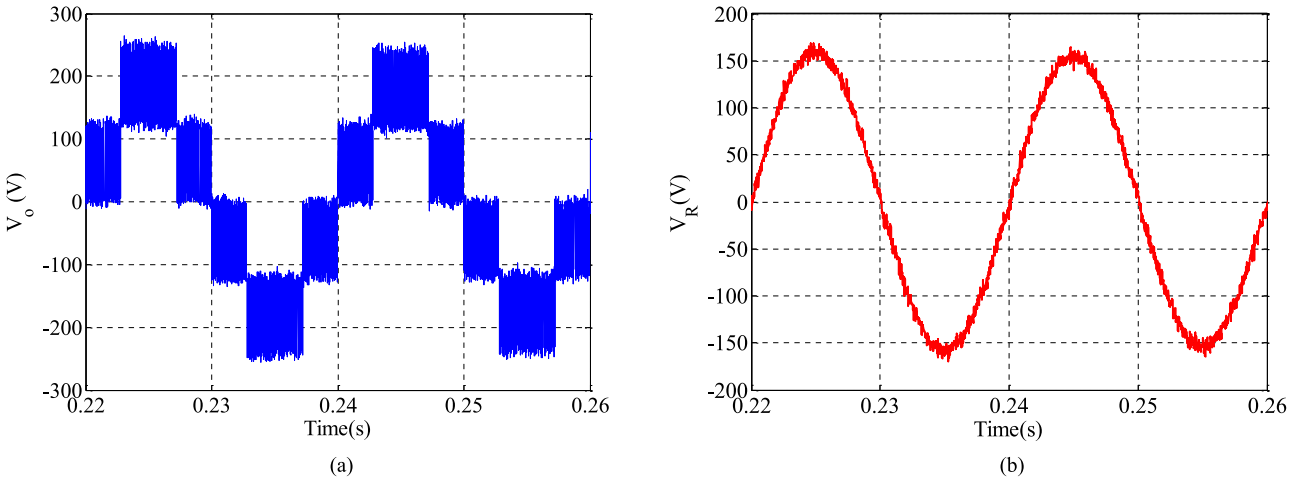

Fig. 11. Experimental result of the proposed inverter when $A_m = 1.3$, $D_{s1} = 50\%$, (a) output voltage V_o, (b) load resistor voltage V_R.

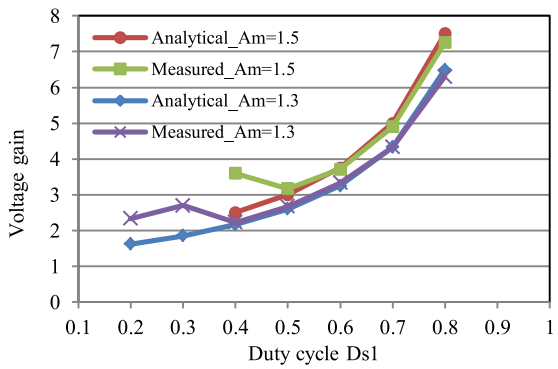

Fig. 12. Voltage gain versus duty cycle of S_1 (D_{s1}).

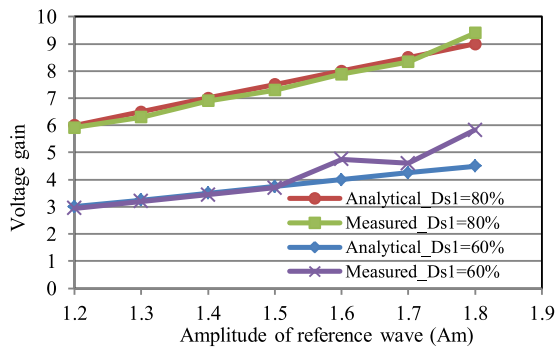

Fig. 13. Voltage gain versus amplitude of reference wave A_m.

good agreement with analytical result if the amplitude A_m is not more than 1.5. The difference can be clearly observed when A_m is higher than 1.5 (condition in (2) is not satisfied). Again, it confirms the analysis in Section III.

It can be inferred here that various combination of A_m and D_{s1} can yield the identical voltage gain. THD can be used as an important factor to choose an optimal combination of A_m and D_{s1}. Different combinations of A_m and D_{s1} have been tested and it is shown in Table IV that a lower THD could be obtained

TABLE IV
THD WITH DIFFERENT COMBINATIONS OF A_m AND D_{S1}

A_m	D_{s1}	Voltage gain	THD of output voltage V_o	THD of resistor voltage V_R
1.5	0.625	4	40.48%	4.8%
1.3	0.675	4	43.34%	5.6%
1.2	0.7	4	44.65%	6.3%
1.1	0.725	4	46.75%	6.8%

if a larger A_m and smaller D_{s1} on the condition that inequality (2) is satisfied.

V. CONCLUSION

This paper proposes an enhanced single-phase step-up five-level inverter. Operating principle and output voltage derivation have been performed. Compared to conventional five-level topologies, the proposed inverter reduces the number of power switches, diodes, size and cost of the system. Simple structure, easy control, and high step-up voltage ratio are the main features of the proposed topology. In addition, only four switches are operated at high frequency and the overall switching losses are reduced. Finally, experimental results validate the effectiveness and performance of the proposed topology.

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