A θ-Converter That Reduces Common Mode Currents, Output Voltage Ripples, and Total Capacitance Required

Qing-Chang Zhong, *Senior Member, IEEE*, and Wen-Long Ming

***Abstract*—In this paper, a single-phase converter consisting of two legs with four switches, called the θ-converter, is proposed. It has a common ac and dc ground, which reduces common mode currents and removes the need for an isolation transformer, and two capacitors: one across the whole dc bus and the other across the output. The dc bus capacitor provides a direct path for the double-frequency ripple current inherently existing in single-phase converters to return *continuously* so the output capacitor can be sized very small, only to filter out switching ripples. Moreover, the dc bus capacitor is intentionally designed to store the system ripple energy with large voltage ripples, which reduces its capacitance. Hence, the total capacitance needed and the output voltage ripples are reduced at the same time. This makes it cost-effective to use highly reliable film capacitors instead of bulky and vulnerable electrolytic capacitors. Because of the removed isolation transformers and bulky electrolytic capacitors, the power density and system reliability are improved. In order to properly operate the converter, two independent controllers are designed for the two legs, respectively, to achieve the desired functions and other normal objectives, such as the unity power factor. Experimental results are presented to demonstrate the high performance of the proposed converter.**

***Index Terms*—Common mode (CM) current, electrolytic capacitor, film capacitor, isolation transformer, voltage ripples, reliability.**

I. Introduction

In order to address various technological, economical, environmental, and social challenges, power electronic converters are playing a more and more important role. In particular, there is an increasing need for power conversion between ac and dc, e.g., for the integration of renewables, electric vehicles, and energy storage systems, and also for the integration of a large number of different loads [1]. Continuous efforts have been made to improve the power density, reliability, and efficiency of such converters by using advanced control and power electronic technologies [1].

For most single-phase converters, an energy buffer is often required at the dc side to keep the ripples of the dc voltage at a low level because of the inherently existing ripple energy. Normally, only bulky electrolytic capacitors are cost-effective to be used. However, the size and weight of bulky electrolytic capacitors make it hard to achieve high power density, which is one of the main goals when designing converters. What is worse is that this leads to a reduced system reliability because electrolytic capacitors are well known as the most vulnerable components in converters [2], [3], and one-third of failures in power electronic converters are due to capacitor failure [4]. Reducing capacitance required, while maintaining low voltage ripples has become a very active research area in recent years. Most of the studies in the literature focus on adding an active circuit at the dc side, in series [5], [6] or in parallel [2], [7]–[10] with the dc bus, to store the ripple energy. In this case, the dc bus capacitors are mainly used to filter the output switching frequency ripples and, hence, the capacitance required can be significantly reduced, which may reach a level that highly reliable film capacitors are cost-effective to be used. These active circuits are often dc/dc or dc/ac converters that consist of two or more active switches, one inductor, and one capacitor.

Another fundamental problem in power electronic converters is that isolation transformers are often needed to reduce electromagnetic interference emissions caused by actively operated switches [7], [11]–[14]. However, isolation transformers are normally bulky and heavy, which reduces power density. Moreover, the system efficiency is reduced by about one to two percent because of isolation transformers [15]. As a result, transformerless converters are highly demanded. In order to remove isolation transformers, effective methods are proposed to reduce CM currents to a low level, either via reducing the CM voltage [15]–[20] or via increasing the impedance on the path of CM currents [21]. However, these approaches suffer from reduced ability to process reactive power [12], [15] and/or degraded performance caused by parasitic capacitors of switches [12], [22]. Another approach is to directly connect the ac and dc grounds together to short circuit the parasitic capacitors; see, e.g., [12], [23], [24].

In order to improve system efficiency, power density, and reliability, it is desirable to remove both the electrolytic capacitors and the isolation transformers. Of course, this can be achieved by combining the aforementioned methods. For example, both electrolytic capacitors and isolation transformers can be removed if the solutions presented in [10] and [12] are combined. Instead of such combinations, as reported in [25]–[27], it is possible to achieve this by slightly changing the conventional topology and the way the converters are operated, without adding any extra active switches.

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In this paper, a novel topology, called the θ-converter because of its shape, is proposed to further reduce the total capacitance needed, following [25] and [26]. For easy reference, the topology in [25] and [26] is called hereafter the ρ-converter. The main change is to put one capacitor across the whole dc bus instead of between the dc ground and the negative pole of the dc bus, as in [25] and [26]. This small change allows the double-frequency ripple current that is inherent in single-phase converters to flow through the dc bus capacitor directly, which makes its path the shortest, and also makes it possible for the ripple current to return *continuously* rather than discontinuously as in [25] and [26]. This helps further reduce the voltage ripples. Moreover, the stored ripple energy can be significantly increased for the same dc bus voltage rating because of the increased voltage across the capacitor. As a result, the total capacitance required is further reduced. For the experimental system presented in this paper, the total capacitance is reduced by $172\times$ compared to that of the conventional converter and by about $3.5\times$ compared to that of the ρ-converter proposed in [25] and [26].

The rest of this paper is organized as follows. The topology, the equivalent circuit and the operation principle of the θ-converter are presented in Section II. The selection of the passive components, including the capacitors and the inductor, to minimize their usage is discussed in Section III. The detailed comparison between the proposed θ-converter and the ρ-converter is made in the Section IV, highlighting the further reduction of the total capacitance required and the path of the double-frequency ripple current. The associated controllers for the two legs of the θ-converter are developed in Section V, with extensive experimental results presented in Section VI to validate the operation and performance of the θ-converter. Conclusion is made in Section VII.

II. Proposed θ-Converter

A. Topology

As shown in Fig. 1(a), the proposed converter consists of two legs: One conversion leg and one neutral leg. Only four switches are used to construct the converter. The conversion leg consists of two switches Q_1 and Q_2, one inductor L_g, and one dc bus capacitor C, and the neutral leg consists of two switches Q_3 and Q_4, one inductor L_N, and one capacitor C_+. Because of its shape, the proposed converter is called the θ-converter. The driving circuit of the θ-converter is exactly the same as that in conventional full-bridge converters, where the two switches Q_2 and Q_4 share the same ground and the two switches Q_1 and Q_3 have their own floating grounds.

In addition, it is worth highlighting that the θ-converter can be operated in both the rectification mode and the inversion mode, without any restriction on the power factor. This means the θ-converter has the capability of bidirectionally exchanging both real and reactive power with the grid, which is highly preferred for grid-tied applications. In order to facilitate the presentation in the sequel, the operation in the rectification mode is taken as an example in this paper. Only slight changes are needed for the operation in the inversion mode.

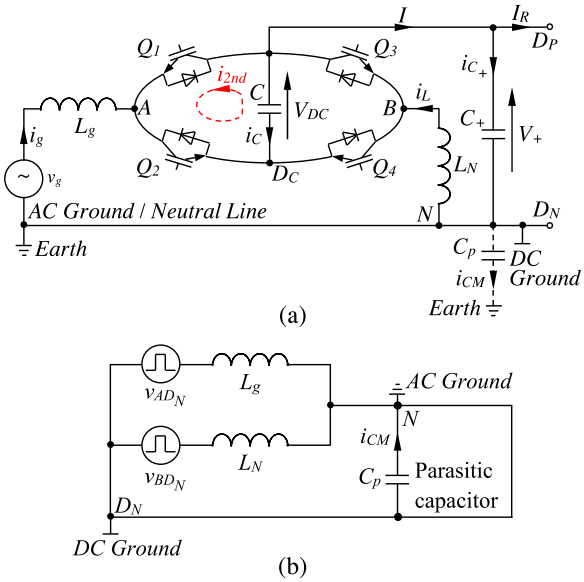

Fig. 1. Proposed θ-converter: (a) Topology; (b) equivalent circuit for analyzing the CM current.

The two legs of the θ-converter are controlled independently, with the option to flexibly achieve different objectives. In the rectification mode, the conversion leg is mainly used to control the grid current i_g and the dc bus voltage $V_{\rm DC}$, and the neutral leg is mainly responsible for regulating the voltage V_+ and for diverting the ripple energy away from the capacitor C_+. As a result, the ripple power is stored in the dc bus capacitor C instead of the capacitor C_+, which means the capacitor C_+ can be sized only to filter out the switching ripples with a very small capacitor. Because the capacitor C (the dc bus) does not supply any loads directly, therefore, it can be designed intentionally to have large voltage variations/ripples. Moreover, the dc bus voltage $V_{\rm DC}$ is higher than V_+. Hence, the capacitor C can be very small as well. The total capacitance required, i.e., $C + C_+$, can be significantly reduced with comparison to that of conventional converters.

It is worth noting that the double-frequency ripple current $i_{2\rm nd}$, which is inherent in single-phase converters, can be controlled to flow through the capacitor C, without flowing through the neutral leg or the load. Actually, this consists of the shortest possible path for $i_{2\rm nd}$, which is a prominent feature. See Section IV for more details.

Similar to the ρ-converter in [25] and [26], the proposed θ-converter has a common ground for the ac and dc sides. The equivalent circuit of the θ-converter for analyzing CM currents is shown in Fig. 1(b). It can be seen that the parasitic capacitor C_p from the dc side to the earth is short circuited by the common ac and dc ground, and the CM current $i_{\rm CM}$ is completely eliminated when the line impedance is ignored. Note that there are other parasitic capacitors, e.g., the ones from switches to the earth, but they are very small with comparison to the C_p and, hence, the influence of these capacitors on the CM current can be neglected [11], [12], [28], [29]. As a result, no isolation transformer is needed, which is achieved without any additional efforts to change the control and/or modulation strategies.

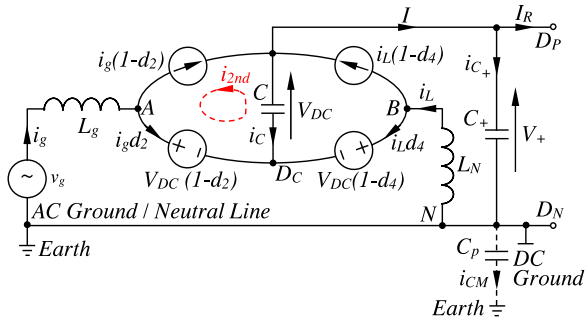

Fig. 2. Average circuit model of the θ-converter.

B. Average-Mode Circuit in the Steady State

For the ac side of the θ-converter, the grid current is often controlled to be in phase with the grid voltage to achieve the unity power factor. In this case, it can be assumed that the grid voltage and the grid current are

$$v_g = V_g \sin \omega t \tag{1}$$

$$i_g = I_g \sin \omega t \tag{2}$$

respectively, where V_g is the peak grid voltage, I_g is the peak grid current, and ω is the grid angular frequency. The product of v_g and i_g, i.e., the system power, contains a dc component and a double-frequency ripple component. As shown in [13] and [14], the system ripple energy in single-phase converters with the unity power factor is

$$E_r = \frac{V_g I_g}{2\omega}. \tag{3}$$

For the dc side of the converter, there is

$$V_+ = V_{\rm DC} - V_- \tag{4}$$

where V_+ and $V_{\rm DC}$ are the voltages across the capacitors C_+ and C, respectively, and V_- is the voltage between the neutral point/ground N and the negative pole D_C of the dc bus, as shown in Fig. 1(a). Note that the output voltage of the converter is V_+, not $V_{\rm DC}$ or V_-. Because of the power balance, the system ripple energy (3) also appears at the dc side, if not appropriately controlled. For example, for conventional converters, bulky electrolytic capacitors are often needed to smooth this ripple energy so that the voltage ripples can be maintained at a low level.

The average circuit model of the θ-converter in the steady state can be developed, as shown in Fig. 2, following the procedures in [30] and [31]. Note that the averaging is carried out for the switching frequency so the dc and low-frequency components are well kept, and it is accurate enough to analyze the behavior of the system at low frequencies.

Since the switching frequency is of several orders high compared to the grid frequency, the grid current can be controlled to well track its reference. As a result, it can be assumed that the fundamental component of the grid current is constant during one switching cycle. According to [31], the duty cycle d_2 of switch Q_2 is

$$d_2 = \frac{V_+}{V_{\rm DC}} - \frac{V_g}{V_{\rm DC}} \sin \omega t. \tag{5}$$

Since the two switches of the conversion leg are operated complementarily, the duty cycle d_1 of switch Q_1 is

$$\begin{aligned} d_1 &= 1 - d_2 \\ &= \frac{V_-}{V_{\rm DC}} + \frac{V_g}{V_{\rm DC}} \sin \omega t. \end{aligned} \tag{6}$$

The switches Q_1 and Q_2 can then be represented by a current source $i_g(1-d_2)$ and a voltage source $V_{\rm DC}(1-d_2)$, respectively. Similarly, the model of the neutral leg can be built. As shown in Fig. 2, switches Q_3 and Q_4 can be represented by a current source $i_L(1-d_4)$ and a voltage source $V_{\rm DC}(1-d_4)$, respectively, where i_L is the current flowing through the neutral inductor L_N and d_4 is the duty cycle of the switch Q_4. It is worth noting that the neutral leg is actually operated as a dc/dc converter, with the duty cycle d_4 given by

$$d_4 = \frac{V_+}{V_{\rm DC}} \tag{7}$$

because in the average mode there is

$$V_{\rm DC}(1-d_4) + V_+ = V_{\rm DC}. \tag{8}$$

Due to the complementary operation, the duty cycle d_3 of the switch Q_3 is

$$d_3 = 1 - d_4 = \frac{V_-}{V_{\rm DC}}. \tag{9}$$

C. Diversion of the Ripple Current

According to the average circuit model of the converter shown in Fig. 2, there is

$$i_{C_+} = i_L + i_g - I_R \tag{10}$$

where i_{C_+} and I_R are the currents flowing through the capacitor C_+ and the load, respectively. Because of the power balance between the ac and dc sides (ignoring losses), there is

$$I_R = \frac{V_g I_g}{2V_+}. \tag{11}$$

Substituting (11) into (10), then

$$i_{C_+} = i_L + I_g \sin \omega t - \frac{V_g I_g}{2V_+}. \tag{12}$$

In order to divert the ripple current away from C_+, i.e., to make $i_{C_+} = 0$ (ignoring the switching component), then the inductor current needs to be controlled as

$$i_L = -I_g \sin \omega t + \frac{V_g I_g}{2V_+} \tag{13}$$

which consists of the load current I_R component and the returning grid current i_g component. This can be achieved by controlling the neutral leg. The detailed control strategies can be found in Section V.

III. Selection of the Passive Components

A. Selection of the Capacitor C

Due to the significantly reduced current flowing through the capacitor C_+, the system ripple energy E_r is now mainly stored

in capacitor C. As a result, there is

$$\begin{aligned} C &= \frac{E_r}{\triangle V_{\rm DC} V_{\rm DC0}} \\ &= \frac{V_g I_g}{2\omega \triangle V_{\rm DC} V_{\rm DC0}} \end{aligned} \tag{14}$$

where $\triangle V_{\rm DC}$ and $V_{\rm DC0}$ are the peak–peak and average values of the voltage $V_{\rm DC}$, respectively. Since the voltage $V_{\rm DC}$ does not supply any loads, it can be designed to have large $\triangle V_{\rm DC}$. Moreover, there is $V_{\rm DC0} > V_+$. As a result, a small capacitor C is often enough.

In order to clearly demonstrate the minimum capacitance of the C, (14) can be rewritten as

$$C = \frac{V_g I_g}{\omega (V_{\rm DCmax}^2 - V_{\rm DCmin}^2)} \tag{15}$$

where $V_{\rm DCmax}$ and $V_{\rm DCmin}$ are the maximum and minimum values of the voltage $V_{\rm DC}$. $V_{\rm DCmax}$ is determined by the voltage ratings of both the capacitor C and the switches, and $V_{\rm DCmin} = V_+ + V_{-\rm min}$ is determined by the minimum value $V_{-\rm min}$ of the voltage V_- and the rated output voltage V_+, which is fixed according to the requirement of the dc load R. In order to ensure the successful boost operation of the converter in the steady state and also to properly control the grid current, the duty cycles d_1 and d_2 should be within $[0, 1]$, which means

$$V_- \geqslant V_g \tag{16}$$

according to (5) and (6). If (16) is not satisfied, then there would be some distortions in the grid current. This can be seen from the experimental results of the ρ-converter, which adopts the same conversion leg as the proposed converter, given in [26, Fig. 7].

Based on the above analysis, there are

$$V_{-\rm min} = V_g \tag{17}$$

and

$$V_{\rm DCmin} = V_+ + V_{-\rm min} = V_+ + V_g. \tag{18}$$

According to (15), the minimum capacitance can be found as

$$\begin{aligned} C_{\rm min} &= \frac{V_g I_g}{\omega (V_{\rm DCmax}^2 - V_{\rm DCmin}^2)} \\ &= \frac{V_g I_g}{\omega (V_{\rm DCmax}^2 - (V_+ + V_g)^2)}. \end{aligned} \tag{19}$$

Of course, the higher the voltage $V_{\rm DCmax}$, the smaller the capacitor C.

In addition to minimizing the capacitance, it is also important to know the current flowing through the capacitor in order to select an appropriate capacitor. According to the average circuit model of the θ-converter, the current i_C flowing through the capacitor C is

$$i_C = -d_2 i_g - d_4 i_L. \tag{20}$$

When $i_{C_+} = i_L + i_g - I_R$ is controlled to be around zero, the inductor current i_L is given in (13). In this case

$$\begin{aligned} i_C &= -\left(\frac{V_+}{V_{\rm DC}} - \frac{V_g}{V_{\rm DC}} \sin \omega t\right) I_g \sin \omega t \\ &\quad - \left(-I_g \sin \omega t + \frac{V_g I_g}{2V_+}\right) \frac{V_+}{V_{\rm DC}} \\ &= \frac{V_g I_g}{2V_{\rm DC}} (1 - \cos 2\omega t) - \frac{V_g I_g}{2V_{\rm DC}} \\ &= -\frac{V_g I_g}{2V_{\rm DC}} \cos 2\omega t. \end{aligned} \tag{21}$$

It only contains a double-frequency component (ignoring the switching-frequency component). The peak–peak value of the current i_C is

$$\triangle i_C = \frac{V_g I_g}{V_{\rm DC}}. \tag{22}$$

With both (19) and (22), the capacitor C can be selected appropriately.

Note that the current flowing through switches Q_1 and Q_2 are, respectively

$$\begin{aligned} i_{Q_1} &= i_g (1 - d_2) \\ &= I_g \sin \omega t \left(1 - \frac{V_+}{V_{\rm DC}} + \frac{V_g}{V_{\rm DC}} \sin \omega t\right) \\ &= \frac{V_- I_g}{V_{\rm DC}} \sin \omega t + \frac{V_g I_g}{2V_{\rm DC}} - \frac{V_g I_g}{2V_{\rm DC}} \cos 2\omega t \end{aligned} \tag{23}$$

and

$$\begin{aligned} i_{Q_2} &= i_g - i_{Q_1} \\ &= \frac{V_+ I_g}{V_{\rm DC}} \sin \omega t - \frac{V_g I_g}{2V_{\rm DC}} + \frac{V_g I_g}{2V_{\rm DC}} \cos 2\omega t. \end{aligned} \tag{24}$$

Both contain the same double-frequency component

$$i_{\rm 2nd} = -i_C = \frac{V_g I_g}{2V_{\rm DC}} \cos 2\omega t. \tag{25}$$

In other words, the double-frequency ripple current $i_{\rm 2nd}$ directly flows through the capacitor C, switches Q_1 and Q_2, which form a closed current path, as shown in Fig. 1.

B. Selection of the Inductor L_g

The grid inductor L_g is chosen to limit the switching-frequency ripples of the grid current i_g. According to the principle of volt-second balance for the inductor L_g, there is

$$\frac{L_g \triangle i_g}{V_- + V_g \sin \omega t} + \frac{L_g \triangle i_g}{V_+ - V_g \sin \omega t} = \frac{1}{f_s} \tag{26}$$

where $\triangle i_g$ and f_s are the peak–peak switching ripple of the grid current and the switching frequency, respectively. As a result, the required inductance can be found as

$$L_g \geqslant \frac{1}{\triangle i_g f_s V_{\rm DC}} (V_+ V_- - V_g^2 \sin^2 \omega t + (V_+ - V_-) V_g \sin \omega t) \tag{27}$$

for a given $\triangle i_g$. In order to calculate the minimum required value of the L_g, let the derivative of the right side of (27) equal to zero. Then

$$\frac{1}{\triangle i_g f_s V_{\rm DC}} (-2\omega V_g^2 \sin \omega t \cos \omega t + (V_+ - V_-) V_g \omega \cos \omega t) = 0. \tag{28}$$

Hence, the right side of (27) achieves its maximum values when

$$\sin\omega t = \frac{V_+ - V_-}{2V_g}. \tag{29}$$

As a result, the minimum required value of L_g is

$$\begin{aligned} L_{g\min} &= \frac{1}{\triangle i_g f_s V_{\rm DC}}\left(V_+V_- - V_g^2\left(\frac{V_+ - V_-}{2V_g}\right)^2\right) \\ &\quad + \frac{(V_+ - V_-)V_g}{\triangle i_g f_s V_{\rm DC}}\frac{V_+ - V_-}{2V_g} \\ &= \frac{2V_+V_- + V_+^2 + V_-^2}{4\triangle i_g f_s V_{\rm DC}} \\ &= \frac{V_{\rm DC}}{4\triangle i_g f_s}. \end{aligned} \tag{30}$$

Obviously, the $L_{g\min}$ only relates to the $V_{\rm DC}$, $\triangle i_g$, and f_s. How the voltage $V_{\rm DC}$ is divided, i.e., the levels of the V_+ and V_-, does not affect the selection of the L_g, which is reasonable because these levels are controlled by the neutral leg. For a given $\triangle i_g$, the required L_g can be reduced if the $V_{\rm DC}$ is lowered and/or the switching frequency f_s is increased. In order not to affect the reduction of the capacitor C, it is better to reduce the required L_g by increasing the switching frequency f_s, if possible.

C. Selection of the Inductor L_N

The inductor current i_L is controlled to track its reference (13), which consists of the return grid current and the load current, by complementarily switching ON and OFF the switches Q_3 and Q_4. As a result, the i_L contains both low-frequency and switching-frequency components. Both of them are important when selecting the inductor. For the low-frequency component, the maximum absolute value of the current i_L is

$$i_{\rm Lmax} = I_g + \frac{V_gI_g}{2V_+} \tag{31}$$

according to (13). As a result, the selected inductor L_N should have a maximum current rating higher than $I_g + \frac{V_gI_g}{2V_+}$ in order to avoid saturation.

For the switching-frequency component, its peak–peak value is

$$\triangle i_L = \frac{V_+d_3}{L_Nf_s} \tag{32}$$

because of the complementary operation of the neutral leg. Since the voltage V_+ is set according to the load R, $\triangle i_L$ reaches to its maximum value $\triangle i_{\rm Lm}$ when the duty cycle d_3 reaches its maximum value $d_{3\max}$. That is

$$\triangle i_{\rm Lm} = \frac{V_+d_{3\max}}{L_Nf_s} = \frac{V_+(1 - \frac{V_+}{V_{\rm DCmax}})}{L_Nf_s}. \tag{33}$$

The minimum inductance can then be found as

$$L_{\rm Nmin} = \frac{V_+(1 - \frac{V_+}{V_{\rm DCmax}})}{\triangle i_{\rm Lm}f_s}. \tag{34}$$

It can be reduced by increasing the switching frequency f_s. Note that increasing $V_{\rm DCmax}$ also increases the required minimum inductance $L_{\rm Nmin}$, although it helps reduce the capacitance C. It is better to reduce the inductance by increasing the switching frequency f_s, if possible.

D. Selection of the Output Capacitor C_+

Because the system ripple energy is diverted from the capacitor C_+, its main function is to smooth the switching ripples. Assuming the switching ripple current flowing through the current i_L, all flows through the capacitor C_+. Then, the peak–peak switching voltage ripples $\triangle V_+$ across the capacitor C_+ can be estimated as [32]

$$\triangle V_+ = \frac{\triangle i_{\rm Lm}}{8C_+f_s} \tag{35}$$

which gives the capacitance required as

$$C_+ = \frac{\triangle i_{\rm Lm}}{8f_s\triangle V_+}. \tag{36}$$

It is obvious that increasing the switching frequency f_s helps reduce the capacitor C_+, in addition to reducing L_N.

E. Selection of the Switches

The voltage stress and the current stress of the four switches Q_1, Q_2, Q_3, and Q_4 are analyzed below to facilitate the selection of the switches.

1) Voltage Stress: Since the four switches are connected across the whole dc bus, their maximum voltage, i.e., the voltage stress, is the voltage $V_{\rm DC}$, which is the same as the case in the ρ-converter [26]. 1200 V-class switches can be enough for applications having a 110- or 220-V ac input as long as the voltage $V_{\rm DC}$ does not reach 1200 V minus the margin needed; see more details in [26]. Reducing the voltage $V_{\rm DC}$ helps reduce the power losses and the voltage stress, as long as it is higher than $V_+ + V_g$. However, the required capacitor C would increase according to (19) if the $V_{\rm DC}$ is reduced, which is against the objective to reduce the total required capacitance. Clearly, for the θ-converter, there is a trade-off between the reduction of power losses and the reduction of the required capacitance. In light of this, the minimum voltage of the $V_{\rm DC}$ is extracted in this paper, which is then controlled to be slightly higher than $V_+ + V_g$, so that the effect of the voltage $V_{\rm DC}$ on system efficiency can be minimized. while the boost operation of the converter is guaranteed; see more details in Section V.

2) Current Stress: Different from the same voltage stress for all switches, the current stress, i.e., the maximum current, of the four switches are different. For the switches Q_1 and Q_2, the maximum current is I_g because only the grid current is carried. On the other hand, for the switches Q_3 and Q_4, the maximum current is $I_g + \frac{V_gI_g}{2V_+}$ according to (13), which is the sum of the grid current I_g and the load current $I_R = \frac{V_gI_g}{2V_+}$. Since the V_+ is higher than the V_g, there is

$$I_g + \frac{V_gI_g}{2V_+} < 1.5I_g. \tag{37}$$

The higher the voltage V_+, the lower the current stress for Q_3 and Q_4. For very high-current applications, devices with 50%

TABLE I
PARAMETERS OF THE θ-CONVERTER

Parameters	Values
Grid voltage (RMS)	110 V
Line frequency f	50 Hz
Switching frequency f_s	19 kHz
Inductor L_g	4.4 mH
Inductor L_N	2.2 mH
dc output voltage V_+^*	200 V
Load R	220 Ω
Capacitor C_+	5 μF
Capacitor C	6 μF

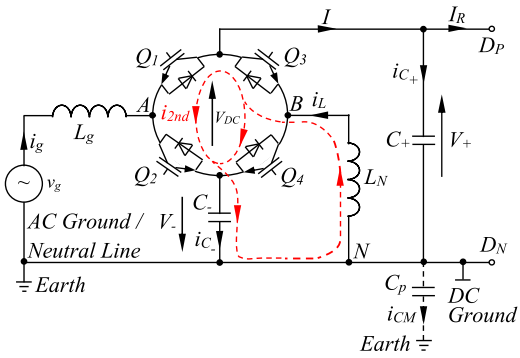

Fig. 3. ρ-converter redrawn from [25] and [26], highlighting the double-frequency current path.

higher current rating could be selected for the switches Q_3 and Q_4 to reduce the cost, but in other applications the same device could be selected for all the switches.

F. Design Example

In order to demonstrate how to select the capacitors and the inductor, a design example is given here. The system parameters are summarized in Table I. Assume $\triangle i_{\mathrm{Lm}} = 4$ A. Then the required minimum inductance is $L_{\mathrm{Nmin}} \approx 1.97$ mH according to (34) for $V_{\mathrm{DCmax}} = 800$ V. Here, a 2.2-mH inductor is used in order to leave some margin. According to (19), there is $C_{\min} = \frac{V_g I_g}{\omega(V_{\mathrm{DCmax}}^2 - (V_+ + V_g)^2)} \approx 2.88$ μF for $I_g = 3$ A. Assume $\triangle V_+ = 6$ V. Then $C_+ = \frac{\triangle i_{\mathrm{Lm}}}{8 f_s \triangle V_+} \approx 4.38$ μF according to (36). In order to leave some margin, a 6-μF and a 5-μF capacitors are selected for C and C_+, respectively.

IV. DETAILED COMPARISON WITH THE ρ-CONVERTER

In this section, the proposed θ-converter is compared to the ρ-converter in [25] and [26], which is redrawn in Fig. 3 for the readers' convenience, in terms of the double-frequency ripple current path, the output voltage ripples, the total capacitance required, the capacitor lifetime, and efficiency. In order for a fair comparison, the dc component and the double-frequency ripple component of the V_{DC} are set to be approximately the same for both, and the references of the output voltages in both converters are set to be the same. In this case, the system ripple energy and the voltage stress of the switches are similar for both converters. In order to facilitate the comparison, a subscription $_\rho$ is added to the variables V_+, $\triangle V_+$, V_-, $\triangle V_-$, V_{DC}, $\triangle V_{\mathrm{DC}}$, Q_1, Q_2, Q_3, Q_4, R, and L_N for the ρ-converter.

A. Path of the Double-Frequency Ripple Current

Because the function of the conversion leg in both converters is the same, the currents following through Q_1 and Q_2 are more or less the same under the assumptions mentioned above. However, the currents following through Q_3 and Q_4 are different. For the θ-converter, the currents flowing through the switches Q_3 and Q_4 are

$$\begin{aligned} i_{Q_3} &= i_L(1-d_4) \\ &= \left(-I_g \sin\omega t + \frac{V_g I_g}{2V_+}\right)\left(1 - \frac{V_+}{V_{\mathrm{DC}}}\right) \\ &= \left(-I_g \sin\omega t + \frac{V_g I_g}{2V_+}\right)\frac{V_-}{V_{\mathrm{DC}}} \end{aligned} \tag{38}$$

and

$$\begin{aligned} i_{Q_4} &= i_L d_4 \\ &= \left(-I_g \sin\omega t + \frac{V_g I_g}{2V_+}\right)\frac{V_+}{V_{\mathrm{DC}}}. \end{aligned} \tag{39}$$

Both do not contain any portion of the double-frequency current $i_{2\mathrm{nd}}$, which confirms the path of $i_{2\mathrm{nd}}$ shown in Fig. 1. For the ρ-converter, the only way to close the path for $i_{2\mathrm{nd}}$ is through Q_3 because the ripple is diverted away from C_+ (and the load). Since the current of the capacitor C_- is controlled to be [26]

$$i_{C-\rho} = -\frac{V_g I_g}{2V_-}\cos 2\omega t = -\frac{V_{\mathrm{DC}}}{V_-} i_{2\mathrm{nd}} \tag{40}$$

which has a larger amplitude than that of $i_{2\mathrm{nd}}$ because $\frac{V_{\mathrm{DC}}}{V_-} > 1$. This current is split into two components: the returning double-frequency $i_{2\mathrm{nd}}$ that flows through Q_3 and the component $\frac{V_g I_g}{2V_{\mathrm{dc}}}\frac{V_+}{V_-}\cos 2\omega t$, that flows through Q_4. Indeed, the currents flowing through the switches Q_3 and Q_4 can be calculated as

$$\begin{aligned} i_{Q_{3\rho}} &= i_{L\rho}(1-d_4) \\ &= \left(-I_g \sin\omega t + \frac{V_g I_g}{2V_-}\cos 2\omega t + \frac{V_g I_g}{2V_+}\right)\left(1 - \frac{V_+}{V_{\mathrm{DC}}}\right) \\ &= -\frac{V_- I_g}{V_{\mathrm{DC}}}\sin\omega t + \frac{V_g I_g}{2V_{\mathrm{DC}}}\cos 2\omega t + \frac{V_g I_g V_-}{2V_+ V_{\mathrm{DC}}} \end{aligned} \tag{41}$$

and

$$\begin{aligned} i_{Q_{4\rho}} &= i_{L\rho} d_4 \\ &= \left(-I_g \sin\omega t + \frac{V_g I_g}{2V_-}\cos 2\omega t + \frac{V_g I_g}{2V_+}\right)\frac{V_+}{V_{\mathrm{DC}}} \\ &= -\frac{V_+ I_g}{V_{\mathrm{DC}}}\sin\omega t + \frac{V_g I_g}{2V_{\mathrm{DC}}}\frac{V_+}{V_-}\cos 2\omega t + \frac{V_g I_g}{2V_{\mathrm{DC}}}. \end{aligned} \tag{42}$$

As a result, the path of the double-frequency current $i_{2\mathrm{nd}}$ of the ρ-converter, as shown in Fig. 3, includes Q_1, Q_2, Q_4 in parallel with C_- and L_N, and Q_3 so it is much longer than that of the proposed θ-converter. Moreover, the double-frequency current flowing through C_- and L_N is larger than $i_{2\mathrm{nd}}$. As summarized in Table II, the number of components that the current $i_{2\mathrm{nd}}$ flows

TABLE II
SUMMARY OF COMPONENTS CARRYING i_{2ND}

	Components	Number of components
θ-converter	Switches Q_1, Q_2, and capacitor C	3
ρ-converter	Switches Q_1, Q_2, Q_3, and Q_4, capacitor C_- and inductor L_N	7

through is 3 for the θ-converter but 7 for the ρ-converter. Since the current $i_{2\text{nd}}$ has to flow through switches Q_1 and Q_2, in order to close the path for $i_{2\text{nd}}$, at least one more component should be connected across the whole dc bus. This means the proposed θ-converter has minimized the number of the components that $i_{2\text{nd}}$ flows through, which reduces the losses and improves the efficiency.

B. Ripples of the Output Voltage V_+

It is worth noting that the returning $i_{2\text{nd}}$ flows through the capacitor C for the θ-converter but through the PWM-controlled switch Q_3 for the ρ-converter. In other words, the ripple current $i_{2\text{nd}}$ of the θ-converter is *continuously* diverted away from the output capacitor, which further reduces the output voltage ripples. However, for the ρ-converter, the ripple current is *discontinuously* diverted away from the output capacitor because the currents flowing through the Switches Q_3 and Q_4 are *discontinuous*. Hence, the performance of the θ-converter to reduce the output voltage ripples is better than that of the ρ-converter.

C. Comparison of Capacitors C_- and C

For the ρ-converter, the system ripple energy E_r is stored in the capacitor C_-. As a result, there is

$$C_- = \frac{V_g I_g}{2\omega V_{-0} \triangle V_-} \tag{43}$$

where V_{-0} and $\triangle V_-$ are the average and peak–peak values of the voltage V_-, respectively. Since the dc bus voltage V_{DC} is assumed to be approximately the same for both converters, there are $V_{-0} \approx V_{\text{DC0}} - V_+$ and $\triangle V_- \approx \triangle V_{\text{DC}}$. (43) can be rewritten as

$$C_- = \frac{V_g I_g}{2\omega (V_{\text{DC0}} - V_+) \triangle V_{\text{DC}}}. \tag{44}$$

For the θ-converter, the ripple energy is stored in the capacitor C. According to (14), the ratio between the two capacitors is

$$\begin{aligned} \frac{C}{C_-} &= \frac{\frac{V_g I_g}{2\omega V_{\text{DC0}} \triangle V_{\text{DC}}}}{\frac{V_g I_g}{2\omega (V_{\text{DC0}} - V_+) \triangle V_{\text{DC}}}} \\ &= \frac{V_{\text{DC0}} - V_+}{V_{\text{DC0}}} \\ &= 1 - \frac{V_+}{V_{\text{DC0}}}. \end{aligned} \tag{45}$$

It is clear that the capacitor C is always smaller than the capacitor C_- because $1 - \frac{V_+}{V_{\text{DC0}}} < 1$.

D. Comparison of the Total Capacitance Required

The dc bus capacitance required for a conventional converter is

$$C_v = \frac{V_g I_g}{2\omega V_{+0} \triangle V_+} \tag{46}$$

corresponding to the required output voltage ripples $\triangle V_+$ for the θ-converter, and is

$$C_{v\rho} = \frac{V_g I_g}{2\omega V_{+0} \triangle V_{+\rho}} \tag{47}$$

corresponding to the required output voltage ripples $\triangle V_{+\rho}$ for the ρ-converter. Note that normally $\triangle V_+ < \triangle V_{+\rho}$ because of the better performance of the θ-converter in reducing output voltage ripples. The ratio of the total capacitance required in the conventional converter to that in the θ-converter is

$$r_\theta = \frac{C_v}{C + C_+}. \tag{48}$$

The ratio of the total capacitance required in the conventional converter to that in the ρ-converter is

$$r_\rho = \frac{C_{v\rho}}{C_- + C_+}. \tag{49}$$

Hence, the ratio of the total capacitance required in the ρ-converter to that in the θ-converter is

$$\begin{aligned} \frac{r_\theta}{r_\rho} &= \frac{C_v}{C + C_+} \times \frac{C_- + C_+}{C_{v\rho}} \\ &= \frac{\triangle V_{+\rho} (C_- + C_+)}{\triangle V_+ (C + C_+)}. \end{aligned} \tag{50}$$

Because $\triangle V_{+\rho} > \triangle V_+$ and $C_- > C$, $\frac{r_\theta}{r_\rho}$ is always greater than one. Accordingly, the total capacitance required in the θ-converter is further reduced with comparison to that in the ρ-converter. For the system with parameters summarized in Table I, there are $C_v \approx 1900$ μF and $C_{v\rho} \approx 740$ μF. As a result, $r_\theta = \frac{C_v}{C + C_+} \approx \frac{1900}{5+6} \approx 172$, $r_\rho = \frac{C_{v\rho}}{C_- + C_+} \approx \frac{740}{5+10} \approx 49$, and $\frac{r_\theta}{r_\rho} \approx 3.5$. Here, $\triangle V_+ = 2$ V and $\triangle V_{+\rho} = 5$ V are used, according to the experimental results to be presented later. In other words, the θ-converter is able to reduce the total capacitance required by about $172\times$ with comparison to the conventional converter and by about $3.5\times$ with comparison to the ρ-converter.

E. Comparison of Capacitor Lifetime

Both converters have two capacitors. The output capacitor C_+ in both converters has the same function, i.e., filtering out switching ripples so that the current flowing through this capacitor is similar for both converters. However, the currents flowing through the capacitors C and C_- are different, although they are used to store the same ripple energy. This is because the voltages across the capacitors C and C_- are different. According to the average circuit model of the ρ-converter [25], there is

$$i_{C_-\rho} = -\frac{V_g I_g}{2V_-} \cos 2\omega t. \tag{51}$$

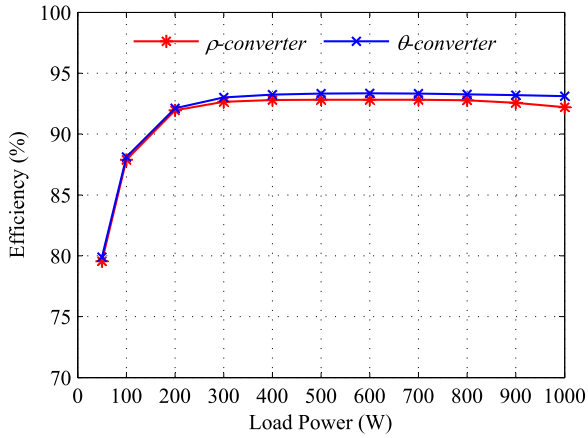

Fig. 4. Efficiency comparison.

According to (21), there is

$$\frac{i_{C_{-\rho}}}{i_C} = \frac{V_{\rm DC}}{V_-}. \tag{52}$$

Since $V_{\rm DC} > V_-$, the current flowing through C_- in the ρ-converter is larger than the current flowing through C in the θ-converter, which means the capacitor C in the θ-converter is expected to have longer lifetime than the capacitor C_- in the ρ-converter in general because of the reduced ripple current.

F. Comparison of Efficiency

Since the number of the components carrying the second-order component is reduced from 7 to 3, the efficiency of the θ-converter should be higher than that of the ρ-converter. In order to compare the efficiency between the two converters, their PLECS simulations were constructed. A 1-kW system was built based on the PLECS and cases with system power ranging from 50 W to 1 kW were tested, with the results shown in Fig. 4. As expected, the efficiency of the θ-converter is always higher than that of the ρ-converter. For example, the efficiency increase is around 0.8% when the system power is 1 kW. In addition, according to the efficiency analysis between the ρ-converter and a conventional full-bridge solution made in [33], the ρ-converter almost always has higher efficiency. As a result, it is obvious that the θ-converter enjoys the highest efficiency among these three systems.

V. Control Design

In general, there are three control objectives, i.e., to maintain the output voltage V_+, to maintain the dc bus voltage $V_{\rm DC}$, and to control the grid current i_g. The first objective can be achieved by controlling the neutral leg, while the others can be achieved by controlling the conversion leg. Note that the control of the two legs are independent from each other and, hence, the design of the controllers is very flexible. Again, only the rectification mode is considered here. The control design follows that in [26] and the readers are encouraged to refer to [26] for more details, including parameter tuning and stability analysis.

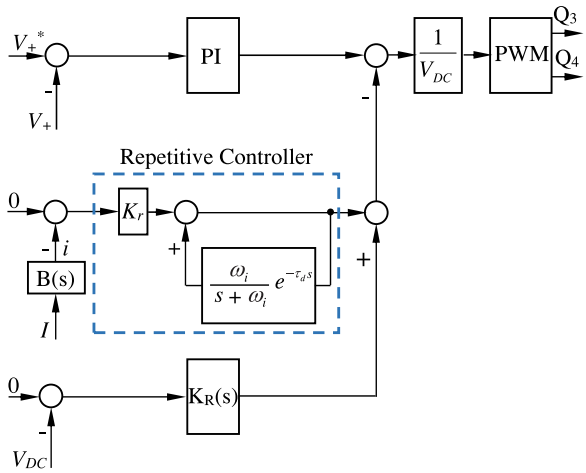

Fig. 5. Controller for the neutral leg.

A. Control of the Neutral Leg

In addition to the switching ripples that are taken care of by the capacitor C_+, there could be two main components in V_+, i.e., a dc component and a low-frequency component. In order to maintain the voltage V_+, both components need to be considered.

1) Regulation of the DC Component of V_+: The dc component of the voltage V_+ needs to be maintained at its reference V_+^* according to the load requirement. In order to achieve this, the voltage V_+ should be measured and its difference from the reference value V_+^* can be fed into a simple proportional-integral (PI) controller, of which the output is scaled before being converted as PWM signals to drive Q_3 and Q_4; see the upper part of Fig. 5.

2) Removal of the Low-Frequency Component in V_+: As analyzed before, it is vital to control the inductor current so that $i_{C_+} = 0$ (ignoring the switching ripples). In order to achieve this, the dc bus current I is measured and its dc component and the high-frequency component are filtered out by a band pass filter, e.g.,

$$B(s) = \frac{10\,000{\rm s}}{(s+10)(s+10\,000)} \tag{53}$$

as shown in Fig. 5. Then, the following repetitive controller:

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}} \tag{54}$$

can be adopted to force the remaining component of the dc bus current I to be zero. Here, the cut-off frequency of the low-pass filter can be chosen as $\omega_i = 2550$ rad/s, and τ_d can be chosen slightly less than the fundamental period $\tau = 0.02$ s as

$$\tau_d = \tau - \frac{1}{\omega_i} = 0.0196\ {\rm s}. \tag{55}$$

See [1] and [34] for more details about the design of repetitive controllers.

3) Removal of the Fundamental Component in V_{dc}: According to (20), the capacitor current i_C may contain a fundamental component because both the grid current i_g and the inductor current i_L have a fundamental component, in particular when

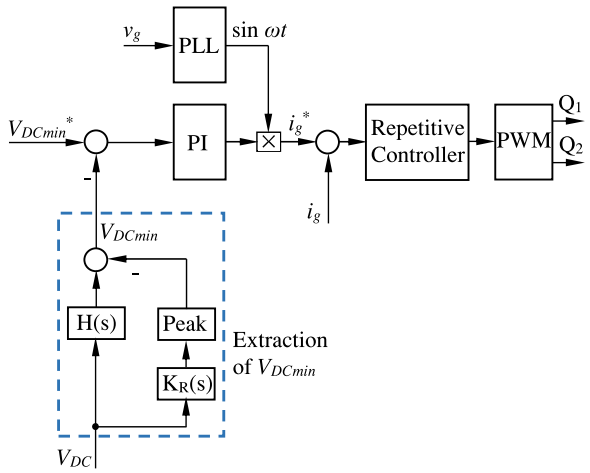

Fig. 6. Controller for the conversion leg.

the inductor current i_L is not regulated to strictly meet condition (13). This should be maintained close to zero. Here, the following resonant controller [35], [36]:

$$K_R(s) = \frac{K_h 2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2} \tag{56}$$

of which the gain at frequency $h\omega$ is K_h with zero phases, is adopted to reduce the fundamental component. In order to tune the controller at the fundamental frequency, ξ and h are chosen as 0.01 and 1, respectively. The gain K_h can be tuned by trial-and-error in experiments.

As shown in Fig. 5, the final duty cycle is formed by adding the outputs of the above three channels. Since the channels are decoupled in the frequency domain, they can be added together without affecting each other. As long as each channel is stable, the stability of the controller can be guaranteed.

B. Control of the Conversion Leg

In order to achieve the unity power factor, it is desirable to control the grid current to be in phase with the grid voltage. Also, the grid current is expected to have low harmonics as well. The repetitive controller used for the neutral leg is adopted here to improve the tracking performance of the grid current. The left work is to generate the reference of the grid current, which should be in phase with the grid voltage. In order to achieve this, the phase signal $\sin\omega t$ of the grid voltage is extracted with a phase-locked-loop [37], as shown in Fig. 6. The peak value of the grid current reference is generated via maintaining the dc bus voltage $V_{\rm DC}$ at its reference value.

It is possible to control the maximum, average, and minimum values of the dc bus voltage $V_{\rm DC}$. Compared to controlling the average voltage, controlling the maximum and minimum dc bus voltages have more benefits. For example, if the maximum voltage is controlled, then the dc bus voltage can always reach the highest level for different loads, which helps reduce the total capacitance required. The approach to control the maximum dc bus voltage is described in [26]. On the other hand, if the minimum voltage is controlled, then the dc bus voltage always has the lowest values for different loads. As mentioned before, a low voltage $V_{\rm DC}$ helps improve system efficiency performance because of reduced switching losses. In light of this, the minimum value of the voltage $V_{\rm DC}$ is controlled at the given minimum dc bus voltage $V_{\rm DCmin}^*$ via a PI controller in this paper. The minimum value of the measured $V_{\rm DC}$ can be obtained by subtracting the peak value $\triangle V_{\rm DC}$ from the average value, which can be easily obtained by using the following hold filter:

$$H(s) = \frac{1 - e^{-\tau s}}{\tau s} \tag{57}$$

as shown in Fig. 6. At the same time, the measured voltage $V_{\rm DC}$ is sent through $K_R(s)$ with $\xi = 0.01, h = 2$, and $K_h = 1$ so that the double-frequency component can be extracted to calculate its peak value $\triangle V_{\rm DC}$.

VI. Experimental Validation

In order to validate the proposed system, extensive experiments were conducted on a prototype based on an intelligent power module controlled by a TMS320F28335 DSP. In the system, four switches with the same rating are used for both legs. The system parameters used for experiments are the same as those summarized in Table I. Here, a 5-μF and a 6-μF metallized polypropylene film capacitors are used for the capacitors C_+ and C, respectively. Compared to conventional converters, the total capacitance required in the θ-converter is reduced by about $172\times$ from 1900 to 11 μF. Both steady-state and transient performance were tested and the corresponding results are shown in Figs. 7–10. Moreover, similar experiments for the ρ-converter were also conducted in order to verify the detailed comparison between the θ-converter and the ρ-converter. The relevant results are shown in Fig. 11.

A. Steady-State Performance

The experimental results for two cases with $V_{\rm DCmin}^* = 450$ V and $V_{\rm DCmin}^* = 500$ V are shown in Fig. 7.

1) Grid Current i_g and dc Voltages V_+ and V_{dc}: As shown in Fig. 7(a), the grid current i_g is always well controlled to be in phase with the grid voltage in both cases. Indeed, the total harmonic distortion (THD) for both cases is around 4%. Since no special measures, e.g., *LCL* filters, were adopted to improve the power quality of the grid current, the 4% THD is already very good. Moreover, the power factor is above 0.99 for both cases.

In addition to the grid current, the dc output voltage V_+ is also well maintained. Importantly, it has very low voltage ripples for both cases, which are about 2 V. Most of the system ripple energy is now stored in the capacitor C instead of the output capacitor C_+ and, hence, the voltage across the capacitor C, i.e., the voltage $V_{\rm DC}$, has large voltage ripples intentionally designed, as shown in Fig. 7(a). According to (15), the voltage ripple $\triangle V_{\rm DC}$ decreases when the $V_{\rm DCmin}$ is increased. Indeed, the voltage $\triangle V_{\rm DC}$ was decreased to 210 from 228 V when $V_{\rm DCmin}^*$ was raised to 500 from 450 V.

2) Currents i_L and i_C: According to (13), the inductor current i_L contains a dc component for the load and a fundamental

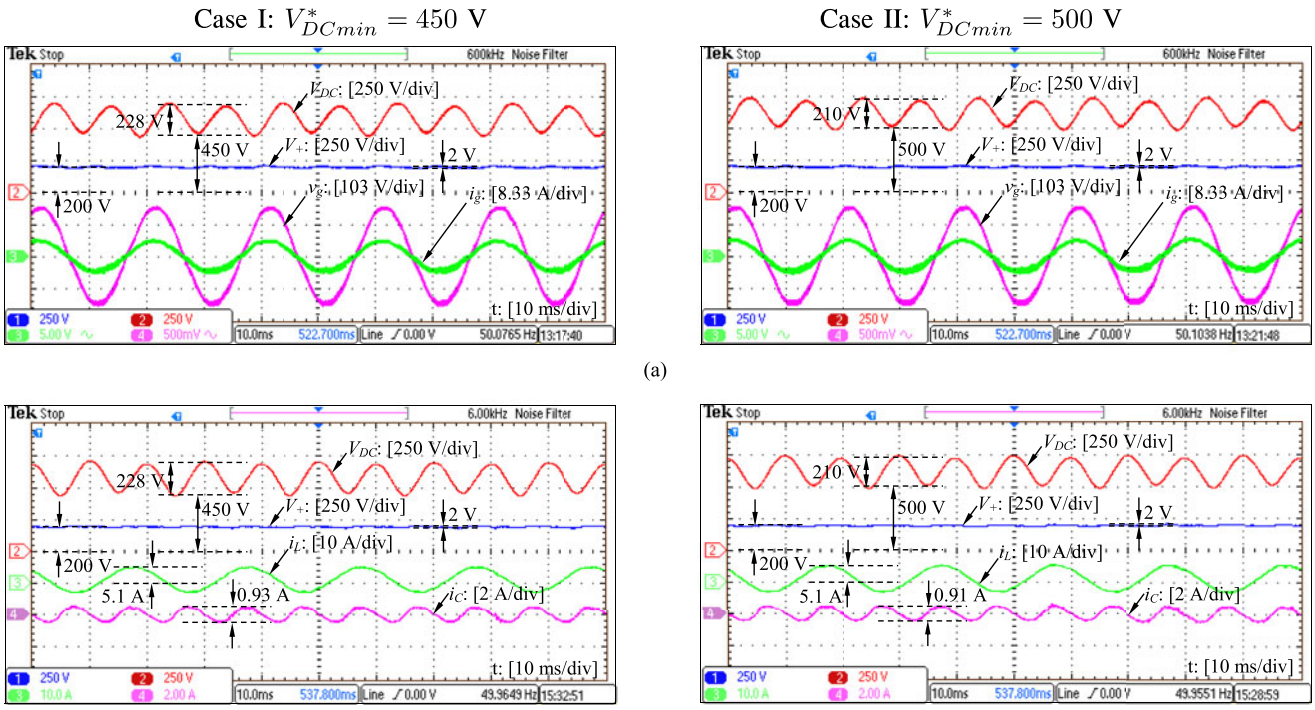

Fig. 7. Steady-state performance of the θ-converter when $V^*_+ = 200$ V: (a) Grid voltage v_g, grid current i_g, and dc voltages V_+ and $V_{\rm DC}$; (b) inductor current i_L and capacitor current i_C.

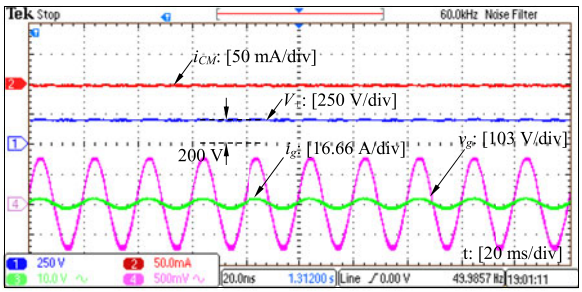

Fig. 8. Measured CM current $i_{\rm CM}$.

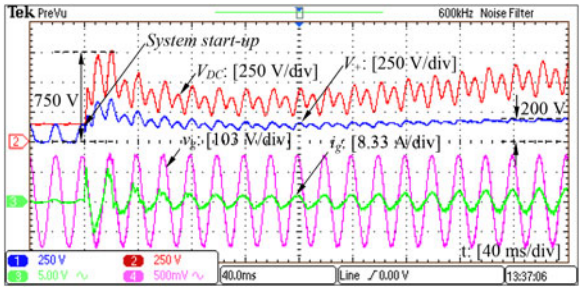

Fig. 9. System start-up.

component for the grid. As shown in Fig. 7(b), the i_L indeed has a dc offset around 0.9 A, which is almost equal to the theoretical dc load current $I_{\rm dc} = \frac{200}{220} \approx 0.909$ A. Also, it can be found that the fundamental component in i_L has the same phase and peak–peak value as the grid current. Note that a 6-kHz noise filter was applied to filter out the switching ripples in the currents in order to clearly see the currents.

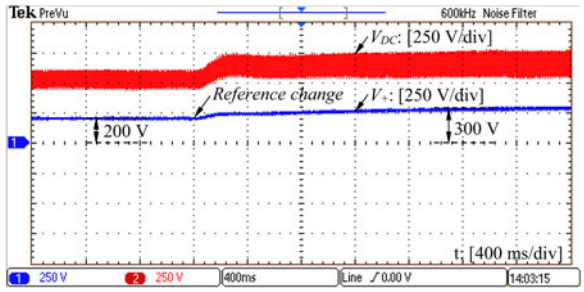

Fig. 10. System transient response when the reference voltage V^*_+ was changed from 200 to 300 V.

As shown in Fig. 7(b), the current i_C mainly consists of a double-frequency component (after filtering out the switching-frequency component). The peak–peak value of the current i_C when $V^*_{\rm DCmin} = 500$ V is lower that when $V^*_{\rm DCmin} = 450$ V, which is consistent with (22).

3) CM Current i_{CM}: A 0.47-μF capacitor was connected as the parasitic capacitor, and the current flowing through this capacitor was measured as the CM current $i_{\rm CM}$, which is shown in Fig. 8. It is clear that the $i_{\rm CM}$ is indeed close to zero. As a result, the objective of eliminating the CM current is achieved without any extra effort.

B. Transient Performance

In order to test the system dynamic performance, two transient cases (system start-up and change of the output voltage) are considered.

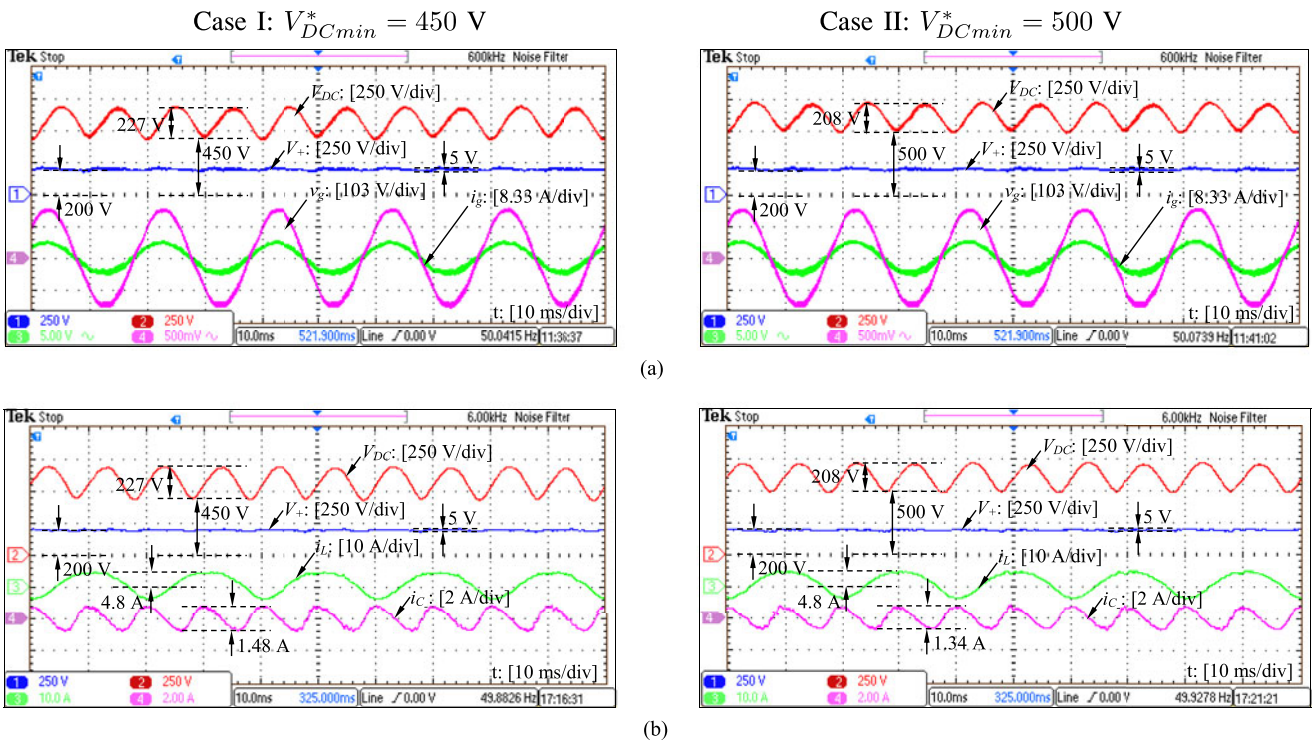

Fig. 11. Steady-state performance of the ρ-converter when $V^*_+ = 200$ V: (a) Grid voltage v_g, grid current i_g, and dc voltages V_+ and $V_{\rm DC}$; (b) inductor current i_L and capacitor current $i_{C\_}$.

1) System Start-Up: Fig. 10 shows the results when the system was disabled first and then was suddenly started. Before the system was started, the converter was operated as a diode bridge rectifier. The voltages V_+, V_-, and $V_{\rm DC}$ are lower than the peak grid voltage, as shown in Fig. 10. Because of the diode-bridge operation, the grid current is distorted. After the system was started, the voltages V_+, V_-, and $V_{\rm dc}$ quickly increased to levels higher than the V_g within one cycle, which ensures the normal boost operation and proper control of the grid current for the converter. The grid current has some distortions in the first few cycles but quickly becomes clean and reaches the steady state.

Importantly, the output voltage V_+ was quickly regulated to its reference value 200 V, and the whole start-up period only took about 12 fundamental cycles. During the start-up, the maximum voltage stress of switches, i.e., the voltage $V_{\rm DC}$, is always lower than 750 V, which is well below the voltage rating 1200 V of the switches.

2) Change of the Output Voltage: Another experiment was carried out by changing the reference output voltage V^*_+ from 200 to 300 V. As shown in Fig. 10, the output voltage V_+ smoothly increased to 300 V without any spikes. It is worth highlighting that the ripples of the voltage V_+ were always maintained at very low levels during the whole transient period. It took about 1.6 s for this transient response, which is because the maximum allowed current of the inductor L_N is limited to about 5 A in the test rig.

C. Comparison With the ρ-Converter

In order to compare the performance improvement of the proposed θ-converter, similar experiments were carried out for the ρ-converter for $V^*_{\rm DCmin} = 450$ V and $V^*_{\rm DCmin} = 500$ V. Note that a $10-\mu$F metallized polypropylene film capacitor is used as the capacitor C_- in the ρ-converter in order to keep the voltage $V_{\rm DC}$ to be similar, which makes the total capacitance to $10+5 = 15\,\mu$F, instead of $6+5 = 11\,\mu$F for the θ-converter.

1) Output Voltage Ripples: Compared to the output voltage V_+ shown in Fig. 7(a), the output voltage V_+ in Fig. 11(a) obviously has larger ripples. To be more precise, the ripples of the output voltage V_+ were increased from 2 to 5 V, while the ripples of the dc bus voltage $V_{\rm DC}$ were kept almost the same on purpose, although the total capacitance used is 36% higher.

2) Current i_L: As discussed before, the only difference of the current i_L in the θ-converter and the ρ-converter is the double-frequency component. As shown in Fig. 11(b), the i_L in the ρ-converter indeed has a double-frequency component, which makes the top of the i_L in the ρ-converter flat. The i_L in the θ-converter does not have this component; see Fig. 7(b).

3) Capacitor Currents i_C and $i_{C\_}$: As can be seen from Figs. 7(b) and 11(b), the peak–peak value of the capacitor current $i_{C\_}$ (about 1.48 A) in the ρ-converter is 59% larger than the capacitor current i_C (about 0.93 A) in the θ-converter. This is consistent with (52).

VII. Conclusion

The θ-converter with a common ac and dc ground has been proposed in this paper to further reduce the total capacitance needed and the voltage ripples. Both isolation transformers and bulky electrolytic capacitors have been removed from the converter. The removal of isolation transformers is naturally achieved because of the common ac and dc ground. At the same

time, the output capacitor is significantly reduced because it does not need to process any low-frequency ripples and only needs to be sized to take care of the switching ripples. All the system ripple energy is stored in a capacitor across the dc bus. Since the dc bus voltage (higher than the output voltage) does not supply any loads, it is designed to have large voltage ripples on purpose, which helps reduce the capacitance. As a result, the total capacitance required is significantly reduced compared to that of conventional converters. Moreover, the normal objectives of conventional converters like unity power factor have been achieved without any compromise. Importantly, all the above objectives are achieved by independently controlling two legs with only four switches and, hence, the θ-converter is very compact. Extensive experimental results have been presented to validate the performance of the converter, with detailed comparison to the ρ-converter.

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