A Three-Phase Bidirectional AC/DC Converter With Y–Δ Connected Transformers

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***Abstract*—This paper proposes a three-phase bidirectional ac/dc converter with Y–Δ connected transformers. The converter achieves both buck-boost ac/dc bidirectional conversion and electrical isolation with the single-stage structure. By introducing three dc–dc transformers, the total power is distributed and the current stress of the rectifier stage decreases. The Y–Δ connected transformers provide extra step-down conversion ratio and facilitate the converters' application in buck conversion. The circuit derivation, operation principles, and control strategy with the SVPWM algorithm are presented. A 3-kW prototype with 380-V dc and a 1.6-kW prototype with 48-V dc were built in the lab and experimental results verify the theoretical analysis well.**

***Index Terms*—Bidirectional ac/dc converter, single-stage structure, SVPWM, Y–Δ connected transformers.**

I. Introduction

While the emergence of severe energy crisis and environment pollution poses austere challenge on people, it brings opportunities for renewable energy power generation. As a typical application, microgrid has attracted more and more attention with its flexible and full use of various renewable energy sources [1]–[5]. The 380-V dc microgrid and ac microgrid are two typical types of microgrid [6]. In the dc microgrid, the grid interface converter implementing three-phase bidirectional ac/dc conversion plays the essential role in energy transfer between the grid and dc bus [7]. In the ac microgrid, a three-phase bidirectional ac/dc converter also finds application for charging and discharging the battery. Besides, in other applications, such as plug-in hybrid electrical vehicles and battery electric vehicles, a bidirectional ac/dc converter is frequently employed as well [8].

The most common solution for the three-phase bidirectional ac/dc converter with 380-V dc and 48-V dc is a two-stage structure composed of a three-phase PWM rectifier and a dc/dc converter to achieve buck conversion [9], [10]. Nevertheless, the decoupling capacitors with large capacitance between two stages always utilize electrolytic capacitors whose life influences the reliability of the converter and the capacitors reduce the power density greatly, which necessitates the research on single-stage three-phase buck-boost ac/dc converters to improve the efficiency and power density [11]–[21].

Three-phase buck-type rectifiers show the advantages on buck ac/dc conversion, but the discontinuous ac current limits the power factor [11]–[14]. The authors in [15] investigated the performance comparison of three-phase soft-switching, bidirectional, isolated ac/dc converter, and evaluates the advantages and drawbacks of the dual-stage and single-stage ac/dc converter. The authors in [16] proposed a novel single-stage high-frequency isolated three-phase PWM rectifier system (VIENNA rectifier II) with sinusoidal input current shape and high-frequency isolation. The authors in [17] presented the design and implementation of a three-phase unity-power-factor single-stage ac–dc converter based on an interleaved flyback topology, which achieves unity power factor and constant output voltage regulation in a single stage. However, the flyback converters operate in the DCM mode and the discontinuous input current necessitates the large *LC* filters, which reduces the power density. A new interleaved three-phase single-stage PFC ac/dc converter was proposed by the authors in [18] to reduce line current harmonics and input electromagnetic interference filter size, but the converter cannot realize bidirectional ac/dc conversion and the output rectification stage does not apply to low-voltage large-current application. The authors in [19] introduced an isolated three-phase rectifier based on the SEPIC converter with high power factor and high-frequency isolation. The converter's DCM operation leads to large input RMS current, which reduces the efficiency.

The three-phase dc-dc converter applies to large power rating application by adopting three dc–dc transformers, which eases the burden of the single component, such as switch, diode, transformer, and so on [22]–[26]. Cha *et al.* proposed a novel three-phase current-fed dc/dc converter with active clamp and a three-phase interleaved dc-dc converter with active clamp which utilize the Δ–Δ connected three-phase transformer [22], [23]. The total power is distributed by three transformers and the current stress of the switches decreases. The authors in [24] focused on a three-phase step-up dc-dc converter with a three-phase Y–Y connected transformer controlled by an average current-mode strategy. It presents greater efficiency with reduced weight and volume as the frequency of input and output current ripple is increased to three times as large as the switching frequency.

Inspired by the three-phase dc–dc converter and the single-stage isolated bidirectional ac/dc converter proposed by the authors in [27], this paper proposes a single-stage three-phase bidirectional ac/dc converter with Y–Δ connected transformers. The converter reduces the current stress of the switches and achieves bidirectional ac/dc conversion as well. The circuit derivation, operation principles, and control strategy with the SVPWM algorithm are presented specifically. A 3-kW/380-V

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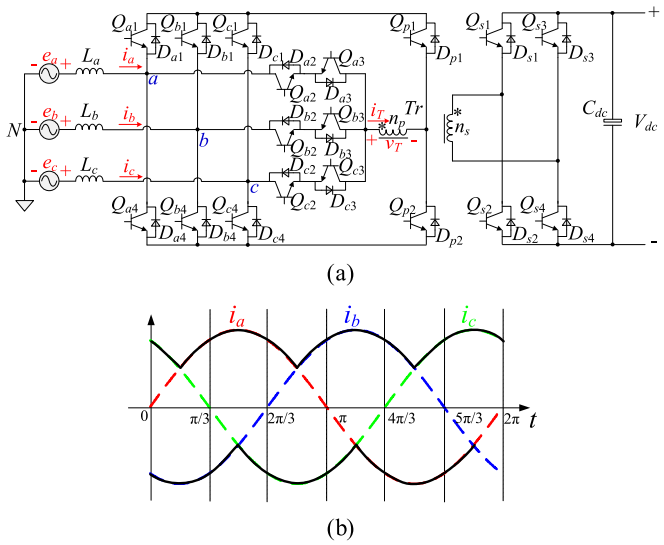


Fig. 1. Single-stage isolated ac/dc converter proposed by the authors in [27].

dc and a 1.6-kW/48-V dc prototype were built in the lab to verify the theoretical analysis.

II. Circuit Derivation and Operation Principles

A. Circuit Derivation

Fig. 1(a) shows the bidirectional ac/dc converter proposed by the authors in [27]. It achieves buck-boost ac/dc bidirectional conversion, sinusoidal ac current, and high-frequency electrical isolation with the single-stage structure. The current flowing through the switches Q_{p1} and Q_{p2} is traced black in Fig. 1(b) and they should deal with the total primary current all the time. It means that the current stress of Q_{p1} and Q_{p2} is larger than that of $Q_{i1\sim4}$ ($i = a, b, c$). Meanwhile, $Q_{s1\sim4}$ are burdened with large current as well in low-voltage large-current applications. In addition, the single dc–dc transformer with the total power is likely to incur the local overheating problem in high-power applications.

To combine the advantages of the three-phase dc/dc converter and the converter in Fig. 1(a), the single-stage three-phase bidirectional ac/dc converters with four different connection types of transformers are derived to reduce the current stress of $Q_{p1,2}$ and $Q_{s1\sim4}$, which is shown in Fig. 2. And two extra transformers are added to share the power. For different voltage ratings, the connection types of transformers vary among Y–Δ, Y–Y, Δ–Y, and Δ–Δ connections. For example, Δ–Y connected transformers bring extra step-up ratio and apply more to high-voltage low-current applications. Similarly, Y–Δ connected transformers bring extra step-down ratio and apply more to buck conversion, which are chosen to do thorough analysis in this paper.

B. Switching States Definition

Fig. 3 shows the proposed single-stage three-phase bidirectional ac/dc converter with Y–Δ connected transformers. The switching states are defined by $j = (S_a S_b S_c)^{\mathrm{ABC}}_{\mathrm{defg/xyz}}$.

1) S_i ($i = a, b, c$) represents the switching states of $Q_{i1\sim4}$. Q_{i1} and Q_{i3}, Q_{i2} and Q_{i4} are complementary switches. Q_{i1} and Q_{i3} are switched ON when $i_i < 0$. Q_{i2} and Q_{i4} are switched ON when $i_i > 0$. When Q_{i2} or Q_{i3} is ON, $S_i = 1$; otherwise, $S_i = 0$.
2) d, e, f, and g represent the switching states of $Q_{p1\sim4}$. When Q_{p1} is ON, $d = 1$; otherwise, $d = 0$. When Q_{p2} is ON, $e = 1$; otherwise, $e = 0$. When Q_{p3} is ON, $f = 1$; otherwise, $f = 0$. When Q_{p4} is ON, $g = 1$; otherwise, $g = 0$.
3) x, y, and z represent the switching states of $Q_{s1\sim6}$. Q_{s1} and Q_{s2}, Q_{s3} and Q_{s4}, Q_{s5} and Q_{s6} are complementary switches. When Q_{s1} is ON, $x = 1$; otherwise, $x = 0$; when Q_{s3} is ON, $y = 1$; otherwise, $y = 0$; when Q_{s5} is ON, $z = 1$; otherwise, $z = 0$.
4) A, B, and C represent the voltage direction of the transformers $a_p, b_p,$ and c_p. The reference positive direction is shown in Fig. 3.

C. Operation Modes

All the reference directions of voltage and current are shown in Fig. 3, and the three-phase current is assumed to be sinusoidal and in phase with the three-phase voltage under the rectifier mode and in opposite phase with the voltage under the inverter mode. Due to the symmetry of the three-phase current, the operation modes when $i_a > 0, i_b < 0, i_c < 0$ are selected for example to do specific analysis.

1) Rectifier Mode: When the converter is not applied in large-current applications under the rectifier mode and the conduction loss of diodes is acceptable, such as 3-kW/380-V output, $Q_{s1\sim6}$ do not need driving signals and $D_{s1\sim6}$ are on for rectification. Therefore, the switching states are simplified to $j = (S_a S_b S_c)^{\mathrm{ABC}}_{\mathrm{defg}}$.

Mode 1 [$j = (100)^{+-0}_{0100}$, Fig. 4(a)]: The switches Q_{a2} and Q_{p2} are switched ON, and the diodes $D_{a3}, D_{b4}, D_{c4}, D_{s1}, D_{s4}$, and D_{s6} are ON. The current flows into the dotted terminal of a_p and out of the dotted terminal of b_p. The energy is transferred from ac side to dc side via phases A and B.

Mode 2 [$j = (100)^{+0-}_{0001}$, Fig. 4(b)]: The switches Q_{a2} and Q_{p4} are switched ON, and the diodes $D_{a3}, D_{b4}, D_{c4}, D_{s1}, D_{s3}$, and D_{s6} are ON. The current flows into the dotted terminal of a_p and out of the dotted terminal of c_p. The energy is transferred from ac side to dc side via phases A and C.

Mode 3 [$j = (110)^{+-0}_{0100}$, Fig. 4(c)]: The switches Q_{a2}, Q_{b3}, and Q_{p2} are switched ON, and the diodes D_{a3}, D_{b2}, D_{c4}, D_{s1}, D_{s4}, and D_{s6} are ON. The current flows into the dotted terminal of a_p and out of the dotted terminal of b_p. The energy is transferred from ac side to dc side via phases A and B.

Mode 4 [$j = (110)^{+0-}_{0001}$, Fig. 4(d)]: The switches Q_{a2}, Q_{b3}, and Q_{p4} are switched ON, and the diodes D_{a3}, D_{b2}, D_{c4}, D_{s1}, D_{s3}, and D_{s6} are ON. The current flows into the dotted terminal of a_p and out of the dotted terminal of c_p. The energy is transferred from ac side to dc side via phases A and C.

Mode 5 [$j = (011)^{-0+}_{0010}$, Fig. 4(e)]: The switches Q_{b3}, Q_{c3}, and Q_{p3} are switched ON, and the diodes D_{a1}, D_{b2}, D_{c2}, D_{s2}, D_{s4}, and D_{s5} are ON. The current flows into the dotted terminal of c_p and out of the dotted terminal of a_p. The energy is transferred from ac side to dc side via phases C and A.

Mode 6 [$j = (011)^{-+0}_{1000}$, Fig. 4(f)]: The switches Q_{b3}, Q_{c3}, and Q_{p1} are switched ON, and the diodes D_{a1}, D_{b2}, D_{c2}, D_{s2}, D_{s3}, and D_{s5} are ON. The current flows into the dotted

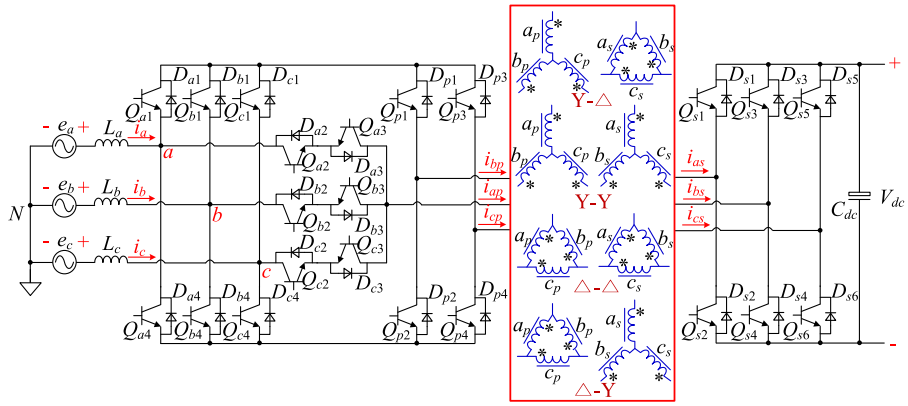


Fig. 2. Single-stage three-phase bidirectional ac/dc converter with four different connection types of transformers.

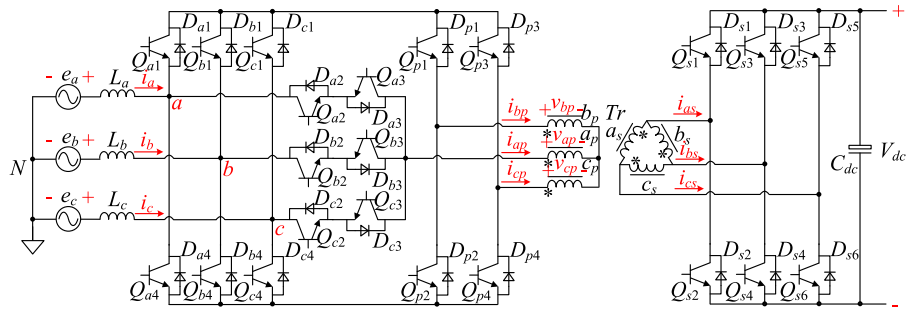


Fig. 3. Proposed single-stage three-phase bidirectional ac/dc converter with Y–Δ connected transformers.

terminal of b_p and out of the dotted terminal of a_p. The energy is transferred from ac side to dc side via phases B and A.

Mode 7 [$j = (111)^{000}_{1100}$ or $j = (111)^{000}_{0011}$, Fig. 4(g)]: The switches $Q_{a2}, Q_{b3}, Q_{c3}, Q_{p1}$, and Q_{p2} or the switches Q_{a2}, Q_{b3}, Q_{c3}, Q_{p3}, and Q_{p4} are switched ON, and the diodes D_{a3}, D_{b2}, and D_{c2} are ON. There is no energy transfer in this mode.

2) Inverter Mode: When the converter operates under the inverter mode, $Q_{p1\sim4}$ do not need driving signals and $D_{p1\sim4}$ are ON for rectification. And the switching states are simplified to $j = (S_a S_b S_c)^{\mathrm{ABC}}_{\mathrm{xyz}}$. As the operation modes of the inverter mode are similar with those of the rectifier mode, only two typical modes when $i_a < 0, i_b > 0, i_c > 0$ are selected to do further analysis.

Mode 1 [($j = (100)^{+-0}_{100}$, Fig. 5(a)]: The switches Q_{s1}, Q_{s4}, Q_{s6}, Q_{a3}, Q_{b4}, and Q_{c4} are switched ON, and the diodes D_{a2} and D_{p2} are ON. The current flows into the dotted terminal of b_p and out of the dotted terminal of a_p. The energy is transferred from dc side to ac side via phases A and B in this mode.

Mode 2 [$j = (111)^{000}_{000}$, Fig. 5(b)]: The switches Q_{s2}, Q_{s4}, Q_{s6}, Q_{a3}, Q_{b2}, and Q_{c2} are switched ON, and the diodes D_{a2}, D_{b3}, and D_{c3} are ON. There is no energy transfer in this mode.

III. SVPWM Algorithm

Considerable research has been done on the SVPWM algorithm for the nonisolated converter [28]–[34], which does not take the voltage–second balance of the transformer and the current direction's influence on the voltage vectors into account. The modified SVPWM algorithm should be put forward for the proposed converter. The voltage vector $\boldsymbol{v}$ is defined as follows:

$$\boldsymbol{v} = v_{aN} + \boldsymbol{\alpha} v_{bN} + \boldsymbol{\alpha}^2 v_{cN} \tag{1}$$

where $\boldsymbol{\alpha} = e^{j\frac{2}{3}\pi}$. The relationship between the switching states and formed voltage vectors is shown in Table I ($i_a > 0, i_b < 0, i_c < 0$). By that analogy, there are altogether six nonzero vectors and the voltage vector plane is divided into six sectors according to the lines with arrows, which is shown in Fig. 6. Within each sector, one phase current direction changes, resulting that the same switching state forms different voltage vectors. Hence, as shown in Fig. 6, each sector should be further divided into two little sectors according to the dotted lines and 12 sectors are considered for vector synthesis, which are numbered by 1–12. Although the division of the sector is the same as that in [27], the difference is that the switching states forming the same voltage vector has changed. Sector 1 (see Fig. 7) is taken for example to give a description of the specific vector synthesis method. To achieve voltage–second balance of three transformers, six nonzero voltage vectors and two zero voltage vectors are chosen to synthesize the target vector

$$\boldsymbol{v} = \left(\delta_{(100)^{+-0}_{0100}} + \delta_{(100)^{+0-}_{0001}} + \delta_{(011)^{-+0}_{1000}} + \delta_{(011)^{-0+}_{0010}}\right)\left(\frac{4}{3}\frac{n_p}{n_s}V_{\mathrm{dc}}\right) + \left(\delta_{(110)^{+-0}_{0100}} + \delta_{(110)^{+0-}_{0001}}\right)\left(-\boldsymbol{\alpha}^2\frac{4}{3}\frac{n_p}{n_s}V_{\mathrm{dc}}\right). \tag{2}$$

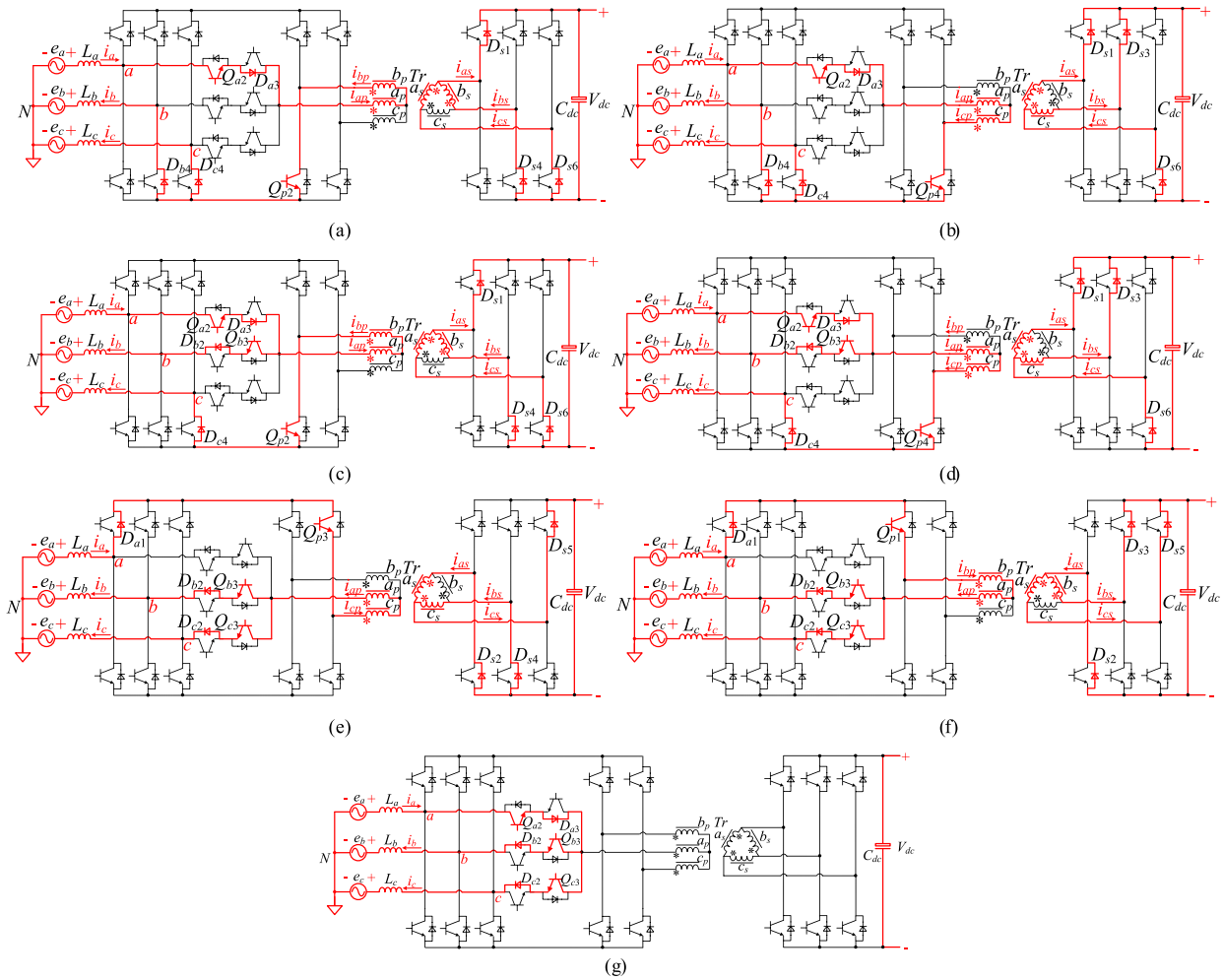


Fig. 4. Operation modes under the rectifier mode.

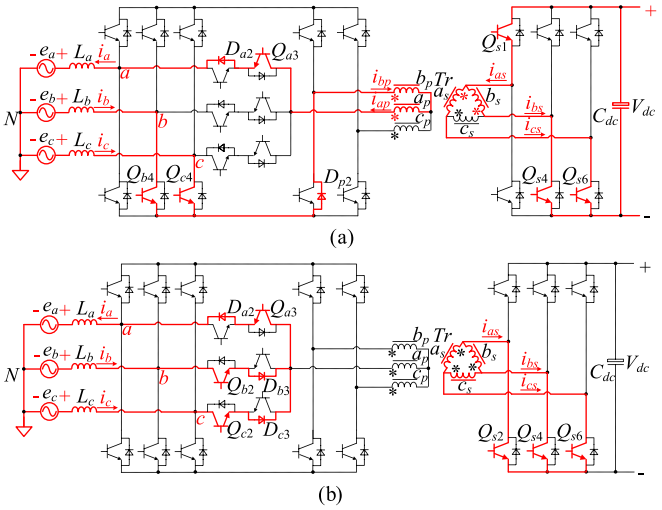


Fig. 5. Operation modes under the inverter mode.

The duty cycle should meet the following equations:

$$\delta_{(100)_{0100}^{+-0}} + \delta_{(100)_{0001}^{+0-}} + \delta_{(011)_{1000}^{-+0}} + \delta_{(011)_{0010}^{-0+}} = \delta_x \quad (3)$$

$$\delta_{(110)_{0100}^{+-0}} + \delta_{(110)_{0001}^{+0-}} = \delta_y \quad (4)$$

$$\delta_{(100)_{0100}^{+-0}} + \delta_{(110)_{0100}^{+-0}} = \delta_{(011)_{1000}^{-+0}} \quad (5)$$

$$\delta_{(100)_{0001}^{+0-}} + \delta_{(110)_{0001}^{+0-}} = \delta_{(011)_{0010}^{-0+}}. \quad (6)$$

The solution of the above equations is not unique. The following solution is chosen in this paper:

$$\delta_{(110)_{0100}^{+-0}} = \delta_{(110)_{0001}^{+0-}} = \frac{\delta_y}{2} \quad (7)$$

$$\delta_{(100)_{0100}^{+-0}} = \delta_{(100)_{0001}^{+0-}} = \frac{\delta_x - \delta_y}{4} \quad (8)$$

$$\delta_{(011)_{1000}^{-+0}} = \delta_{(011)_{0010}^{-0+}} = \frac{\delta_x + \delta_y}{4}. \quad (9)$$

To minimize the switching loss, the switching sequence is as follows:

$$(011)_{1000}^{-+0} \rightarrow (111)_{1100}^{000} \rightarrow (110)_{0100}^{+-0} \rightarrow (100)_{0100}^{+-0}\big|_{T_s/2}$$

$$(100)_{0001}^{+0-} \rightarrow (110)_{0001}^{+0-} \rightarrow (111)_{0011}^{000} \rightarrow (011)_{0010}^{-0+}\big|_{T_s}. \quad (10)$$

Fig. 8 shows the waveforms of driving signals in Sector 1. To form the same voltage vector, the switching states under the inverter mode should be different from the rectifier mode.

TABLE I
VOLTAGE VECTORS VERSUS SWITCHING STATES

S_a	S_b	S_c	d	e	f	g	$Sign\{v_{Ta}\}$	$Sign\{v_{Tb}\}$	$Sign\{v_{Tc}\}$	$\boldsymbol{v}$
0	0	0	0/1	0/1	0/1	0/1	0	0	0	0
0	0	1	0/1	0/1	0/1	0/1	0	0	0	0
0	1	0	0/1	0/1	0/1	0/1	0	0	0	0
0	1	1	1	0	0	0	−	+	0	$(4n_p/3n_s)V_{\rm dc}$
			0	0	1	0	−	0	+	
1	0	0	0	1	0	0	+	−	0	$(4n_p/3n_s)V_{\rm dc}$
			0	0	0	1	+	0	−	
1	0	1	0	1	0	0	+	−	0	$-\alpha\,(4n_p/3n_s)V_{\rm dc}$
			0	0	0	1	+	0	−	
1	1	0	0	1	0	0	+	−	0	$-\alpha^2\,(4n_p/3n_s)\,V_{\rm dc}$
			0	0	0	1	+	0	−	
1	1	1	1	1	0	0	0	0	0	0
			0	0	1	1	0	0	0	

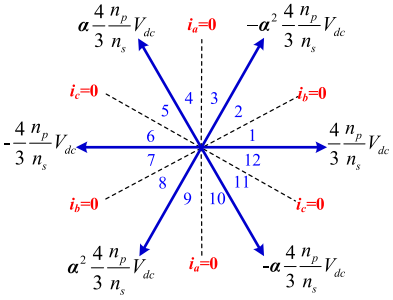


Fig. 6. Sector partition.

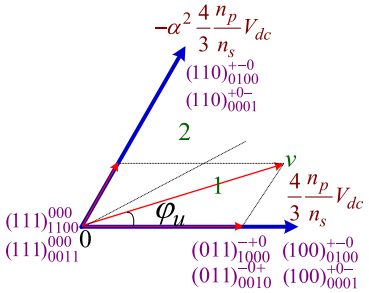


Fig. 7. Vector diagram of Sector 1.

TABLE II
CORRESPONDENCE OF SWITCHING STATES UNDER RECTIFIER MODE AND INVERTER MODE

Rectifier mode	Inverter mode	Rectifier mode	Inverter mode
$(011)^{-+0}_{1000}$	$(011)^{-+0}_{011}$	$(100)^{+0-}_{0001}$	$(100)^{+0-}_{110}$
$(111)^{000}_{1100}$	$(111)^{000}_{111}$	$(110)^{+0-}_{0001}$	$(110)^{+0-}_{110}$
$(110)^{+-0}_{0100}$	$(110)^{+-0}_{100}$	$(111)^{000}_{0011}$	$(111)^{000}_{000}$
$(100)^{+-0}_{0100}$	$(100)^{+-0}_{100}$	$(011)^{-0+}_{0010}$	$(011)^{-0+}_{001}$

The correspondence between them is shown by Table II, and the switching sequence under the inverter mode is shown as follows:

$$(011)^{-+0}_{011}\rightarrow(111)^{000}_{111}\rightarrow(110)^{+-0}_{100}\rightarrow(100)^{+-0}_{100}\Big|_{T_s/2}$$

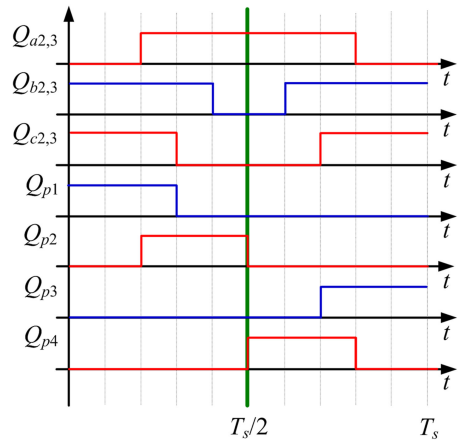


Fig. 8. Driving signals in Sector 1 under the rectifier mode.

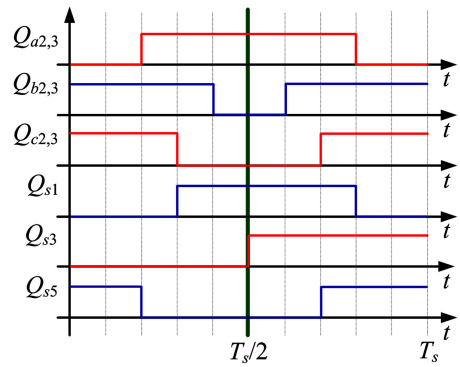


Fig. 9. Driving signals in Sector 1 under the inverter mode.

$$(100)^{+0-}_{110}\rightarrow(110)^{+0-}_{110}\rightarrow(111)^{000}_{000}\rightarrow(011)^{-0+}_{001}\Big|_{T_s}. \quad (11)$$

It is seen from (11) that the switching frequency of the switches $Q_{s5,6}$ is twice that of other switches. So the switching sequence should be adjusted as follows:

$$\begin{aligned}&(011)^{-0+}_{001}\rightarrow(111)^{000}_{000}\rightarrow(110)^{+-0}_{100}\rightarrow(100)^{+-0}_{100}\Big|_{T_s/2}\\&(100)^{+0-}_{110}\rightarrow(110)^{+0-}_{110}\rightarrow(111)^{000}_{111}\rightarrow(011)^{-+0}_{011}\Big|_{T_s}.\end{aligned} \quad (12)$$

Fig. 9 shows the waveforms of driving signals in Sector 1. Through analysis, the driving signals of $Q_{p1\sim4}$ (rectifier mode)

TABLE III
RELATIONSHIP BETWEEN THE DRIVING SIGNALS OF $Q_{x,y}$ AND $Q_{i1\sim4}$

Sector	1	2	3	4	5	6	7	8	9	10	11	12
Q_x	$Q_{c2,3}$				$Q_{a2,3}$				$Q_{b2,3}$			
Q_y	$Q_{a2,3}$			$Q_{b2,3}$				$Q_{c2,3}$				$Q_{a2,3}$

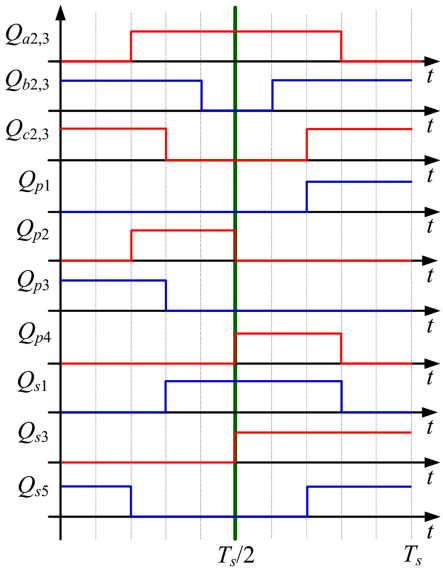


Fig. 10. Driving signals in Sector 1 for synchronous rectification under the rectifier mode.

and $Q_{s1\sim6}$ (inverter mode) are related to the driving signals of $Q_{i1\sim4}$ ($i = a, b, c$). To clarify the relationship among all the driving signals, two intermediate signals Q_x, Q_y are set, whose relationship with the driving signals of $Q_{i1\sim4}$ is shown in Table III. Another signal Q_z is also set, which is at low level in the first half cycle and at high level in the second half cycle. The driving signals of $Q_{p1\sim4}$ and $Q_{s1\sim6}$ can be derived as follows:

$$Q_{p1} = Q_x \,\&\, \overline{Q_z} \tag{13}$$
$$Q_{p2} = Q_y \,\&\, \overline{Q_z} \tag{14}$$
$$Q_{p3} = Q_x \,\&\, Q_z \tag{15}$$
$$Q_{p4} = Q_y \,\&\, Q_z \tag{16}$$
$$Q_{s1} = \overline{Q_{s2}} = (\overline{Q_x} \,\&\, \overline{Q_z}) \parallel (Q_y \,\&\, Q_z) \tag{17}$$
$$Q_{s3} = \overline{Q_{s4}} = Q_z \tag{18}$$
$$Q_{s5} = \overline{Q_{s6}} = (Q_x \& Q_z) \parallel (\overline{Q_y} \& \overline{Q_z}). \tag{19}$$

IV. SYNCHRONOUS RECTIFICATION

The Y–Δ connected transformers bring extra step-down ratio, which makes the converter apply more to low-voltage large-current applications, such as the battery charging and discharging. To reduce the conduction loss under the rectifier mode when the converter deals with the large output current,

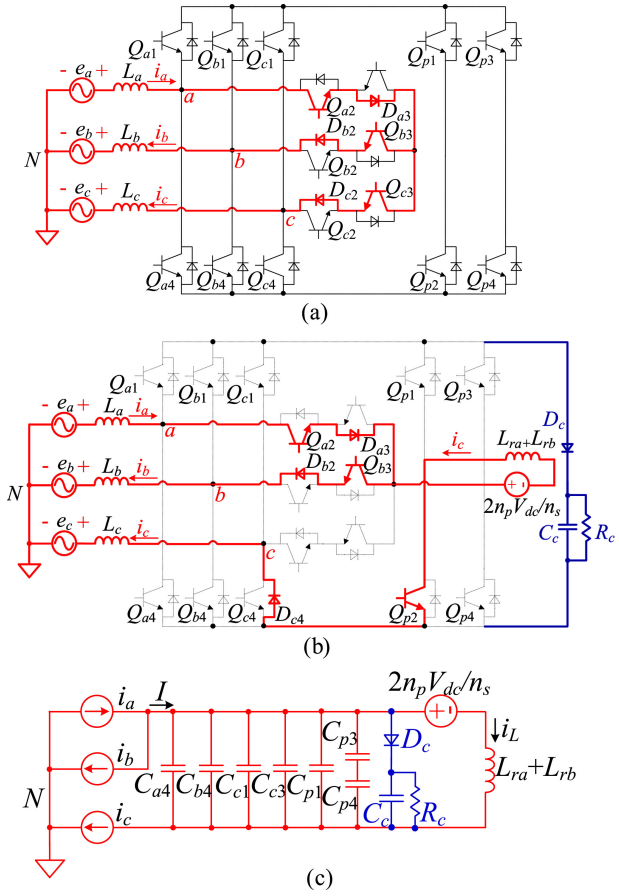


Fig. 11. Equivalent circuits of the switching states $(111)^{000}_{0110/000}$ and $(110)^{+-0}_{0100/100}$.

synchronous rectification should be applied. The switching sequence in Sector 1 is as follows:

$$(011)^{-0+}_{0010/001} \rightarrow (111)^{000}_{0110/000} \rightarrow (110)^{+-0}_{0100/100} \rightarrow (100)^{+-0}_{0100/100}\Big|_{T_s/2} (100)^{+0-}_{0001/110} \rightarrow (110)^{+0-}_{0001/110} \rightarrow (111)^{000}_{1001/111} \rightarrow (011)^{-+0}_{1000/011}\Big|_{T_s}. \tag{20}$$

The driving signals are shown in Fig. 10, and the relationship among all the driving signals is as follows:

$$Q_{p1} = Q_x \,\&\, Q_z \tag{21}$$
$$Q_{p2} = Q_y \,\&\, \overline{Q_z} \tag{22}$$
$$Q_{p3} = Q_x \,\&\, \overline{Q_z} \tag{23}$$
$$Q_{p4} = Q_y \,\&\, Q_z \tag{24}$$
$$Q_{s1} = \overline{Q_{s2}} = (\overline{Q_x} \,\&\, \overline{Q_z}) \parallel (Q_y \,\&\, Q_z) \tag{25}$$
$$Q_{s3} = \overline{Q_{s4}} = Q_z \tag{26}$$
$$Q_{s5} = \overline{Q_{s6}} = (Q_x \,\&\, Q_z) \parallel (\overline{Q_y} \,\&\, \overline{Q_z}). \tag{27}$$

TABLE IV
COMPONENTS COMPARISON

	Topologies	Switches and diodes	Inductors	Capacitors	Transformers
Single-stage bidirectional	The proposed converter	22 switches	$L_{\rm ac}$	$C_{\rm dc}$	3
	The converter by [14]	6 switches + 25 diodes	$L_{\rm ac}, L_{\rm dc}$	$C_{\rm ac}, C_{\rm dc}$	Nonisolated
Single-stage unidirectional	The converter by [19]	3 switches + 15 diodes	$L_{\rm ac}$	$C_{\rm dc}$	3
	VIENNA rectifier II [16]	5 switches + 22 diodes	$L_{\rm ac}$	$C_{\rm dc}$	1
Two-stage bidirectional	T-type rectifier [38]+ Full-bridge converter	20 switches	$L_{\rm ac}, L_{\rm dc}$	$C_{\rm de}, C_{\rm dc}$	1
	Three-phase PWM [35]+ Full-bridge converter	14 switches	$L_{\rm ac}, L_{\rm dc}$	$C_{\rm de}, C_{\rm dc}$	1
	T-type rectifier + Three-phase dc-dc converter	24 switches	$L_{\rm ac}, L_{\rm dc}$	$C_{\rm de}, C_{\rm dc}$	3

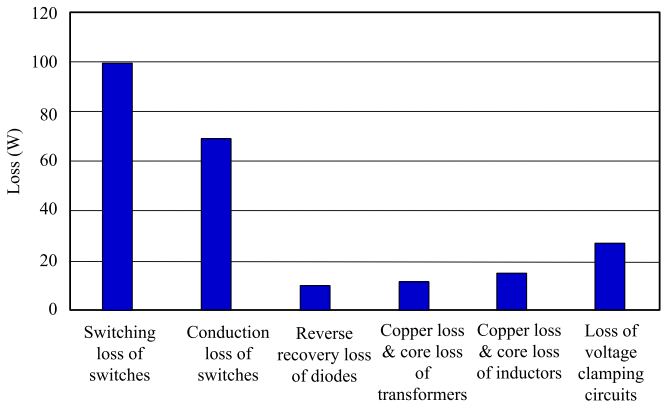


Fig. 12. Calculated power loss distribution of the prototype.

V. CIRCUIT CHARACTERISTICS

A. Influence of the Transformer Leakage Inductor

In practical applications, the transformer is not ideal and introduces a leakage inductor. The leakage inductor influences the mode transition. Taking the rectifier mode with synchronous rectification for example, the equivalent circuits of the switching states $(111)^{000}_{0110/000}$ and $(110)^{+-0}_{0100/100}$ are shown by Fig. 11(a) and (b) separately. When the switching state transfers from $(111)^{000}_{0110/000}$ to $(110)^{+-0}_{0100/100}$, the current i_c should have flown through A-phase and B-phase transformer, Q_{p2} and D_{c4}. However, at the instant of transition, due to the existence of A-phase and B-phase leakage inductor $L_{\rm ra}$ and $L_{\rm rb}$, the current i_c has to find other paths which causes resonance between leakage inductors and junction capacitors of Q_{a4}, Q_{b4}, and some other switches. As shown in Fig. 11(c), the resonance causes voltage spike across some switches, such as Q_{a4}, Q_{b4}, Q_{p1}. The overvoltage has to be limited by the voltage clamping circuit composed of D_c, R_c, and C_c, which is added in Fig. 11(b) [16]. With the proper design of the voltage clamping circuit, a large part of the ac current is fed into C_c, while there is a surge from ac mains. As the authors in [16] described, this should be taken into considerations for the selection of C_c.

The initial voltage across C_c is supposed to be $V_{c\_\rm initial}$. $I_L(0)$ is the initial leakage inductor current when the clamping circuit starts to work. As shown in Fig. 11(b), the voltage across the switches is estimated as follows:

$$v_s(t) \approx \frac{2n_pV_{\rm dc}}{n_s}(1-\cos\omega_r t) + [I - I_L(0)]Z_r\sin\omega_r t + V_{c\_\rm initial}\cos\omega_r t \quad (28)$$

where

$$\omega_r = 1/\sqrt{(L_{\rm ra}+L_{\rm rb})(C_{\rm oss}+C_c)},$$
$$Z_r = \sqrt{(L_{\rm ra}+L_{\rm rb})/(C_{\rm oss}+C_c)},$$

and $C_{\rm oss}$ represents the capacitance value of all the paralleled junction capacitors. When i_L reaches I, the voltage across the switches reaches the peak value $V_{s\_\rm peak}$, and then, D_c is OFF and C_c is discharged via R_c until the next spike. This is a completed clamping process. As the current *I* in Fig. 11(c) varies with different switching states and the RCD clamping process happens several times in one switching cycle, it is hard to perform accurate analysis for the whole power frequency cycle. In order to simplify the analysis, the RCD clamping process is supposed to only happen once in half of the switching cycle. Considering that the maximum current is the peak value of phase current, the value of C_c can be estimated according to (28) with the presupposed $V_{s\_\rm peak}$ and $V_{c\_\rm initial}$. The selection of R_c should guarantee that the voltage of C_c is discharged to $V_{c\_\rm initial}$ within the half switching cycle. If the loss dissipated by R_c cannot be accepted, $V_{c\_\rm initial}$ should be adjusted, and R_c and C_c should be calculated again. The power loss is estimated by considering the current *I* in Fig. 11(c) is the average value of the phase current. The above analysis provides reference for the design of the RCD clamping circuit, but the final value should be adjusted in the experiment.

B. Design Considerations of the Switches

According to Fig. 7, the ac phase voltage's peak value should meet the following equation according to the maximum dc voltage utilization:

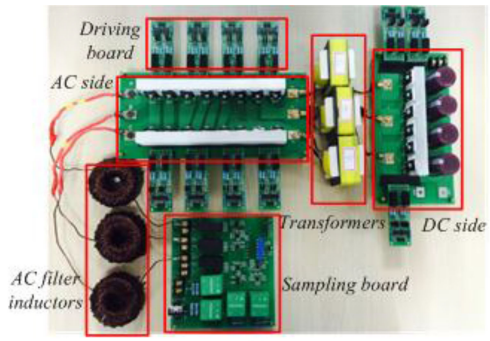
$$v_{\rm ap} \le \frac{2\sqrt{3}}{3}\frac{n_p}{n_s}V_{\rm dc}. \quad (29)$$

Taking the 1.6-kW/48-V dc prototype for example, when $v_{\rm ap}$ is 311 V and $V_{\rm dc}$ is 48V, the turns ratio of the transformer should meet the following equation:

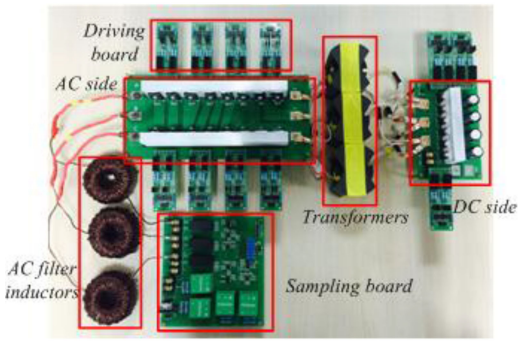
$$\frac{n_p}{n_s} \ge 5.61. \quad (30)$$

So the turns ratio is selected as 31/5. On the premise of proper design of the voltage clamping circuit and regardless of the voltage spike, the voltage stress of the switches $Q_{i1\sim4}(i = a, b, c)$ and $Q_{p1\sim4}$ equals twice the voltage across the primary side of the transformer

$$V_{\max} = 2\times\frac{n_p}{n_s}\times V_{\rm dc} = 595.2\ {\rm V}. \quad (31)$$



(a)



(b)

Fig. 13. Photographs of the prototypes.

TABLE V
COMPONENTS OF TWO PROTOTYPES

3 kW/380-V dc		1.6 kW/48-V dc	
$Q_{i1\sim4}$	IKW25N120H3	$Q_{i1\sim4}$	IKW15N120H3
$Q_{p1\sim4}$	IKW25N120H3	$Q_{p1\sim4}$	IKW15N120H3
$Q_{s1\sim6}$	IKW25N120H3	$Q_{s1\sim6}$	IPP110N20N3G
Inductor magnetic core	KH250–060A	Inductor magnetic core	KH250–060A
Transformer magnetic core	EE65B	Transformer magnetic core	PM74
Driver	HCPL3120	Driver	HCPL3120

If the voltage spike is taken into considerations, the maximum voltage of the switches should be calculated according to (28). Q_{i1} and Q_{i3} are switched ON when $i > 0$, and Q_{i2} and Q_{i4} are switched ON when $i < 0$, and Q_{i1} and Q_{i3} are switched ON complementarily, so are Q_{i2} and Q_{i4}. η is assumed to be 0.86. Therefore, the rms current of $Q_{i1\sim4}$ is estimated as follows:

$$I_{\mathrm{rms\_}Qi1\sim4} = \frac{P_o}{\eta \times 3 \times V_{\mathrm{rms}}} \times \frac{1}{2} = 1.41\ \mathrm{A}. \tag{32}$$

According to Fig. 10, Q_{p1} only conducts during about 0.25 T_s. The rms current of $Q_{p1\sim4}$ should be half of the current in Fig. 1(b)

$$I_{\mathrm{rms\_}Qp1\sim4} = \frac{1}{2} \times \frac{\sqrt{2}P_o}{\eta \times 3 \times V_{\mathrm{in\_rms}}} \times 0.8407 = 1.68\ \mathrm{A}. \tag{33}$$

The peak current of $Q_{i1\sim4}(i = a, b, c)$ and $Q_{p1\sim4}$ is

$$I_{\mathrm{peak\_}Qi1\sim4} = \frac{\sqrt{2}P_o}{\eta \times 3 \times V_{\mathrm{rms}}} = 3.99\ \mathrm{A}. \tag{34}$$

The voltage stress of the switches $Q_{s1\sim6}$ equals the dc-side voltage V_{dc}. Taking Q_{s1} for example, the current flowing through Q_{s1} equals the current of the transformer during about 0.25 T_s and equals twice the current of the transformer during about 0.25 T_s

$$I_{\mathrm{rms\_}Qs1} = \frac{\sqrt{5}}{2} \times \frac{\sqrt{2}P_o}{\eta \times 3 \times V_{\mathrm{in\_rms}}} \times \frac{n_p}{n_s} \times 0.8407 = 23.23\mathrm{A}. \tag{35}$$

Through the above analysis, compared with the traditional three-phase PWM rectifier [35], the proposed converter reduces the current stress of ac-side switches while the voltage stress is the same; and compared with the converter proposed by the authors in [27], the proposed converter reduces the current stress of $Q_{p1\sim2}$ and the dc-side switches as well.

C. Comparison With Some Other Converters

For the situation with three-phase 380 VAC input, 380-V dc and 48-V dc output, three-phase converters are designed in a two-stage concept in most cases. A three-phase PWM rectifier or a T-type rectifier (VIENNA rectifier [36]) is frequently utilized for power factor correction and a dc–dc converter is applied for high-frequency isolation and matching of input and output voltage levels. The components comparison between the proposed converter and some typical converters is shown in Table IV. C_{de} represents the decoupling capacitor between two stages. The diodes of the converter in this paper utilize the paralleled diodes of the IGBTs. The converters proposed by the authors in [14] and [16] have fewer active switches than the proposed converter, but the total number of discrete power semiconductors is larger. Furthermore, the conduction loss of the converters in [14], [16], and [19] is larger as each phase current flows through more diodes. The converter developed by the authors in [14] does not achieve electrical isolation and the converters developed by the authors in [16] and [19] do not achieve bidirectional energy flow. Compared with the two-stage converters, it removes the decoupling capacitors between two stages, and the filter inductor of converter has numerous switches; the current of the ac-side switches and dc-side switches is distributed without considering the current sharing, and the converter is suitable for large output current application.

Fig. 12 shows the calculated loss breakdown for nominal operation of the 3-kW prototype. One reason for limiting the efficiency improvement lies in the voltage clamping circuit. Trying to reduce the leakage inductance can improve the efficiency. With regard to higher efficiency, a flyback converter should be provided instead of the resistor R_c as an alternative solution, which is presented in detail in [16] and [37]. Another reason is that the switching loss and the conduction loss of IGBTs occupies a large part of all the power loss, and SiC-MOSFET can be employed instead to further improve the efficiency.

VI. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a 3-kW prototype with 380-V dc and a 1.6-kW prototype with 48-V dc controlled by TMS320F2812 were built in the lab. Fig. 13(a) and (b) shows

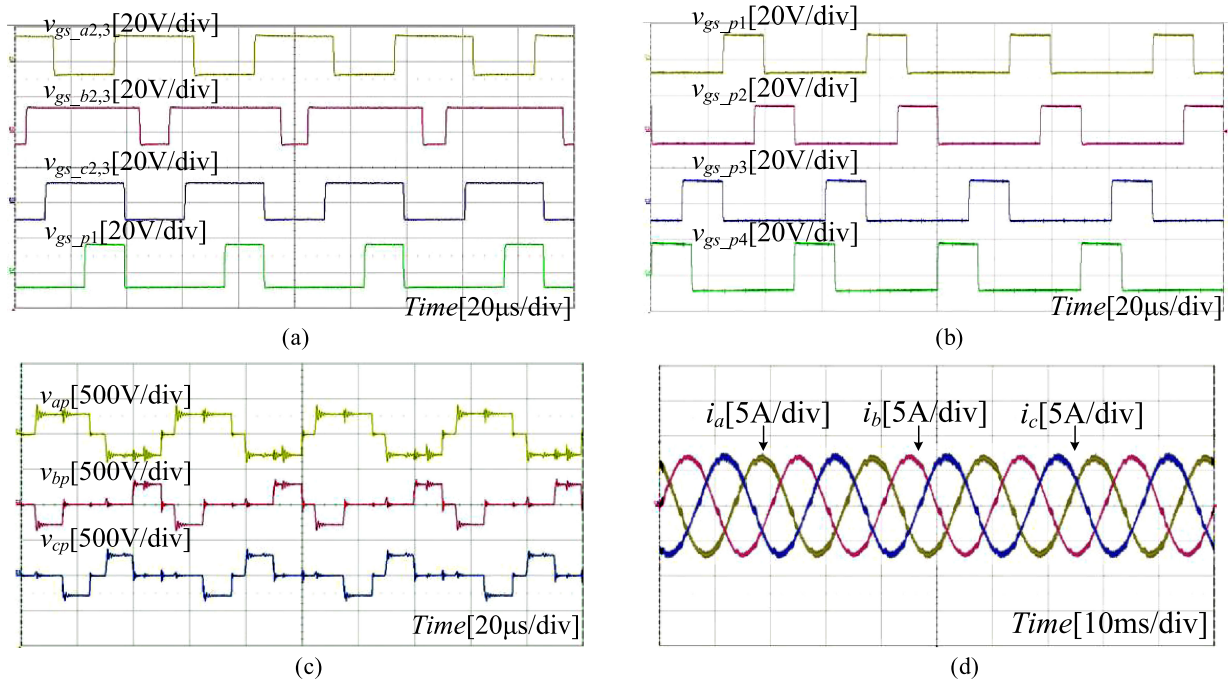


Fig. 14. Experimental results of the 3 kW/380-V dc prototype under the rectifier mode.

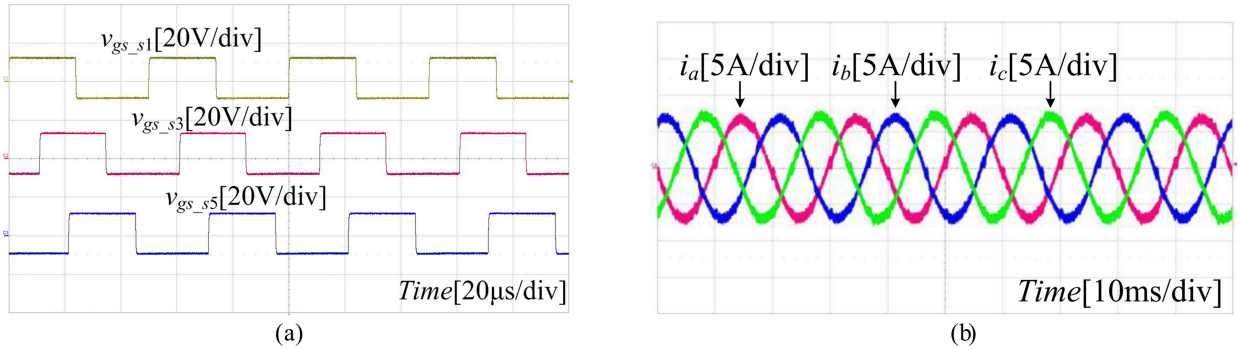


Fig. 15. Experimental results of the 3 kW/380-V dc prototype under the inverter mode.

the photographs of the 380-V dc and 48-V dc prototypes separately. The components of two prototypes are listed in Table V. The parameters and specifications are as follows:

1) AC line voltage: $v_{\rm ac} = 380$ V;
2) AC voltage frequency: $f = 50$ Hz;
3) DC voltage: $V_{\rm dc1} = 380$ V; $V_{\rm dc2} = 48$ V;
4) rated output power: $P_{o1} = 3$ kW(380-V dc); $P_{o2} = 1.6$ kW(48-V dc);
5) filter inductor: $L_a = L_b = L_c = 3.3$ mH;
6) filter capacitor: $C_{\rm dc} = 330\ \mu{\rm F} * 4$;
7) transformer turns ratio: $n_p/n_s = 48/64$(380-V dc); $n_p/n_s = 31/5$(48-V dc);
8) switching frequency: $f_s = 20$ kHz.

Fig. 14 shows the experimental results of the 3-kW/380-V dc prototype under the rectifier mode. Fig. 14(a) and (b) shows the driving signals of the switches in Sector 1. Fig. 14(a) shows the waveforms of $v_{\rm gs\_a2,3}$, $v_{\rm gs\_b2,3}$, $v_{\rm gs\_c2,3}$, and $v_{\rm gs\_p1}$. Fig. 14(b) shows the waveforms of $v_{\rm gs\_p1}$, $v_{\rm gs\_p2}$, $v_{\rm gs\_p3}$, and $v_{\rm gs\_p4}$. The driving sequence is consistent with Fig. 8. Fig. 14(c) and (d) shows the waveforms of the three-phase input current and the voltage across three transformers. It is seen that three transformers achieve voltage–second balance.

Fig. 15 shows the experimental results of the 3-kW/380-V dc prototype under the inverter mode. Fig. 15(a) shows the waveforms of $v_{\rm gs\_s1}$, $v_{\rm gs\_s3}$, and $v_{\rm gs\_s5}$. Fig. 15(b) shows the current waveforms of the ac side. Fig. 16 shows the experimental results of the 1.6-kW/48-V dc prototype. Fig. 16(a) shows three-phase current waveforms and Fig. 16(b) shows the voltage waveforms across the secondary side of three transformers. Fig. 16(c) shows the current waveforms of three transformers. Fig. 16(d) shows the waveforms of $v_{\rm ds\_a1}$, $v_{\rm ds\_a3}$, $v_{\rm ds\_p1}$, and $v_{\rm ds\_p2}$. Fig. 16(e) shows the waveforms of $v_{\rm ds\_a2}$, $v_{\rm ds\_a4}$, $v_{\rm ds\_p3}$, and $v_{\rm ds\_p4}$. Fig. 16(f) shows the waveforms of $v_{\rm ds\_s1}$, $v_{\rm ds\_s3}$, and $v_{\rm ds\_s5}$. Fig. 17(a) and (b) shows the efficiency curves of 3-kW/380-V dc prototype and 1.6-kW/48-V dc prototype separately. It is concluded that the experimental results verify the theoretical analysis well.

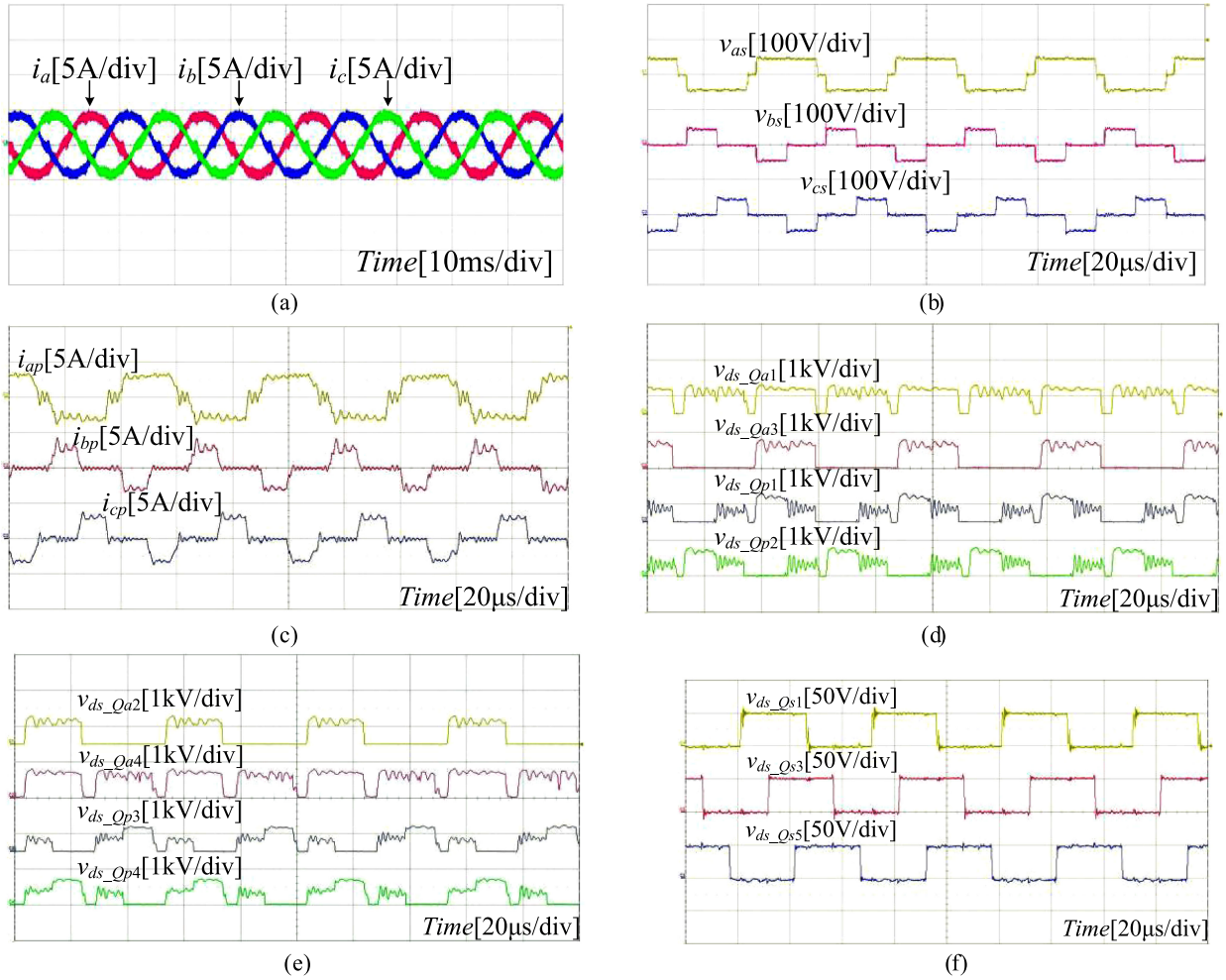


Fig. 16. Experimental results of the 1.6 kW/48-V dc prototype.

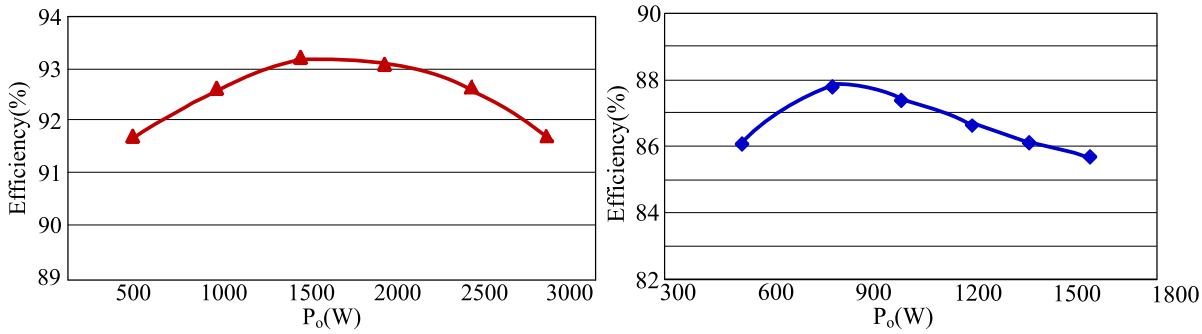


Fig. 17. Efficiency curves of two prototypes.

VII. Conclusion

This paper proposes a three-phase bidirectional ac/dc converter with Y–Δ connected transformers. It achieves bidirectional energy flow, high-frequency electrical isolation, and unity power factor control. The connection types and turns ratio of the transformers can be adjusted for different output voltage levels. The modified SVPWM algorithm is proposed to achieve the voltage–second balance of the transformers. The main circuit, operation modes, and SVPWM algorithm are presented specifically. A 3-kW/380-V dc prototype and a 1.6-kW/48-V dc prototype were built in the lab and experimental results verify the theoretical analysis.

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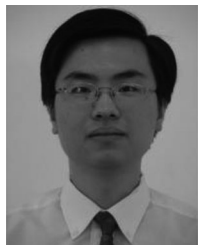

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