# Letters

## A Real-Time Variable Turn-Off Current Strategy for a PFC Converter With Voltage Spike Limitation and Efficiency Improvement

Qunfang Wu, Qin Wang, Jialin Xu, and Lan Xiao

***Abstract*—The voltage source driver (VSD) is widely used in a conventional gate drive circuit of the power factor correction (PFC) converter. However, the fixed drive current of the VSD circuit could not optimize the switching losses, and the turn-off voltage spike across the power switch is freewill. In this letter, a real-time variable turn-off current strategy of a power switch for the PFC converter is presented. The turn-off current can be modulated real timely with the input voltage varying periodically, and the voltage spike across power switch can be controlled under the peak value that set at the peak input voltage region. The operation principle, design considerations, and the analysis of turn-off switching losses with the proposed strategy are presented by a boost PFC converter in detail. Furthermore, a prototype of the boost PFC converter was built to verify the effectiveness of the proposed strategy. As a result, the turn-off voltage spike is well limited and the efficiency is effectively improved compared with the VSD. The proposed idea can be also further extended to any other PFC converters.**

***Index Terms*—Efficiency improvement, PFC converter, real timely, turn-off current, voltage spike limitation.**

### I. Introduction

THE gate driver has a great influence on the switching speed, switching losses, current/voltage variations (di/dt and dv/dt), efficiency, and electromagnetic interference (EMI) of the converters [1], [2]. In ac–dc applications, the power factor correction (PFC) technique is used widely [3], [4], where the conventional voltage source drivers (VSDs) are most commonly utilized. However, the VSDs have a big defect that all the gate driver energy dissipates through the drive resistance and the fixed drive current cannot optimize the switching losses of the power switch [5].

In order to improve the performance of VSDs, resonant gate drivers (RGDs) have been proposed to recycle the gate energy dissipation in conventional VSDs [6], [7], whose basic principle is to use the *LC* resonance to recover the gate drive energy stored in the parasitic capacitor of the power MOSFET to minimize the excessive drive losses. Similarly to the RGDs, current-source drivers (CSDs) have been proposed in [8]–[10], which can reduce the switching losses by generating the constant drive current to charge and discharge the gate capacitance to accelerate the turn-on/turn-off speed. For this technology, the switching losses are reduced. However, the gate drive losses needed to be compromised in the design of the CSDs. To optimize this issue, the adaptive drive current inherently depending on the switching current of the power switch for a boost PFC converter is built [11], [12]. Nevertheless, they ignore the problem that the stronger drive current means faster switching speed, also means higher current/voltage spike during the switching transient, which leads to the problem of EMI. In addition, although the current/voltage variations di/dt and dv/dt could be controlled in [13] and [14] and the current /voltage spike can be limited, they lose the merits of the CSDs.

In view of these problems, a new turn-off current strategy for the PFC converter is proposed in this letter. The turn-off current of the power switch is real-time modulating with the change of the input voltage. The turn-off switching losses can be reduced, and simultaneously, the voltage spike can be limited to a decent value. The drive principle, design consideration, turn-off switching losses analysis, and gate drive circuit are discussed at length. Finally, the experimental prototype with a boost PFC converter was built and the key waveforms were tested and compared to the conventional VSDs. The results are presented to verify the validity of the proposed drive strategy.

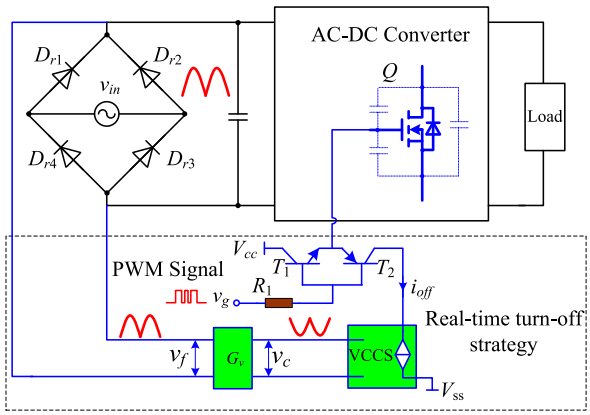


Fig. 1. Proposed turn-off strategy.

### II. Proposed Turn-Off Drive Strategy

#### A. Proposed Turn-Off Strategy

Fig. 1 shows the typical PFC structure and the proposed real-time turn-off strategy. The real-time turn-off part includes a regulator $G_v$, a voltage-controlled current source (VCCS), and

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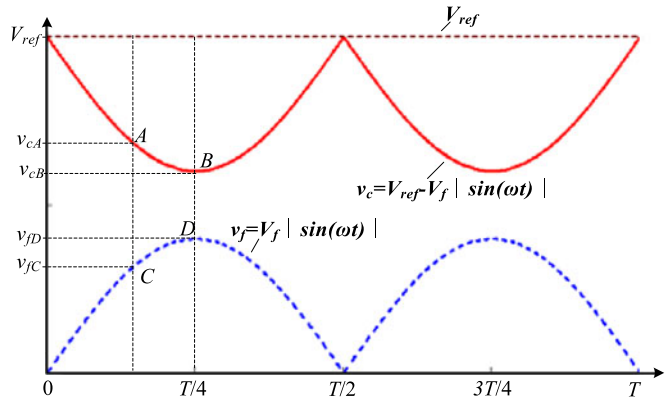


Fig. 2. Relationship between control signals.

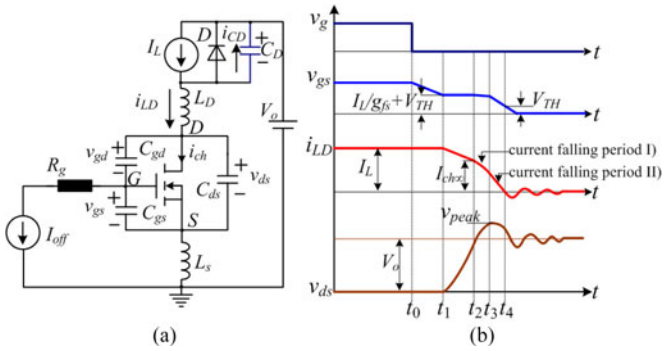


Fig. 3. (a) Equivalent switching circuit model of the boost converter. (b) Qualitative waveforms of the turn-off transient.

the conventional drive circuit. As shown in Fig. 1, the VCCS is in series with the transistor $T_2$ in the turn-off loop of the power switch $Q$ (MOSFET). The regulator $G_v$ adjusts the uncontrolled rectifier output voltage $v_f$ reversely and outputs the control signal $v_c$. By the VCCS, the signal $v_c$ determines the turn-off current $i_{\rm off}$. $i_{\rm off}$ will vary with the change of $v_f$. Therefore, the real-time variable turn-off strategy for the power switch $Q$ can be realized.

It is worth noticing that the faster turn-off speed is, the lower switching losses will be. However, the faster turn-off speed must result in higher voltage spike. Therefore, the principle of the proposed turn-off strategy is that the turn-off current $i_{\rm off}$ is modulated by $v_f$ real timely and simultaneously and the voltage spike should be controlled under a reasonable peak value to ensure the effective operation of the power switch. With the proposed strategy, the relationship between control signals is shown in Fig. 2. $V_{\rm ref}$ is a constant voltage. $v_f = V_f \mid \sin(\omega t) \mid$, where $v_f$ is the amplitude of $v_f$ and $\omega = 2\pi \bullet f_L$, $f_L$ is the line frequency. From Fig. 2, the signal $v_c$ can be derived as $V_{\rm ref} - V_f \mid \sin(\omega t) \mid$, it means that the control voltage $v_c$ will be higher when the input voltage is lower, also means the turn-off current $i_{\rm off}$ will be larger. For example, C and D are two points on the curve $v_f$ in a half-line period $T/2$. Correspondingly, $v_{\rm cA}$ and $v_{\rm cB}$ are the control voltages of the VCCS. Because of $v_{\rm fD} > v_{\rm fC}$, the control voltage can be designed as $v_{\rm cB} < v_{\rm cA}$, which means $i_{\rm offA} > i_{\rm offB}$. This implies that the switching speed at point A is faster than point B, and the overlapping area of the drain–current and the drain–source voltage during switching transient can be smaller. Therefore, the turn-off switching losses will be lower and the efficiency can be improved.

### B. Analytical Modeling of Turn-Off Transition

The key point of the modeling is to investigate the relationship among the switching losses, voltage spike, and turn-off current. Although the relationship between switching losses and drive gate current has been discussed at length in [11] and [12], and the main drawback is that they ignore the larger drive current that leads to higher voltage spike. In this section, a typical boost PFC converter is employed to clarify the relationship between the voltage spike and gate drive current during the turn-off process. The analytical modeling of switching transition with CSD has been discussed in detail in [15] and [16], however, they neglect the parasitic capacitor of diode $D$, which has an influence on the switching transient in the real circuit. In this letter, the turn-off transition modeling considers the effect of the parasitic capacitor of the diode. The simplified equivalent circuit of the boost converter is shown in Fig. 2(a), where $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ are the parasitic capacitors of the MOSFET, $L_D$ and $L_S$ are the switching loop inductance including the drain stray inductance and the common source inductance, $R_g$ is the gate drive resistor including the internal parasitic resistor and the external gate drive resistor, the filter inductor and gate turn-off current are replaced by two current sources ($I_L$ and $I_{\rm off}$), in addition, it is noted that the diode $D$ is modeled by a diode in parallel with its parasitic capacitance $C_D$.

To simplify the analysis of the turn-off transient, the following assumptions are made:

1) $C_{\rm iss} = C_{\rm gd} + C_{\rm gs}$ and $C_{\rm oss} = C_{\rm gd} + C_{\rm ds}$ are represented the input and output capacitances of the MOSFET, respectively;
2) $i_{\rm ch} = g_{\rm fs}(v_{\rm gs} - V_{\rm TH})$, where $i_{\rm ch}$, $g_{\rm fs}$, and $V_{\rm TH}$ are the MOSFET channel instantaneous current, transconductance, and threshold voltage, respectively;
3) when $v_{\rm gs} < V_{\rm th}$, $i_{\rm ch} = 0$ and MOSFET is OFF.

Based on the assumptions, the qualitative waveforms of the turn-off transient are shown in Fig. 2(b). At $t_0$, the PWM signal $v_g$ is set as zero. The turn-off current $i_{\rm off}$ begins to discharge the input capacitor $C_{\rm iss}$ and the voltage $v_{\rm gs}$ begins to fall. At $t_1$, when $v_{\rm gs}$ falls down to $I_L/g_{\rm fs} + V_{\rm TH}$, the MOSFET begins to operate in the saturation region. The channel instantaneous current $i_{\rm ch}$ decreases suddenly and the excess current $i_L - i_{\rm ch} - i_{\rm CD}$ charges the capacitors $C_{\rm gd}$ and $C_{\rm ds}$. Simultaneously, the voltage $v_{\rm ds}$ starts to increase until it reaches $V_o$ and the current $i_{\rm LD}$ begins to decrease from $I_L$. In this interval, the parasitic capacitor $C_D$ of the diode discharges from $V_o$ to zero.

It is worth mentioning that the diode $D$ ceases to block the voltage and the inductor current $I_L$ starts to divert from the MOSFET to the diode after the voltage of $C_D$ drops to zero. However, since the power loop inductors ($L_D + L_S$) impede a sudden change in the drain current, the drain–source voltage $v_{\rm ds}$ continues increasing to the peak voltage. Commonly, the peak voltage of $v_{\rm ds}$ can be solved by the circuit equations (1)–(4),

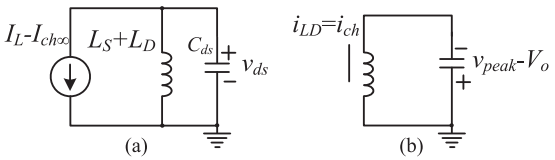


Fig. 4. Equivalent circuits: (a) for current falling period I, and (b) for current falling period II.

from Fig. 2(a)

$$I_{\rm off} = -C_{\rm gs}\frac{dv_{\rm gs}}{dt} + C_{\rm gd}\frac{dv_{\rm gd}}{dt} \tag{1}$$

$$i_{\rm LD} = g_{\rm fs}(v_{\rm gs} - V_{\rm TH}) + C_{\rm gd}\frac{dv_{\rm gd}}{dt} + C_{\rm ds}\frac{dv_{\rm ds}}{dt} \tag{2}$$

$$v_{\rm ds} = V_o + L_D\frac{di_{\rm LD}}{dt} + L_s\frac{d(i_{\rm LD} - I_{\rm off})}{dt}$$

$$= V_o + (L_D + L_S)\frac{di_{\rm LD}}{dt} \tag{3}$$

$$v_{\rm ds} = v_{\rm gs} + v_{\rm gd}. \tag{4}$$

However, the solution of (1)–(4) is very complicated and the results are not convenient to analyze. It is necessary to scrutinize from another perspective. Here, the analytical method in [17] is adopted. This interval can be subdivided into two stages including 1) current falling period and 2) current falling period. The specific demonstration is as follows.

*1) Current Falling Period (I) [t2–t3]:* In this short moment, assume that the gate voltage keeps constant as well as the channel current. The circuit condition can be simplified by the independent current and the voltage source in the circuit, which is a simple parallel resonant circuit as shown in Fig. 4(a). It is clear that the inductors $L_D + L_S$ will resonate with capacitor $C_{\rm ds}$, thereby, $v_{\rm ds}$ can be expressed from Fig. 4(a)

$$v_{\rm ds}(t) = V_o + (I_L - I_{\rm ch\infty})(L_D + L_S)\frac{1}{\sqrt{(L_D + L_S)C_{\rm ds}}} \times \sin\left[\frac{1}{\sqrt{(L_D + L_S)C_{\rm ds}}}(t - t_2)\right] \tag{5}$$

where

$$I_{\rm ch\infty} = 2\left(\frac{I_L}{g_{\rm fs}} + V_{\rm TH}\right) - \frac{I_{\rm off}(C_D + C_{\rm oss})}{g_{\rm fs}C_{\rm gd}} \tag{6}$$

$I_{\rm ch\infty}$ is the approximation value of the channel current at $t_2$, which is derived based on [17].

This stage ends when $i_{\rm LD}$ arrives at the channel current $I_{\rm ch\infty}$ at $t_3$, the voltage $v_{\rm ds}$ has reached its peak value $v_{\rm peak}$ and it can be given by

$$v_{\rm peak} = v_{\rm ds}(t_3) = V_o + (I_L - I_{\rm ch\infty})(L_D + L_S) \times \frac{1}{\sqrt{(L_D + L_S)C_{\rm ds}}} \times \sin\left[\frac{1}{\sqrt{(L_D + L_S)C_{\rm ds}}}(t_3 - t_2)\right] \tag{7}$$

TABLE I
RELATIONAL PARAMETERS OF THE BOOST PFC CONVERTER

| | | | |
|---|---|---|---|
| Input voltage | 180–265 VAC | Inductor $L$ | 1mH |
| Rated power | 1.5 kW | $L_D + L_S$ (approximate value) | 1.5$\mu$H |
| Output voltage | 380 VDC | Input capacitor $C_f$ | 1$\mu$F |
| Switching frequency | 250 KHz | | |
| MOSFET(Q):SPW20N60C3; Diode(D):RHRG1560_F085 | | | |
| $C_{\rm oss}$(Q) | 160 pF | $C_{\rm iss}$(Q) | 2400 pF |
| $C_{\rm rss}$(Q) | 7 pF | $g_{\rm fs}$(Q) | 17.5 |
| $V_{\rm TH}$(Q) | 3V | $C_D$(D) | 30 pF |

*2) Current Falling Period (II) [t3–t4]:* During this period, the voltage $v_{\rm peak} - V_o$ effects $L_D + L_S$. The drain current $i_{\rm LD}$ will be forced to continue falling to zero. As the current difference $i_{\rm LD} - i_{\rm ch}$ charges the capacitor $C_{\rm ds}$, however, there will not be a large amount of current to charge $C_{\rm ds}$ because the value of $i_{\rm LD}$ is very close to that of $i_{\rm ch}$. Hence, the voltage $v_{\rm ds}$ can be equal to $v_{\rm peak}$ approximately. To simplify this period, the channel current $i_{\rm ch}$ is assumed to be controlled by the voltage $V_o$. The equivalent circuit is shown in Fig. 4(b) and $i_{\rm ch}$ can be approximated as expression (7).

At $t_4$, the channel current $i_{\rm ch}$ decreases to zero and $v_{\rm gs}$ decrease to $V_{\rm TH}$, the second stage ends. Then, the MOSFET works in the cutoff region and the stray resistance will damp a resonate circuit formed by $L_D + L_S$ and $C_{\rm oss}$ until the voltage $v_{\rm ds}$ reaches its steady-state value $V_o$.

## III. DESIGN CONSIDERATION AND THE REALIZATION CIRCUIT

### A. Design Consideration

From (7), it is easy to find that the voltage peak value is determined by $V_o$, $I_L$, $i_{\rm off}$, $L_D$, $L_S$, and the inherent parameters of the MOSFET and the diode (i.e., $g_{\rm fs}$, $V_{\rm TH}$, $C_{\rm oss}$, $C_{\rm ds}$, $C_{\rm gs}$, $C_D$). An example of the boost PFC converter setup is used to demonstrate the design of the turn-off current $i_{\rm off}$. The related parameters are listed in Table I.

Combing the turn-off strategy shown in the Section II-A with the parameters, the relationship between $v_{\rm peak}$, $i_{\rm LD}$, and $i_{\rm off}$ can be drawn as shown in Fig. 5. If the drain–source voltage peak value and the power loop inductance ($L_D + L_S$) remain constant, the turn-off current $i_{\rm off}$ will decrease with the current $i_{\rm LD}$ rising. Therefore, in practice, if $v_{\rm peak}$ is limited to 550 V, from Fig. 5, the turn-off current $i_{\rm off}$ can be approximately designed as

$$i_{\rm off} = I_{\rm ref} - Ki_{\rm LD} \tag{8}$$

and

$$i_{\rm LD} = I_{\rm LD}\,|\sin(\omega t)| \tag{9}$$

So

$$i_{\rm off} = I_{\rm ref} - KI_{\rm LD}\,|\sin(\omega t)| \tag{10}$$

where $I_{\rm ref}$ and $K$ are two constants, $i_{\rm LD}$ is the amplitude value of $i_{\rm LD}$.

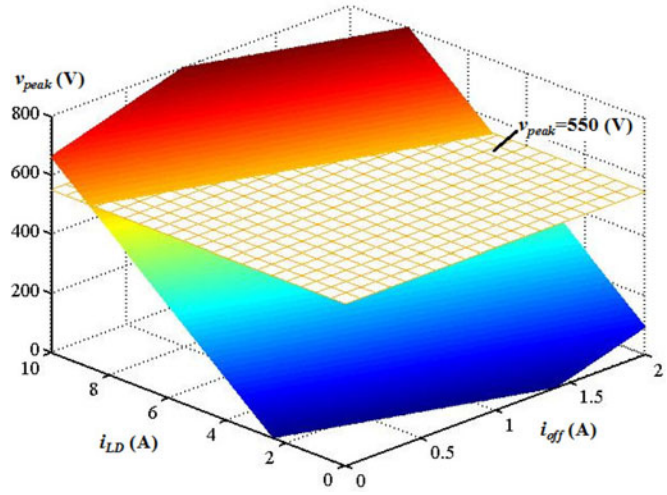


Fig. 5. Relationship between $v_{\rm peak}$, $i_{\rm off}$, and $i_{\rm LD}$.

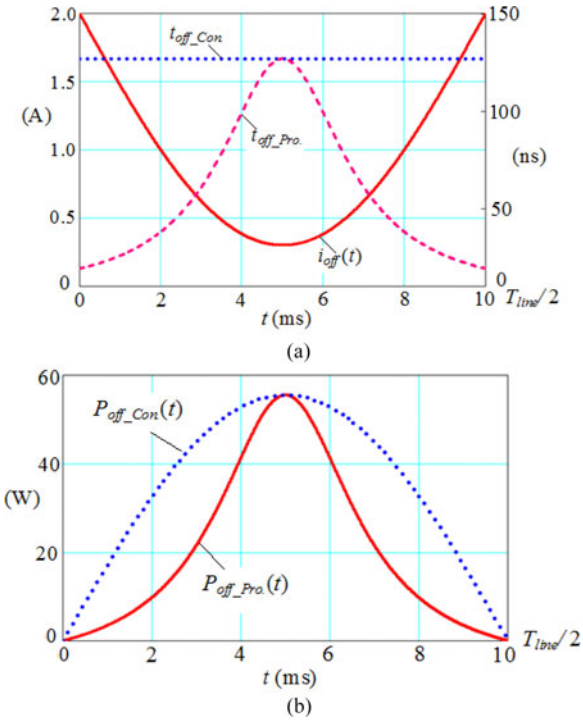


Fig. 6. Turn-off time and calculated turn-off switching losses comparison with the proposed turn-off strategy and the conventional VSD in the half-line period ($V_{\rm in} = 180\ VAC$, $V_o = 380$ V, and $P_o = 1500\ W$): (a) turn-off time comparison and (b) calculated turn-off switching losses comparison.

### B. Turn-Off Switching Losses Comparison Analysis

In order to demonstrate the turn-off switching losses reduction with the proposed turn-off strategy, the boost PFC converter with the same specifications and components is presented in Table I as an example. With the proposed turn-off strategy, the turn-off switching losses of the switch for the boost PFC converter are

$$P_{\rm off\_Pro.}(t) = \frac{1}{2} f_s V_o I_{\rm LD} \sin(\omega t) T_{\rm off} \tag{11}$$

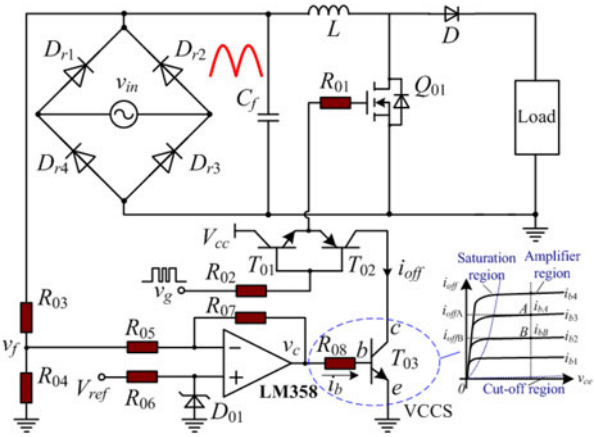


Fig. 7. Proposed gate drive circuit.

$$T_{\rm off} = \frac{Q_{\rm pl} - Q_{\rm th} + Q_{\rm gd}}{i_{\rm off}(t)} \tag{12}$$

where $T_{\rm off}$ is the falling time of the MOSFET [$t_1 \sim t_4$ shown in Fig. 3(b)], $Q_{\rm pl}$ is the MOSFET total gate charge at the beginning of the Miller plateau, $Q_{\rm th}$ is the total gate charge at the threshold, and $Q_{\rm gd}$ is the gate-to-drain charge, respectively. For the MOSFET of SPW20N60C3 from Infineon, $Q_{\rm pl} = 11$ nC, $Q_{\rm th} = 6$ nC, and $Q_{\rm gd} = 33$ nC.

Considering the turn-off voltage spike that should be limited less than 550 V from Fig. 5, the turn-off current can be set within 0.3–2 A changing periodically. Fig. 6(a) shows the turn-off transient time comparison between the proposed turn-off strategy and conventional VSD. $T_{\rm off\_Pro.}$ and $T_{\rm off\_Con.}$ represent the turn-off transient time with the proposed strategy and the conventional VSD. During the half-line period, it is noted that $T_{\rm off\_Pro.}$ is always less than $T_{\rm off\_Con.}$ except that at the peak input voltage point, and in addition, the reduction of the turn-off time between $T_{\rm off\_Pro.}$ and $T_{\rm off\_Con.}$ increases when the turn-off current $i_{\rm off}$ increases. Based on the proposed variable turn-off current concept presented in Section II, as $i_{\rm off}$ modulates with the input line voltage and current, the turn-off transient time and the turn-off switching losses with the proposed strategy are also reduced.

Based on the turn-off switching losses analysis, the calculated turn-off switching losses comparison using the Mathcad software is illustrated in Fig. 6(b). $P_{\rm off\_Pro.}$ and $P_{\rm off\_Con.}$ represent the turn-off switching losses with the proposed strategy and the conventional VSD, respectively. Obviously, $P_{\rm off\_Pro.}$ is less than $P_{\rm off\_Con.}$ during the half-line period, and moreover, the loss reduction becomes larger when $i_{\rm off}$ modulates with the input line voltage and current. It is noted that $P_{\rm off\_Pro.}$ is equal to $P_{\rm off\_Con.}$ at the peak input voltage point. This is because they have the same turn-off current to ensure that the voltage spike is less than 550 V. By calculating the turn-off switching losses with the proposed turn-off strategy and the conventional VSD from Fig. 6(b), at 180-VAC input, 380-V output voltage, the proposed turn-off strategy reduces the turn-off switching losses of 14.52 W and it translates into an efficiency improvement of 0.968%.

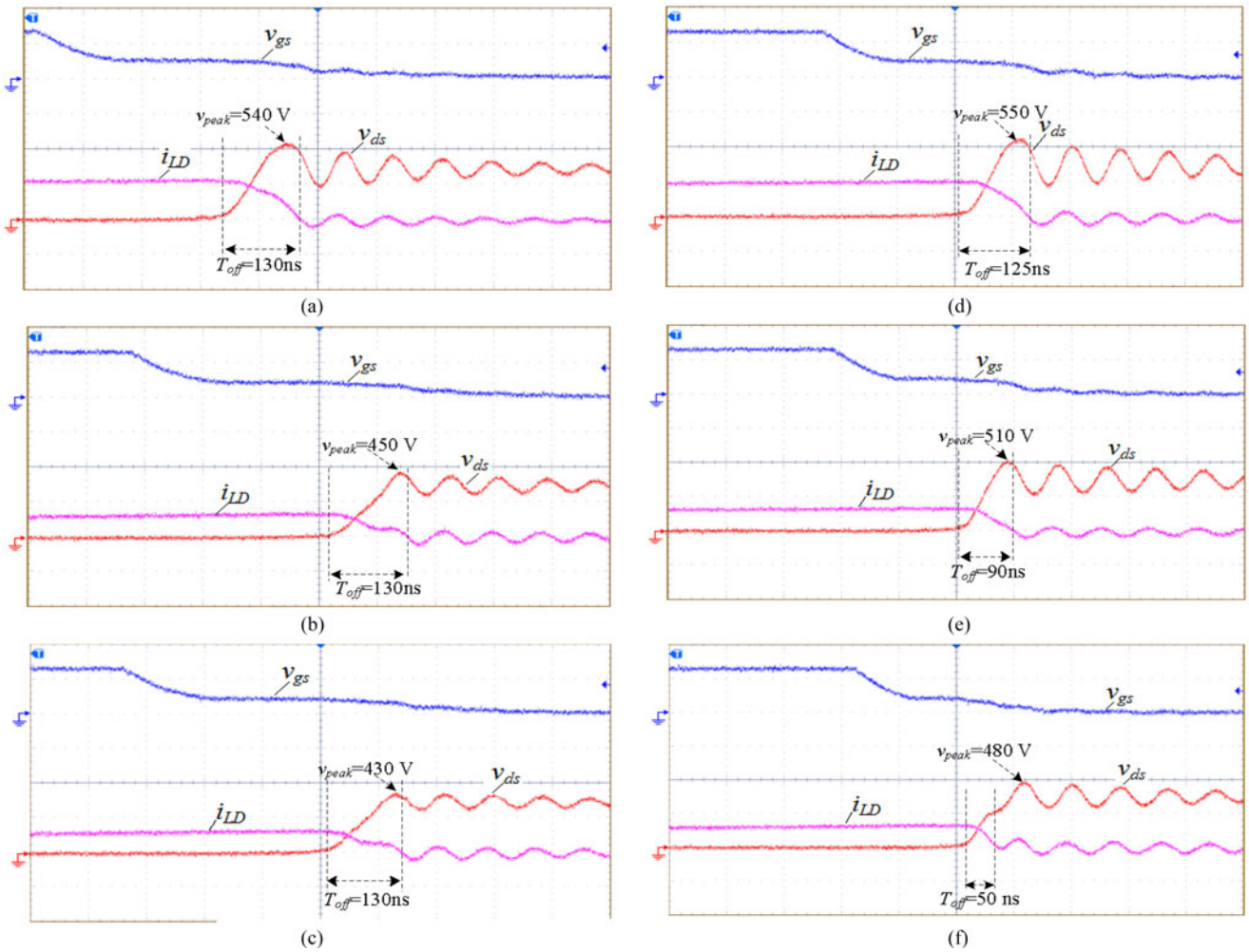


Fig. 8. Key experimental waveforms under the different input voltage with the VSD and the proposed turn-off strategy (100 ns/div); (a)–(c): with the VSD; (d)–(f): with the proposed turn-off strategy. (a), (b), (d), and (e): $v_{\rm gs}$. (10 V/div), $i_{\rm LD}$ (10 A/div), $v_{\rm ds}$ (250 V/div); (c) and (f): $v_{\rm gs}$. (10 V/div), $i_{\rm LD}$ (5 A/div), $v_{\rm ds}$ (250 V/div).

### C. Design of the Gate Drive Circuit

According to Fig. 5, the turn-off current $i_{\rm off}$ can be designed less than 2.0 A to limit the voltage spike. In a real circuit, a simple bipolar transistor circuit can be adopted as the VCCS to implement this function, which is not limited to this kind of method.

Fig. 7 shows the gate drive circuit of the proposed turn-off strategy, where a simple bipolar transistor circuit is used as VCCS (when $v_{\rm cA} > v_{\rm cB}$, then, $i_{\rm bA} > i_{\rm Bb}$ and $i_{{\rm off}\,A} > i_{{\rm off}\,B}$) and an IC LM358 is adopted to achieve subtraction operation. If the Zener diode $D_{01}$ is 5.1 V, the magnification of $T_{03}$ is $\beta$ and $R_{05} = R_{07}$, then, the turn-off current $i_{\rm off}$ can be derived by

$$i_{\rm off} = \frac{\beta}{R_{08}}(10.2 - \frac{R_{04}}{R_{03}+R_{04}} v_{\rm in}\,|\sin \omega t|) \qquad (13)$$

Obviously, (13) matches with (10).

## IV. Experimental Results

To verify the proposed real-time variable turn-off current strategy, one boost PFC converter prototype has been built. The specifications are listed in Table I and the control IC is UC2818. It is noticed that the smaller power loop inductance will bring a better performance with the lower voltage spike during the turn-off transient. However, in this prototype, to reflect the principle of the proposed turn-off strategy, the power loop inductance ($L_D + L_S$) is set about 1.5 $\mu$H. According to the analysis in Section-III-A, if the voltage spike value is limited to 550 V, the turn-off current $i_{\rm off}$ can be designed as changing between 0.3 and 2 A, which can be obtained from Fig. 5. Corresponding to the proposed gate drive circuit shown in Fig. 7, $T_{03}$ can choose transistor 2SC2655, and the turn-off current $i_{\rm off}$ can be achieved by regulating $R_{03}$, $R_{04}$ , and $R_{08}$. However, in the real experimental process, due to the nonlinear characteristic of the MOSFET, $i_{\rm off}$ was regulated within a small variation to attain a better performance, i.e., 0.5–1.5 A.

The key experimental waveforms have been tested with the VSD and the proposed strategy under various input voltage

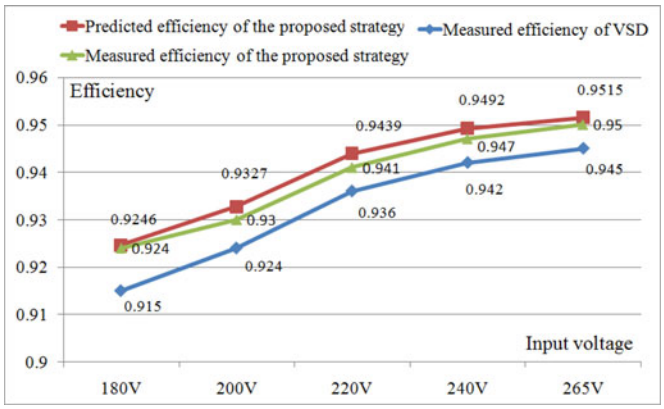


Fig. 9. Efficiency comparison between predicted and measured for the VSD and the proposed strategy.

and current. For $V_{\rm in} = 180\,VAC$, results for the peak line input voltage, near 50% peak line input voltage and near 20% peak line input voltage are shown in Fig. 8. Fig. 8(a)–(c) shows the waveforms of $i_{\rm LD}$, $v_{\rm ds}$, and $v_{\rm gs}$ with VSD, which have the same turn-off transition time (about 130 ns). Fig. 8(d) and (e) illustrates the typical waveforms of $i_{\rm LD}$, $v_{\rm ds}$, and $v_{\rm gs}$ with the proposed strategy. Fig. 8(a) and (d) have similar turn-off transition time and turn-off voltage spike because their turn-off currents are designed closely to ensure the safety operation of the switch. From Fig. 8(e), it is observed that the turn-off transition time of the proposed strategy is reduced to 90 ns compared to 130 ns of the VSD as seen from Fig. 8(b) at near 50% peak line input voltage. Similarly, from Fig. 8(f), the turn-off transition time of the proposed strategy is reduced to 50 ns compared to 130 ns as seen from Fig. 8(c) at near 20% peak line input voltage. It is noted that the voltage spike would not exceed the peak value (550V) with the turn-off current modulating periodically. Obviously, the experimental results match closely with theoretical predicted shown in Section-III. This leads to a significant reduction of the turn-off switching losses.

Fig. 9 shows the efficiency comparison between predicted and measured for the VSD and the proposed strategy with different line input voltage under the rated load condition. Due to the fast turn-off speed and the turn-off switching losses reduction of the proposed strategy, the efficiency improvement is realized throughout the whole input voltage. As shown in Fig. 9, with 220-VAC input voltage and 1.5-kW output, a measured efficiency improvement of 0.5% is achieved over the VSD. Particularly, with 110-VAC input voltage, a measured efficiency improvement of 0.9% is achieved over the VSD. Moreover, the predicted efficiency is very close to the measured. It is verified that the analysis of turn-off switching losses presented in Section-III is impactful.

## V. Conclusion

The conventional VSDs have the fixed drive current which could not optimize the turn-off switching losses. To relieve this problem, this letter presents a new turn-off strategy applied in PFC converter, which could limit the voltage spike across the power switch when the turn-off speed is modulated real timely with the variation of input line voltage. The working principle of the proposed strategy is presented and the peak voltage spike across the power switch can be obtained from a simple analytical modeling of the turn-off process. The turn-off switching losses analysis is discussed in detail. The gate drive circuit is designed and the prototype with a boost PFC converter has been established to verify the proposed turn-off strategy. The efficiency using the proposed driver increases more 0.9% than that using the VSD strategy with 110-VAC input and 380-V/1.5-kW output. The proposed strategy can be used in any other PFC converter.

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