A High-Efficiency Current-Mode Buck Converter With a Power-Loss-Aware Switch-On-Demand Modulation Technique for Multifunction SoCs

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***Abstract*—Modern multifunction systems on chip often require a high-efficiency buck converter over a wide load current range as the main power source, for which complex multimode operation with mode detection/change is a frequent compromise between efficiency and transient response. This paper proposes a novel power-loss-aware switch-on-demand modulation (PLASOM) technique based on accurate power loss modeling to switch critical components/parameters of power loss on demand: the ON/OFF status and the size of the power transistor, the dead time, and the ON/OFF status of power-hungry subcircuits. The proposed PLASOM-based converter can work as either an adaptive on-time mechanism with constant frequency or a cycle-extended adaptive ON/OFF-time mechanism with variable frequency without mode detection/change, so that the conversion efficiency and transient response can be improved. A proposed buck converter with the PLASOM technique was implemented using the TSMC 90-nm 1/3.3-V CMOS process. Experimental results show that a conversion efficiency higher than 90% was achieved over the 1–500 mA load current range, whereas the voltage variation/recovery time during the 0.1–500 mA load transient were less than 50 mV/25 μs. Performance evaluations indicate that the proposed PLASOM technique is favorable for wide load current range buck converters in terms of conversion efficiency, transient response, and voltage ripples.**

***Index Terms*—Conversion efficiency, current mode, power loss model, switching buck converter, transient response, wide load current range.**

I. Introduction

WEARABLE and portable devices (e.g., smartwatches and smartphones) have become mainstream technology but place ever-increasing demands on high-performance, low-power, multifunction systems on chip (SoCs) and multiprocessors. As low power dissipation becomes a major design challenge, well-planned power management by the adoption of different voltage scaling policies [1]–[2] is required to minimize power/energy budgets while maintaining acceptable performance. The lower section of Fig. 1 illustrates a general-purpose multifunction SoC with a closed adaptive voltage scaling (AVS) loop, where the continuously monitored real-time timing information is returned to the power management unit to supply an optimal voltage level for each subfunctional block. The upper-left section of Fig. 1 shows a possible load current profile [3], in which the load current varies within a wide range because of the switching actions of the multifunction SoCs with voltage scaling techniques. Obviously, a global power supply (GPS in Fig. 1) based on a switching buck converter with high conversion efficiency and good regulation ability over a wide conversion range and a wide load current range is indispensable. Intel recently proposed the concept of "race-to-idle" [4]–[5], which emphasizes low energy consumption by executing tasks at higher voltage levels to finish tasks sooner and then switches to a power-down state to further minimize leakage power. Moreover, an intermittent discharge behavior [6] is preferred to optimize battery lifetime because a battery can recover some of the charge consumed by utilizing an idle period [6]–[7]. As a result, the system stays in the light-load condition for a long time (as two possible load current profiles shown in the upper-center and upper-right sections of Fig. 1). In such a scenario, a buck converter-based GPS should further enhance the conversion efficiency under the light-load condition.

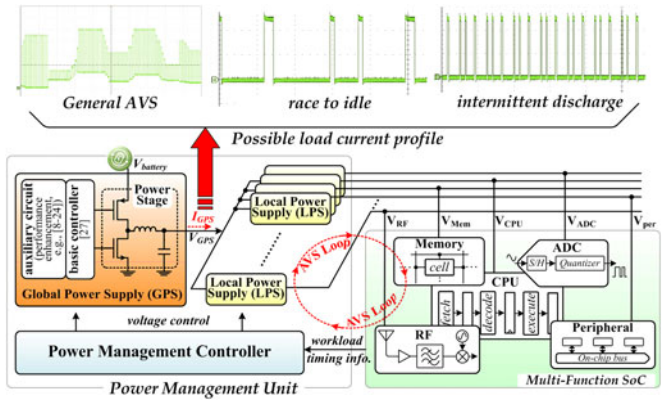

Fig. 1. General multifunction SoC with an AVS loop and several possible load current profiles.

Fig. 2 demonstrates the conceptual architecture of a high-efficiency switching buck converter over a wide load range, where various power loss reduction techniques [8]–[24] (categorized as numbers ❶–❻ in Fig. 2) have been proposed to improve the conversion efficiency. A popular technique to reduce both the switching loss (P_S) under the light-load condition and the conduction loss (P_C) under the heavy-load condition is to adaptively resize the power transistor [8]–[10], [30]–[31] (denoted as ❶ in Fig. 2), according to a complex load current

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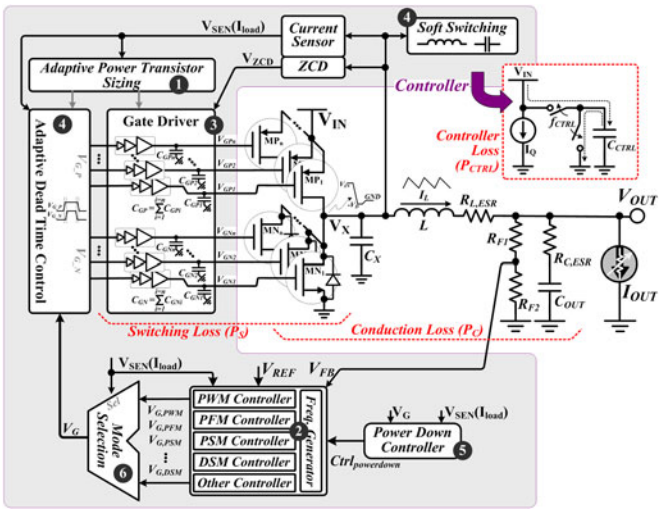

Fig. 2. Architecture of a high-efficiency buck converter with a wide load current range.

segmentation process. To further reduce the switching power consumed by bulky power MOS transistors, a variable switching frequency is frequently applied (e.g., variable frequency pulse width modulation (PWM) [11]–[12], pulse frequency modulation (PFM) [13], pulse/dithering skip modulation (PSM/DSM) [22], and off-time modulation [32]–[33]) (denoted as ❷ in Fig. 2). However, the output voltage ripple increases with the decreasing switching frequency; additionally, extra frequency generators are required. Because large gate capacitors of bulky power MOS transistors contribute considerably to switching loss, another popular power loss reduction technique is to design a low-swing gate driver [14] (denoted as ❸ in Fig. 2), of which the dead-time controller cannot be optimized easily, which incurs a shoot-through current. Many adaptive dead-time controls [15]–[17] and soft-switching techniques [18], [34] have been widely applied to reduce *V–I* overlap switching loss during the dead-time period (denoted as ❹ in Fig. 2). Dead-time always varies with the operating conditions (e.g., load current, input voltage, temperature, and process corners); as a result, dead-time optimization is a costly process. Soft-switching emulates the resonant behavior to achieve zero-voltage switching or zero-current switching; however, complex controllers and extra passive components (e.g., inductors and capacitors) increase the bill of material cost. As the load current requirement becomes quite small (ultra-light-load condition), the controller contributes significant power loss (P_{CTRL}). Powering down unused circuit blocks [19]–[21], [35] (denoted as ❺ in Fig. 2) can effectively reduce P_{CTRL}; however, frequently reactivating power-down blocks for a fluctuating load current profile in a multifunction SoC diminishes the power-saving efficiency and deteriorates the response speed. All of the above techniques often cooperate in multimode operation (e.g., PFM, PSM/DSM, and PWM) to achieve a high efficiency over a wide load current range [22]–[24], [36]–[37] (denoted as ❻ in Fig. 2). Multimode operations not only increase the design complexity but also require more silicon estate. Moreover, the transient response is severely deteriorated because of the delay time to make a mode change decision. Compared to single-mode converters (e.g., PWM only [27]), it is obviously difficult for the complicated high-efficiency buck converter shown in Fig. 2 to maintain a high efficiency in ultra-light-load conditions.

The concept of switch-on-demand modulation [28] was recently raised to reduce the switching loss only with no theoretical analyses and eventually achieved high efficiency within a limited load current range. In this paper, a power-loss-aware switch-on-demand modulation (PLASOM) technique is proposed to achieve a high-efficiency buck converter over a wide load range with single-mode operation and simple controller circuitry. Both the voltage ripples and transient behaviors are improved by the PLASOM techniques. The detailed working principles of the proposed PLASOM technique are introduced in Section II, along with a simple analytical power loss model and numerical design examples, which demonstrate that the proposed PLASOM switches critical components and/or parameters of power loss on demand and raises the overall efficiency over an ultra-wide load range. Section III shows a concise small-signal analysis of the proposed PLASOM, while detailed key circuit implementations of a buck converter with the proposed PLASOM technique are described in Section IV. The circuit in Section IV was designed and implemented using TSMC 90-nm CMOS technology, which can achieve above 90% efficiency over a load current range of 1–500 mA. The detailed experimental results are summarized in Section V, and the conclusion of this paper is given in Section VI.

II. Working Principles of the Proposed PLASOM Technique and Analytical Power Loss Models

In the following section, a simple analytical power loss model is first derived. Numerical examples with related parameters extracted from typical switching buck converter designs are used to show the power loss distributions and further demonstrate the basic concepts and working principles of the proposed PLASOM technique.

A. Analytical Power Loss Model

The power loss of a switching buck converter over a wide load range (see the circuit diagram in Fig. 2) can be categorized as conduction loss (P_C), switching loss (P_S), and controller loss (P_{CTRL}) [11], [25]–[26], where P_C, P_S, and P_{CTRL} are governed by the inductor-current and on-resistance of the power transistor, the switching frequency and parasitic capacitance, and the quiescent current, respectively. A power loss model for a buck converter over a wide load current range was proposed as arranged in Table I, which was refined mainly in two aspects to improve accuracy. Table II defines the corresponding parameters in Table I. First, the switching loss was classified into three categories: switching node (V_X), gate driver, and dead time. As the conceptual waveforms of V_X show in Fig. 3, for both continuous conduction mode (CCM) and discontinuous conduction mode (DCM), voltage drops (V_{DN}) resulting from body diode conduction contribute an additional switching power loss. The overall energy transferred to V_X within one switching cycle will be exhaustively consumed, which is

TABLE I
ANALYTIC POWER LOSS MODEL

Power Loss Models			Power Loss Reduction Techniques & Corresponding Effective Parameters					
Categories		Equation	❶	❷	❸	❹	❺	❻
Switching Loss (P_S)	Switching Node (V_X of Fig.2)	*CCM Mode* ($P_{SN,CCM}$) $C_X \cdot \left[V_{DN}^2 + V_{IN}(V_{IN}+V_{DN})\right] \cdot f_{SW}$ *DCM Mode* ($P_{SN,DCM}$) $C_X \cdot \left[V_{DN}^2 + V_{OUT}^2 + (V_{IN}-V_{OUT}) \cdot V_{IN}\right] \cdot f_{SW}$	N.A.	[If I_{OUT}↓] f_{SW}↓	N.A.	N.A.	N.A.	[If I_{OUT}↓] f_{SW}↓ [If I_{OUT}↑] *fixed* f_{SW} PWM Mode
	Gate Driver	$P_{GD} = (C_{GN}+C_{GP}) \cdot V_{swing}^2 \cdot f_{SW} + 2 \cdot I_{DC,BUF} \cdot V_{swing} \cdot t_{DC,BUF} \cdot f_{SW}$	[If I_{OUT}↓] C_{GN}↓ C_{GP}↓	[If I_{OUT}↓] f_{SW}↓	V_{swing}↓	N.A.	N.A.	
	Dead Time	*CCM Mode* ($P_{DT,CCM}$) $V_{DN} \cdot I_{OUT} \cdot (t_{DT}+t_{DN,ON}) \cdot f_{SW}$ *DCM Mode* ($P_{DT,DCM}$) $t_{DT} > t_{DT,OPT} \Rightarrow V_{DN} \cdot I_{OUT} \cdot t_{DN,ON} \cdot f_{SW}$ $t_{DT} < t_{DT,OPT} \Rightarrow \Delta Q \cdot f_{SW} \cdot V_{DSN} \Rightarrow [C_X \cdot V_{IN} - I_{OUT} \cdot t_{DT}] \cdot f_{SW} \cdot V_{DSN}$	N.A.		N.A.	$t_{DN,ON}$↓ or ΔQ↓	N.A.	
Conduction Loss (P_C)	(d_1+d_2=1 for CCM and d_1+d_2<1 for DCM)		[If I_{OUT}↑] R_{DSN}↓ R_{DSP}↓	[If I_{OUT}↓] (d_1+d_2)↓	N.A.	N.A.	N.A.	[If I_{OUT}↑] Avoid DCM $I_{L,AC,RMS}$↓
	DC Loss	$P_{C,DC} = I_{OUT}^2 \cdot (R_{L,ESR} + d_1 \cdot R_{DSP} + d_2 \cdot R_{DSN})$						
	AC Loss	$P_{C,AC} = I_{L,AC,RMS}^2 \cdot (R_{L,ESR} + R_{C,ESR} + d_1 \cdot R_{DSP} + d_2 \cdot R_{DSN})$		N.A.	N.A.	N.A.	N.A.	
Controller Loss	Dynamic Loss	$P_{CTRL,d} = C_{CTRL} \cdot V_{IN}^2 \cdot \alpha \cdot f_{SW}$	N.A.	N.A.	N.A.	N.A.	I_{Q1}↓	N.A.
	Quiescent Loss	$P_{CTRL,q} = V_{IN} \cdot (I_{Q1} + I_{Q2} \cdot t_{ctrl,on} \cdot f_{SW})$						

Main Drawbacks
❶~❻: complicated controller design and lower efficiency in light load conditions (P_{CTRL}↑)
❶~❺: requires multi-mode operation to maintain high efficiency for ultra-wide load range
❺~❻: deteriorated transient response
❷: increased ripple conduction loss and output voltage ripple
❷: unpredictable switching frequency (f_{SW})
❷: unrealistically high f_{SW} for heavy load

the source of the V_X power loss. The conceptual waveforms of dead-time periods A and B are also shown in the lower panel of Fig. 3 to demonstrate the *V–I* overlap dead time switching power loss, where the relationship between the designated/optimized dead time ($t_{\mathrm{DT}}/t_{\mathrm{DT,OPT}}$), load current ($I_{\mathrm{OUT}}$), and conduction time of the body diode ($t_{\mathrm{DN,ON}}$) were derived (i.e., two different power losses: body diode conduction loss in the case of ($t_{\mathrm{DT}} > t_{\mathrm{DT,OPT}}$) and charge loss of the switching node in the case of ($t_{\mathrm{DT}} < t_{\mathrm{DT,OPT}}$)). Furthermore, the controller loss was categorized into dynamic loss and quiescent loss, where the quiescent loss is further divided into two parts (i.e., always-on and power-down circuits). Through modeling the dynamic loss, the connections between the power loss and design complexity (C_{CTRL}) of the controller can be considered. Separating the quiescent currents sunk by always-on circuitry and power-down circuitry makes the power loss model more suitable for modern controller designs with partial shutdown techniques. As a result, the tailored power loss model can achieve accurate power loss distributions for a modern wide load range buck converter.

A well-known PWM current-mode switching buck converter (i.e., [27]) is designed using TSMC 90-nm CMOS technology, from which the parameters defined in Table II are extracted as a numerical example. The power loss distributions evaluated by the proposed power loss model (see Table I) based on the numerical example (see Table II) are sketched in Fig. 4. Fig. 4 also illustrates the simulated and evaluated power efficiencies for comparison, where the inaccuracy is less than 2%, to show the feasibility of the proposed power loss model.

B. Working Principles of the Proposed PLASOM

Table I summarizes the effective power loss reduction parameters realized by the previous efficiency improvement techniques (types ❶–❻) mentioned in Section I. The main drawbacks of each previous technique are also shown, illustrating that multimode operation is often requested to achieve high efficiency over the ultra-wide load current range. As a result, a delayed decision of mode change deteriorates the transient response and further reduces the effectiveness of the power loss reduction for a fluctuating load current profile. Observing the power loss distribution depicted in Fig. 4, the power loss can be reduced accordingly by switching the values of the critical parameters on demand (i.e., highlighted as ①–④ of Fig. 4), which is the basic concept of PLASOM. To detail the basic concepts and working principles, a conventional current-mode switching buck converter with the proposed PLASOM shown in Fig. 5 was further used as a design example, of which Fig. 6 depicts the conceptual operating waveforms. Fig. 5 shows that the gate pulse (V_G) counter contributes to the main overhead of the PLASOM.

First, the PLASOM switches ON/OFF the power transistor on demand depending on the output voltage level (i.e., energy demand, highlighted as ① in Fig. 4). In a heavy-load

TABLE II
PARAMETERS OF THE ANALYTICAL POWER LOSS MODEL

Selected Parameters			
Parameter (Symbol)	PWM Converter [27] and Proposed PLASOM	Parameter (Symbol)	PWM Converter [27] and Proposed PLASOM
Input Voltage (V_{IN})	3.3 V	Output Voltage (V_{OUT})	1.8 V
Inductor Current (I_L)	0 –500 mA	Load Current (I_{OUT})	0 –500 mA
Filter Inductor (L)	4.7 μH	Filter Capacitor (C_{OUT})	10 μF
ESR of Inductor ($R_{L,\mathrm{ESR}}$)	0.03 Ω	ESR of Capacitor ($R_{C,\mathrm{ESR}}$)	0.1 Ω

Derived Parameters					
Parameter (Symbol)	PWM Converter [27]	Proposed PLASOM	Parameter (Symbol)	PWM Converter [27]	Proposed PLASOM
Inductor Current Ripple in RMS ($I_{L,\mathrm{AC,RMS}}$)	$\frac{(V_{\mathrm{IN}}-V_{\mathrm{OUT}})\cdot d_1}{\sqrt{3}\cdot L\cdot f_{\mathrm{SW,Max}}}$		Body Diode Conduction Time ($t_{\mathrm{DN,ON}}$ of Fig. 3)	$t_{\mathrm{DT}}-\left(\frac{C_X\cdot V_{\mathrm{IN}}}{I_{\mathrm{OUT}}}\right)$	
Optimal Dead Time ($t_{\mathrm{DT,OPT}}$)	$\frac{C_X\cdot V_{\mathrm{IN}}}{I_{\mathrm{OUT}}}$		Voltage Drop in Case of $t_{\mathrm{DT}}<t_{\mathrm{DT,OPT}}$ (V_{DSN} of Fig. 3)	$V_{\mathrm{IN}}-\left(\frac{I_{\mathrm{OUT}}\cdot t_{DT}}{C_X}\right)$	

Extracted Parameters					
Parameter (Symbol)	PWM Converter [27]	Proposed PLASOM	Parameter (Symbol)	PWM Converter [27]	Proposed PLASOM
Switching Frequency (f_{SW})	1 MHz ($f_{\mathrm{SW,Max}}$)	(A/B) $\times$ $f_{\mathrm{SW,Max}}$ $A,B=1-B_{\mathrm{max}}(A\leq B)B_{\mathrm{max.}}=110$	Equivalent Capacitance of Node V$_{\mathrm{X}}$ (C_{X})	120 pF	
Cycle Time (t_{SW})	1 μs ($t_{\mathrm{SW,Min}}$)	$1/f_{\mathrm{SW}}$	Duty Ratio of MP ON and MN OFF (d_1)	0 – 1	
Duty Ratio of MP OFF and MN OFF for DCM (d_3)	0 – 1		Duty Ratio of MP OFF and MN ON (d_2)	0 – 1	
On Resistance of MP (R_{DSP})	0.1 Ω	0.1 Ω@[I$_{\mathrm{OUT}}>$50 mA] 0.2 Ω@[I$_{\mathrm{OUT}}<$50 mA]	On Resistance of MN (R_{DSN})	0.1 Ω	0.1 Ω@[I$_{\mathrm{OUT}}>$50 mA] 0.2 Ω@[I$_{\mathrm{OUT}}<$50 mA]
Gate Capacitance of MP (C_{GP})	84 pF	84 pF@[$I_{\mathrm{OUT}}>$50 mA] 42 pF@[$I_{\mathrm{OUT}}<$50 mA]	Gate Capacitance of MN (C_{GN})	50 pF	50 pF@[I$_{\mathrm{OUT}}>$50 mA] 25 pF@[I$_{\mathrm{OUT}}<$50 mA]
Time Period of Short-Circuit Current of Gate Driver ($t_{\mathrm{DC,Buf}}$)	0.3 ns	0.3 ns	Switching Short-Circuit Current of Gate Driver ($I_{\mathrm{DC,Buf}}$)	1 mA	1 mA@[I$_{\mathrm{OUT}}>$50 mA] 0.5mA@[I$_{\mathrm{OUT}}<$50mA]
Dead Time (t_{DT})	4 ns	4 ns@[$I_{\mathrm{OUT}}>$ 30 mA] 8 ns@[$I_{\mathrm{OUT}}<$ 30 mA]	Body Diode Conduction Voltage (V_{DN})	0.7 V	
Output Swing of Gate Driver (V_{swing})	V$_{\mathrm{IN}}$ (3.3 V)		Power-On Time of Power-off Control Circuit ($t_{\mathrm{ctrl},on}$)	N.A.	$d_1\times t_{\mathrm{SW,Min}}$
Switching Activity of Control Logic (α) – Estimation	0.5	0.5	Equivalent Capacitance of Controller (C_{CTRL})	0.1593 nF	0.1609 nF (1% Overhead)
Quiescent Current of Always-on Control Circuit (I_{Q1})	200 μA	50 μA	Quiescent Current of Power-off Control Circuit (I_{Q2})	0	150 μA

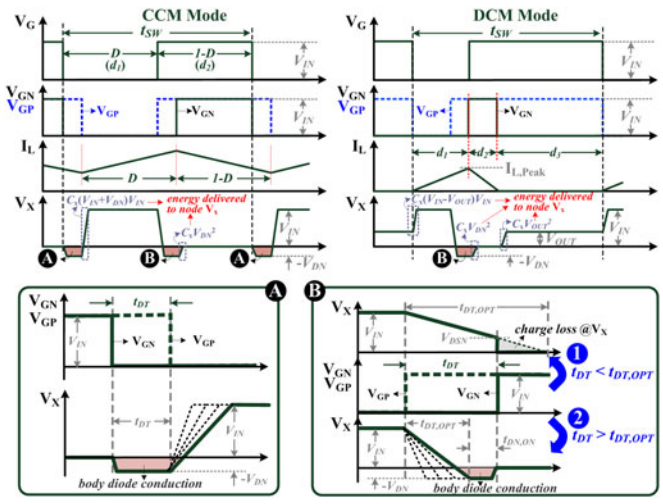

Fig. 3. Waveforms of switching node (V_X) and dead-time period (A and B).

condition (e.g., 200–500 mA), the PLASOM adaptively adjusts the on-time of a sufficiently large power transistor with constant f_{SW} to reduce the conduction loss. As I_{OUT} decreases, the power loss distribution (see Fig. 4) shows a crossover point of switching loss and conduction loss (i.e., 100–70 mA), in which a high constant f_{SW} is not efficient. The upper-left and upper-right sections of Fig. 6(a) show the conceptual operating waveforms of the heavy load (e.g., 200–500 mA) and light load (e.g., <70 mA) conditions, respectively. Because the error amplifier (EA) output (V_{EA}) traces the output voltage (V_{OUT}) through the feedback signal (V_{FB}), the voltage level of V_{EA} reflects the energy requirements of the load circuit (i.e., I_{OUT}). Therefore, the PLASOM periodically checks the voltage level of V_{EA} during a predefined short time interval (e.g., high level of clock signal, *CLK*) to determine whether the cycle-extended adaptive off-time manner will be activated (i.e., variable f_{SW}). In the case in which V_{EA} is higher than V_{CCS} (i.e., summing of compensated ramp and sensed inductor current, $V_{\mathrm{RAMP}}+V_{\mathrm{SEN}}$), when *CLK* is high, the gate-controlling pulse of the power transistor (V_{G}) is switched to low (to turn ON MP$_1$ and MP$_2$ in Fig. 5), while V_G is switched back to high after V_{EA} comes across V_{CCS}. However, if V_{EA} is lower than V_{CCS} when *CLK* is high, the PLASOM activates a cycle-extended adaptive off-time mechanism to

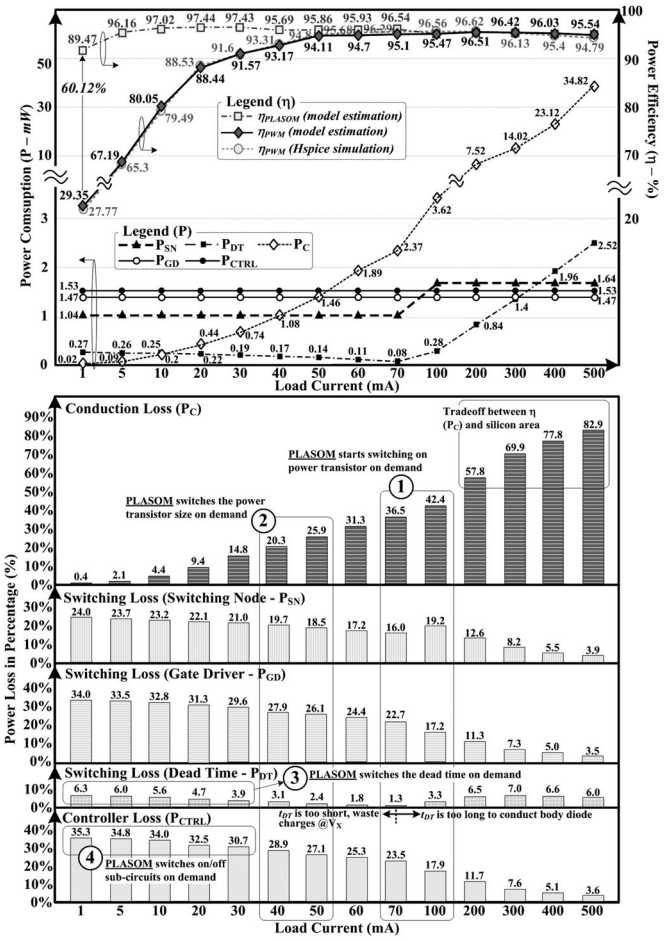

Fig. 4. Power efficiency and power loss distribution of a conventional PWM buck converter.

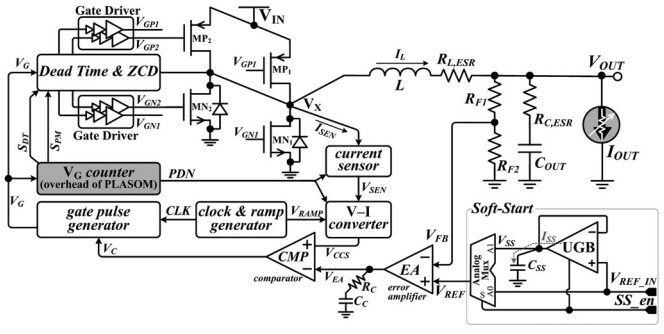

Fig. 5. Block diagram of the proposed current-mode converter with the PLASOM technique.

extend the off-time ($T_{\rm OFF}$) into the succeeding switching cycle, in which case the load circuit has sufficient energy and continues switching off the power transistor on demand (highlighted as ① in Fig. 6). It is noted that $V_{\rm OUT}$ becomes higher while $V_{\rm EA}$ becomes lower as $I_{\rm OUT}$ decreases (i.e., load regulation performance because of the finite loop gain of the buck converter). As a result, a specific $V_{\rm OUT}$ (and $V_{\rm EA}$) corresponds to an average $I_{\rm OUT}$ so that the pulsewidth of *CLK* defines the level of $I_{\rm OUT}$ for PLASOM to activate the cycle-extended adaptive off-time mechanism [as magnified in the lower-left section of Fig. 6(a)]. The pulsewidth of *CLK* (from $t_{\rm CLK\_pw1}$ to $t_{\rm CLK\_pw2}$) is extended in the lower-left section of Fig. 6(a) such that the voltage level of $V_{\rm EA}$ finally exceeds $V_{\rm CCS}$ before *CLK* goes low to switch V_G to low, in which case the threshold voltage of the activating cycle-extended adaptive off-time mechanism (i.e., $th_{\rm ot2} < th_{\rm ot1}$) is equivalently lowered (i.e., $V_{\rm EA}$ should be lower, which corresponds to a lower $I_{\rm OUT}$ level). In the proposed PLASOM, the pulsewidth of *CLK* is designated to activate a cycle-extended adaptive off-time mechanism at the point at which the switching loss exceeds the conduction loss (e.g., $I_{\rm OUT} = 100$–70 mA according to the power loss analysis in Fig. 4). In case the average $I_{\rm OUT}$ continues to decrease after the PLASOM activates the cycle-extended adaptive off-time mechanism, the off-time of the power transistor is expected to be extended into more succeeding cycles [e.g., $T_{\rm OFF2} > T_{\rm OFF1}$ in Fig. 6(a)].

Then, the load current continues to decrease, and the switching loss becomes considerably greater than the conduction loss (e.g., 40–50 mA, highlighted as ② in Fig. 4). The reduction of the switching power loss through a set of smaller power transistors (e.g., size down by a ratio of 2) can be guaranteed to be considerably more than the increase in the conduction loss. Thus, the PLASOM switches the size of the power transistor on demand. Furthermore, if the load current is sufficiently low (e.g., 20–30 mA, highlighted as ③ in Fig. 4), the additional charge loss at the V_X becomes significant, along with the dead time power loss. The PLASOM switches the dead time to a longer period on demand. The average level of $I_{\rm OUT}$ can be estimated by simply counting the off-time in cycle counts, as shown in the lower-right section of Fig. 6(a). As the off-time continues to accumulate, the PLASOM will switch the size of the power transistor on demand [② of Fig. 6(a)] at the point $\rm TH_{PTsize}$ (i.e., $I_{\rm OUT} \approx 50$ mA according to the power loss analysis in Fig. 4) and will switch the dead time on demand [③ of Fig 6(a)] at the point $\rm TH_{DT}$ (i.e., $I_{\rm OUT} \approx 30$ mA according to the power loss analysis in Fig. 4).

Finally, the controller loss becomes significant ($> 30\%$) in the light-load condition ($<$30 mA, highlighted as ④ in Fig. 4), and the PLASOM switches ON/OFF the power-hungry subcircuits of the controller on demand [e.g., switch OFF the current sensor/*V–I* converters in the $T_{\rm OFF}$ period, as shown in ④ of Fig. 6(a)]. Thus, the PLASOM significantly reduces the controller loss because of a longer $T_{\rm OFF}$ as $I_{\rm OUT}$ decreases. Immediately after the power transistor is switched ON to supply energy, the current sensor/*V–I* converters are also switched ON immediately. Because the PLASOM switches these power-hungry subcircuits ON/OFF on demand (i.e., they are activated for each demanding switching cycle) without any decision delay, the buck converter with the proposed PLASOM can achieve a higher light-load efficiency with better transient behavior.

In addition, it can be expected that the power transistor is switched ON immediately for any *CLK* cycle (at a frequency of $f_{\rm SW,Max}$) when the output voltage is sufficiently low (i.e., demands energy) because of the cycle-extended adaptive off-time mechanism, and the maximum peak inductor current ($I_{L,\rm peak\_Max}$) can therefore be constrained to a small value close to the current ripple (ΔI_L) in the heavy-load condition [⑤ of Fig. 6(a)]. As a result, the proposed PLASOM will

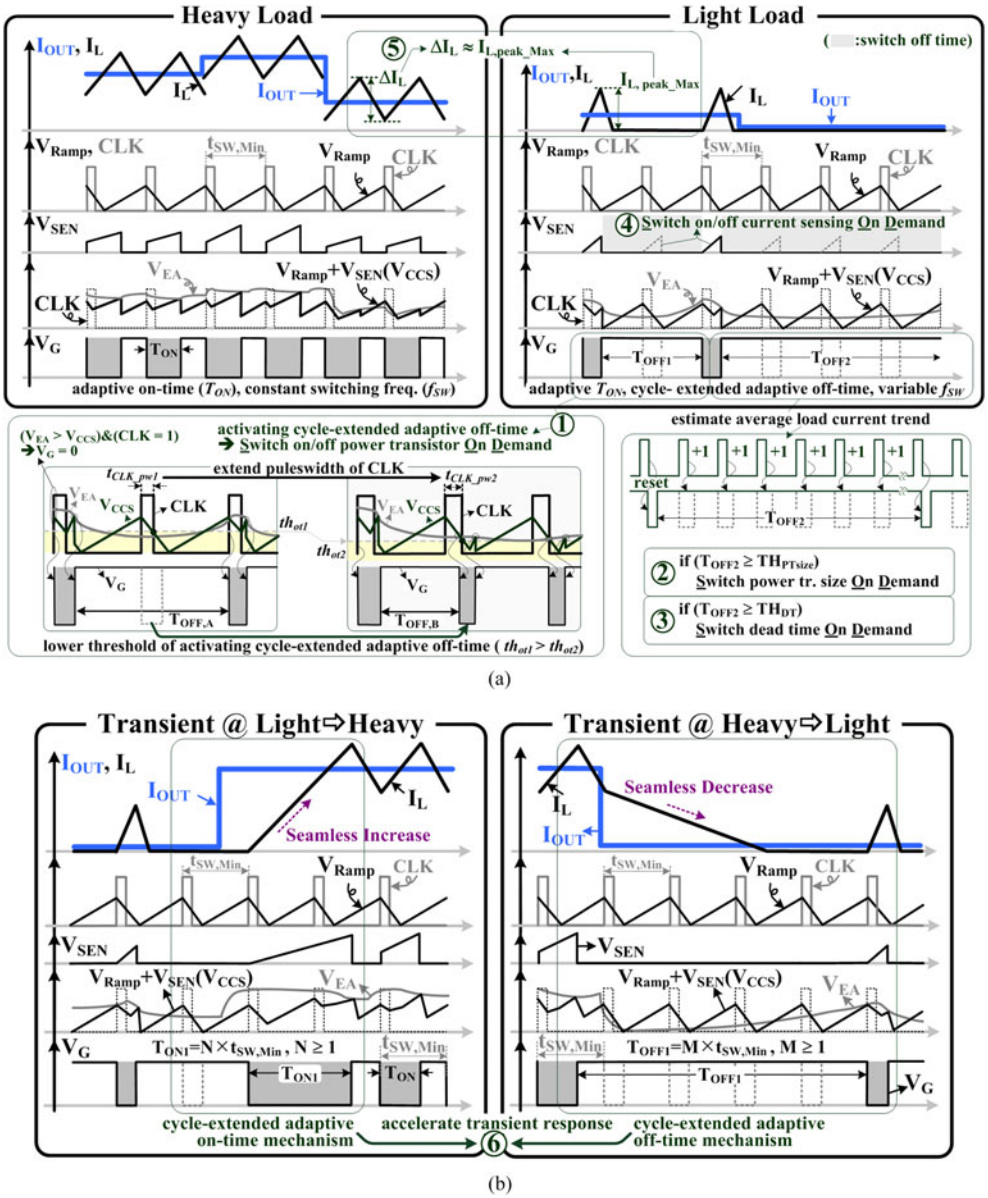

Fig. 6. Conceptual waveforms of the proposed current-mode switch buck converter with the PLASOM technique: (a) gradually changing I_{OUT} and (b) transient I_{OUT}.

induce a small voltage ripple in the light-load condition, in which the conventional PFM controller induces a large voltage ripple because of the large $I_{L,\mathrm{peak\_Max}}$. Fig. 6(b) shows the conceptual waveforms of the transient load, where the dc level of the inductor current is far away from I_{OUT}. In the case of a light- to heavy-load transition, the PLASOM extends the on-time into succeeding switching cycles to seamlessly increase the inductor current until enough energy is supplied. In the case of a heavy- to light-load transition, the PLASOM extends the off-time into succeeding switching cycles to seamlessly decrease the inductor current until the supplied energy is no longer sufficient. With its cycle-extended adaptive on/off-time mechanisms [⑥ of Fig. 6(b)], the buck converter with the proposed PLASOM offers a rapid transient response.

Conceptually, the proposed PLASOM can accordingly adjust the corresponding design parameters of the power loss model (e.g., f_{SW}, C_{GN}, C_{GP}, t_{DT}, R_{DSN}, R_{DSP}, I_{Q1}, and I_{Q2}) by a simple controller and thus improve the overall power efficiency over a wide load current range. The values of the power loss parameters of the buck converter with the PLASOM technique (i.e., Fig. 5) are also estimated as another numerical example in Table II (a 1% area overhead of the controller was introduced by enlarging C_{CTRL} by 1%). Meanwhile, the evaluated power efficiency is also illustrated in the upper section of Fig. 4 for comparison, where a maximum 60.12% efficiency improvement is achieved.

III. Small-Signal Analysis of the Proposed PLASOM

In this section, small-signal models for buck converters with the proposed PLASOM (e.g., Fig. 5) were derived, where the general averaged switch model described in [29] was adopted.

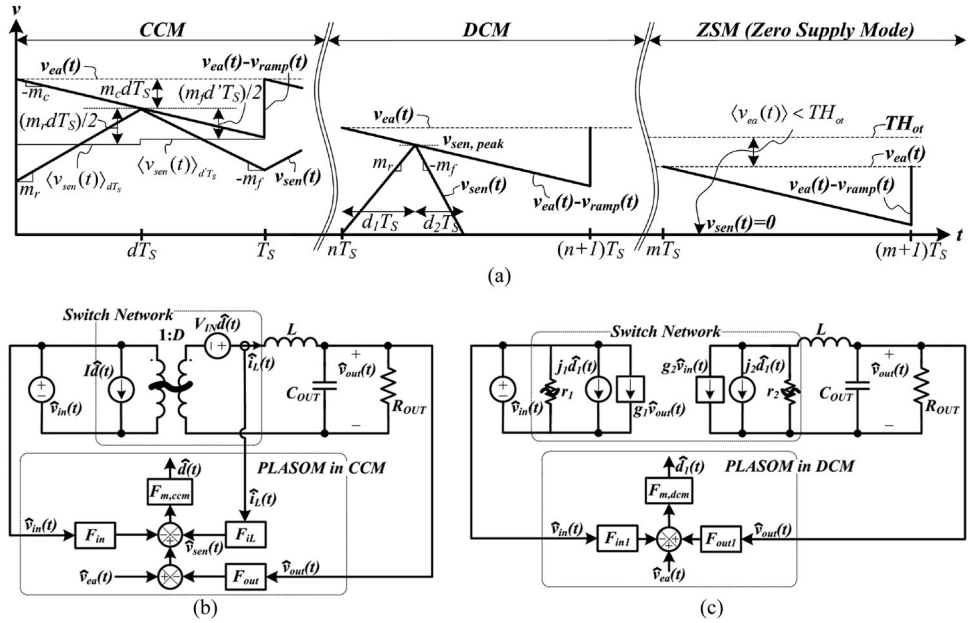

Fig. 7. (a) Critical node waveforms, (b) CCM small-signal model, and (c) DCM small-signal model of the buck converter with the proposed PLASOM.

The proposed PLASOM technique can operate in CCM and DCM, similar to the conventional PWM technique. In the small-signal analysis, the waveforms shown in Fig. 7(a) were used to derive the expressions relating the sensed inductor current information ($v_{\rm sen}(t)$) to the duty control signal ($v_{ea}(t)$) of the PLASOM. The expressions of the parameters shown in this section are the same as those defined in [29] (i.e., $v(t)$, V, $\widehat{v}(t)$, and $\langle v(t)\rangle_{T_S}$ represent the dc + ac term, dc term, small ac term, and average value of signal v, respectively). The derived average sensed inductor current information ($\langle v_{\rm sen}(t)\rangle_{T_S}$) is shown in (1), where v_{ea}, m_c, m_r, m_f, d, and T_S represent the duty control signal (i.e., output of the EA), slope of the compensation ramp waveform ($v_{\rm ramp}$), rising and falling slopes of $v_{\rm sen}$, duty ratio, and period of the switching cycle, respectively:

$$\begin{aligned}\langle v_{\rm sen}(t)\rangle_{T_S} &= \langle v_{ea}(t)\rangle_{T_S} - m_c dT_S - d\left(m_r dT_S\right)/2 \\ &\quad -d'\left(m_f d'T_S\right)/2. \end{aligned} \tag{1}$$

To analyze the small-signal behavior, small perturbations are injected into (1) by replacing $\{\langle v_{\rm sen}(t)\rangle_{T_S}, \langle v_{ea}(t)\rangle_{T_S}, d, m_r, \text{and } m_f\}$ with $\{V_{\rm SEN}+\widehat{v}_{\rm sen}(t), V_{\rm EA}+\widehat{v}_{ea}(t), D+\widehat{d}(t), M_R+\widehat{m}_r(t), \text{and } M_F+\widehat{m}_f(t)\}$. Here, the variation of m_c is assumed to be constant (i.e., M_C) to simplify the analysis; thus, (1) was substituted as

$$\begin{aligned}\left(V_{\rm SEN}+\widehat{v}_{\rm sen}(t)\right) = &\left(V_{\rm EA}+\widehat{v}_{ea}(t)\right) - M_C\left(D+\widehat{d}(t)\right)T_S \\ &-\frac{T_S}{2}\left(M_R+\widehat{m}_r(t)\right)\left(D+\widehat{d}(t)\right)^2 \\ &-\frac{T_S}{2}\left(M_F+\widehat{m}_f(t)\right)\left(D'-\widehat{d}(t)\right)^2. \end{aligned} \tag{2}$$

To further simplify the analysis, only the first-order ac terms of (2) are kept, and the assumption of $M_R D = M_F D'$ (equilibrium status) was made. After correlating the slope variations ($\widehat{m}_r(t)$ and $\widehat{m}_f(t)$) and $\widehat{v}_{\rm sen}(t)$ with the converter voltages ($\widehat{v}_{\rm in}(t)$ and $\widehat{v}_{\rm out}(t)$), inductor current ($\widehat{i}_L(t)$), and current sensing coefficient ($K_{\rm SEN}$), (2) was substituted as

$$\begin{aligned}K_{\rm SEN}\,\widehat{i}_L(t) = &\,\widehat{v}_{ea}(t) - M_C T_S\,\widehat{d}(t) - \frac{D^2 T_S}{2} \\ &\cdot\frac{K_{\rm SEN}\left(\widehat{v}_{\rm in}(t)-\widehat{v}_{\rm out}(t)\right)}{L} - \frac{D'^2 T_S}{2}\cdot\frac{K_{\rm SEN}\widehat{v}_{\rm out}(t)}{L}. \end{aligned} \tag{3}$$

Finally, the duty cycle perturbation ($\widehat{d}(t)$) for the PLASOM to operate in CCM can be expressed as

$$\begin{cases}\widehat{d}(t) = F_{m,\rm ccm}\left(\widehat{v}_{ea}(t) - F_{iL}\cdot\widehat{i}_L(t) - F_{\rm in}\cdot\widehat{v}_{\rm in}(t)\right. \\ \qquad\left. -F_{\rm out}\cdot\widehat{v}_{\rm out}(t)\right) \\ F_{m,\rm ccm} = \frac{1}{M_C T_S}, F_{iL} = K_{\rm SEN}, F_{\rm in} = \frac{D^2 T_S K_{\rm SEN}}{2L}, \\ F_{\rm out} = \dfrac{(1-2D)T_S K_{\rm SEN}}{2L}. \end{cases} \tag{4}$$

As the load current decreases, the proposed PLASOM enters the DCM, in which the PLASOM switches on power switches by a nonzero duty (d_1), as shown in the center of Fig. 7(a). The relation between the sensed peak inductor current information ($v_{\rm sen,peak}$) and $v_{ea}(t)$ was first derived as

$$\begin{aligned}v_{ea}(t) = &\; v_{\rm sen,peak} + m_c d_1 T_S = K_{\rm SEN}\cdot i_{L,\rm peak} + m_c d_1 T_S \\ = &\left(m_r + m_c\right) d_1 T_S. \end{aligned} \tag{5}$$

Small perturbations are injected, leading to

$$V_{\rm EA}+\widehat{v}_{ea}(t) = \left(M_R+\widehat{m}_r(t)+M_C\right)\left(D_1+\widehat{d}_1(t)\right)T_S. \tag{6}$$

After correlating $\widehat{m}_r(t)$ with the converter voltages and removing the dc terms, the first-order ac terms of (6) were given

in (7), where the duty perturbation ($\hat{d}_1(t)$) for the PLASOM to operate in DCM was also derived

$$\hat{v}_{ea}(t) = (M_R + M_C)\,\hat{d}_1(t)T_S + \frac{K_{\rm SEN}D_1T_S}{L}(\hat{v}_{\rm in}(t) - \hat{v}_{\rm out}(t))$$

$$\Rightarrow \begin{cases} \hat{d}_1(t) = F_{m,\rm dcm}\left(\hat{v}_{ea}(t) - F_{\rm in1}\hat{v}_{\rm in}(t) + F_{\rm out1}\hat{v}_{\rm out}(t)\right) \\ F_{m,\rm dcm} = \dfrac{1}{(M_R + M_C)\,T_S}, F_{\rm in1} = F_{\rm out1} = \dfrac{K_{\rm SEN}D_1T_S}{L}. \end{cases} \tag{7}$$

As the load current continues to decrease, the proposed PLASOM occasionally enters ZSM (zero supply mode), when the average $v_{ea}(t)$ ($\langle v_{ea}(t)\rangle$) is smaller than the threshold voltage ($\rm TH_{ot}$) for the PLASOM to activate cycle-extended off-time modulation. As a result, the duty perturbation ($\hat{d}_1(t)$) should always be 0 because the proposed PLASOM induces a zero duty in the ZSM. Fig. 7(b) and (c) illustrates the block diagrams of the small-signal models for a current-mode buck converter with the proposed PLASOM.

IV. Key Subcircuit Implementations

The key subcircuits of the proposed current-mode switching buck converter with PLASOM (i.e., Fig. 5) were classified into five categories: 1) soft-start (SS) circuit; 2) gate pulse, ramp, and clock generators; 3) two-step dead time (zero current detection (ZCD) included) and gate driver; 4) current sensor and *V–I* converter; and 5) the periodical power-down mechanism.

A. SS Circuit

The SS circuit (lower-right section in Fig. 5) often generates a linearly ramped-up reference voltage to limit the rush current and voltage overshoot during the power-on period of the power converter. In this work, an SS circuit based on a voltage follower (i.e., unity-gain buffer, UGB) was proposed, which can avoid an increase in the reference voltage ($V_{\rm REF}$) above the desired value (e.g., $V_{\rm REF\_IN} = 1$ V) if the input supply voltage ($V_{\rm IN}$) suffers from an unexpected spike. The slew rate of the UGB is designated, and the SS capacitor ($C_{\rm SS}$) is selected to meet the SS time requirement (e.g., 1 ms). After finishing the SS operation (e.g., $V_{\rm REF}$ approaching $\rm V_{REF\_IN}$), the mode select pin (*SS_en*) falls and bypasses $V_{\rm REF\_IN}$ to the EA to directly accelerate the voltage-scaling requirement (i.e., $V_{\rm REF\_IN}$ may be adaptively adjusted). In addition, *SS_en* is also used to power-down the UGB to conserve static power after finishing the SS operation.

B. Ramp and Clock Generators, Gate Pulse Generator (GPG), and VG Counter

Fig. 8(a) illustrates the clock and ramp generators, in which the control voltage $V_{\rm Ctrl}$ and resistor R_I determine the charge speed of C_I. Generally, the clock frequency and slope of the ramp waveform depend on $V_{\rm Ctrl}$, R_I, C_I, V_H, and V_L, considering the compensation of subharmonic oscillation [27]. Furthermore, a pulsewidth adjuster generates a tailored clock signal (*CLK*) by extending or shrinking the pulsewidth of *ckt*

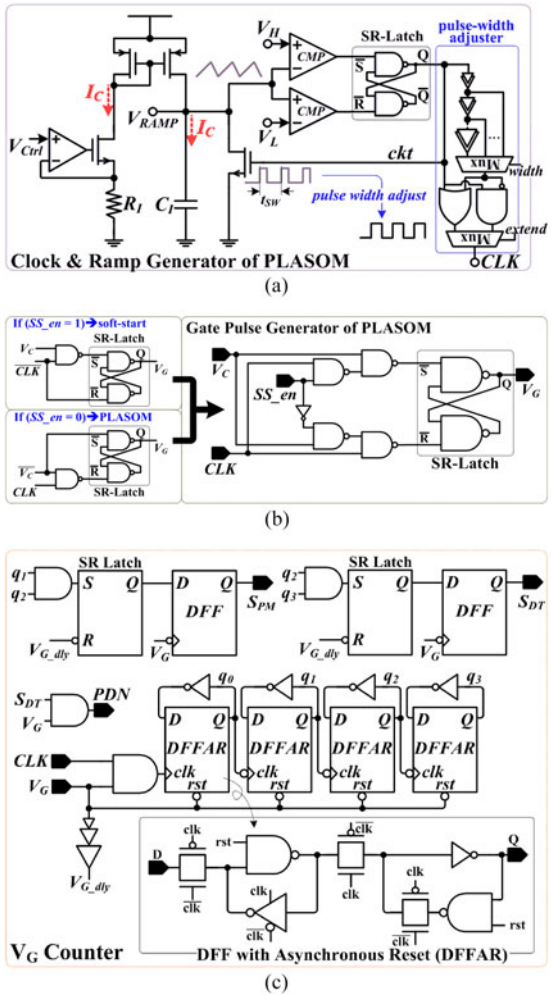

Fig. 8. (a) Ramp and clock generators. (b) GPG. (c) $V_{\rm G}$ counter.

(controlled by *width* and *extend* signals) to specify the threshold of activating the cycle-extended off-time mechanism of PLASOM. The pulsewidth adjuster is composed of several delay cells, one OR gate, one AND gate, and two multiplexers, in which the OR/AND gates execute logic operations on the clock signals *ckt* and delayed *ckt* to reshape the duty cycle of the *ckt*.

The GPG of PLASOM has two configurations, as the schematic illustrates in Fig. 8(b). When *SS_en* equals 1, the buck converter enters an SS period in which the PLASOM turns ON/OFF the power transistor at a constant frequency and in an adaptive on-time (depends on comparing the results of $V_{\rm EA}$ and $V_{\rm CCS}$, i.e., V_C) manner. The gate pulse V_G generated by the SR-Latch during the SS period should be reset each switching cycle, and thus, the reset of the SR-Latch controlled by the *CLK* signal has a higher priority than the SR-Latch setting controlled by the V_C signal. After finishing the SS operation (i.e., *SS_en* = 0), the buck converter switches back to PLASOM, in which the power transistor is switched ON/OFF either in an adaptive on-time mode with a constant frequency or a cycle-extended adaptive on/off-time mode with variable frequency, depending on the energy demands of the load circuit. During the PLASOM operation, the SR-Latch of the GPG should have

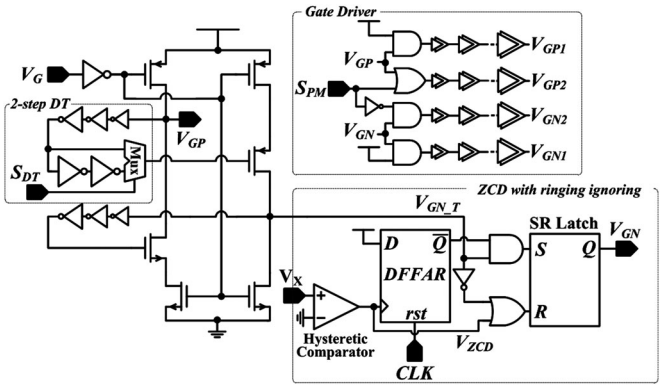

Fig. 9. Dead time control, ZCD with ringing ignoring, and gate driver.

a higher priority on set than reset to potentially activate the cycle-extended off-time mechanism.

As the average energy requirements of the load circuit decrease to a certain low level, the PLASOM activates the cycle-extended adaptive off-time mechanism so that V_G will not toggle for each *CLK* cycle. With a lower energy demand, V_G has a lower toggle rate. A simple counter-based load current estimator (V_G counter) is therefore designated, as shown in Fig. 8(c). First, a simple 4-bit binary counter enables accumulation at the time at which the *CLK* signal rises and V_G remains equal to 1 (i.e., current load estimation result). During the accumulation period of the 4-bit counter, two SR-latches will be set at the time at which the counter reaches predefined values (i.e., 6 for the switching power transistor size and 12 for the switching dead time in the proposed design). The outputs (Q) of the SR-latches will be held by two D-type flip-flops at the negative edge of the V_G signal to indicate the switching demands of the power transistor size ($S_{\rm PM}$) and dead time ($S_{\rm DT}$). The statuses of $S_{\rm PM}$ and $S_{\rm DT}$ will be updated each time the V_G signal toggles, at which point a loading estimation will be performed. After updating $S_{\rm PM}$ and $S_{\rm DT}$, the SR-latches are reset by the inverse of the delayed V_G signal ($V_{G\_{\rm dly}}$) to clear the current loading estimation results. Additionally, the 4-bit counter is reset each time the V_G toggles to repetitively estimate the loading status.

C. Two-Step Dead Time Control (ZCD Included) and Gate Driver

For the waveforms of the switching node (V_X) shown in Fig. 3, the turned-on/off sequence of the power transistors (MP_1, MP_2, MN_1, and MN_2 in Fig. 5) should be well controlled to reduce the shoot-through current loss and *V–I* overlap switching loss. The proposed dead time control and gate driver are based on the concept of a general short-circuit free buffer design [27] (see Fig. 9), where three design innovations improve the power loss reduction. First, a simple two-step dead time control (two-step delay time controlled by $S_{\rm DT}$) provides two dead-time periods between the rising of $V_{\rm GP}$ and $V_{\rm GN}$ to reduce the charging loss or body diode conduction loss, as illustrated in Fig. 3. Furthermore, $V_{\rm GN}$ should be forced to zero when the zero current/voltage status is detected. A general ZCD circuit was implemented by a hysteretic comparator by comparing the voltages of the switching node and ground. This, however, results in a false transition of $V_{\rm GN}$ because of the ringing phenomenon of the switching node during the dead-time period. Thus, a simple ringing ignoring circuit was proposed, as shown in the lower-right section of Fig. 9. For every *CLK* cycle, when zero current is detected ($V_{\rm ZCD}$ equals logic 1) for the first time, $V_{\rm GN}$ is forced to zero through the reset function of an SR-latch, and the set function is blocked by the output of a D-type flip-flop with asynchronous reset. As a result, $V_{\rm GN}$ will not be set to 1 in the current switching cycle, even though $V_{\rm ZCD}$ toggles frequently because of the ringing of the switching node. Finally, a two-level gate driver is designed to stop switching part of whole power transistors when the switching loss becomes significant in the power loss distributions. In the upper-right section of Fig. 9, $V_{\rm GP2}$ and $V_{\rm GN2}$ are blocked when $S_{\rm PM}$ becomes equal to 1.

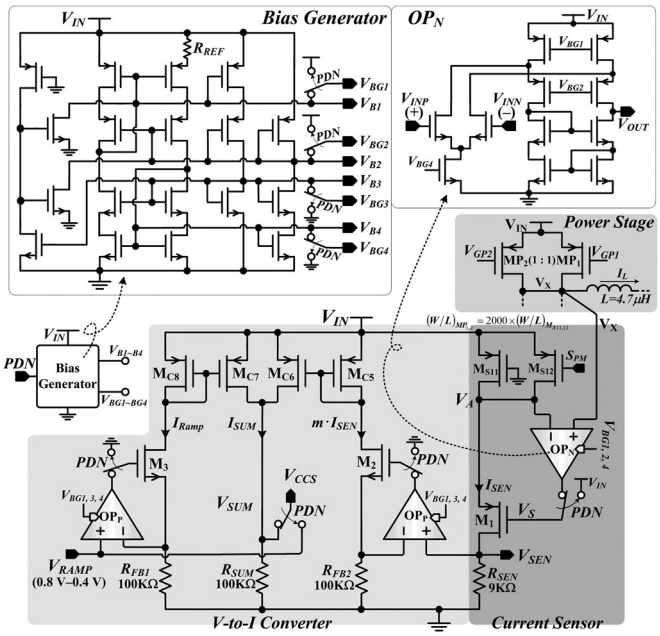

Fig. 10. Current sensor and *V–I* converter (with periodic power-down mechanism).

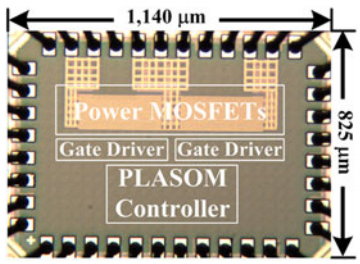

Fig. 11. Micrograph.

D. Current Sensor and V–I Converter

The detailed schematics of the current sensor and *V–I* converter are illustrated in Fig. 10, with the power-down signal (PDN) and the corresponding switches neglected. Because the inaccuracy of the current sensor degrades the regulation

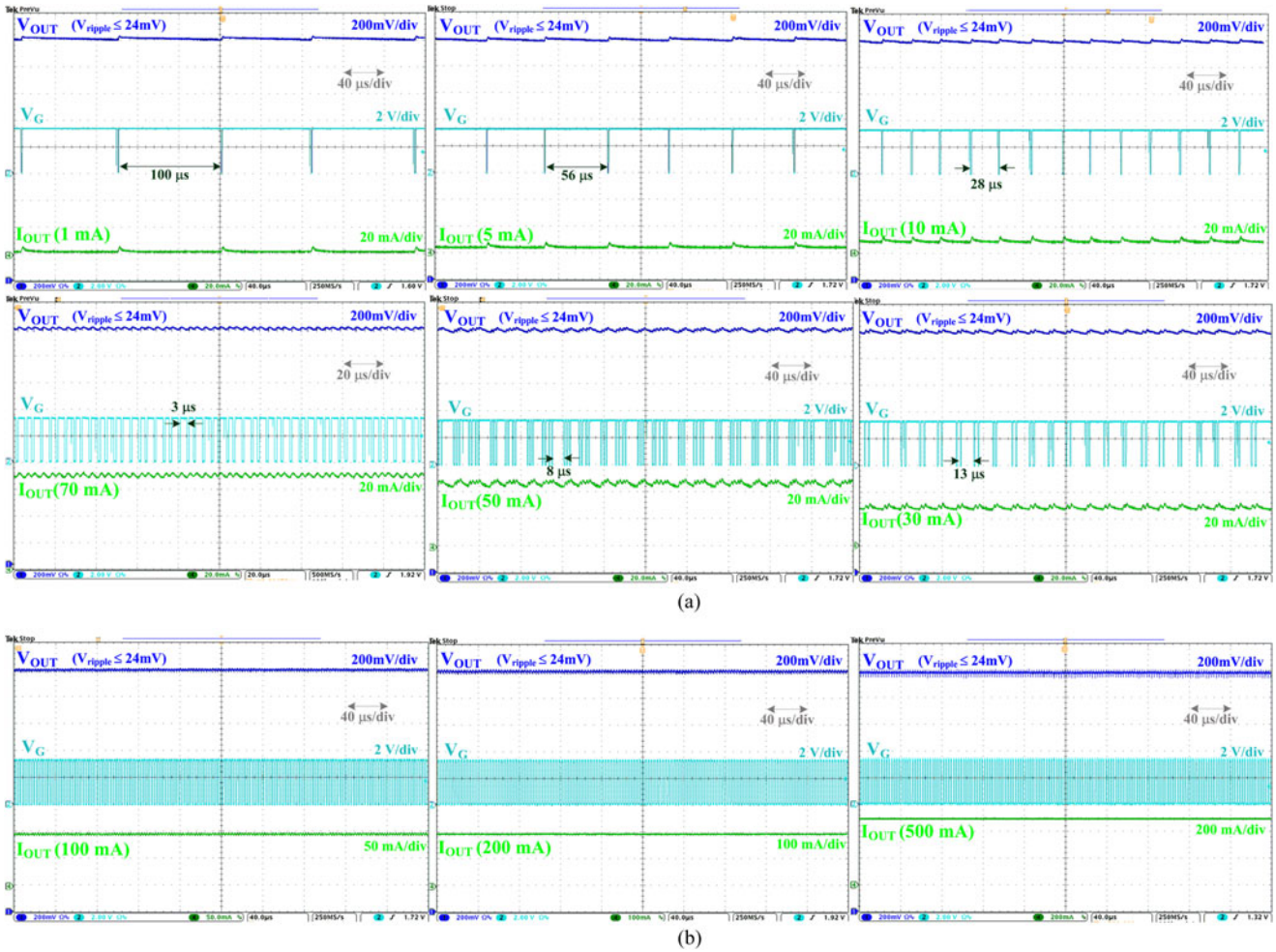

Fig. 12. Measured steady-state waveforms ($V_{\rm IN}/V_{\rm OUT} = 3.3\ {\rm V}/1.8\ {\rm V}$): (a) $I_{\rm OUT} = 1$, 5, 10, 30, 50, and 70 mA (cycle-extended adaptive off-time with variable frequency) and (b) $I_{\rm OUT} = 100$, 200, and 500 mA (adaptive on-time with constant frequency).

performance, a conventional high-accuracy current-sensing circuit was adapted into the current-mode buck converter design, where a high-gain amplifier (OP_N) along with a transistor M_1 constructing a high-gain loop ($V_{\rm A}$–$OP_{\rm N}$–M_1) are used to equalize V_X and V_A. For a wide load current range requirement (e.g., 0.1–500 mA), a ratio of 2000:1 was selected for a transistor size of $MP_1 (= MP_2)$ and $M_{S11} (= M_{S12})$ to achieve a balancing point of power consumption and noise immunity (e.g., the resultant sensed current ($I_{\rm SEN}$) is in the range of 250–50 μA). Two sensing transistors (i.e., M_{S11} and M_{S12}) are accompanied by a two-step power transistor sizing to maintain the same sensing ratio (2000:1). An *N*-type folded-cascode amplifier (OP_N) is used to achieve the requirements of high gain, high bandwidth, and wide input common mode (0.8–3.3 V), whereas a wide-swing bias generator is adopted for OP_N to minimize the voltage drop (i.e., only two overdrive voltages) on output (e.g., V_S requires 2.4–3 V in the design detailed herein). Thus, the current sensing resistance ($R_{\rm SEN}$) is selected to be 9 kΩ (resulting in a sensed voltage ($V_{\rm SEN}$) of 2.25–0.45 V) to ensure that M_1 stays in the saturation region and maintains a high gain loop. Then, a general current summation circuit is adopted as the *V–I* converter, where two high gain amplifiers (OP_P) allow $V_{\rm RAMP}$ and $V_{\rm SEN}$ to be accurately sensed by $R_{\rm FB1}$ and $R_{\rm FB2}$. The OP_P using a p-type folded cascode configuration was designed because the two input signals $V_{\rm RAMP}$ and $V_{\rm SEN}$ are in the voltage ranges of 0.4–0.8 V and 0.45–2.25 V, respectively. Furthermore, $R_{\rm FB2}$ was chosen to be 100 kΩ for m to be 9/100 to ensure that the current range of $M_{C5}(m \times I_{\rm SEN})$ is comparable to $I_{\rm Ramp}$ (i.e., a few μA). Finally, $R_{\rm SUM} = R_{\rm FB1} = R_{\rm FB2}$ were chosen to achieve $V_{\rm SUM} = V_{\rm RAMP} + V_{\rm SEN}$.

E. Periodic Power-Down Mechanism

The current sensor and *V–I* converter circuits contribute most significantly to quiescent power loss, mainly during the short effective period (i.e., sensing current of MP_1 and MP_2 during $V_G = 0$, getting shorter in light-load condition). To avoid delaying the transient response upon cutting down the quiescent power loss, a periodic power-down scheme is proposed by switching off idle circuits on demand for each switching cycle. As shown in Fig. 10, all bias voltages ($V_{\rm BG1}$–$V_{\rm BG4}$) are switched to the supply voltage ($V_{\rm IN}$) or the ground to cut down the corresponding biased currents of the amplifiers (OP_N and OP_P) when the power-down signal (PDN) is issued. The gate terminals of transistor M_1, and $M_2 (M_3)$ should be switched to $V_{\rm IN}$ and the ground while switching $V_{\rm CCS}$ to $V_{\rm RAMP}$ because

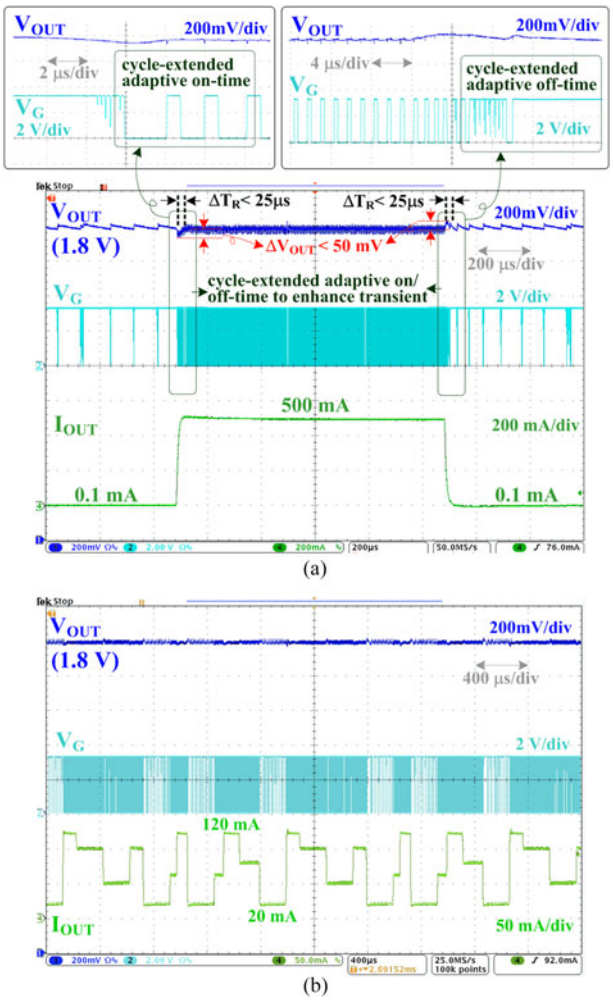

Fig. 13. (a) Measured transient response for the condition of $V_{\rm IN}/V_{\rm OUT} = 3.3\ {\rm V}/1.8\ {\rm V}$, $I_{\rm OUT} = 0.1\ {\rm mA}\leftrightarrow 500\ {\rm mA}$. (b) Measured regulated output for the fluctuating load current profile.

all amplifiers are powering down. As a result, the current sensor and *V–I* converter are easily deactivated during the power-down period. It is noted that several nodes were forced to $V_{\rm IN}$ or the ground during the power-down period, which also consumes additional switching power. Thus, the periodical power-down signal (PDN) was issued when both the V_G and $S_{\rm DT}$ equal 1 (i.e., $I_{\rm OUT} < 30$ mA), as shown in Fig. 8(c), which ensures that the power-down scheme can be activated for a long period of time (i.e., at a relatively low switching frequency resulting from the proposed PLASOM).

V. Experimental Results and Performance Evaluations

The proposed current-mode switching buck converter with PLASOM (see Fig. 5, with the subcircuits of Section IV) was designed and implemented using TSMC 1/3.3-V 90-nm CMOS process technology. The chip micrograph is shown in Fig. 11, with a total area of 0.94 mm^2. The proposed converter can convert an input voltage of 3.0–3.6 V to an output voltage of 1.0–1.8 V in a load current range of 0–500 mA, while an external

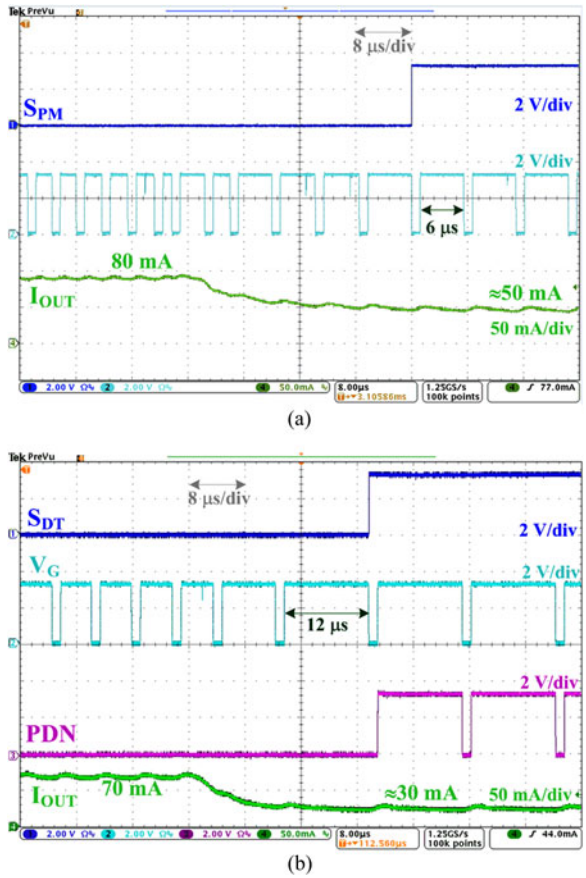

Fig. 14. Measured waveforms of (a) $S_{\rm PM}$ and (b) $S_{\rm DT}$ and PDN.

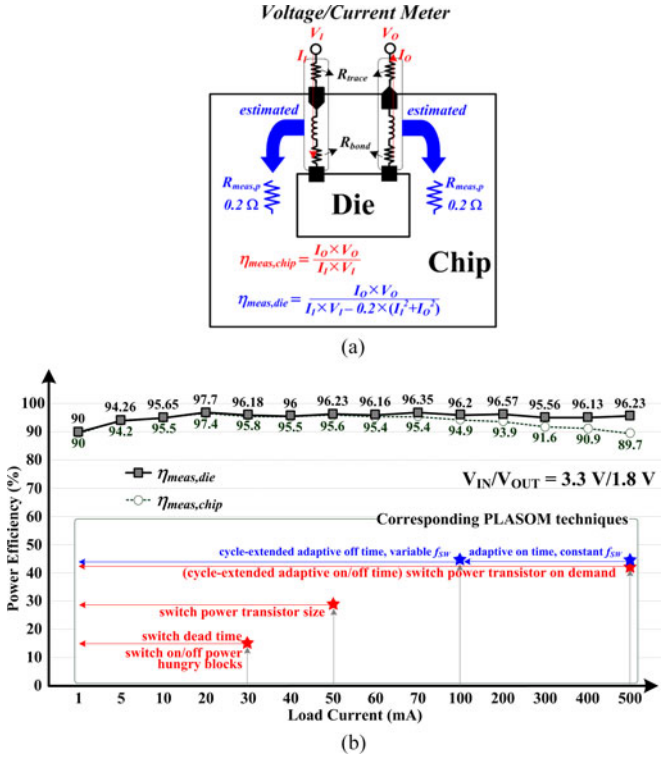

Fig. 15. (a) Conceptual diagram of the test chip. (b) Measured power efficiency.

TABLE III
PERFORMANCE EVALUATIONS

Parameters \ Design	[10]	[11]	[12]	[14]	[16]	[19]	[20]	[21]	[22]	This Work
Year	2007	2012	2008	2007	2010	2007	2008	2013	2007	2015
Technology (CMOS)	0.35 µm	0.35 µm	0.35 µm	0.5 µm	0.35 µm	0.6 µm	0.35 µm	0.18 µm	0.35 µm	90 nm
Publication	*IET CDS.*	*TPE*	*ISSCC*	*ISSCC*	*EL*	*TPE*	*TPE*	*TVLSI*	*JSSC*	–
Category (Fig. 2)	❶	❷		❸	❹	❺			❻	–
Power Loss Reduction (Tab. I)	P_{GD}, P_C	P_S, $P_{C,DC}$		P_{GD}	P_{DT}	P_{CTRL}			P_S, $P_{C,DC}$	P_S, P_C, P_{CTRL}
V_{IN} (V)	3.6	2.4 – 3.6	1.8 – 3.0	3.6	3.6	2.2 – 6.0	2.7 – 5.0	2.7 – 3.6	3.3	3.0 – 3.6
V_{OUT} (V)	2	0.7 – 3.3	0.9	1/1.5/1.8	1.8	0.6 – 5.8	1.0 – 1.8	1.8	1.65	1.0 – 1.8
Control mechanism	One Cycle	PWM	ASFPWM	PWM	PWM	PWM, PFM	PWM, PFM	DOTM	PWM, DSM, PFM	PLASOM
Filter Inductor L (µH)	N.A.	4.7	2.2	3.3	0.47	4.7	10	2.2	4.7	4.7
Filter Capacitor C_{OUT} (µF)	N.A.	10	2.2	4.7	4.7	10	10	10	4.7	10
Switch Frequency f_{SW} (MHz)	N.A.	0.2 – 2	0.25, 0.5, 1.0, 2.0	3.0	10	1.1	0.1 – 0.6	0.044 – 1.65	1 (max.)	1 (max.)
Load Current Range I_{OUT} (mA)	0 – 400	0 – 1050	5 – 500	10 – 400	20 – 600	0.5 – 1000	1 – 460	3 – 400	0.1 – 500	0 – 500
Output Ripple V_{ripple} (mV)	N.A.	16	< 30	N.A.	N.A.	< 3 (PWM)	36	20	< 35	24
Transient Response ΔV_{OUT} (mV)/ΔT_R (µs) @(I_{OUT1}–I_{OUT2}, mA)	100/62 (0 – 400)	>200/85 (50 – 1050)	N.A.	N.A.	N.A.	<90/<20 (200 – 700)	N.A.	150/60 (3 – 400)	66/N.A. (30 – 120)	<50/<25 (0.1 – 500)
Transient Response ΔV_{OUT} (mV)/ΔT_R (µs) @(I_{OUT2}–I_{OUT1}, mA)	100/64 (400 – 0)	200/140 (1050 – 50)	N.A.	N.A.	N.A.	<90/<20 (700 – 200)	N.A.	160/190 (400 – 3)	N.A.	<50/<25 (500 – 0.1)
Max. Power Efficiency η_{max} (%) @(I_{OUT1}–I_{OUT2} in mA)	96 (0 – 400)	96.3 (0 – 1050)	90 (2 – 500)	89.1 (10 – 400)	85 (20 – 600)	96.7 (0.9–800)	95 (3 – 460)	95.2 (3 – 400)	95 (3 – 500)	> 97.4 (1 – 500)
Min. Power Efficiency η_{min} (%) @(I_{OUT1}–I_{OUT2} in mA)	N.A.	> 80 (N.A.)	55 (2 – 500)	66 (10 – 400)	45 (20 – 600)	88.5 (0.9–800)	85 (3 – 460)	91 (3 – 400)	90 (3 – 500)	90 (1 – 500)

4.7-μH inductor (L) and an external 10-μF capacitor ($C_{\rm OUT}$) are connected for measurements.

A. Steady-State Performance

Fig. 12 shows that the proposed current-mode switching buck converter with PLASOM can properly regulate the output for a wide load current range of 1–500 mA when it converts 3.3 to 1.8 V. The cycle-extended adaptive off-time mechanism is activated in the light-load condition [e.g., 1–70 mA in Fig. 12(a)], where the off-time periods are extended to approximately 100 μs under a load current ($I_{\rm OUT}$) of 1 mA. When the load current demand increases to the heavy-load condition [i.e., >70 mA in the design proposed herein, as shown in Fig. 12(b)], the proposed converter with PLASOM operates in an adaptive on-time mode with constant frequency (i.e., at a maximum $f_{\rm SW}$ of 1 MHz). Fig. 12 also shows that the ripple voltage is kept smaller than 24 mV over a wide load current range because of the PLASOM.

B. Transient Performance

Fig. 13(a) shows the measured waveforms of the load transient test by switching the load current between 0.1 and 500 mA, where the input/output voltage ($V_{\rm IN}/V_{\rm OUT}$) is set to (3.3/1.8 V). The maximum output variations (overshoot/undershoot, $\Delta V_{\rm OUT}$) are smaller than 50 mV, and the transient recovery time (ΔT_R) is less than 25 μs. It can be observed that either the cycle-extended adaptive on-time mechanism or cycle-extended adaptive off-time mechanism is activated during a light- to heavy-load transition (i.e., 0.1–500 mA) or a heavy- to light-load transition (500–0.1 mA) to accelerate the transient response by seamlessly increasing/decreasing the inductor current, respectively. To emulate the fluctuating load current profile induced by a general multifunction SoC, Fig. 13(b) shows the measured waveform of a fluctuating load current profile, where the proposed converter with PLASOM still properly regulates the output with small output variations.

C. Power Efficiency

The functions of switching the power transistor size and dead time on demand are demonstrated in Fig. 14(a) and (b), respectively, where the signal $S_{\rm PM}/S_{\rm DT}$ was set in case the off-time period reaches a predefined value (e.g., $\rm TH_{PTsize}/TH_{DT} = 6/12$ for V_G counter, approximately 6/12 μs). Fig. 14(b) also demonstrates that the function of power-down (PDN*)* was activated when the load current decreases to around 30 mA. Fig. 15(a) shows the conceptual diagram of the test chip, in which the parasitic resistance induced by bonding wire and PCB trace (i.e., equivalent resistance ($R_{{\rm meas},p}$) is estimated to be 0.2 Ω) induces extra power loss other than the converter. Fig. 15(b) shows the measured power efficiency, in which $\eta_{\rm meas,chip}$ stands for the measured efficiency of the test chip, while the efficiency curve $\eta_{\rm meas,die}$ excludes the power loss of $R_{{\rm meas},p}$. The measured efficiency verifies that the high power efficiency (>90%) of a switching buck converter over a wide load range (1–500 mA) is achieved by adopting the proposed PLASOM controller. The lower section of Fig. 15(b) also depicts the load current range for the corresponding PLASOM techniques to be activated.

D. Performance Evaluations

Table III summarizes the performance comparisons between the proposed switch buck converter with PLASOM and several

previous works. Because the proposed PLASOM switches the power transistor status (ON/OFF, and size), dead time, and subblocks status (ON/OFF) on demand, the conversion power efficiency is superior compared to those previous works in a wide load current range of interest (i.e., 1–500 mA). In addition, the proposed PLASOM offers a cycle-extended adaptive on/off-time mechanism without mode decision/change so that the transient response [i.e., in terms of transient overshoot/undershoot $(\Delta V_{\mathrm{OUT}})$] and recovery time (ΔT_R)] of the buck converter are greatly improved compared to those in a prepublished high-efficiency converter. Although the design in [19] offers a slightly better recovery time (< 20 μs versus $<$ 25 μs), it is tested by a switching load current between 200 and 700 mA, in which the mode detection/change (PWM↔PFM, i.e., worst case) is not triggered. Finally, the output ripple is controlled ($<$24 mV) to be comparable to those of previous works. In summary, the proposed current-mode switching buck converter with PLASOM is more favorable than those of previous works [10]–[12], [14], [16], [19]–[22], simultaneously achieving high conversion efficiency, rapid transient response, a small output ripple, and reduced design complexity.

VI. Conclusion

This paper presents a current-mode switching buck converter with the proposed PLASOM technique, which can achieve high conversion efficiency, fast transient response, and small ripples simultaneously over a wide load current range. The proposed converter with PLASOM was designed and fabricated using the TSMC 90-nm CMOS process to convert an input of 3.3 V to an output of 1.8 V, while achieving an above 90% power efficiency over a 1–500 mA load current range, a smaller than 50 mV/25 μs output variation/recovery time for a 0.1–500 mA load transient test, and a 24-mV output ripple. Experimental results and performance evaluations verify the feasibility of the proposed PLASOM technique.

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