A Gate Driver With Integrated Deadtime Controller

Romain Grezaud, François Ayel, Nicolas Rouger, and Jean-Christophe Crebier, *Member, IEEE*

***Abstract*—Deadtimes are required to avoid simultaneous conduction of high-side and low-side power transistors in half-bridge power converters. During these secure times, free-wheeling current flow generates extra power losses. Very short deadtimes are desired but they cannot be safely set in conventional isolated power converters because of a digital input propagation delay mismatch. A specific deadtime management is introduced in this paper to ensure proper operation of a high-voltage synchronous power converter. A controller integrated in each isolated gate driver secures synchronous switching by detecting the opposite switch turn-off before turn-on. With such a selfswitching technique, very short but safe nonoverlap times can be set. A gate driver has been implemented in a 0.35 μm 20-V CMOS process. The monolithically integrated controller consumes only 140 μA and 0.22 mm^2 of silicon area. The proposed local deadtime management has been validated in two synchronous buck converters without external free-wheeling diodes: a 500-W 250-V to 55-V converter based on SiC JFETs and a 30-W 45-V to 10-V converter based on eGaN FETs. In either case, the proposed controller allows a higher efficiency from 10% of the rated load with resulting deadtimes as short as 15 ns.**

***Index Terms*—Analog integrated circuits, crosstalk, deadtime optimization, driver circuits, synchronous buck converter, wide-band gap semiconductors.**

I. Introduction

POWER electronics is constantly evolving toward smaller and more efficient power conversion systems. Such a progress is relevant only if the price, complexity, and reliability of the overall system are not sacrificed. Between each conduction period of a synchronous power converter, a safe deadtime must be set in order to avoid significant shoot-through current loss. Although every switch is OFF in this safety state, a free-wheeling current is still flowing through body diodes generating extra power loss [1], [2]. Thus, higher performance Schottky diodes are commonly used in antiparallel with power transistors to conduct almost all current in reverse instead of body diodes [3]. Moreover long deadtime can lead to distortion of output voltages and currents of power converters [4]–[6]. In this paper, we propose a safe selfswitching technique to reduce deadtime and its undesirable effects in a synchronous power converter without additional externally connected diodes in antiparallel.

By removing external diodes, the number of sources of failure, and the cost and size of power conversion systems decrease but more losses are generated during the deadtimes. These extra losses are evaluated by a calorimetric method in a GaN device-based power converter in [1]. Contrary to low-voltage synchronous converters [7], a short deadtime is difficult to guarantee in industrial high-voltage power converters. In fact, the high voltage between high side and low side implies the use of separate gate drivers and additional isolation circuits. Digital input propagation paths can no longer be matched inside a single half-bridge gate driver chip [8], [9]. As a result, a significant difference can appear between the effective deadtime and the theoretical one set by the microcontroller (MCU).

Previous work focused on dynamic deadtime generation techniques to safely shorten deadtime. It was found that additional isolated feedback loops between high side and low side can be used to keep half-bridge gate drivers synchronized over a wide temperature range [10]. The optimal deadtime for a fixed operating point is calculated by FPGA or MCU in [11]–[13] from online output current or voltage measurements and from an accurate analytical model of the whole power converter. Other work focused on the body diode conduction detection on the half-bridge high-voltage switch node [14]–[23]. In that case, the advanced gate drivers must be properly design with high-voltage devices to withstand the maximum supply voltage in the power converter.

In this paper, we introduce a dynamic dead-time generation capable of safely setting a very short deadtime in high-voltage synchronous converters without any additional isolation barriers, complex calculations, load-side monitoring, or high-voltage devices. We propose to detect the reverse conduction mode directly on the gate side of power transistors by taking advantage of the gate-to-drain parasitic capacitance. In this way, deadtimes are generated and managed closer to power transistors by each isolated gate driver instead of the MCU. Moreover, with this particular deadtime management, the only limiting factor in dc to raise the maximum operating voltage is the breakdown voltage of power transistors and characteristics of isolation barriers. A gate driver integrating the deadtime controller has been implemented in an AMS 0.35-μm 20-V CMOS process, and in two wide-bandgap (WBG) devices-based synchronous buck converters without externally connected diodes in antiparallel.

This paper first introduces the behavior of half-bridge power converters without diodes highlighting the impact of deadtime. Then, the gate driver is detailed with its integrated dynamic deadtime controller. Finally, experimental results are presented to evaluate the benefit of the integrated deadtime management in diode-less synchronous buck converters.

Manuscript received May 12, 2014; revised July 10, 2014, September 21, 2014, October 14, 2015, and December 14, 2015; accepted January 02, 2016. Date of publication January 13, 2016; date of current version July 08, 2016. Recommended for publication by Associate Editor T. Lebey.

R. Grezaud and F. Ayel are with the CEA Leti, MINATEC Campus, University Grenoble Alpes, Grenoble 38054, France (e-mail: romain.grezaud@cea.fr; francois.ayel@cea.fr).

N. Rouger and J.-C. Crebier are with the Grenoble Electrical Engineering Laboratory (G2ELab), University Grenoble Alpes, CNRS, Grenoble 38400, France (e-mail: nicolas.rouger@g2elab.grenoble-inp.fr; jean-christophe.crebier@g2elab.grenoble-inp.fr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2517679

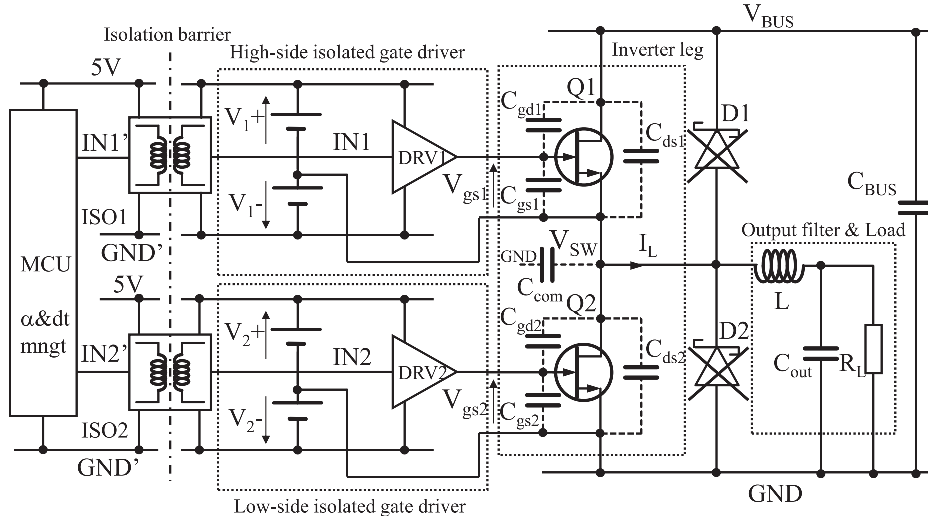


Fig. 1. Circuit schematic of the synchronous buck converter without additional antiparallel diodes.

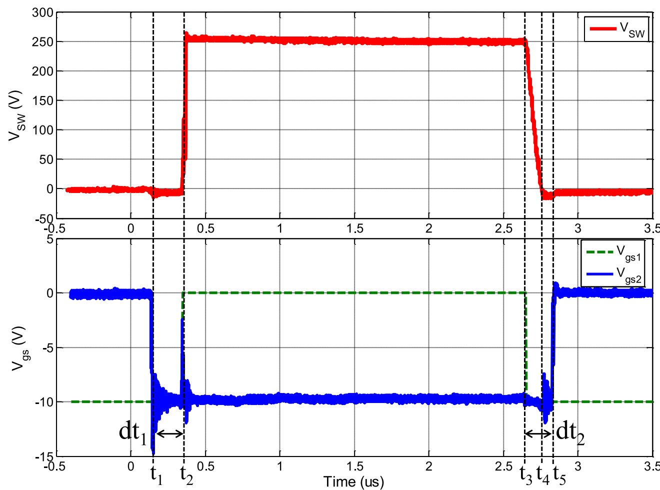


Fig. 2. Experimental waveforms of the diode-less SiC JFET-based buck converter for 250-V input voltage, 500-mA output current, and 100-kHz switching frequency with 200 ns deadtimes.

II. Diode-Less Half-Bridge Power Converter

A. Half-Bridge Power Converter Operation

The elementary inverter leg structure is made of power transistors Q1 and Q2 connected in series between two power supply terminals V_{BUS} and GND. In this paper, we focus on the synchronous buck converter structure of a generic high-voltage step-down dc/dc converter shown in Fig. 1 but without any Schottky diode D1 and D2, usually externally connected in antiparallel. Nevertheless, our study can be used in other dc/dc, ac/dc, and dc/ac converter topologies based on a commutation cell and an inductive load without further modification.

Each power transistor is driven by a gate driver connected between gate and source and supplied by a positive V+ and a negative V– isolated power supply. There are different structures of gate driver output stage [24] but only the most common CMOS push–pull output buffer has been considered in this paper. The chosen normally-on SiC JFET having a threshold voltage $V_{\mathrm{gs,th}}$ equal to -5 V, its gate is driven between 0 V $=$ V$_{1,2}+$ and -10 V $=$ V$_{1,2}-$. The chosen normally-off EPC2007 eGaN FET is driven between -2.5 V and $+3.3$ V to avoid any parasitic turn-on because of a minimum 0.7-V threshold voltage and to limit the gate–source voltage under the maximum voltage of 6 V even with non-negligible parasitic inductance in the gate drive loop. Each gate driver is a low-voltage circuit referenced to the source of their respective power transistor. These floating circuits receive an isolated input signal IN1 and IN2 from an MCU or FPGA to alternately drive Q1 and Q2. The duty cycle α and deadtimes *dt* are generated and managed by this digital control unit. A conventional digital PWM control has been used in this study.

Fig. 2 shows waveforms of the SiC JFET-based synchronous buck converter without external diodes for an input voltage V_{BUS} equal to 250-V, 500-mA output current and fixed 200-ns deadtimes. During a switching period, we distinguish following four main time domains.

1) Before time t$_1$, V_{gs2} is high and V_{gs1} is low. The output current I_L flows in reverse through Q2. The drain to source drop V_{ds2}, equal to the voltage at the switching node V_{SW}, is minimal.
2) The time dt_1 between t_1 and t_2 is defined as the first deadtime. During dt_1, V_{gs1} and V_{gs2} are low in order to prevent Q1 and Q2 from being on together. With no more antiparallel diodes, Q2 is still freewheeling the current I_L while V_{gs2} is below $V_{\mathrm{gs,th}}$. The drain to source voltage drop V_{ds2} is higher during deadtime as detailed hereinafter.
3) Between t$_2$ and t$_3$, Q1 is ON and V_{SW} is approximately equal to the input voltage V_{BUS}. The current I_L flows from the power supply to the load through Q1.
4) For the second deadtime dt_2 between t$_3$ and t$_5$, V_{gs1} and V_{gs2} are low. From t_3 to t_4 the capacitive node V_{SW} is discharged by the constant current I_L. After t_4, Q2 conducts the current exactly as on time dt$_1$.
5) From time t_5, V_{gs2} is over $V_{\mathrm{gs,th}}$. Q2 conducts the current I_L as before time t_1.

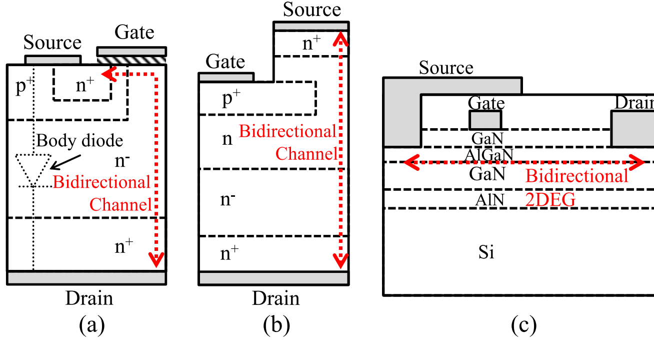


Fig. 3. Schematic cross-section of (a) vertical SiC or Si MOSFET, (b) vertical SiC trench JFET and (c) lateral GaN HEMT.

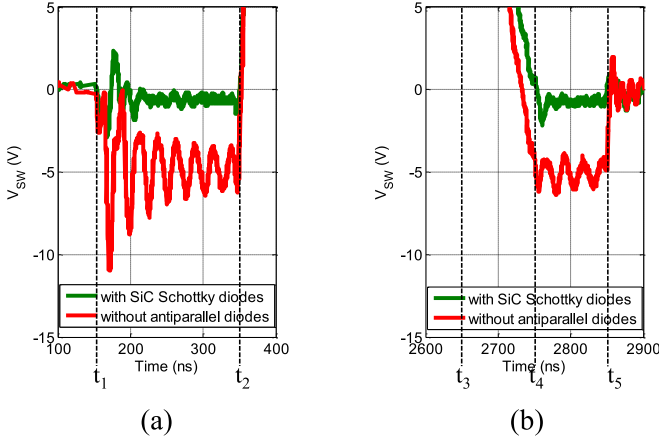


Fig. 4. Reverse conduction comparison during deadtimes of the SiC JFET-based buck converter with and without additional antiparallel diodes for 500-mA output current at (a) Q1 turn-on and (b) Q1 turn-off.

B. Reverse Conduction Without External Antiparallel Diodes

WBG devices such as GaN HEMTs, SiC MOSFETs, and SiC JFETs demonstrate outstanding static and dynamic performance. They are expected to be used in high temperature [25], [26], high power density [7], [27], [28] and high-frequency [7], [29]–[31] power converters instead of silicon devices because they offer a better intrinsic performance in these fields [32], [33]. As for conventional Si MOSFETs, these WBG devices are bidirectional. In other words, their direct and reverse conduction characteristics are identical when the gate–source voltage $V_{\rm gs}$ is higher than the threshold voltage $V_{\rm gs,th}$. However, subthreshold reverse conduction characteristics depend on the internal transistor structure.

A schematic cross-section of a vertical Si or SiC MOSFET [3], [34], a vertical SiC trench JFET [35]–[37], and a lateral GaN HEMT [7] are depicted in Fig. 3(a), (b) and (c), respectively. In the first device, the current can flow through a bidirectional lateral–vertical channel and in reverse though a parasitic P-N junction diode. SiC MOSFETs have lower reverse recovery charge than Si MOSFETs [38] but also a higher forward voltage drop: 3–3.5 V [39] compared to 0.8–1.2 V for a -25A current flow [40] (temperature and device dependent). In the second and third devices, the current can only flow through a pure vertical channel or a lateral two-dimension electron gas (2DEG). In fact, pure vertical SiC trench JFETs and lateral GaN HEMTs do not have a built-in body diode. Current can even flow from source to drain when $V_{\rm gs}$ is lower than $V_{\rm gs,th}$ but with characteristics depending on the gate voltage. In that case, linear approximation (1) can be applied to the conduction characteristic in the third quadrant: the lower the $V_{\rm gs}$, the higher the $V_{\rm ds}$ and so the higher the reverse voltage drop

$$V_{\rm ds} = V_{\rm ds,dt} = V_{\rm gs} - V_{\rm gs,th}. \tag{1}$$

For the experimental implementation of the proposed deadtime management, we chose a 1200-V/27-A normally-on vertical SiC trench JFET and a 100-V/6-A normally-off lateral GaN HEMT. The drain–source voltage drop during deadtimes $V_{\rm ds,dt}$ is estimated by (1) at -5V with SiC JFETs and -4V with GaN HEMTs. An experimental reverse conduction comparison is shown in Fig. 4(a) and (b) at Q1 turn-on and Q1 turn-off for a 500 mA output current. When high performance SiC Schottky diodes are used, the voltage drop at the half-bridge switch node $V_{\rm SW}$ is almost -1 V while we observe an almost -5 V voltage drop without any antiparallel diodes.

III. Deadtime Issue

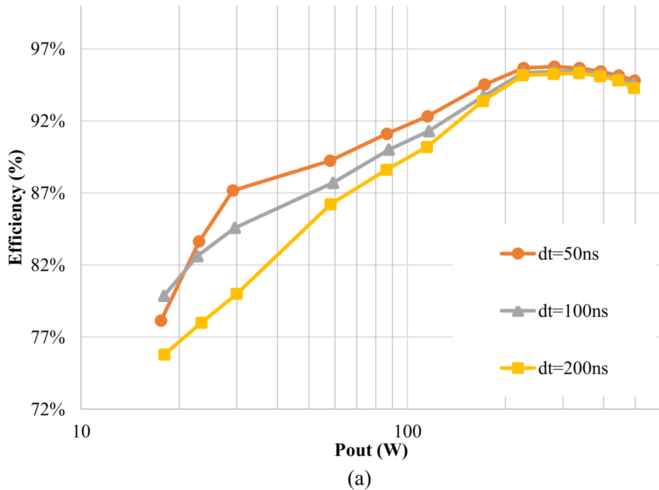
A. Deadtime Influence

By removing Schottky diodes in antiparallel, the number of sources of failure, and the cost and size of power converters decrease but the drain to source voltage drop $V_{\rm ds,dt}$ is higher during deadtime, generating extra conduction losses. Expression of these deadtime reverse conduction losses $P_{\rm dt}$ is given by (2). For the chosen diode-less SiC JFET, $V_{\rm ds,dt}$ is approximated using (1). One observes that conduction losses generated during the deadtime depend on deadtimes dt_1 and dt_2, turn-off time $t_{\rm off}$, the switching frequency *f*, and the RMS output current $\overline{I_L}$.

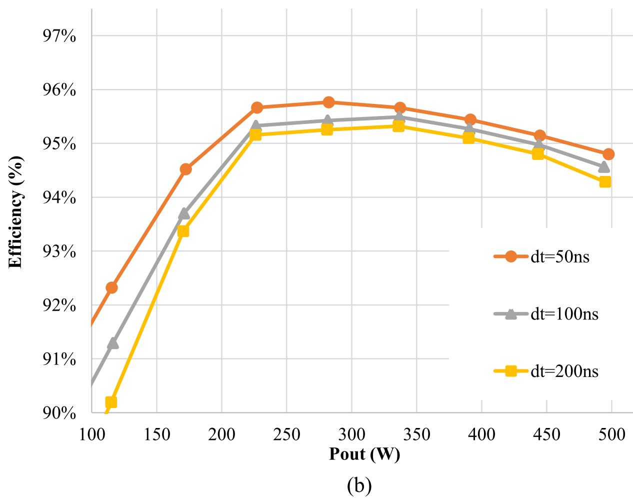
To observe the impact of deadtime on power losses as a function of the output power $P_{\rm out}$, we made measurements on a 250-V input to 55-V output and 100-kHz switching frequency buck converter. Fig. 5 shows the experimental results of the converter operating with deadtime dt_1 equal to dt_2 from 50 to 200 ns at different loads. Agilent 34411 A and 34405A digital multimeters were used for input and output power measurements. 95.7% peak efficiency is reached with a 50-ns deadtime at almost 280-W output power. The best efficiency is obtained with 50-ns deadtime and the worst with 200 ns. However, at the lightest load, the best efficiency is not obtained with the shortest deadtime but with 100 ns. In fact, for this particular case, the time $t_{{\rm off},m}$ given by (3) and taken by $V_{\rm SW}$ node to completely fall to ground is longer than 50 ns. In this case, the low-side transistor Q2 is turned ON (hard switching condition) and more losses are generated. Except for the lightest load, shorter deadtimes are the most efficient but are also the most difficult to guarantee

$$P_{\rm dt} = V_{\rm ds,dt} \cdot (dt_1 + dt_2 - t_{\rm off}) \cdot \overline{I_L} \cdot f \tag{2}$$

$$t_{{\rm off},m} \approx 2C_{\rm oss} \cdot \frac{V_{\rm BUS}}{\overline{I_L}}. \tag{3}$$



(a)



(b)

Fig. 5. Experimental efficiency comparison for deadtime from 50 to 200 ns in a 250-V input, 55-V output, and 100-kHz switching frequency diode-less SiC vertical JFET-based buck converter on a (a) logarithmic scale (b) linear scale.

B. Matching Issue Between High Side and Low Side

In high-voltage synchronous converters such as the one in Fig. 1, input signals IN1' and IN2' generated by the MCU are isolated and translated to signals IN1 and IN2 by two separate isolators ISO1 and ISO2. These isolated signals are received by DRV1 and DRV2 to alternately switch Q1 and Q2. Although high-side and low-side paths are equivalent, their propagation delays are mismatched because of the inherent industrial process dispersions between two separate chips. For instance, the isolator propagation delay dispersion is over 150 ns with opto-couplers [41] but it can be reduced to 10 ns with more expensive and complex top grade digital isolators [42]. A gate driver specifically designed for WBG transistors [43] demonstrates 19 ns propagation delay dispersion. Due to the mismatch of both sides, the MCU cannot guarantee the effective deadtime on each gate. It has to deal with a deadtime longer than 50 ns with special matching RF-based digital isolators [42] and 200 ns with high-speed opto-couplers [41]. Integrating the deadtime management directly in gate drivers after the isolation barrier will help to relax constraints on input signal propagation delay matching while safely setting reduced deadtime.

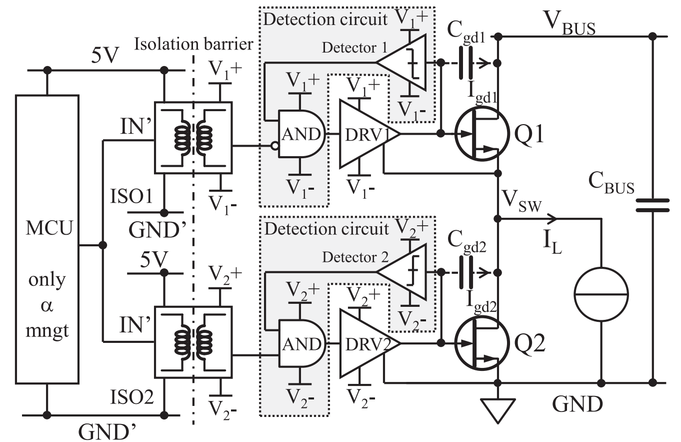


Fig. 6. Circuit schematic of the synchronous buck converter implementing a selfswitching technique at turn-on to safely generate reduced deadtime.

IV. Integrated Deadtime Controller

Previous work has already introduced autoadaptive deadtime management to improve synchronous power converter operations. Some of this work focused on deadtime management by load side monitoring [11], [12]. In [13], an MCU is able to adjust the deadtime by updating a preset deadtime optimization model with online monitoring of gate–source and drain–source voltage commutation times. To be effective, these methods require additional measurements, an accurate converter model and fast calculations. Other work focused on body diode reverse conduction detection from the high-voltage switch-node $V_{\rm SW}$ [14]–[23]. As a result, additional high-voltage sensors are then required for zero-voltage crossing detection. In some isolated half-bridge gate drivers [10], a protection against cross conduction over a wide temperature range was implemented. A specific isolated bidirectional data transmission line between high side and low side keeps the drivers informed about each power transistor switching state. In order to provide a fast, compact, and cost-effective autoadaptive deadtime solution, we propose to manage deadtime on the gate side. In [44] and [45], the active gate drivers for IGBT modules are able to reduce switching loss and to provide a fast overcurrent and overvoltage protection directly on the gate side by sensing the voltage across the parasitic inductance between the Kelvin emitter and the power emitter. In our study, we propose to detect the opposite transistor turn-off through the gate–drain parasitic capacitance of power transistors. In this way, the deadtime controller can be monolithically integrated in each isolated gate driver.

A. Selfswitching Technique

A selfswitching technique at turn-on has been used to generate a very short deadtime with a safe operation. The schematic of the synchronous buck converter implementing such deadtime management is illustrated in Fig. 6. Deadtimes are no longer generated through the MCU but directly on the gate side by both isolated gate drive circuits. The only useful information provided by the MCU is then the duty cycle α.

To secure synchronous switching, the proposed deadtime generation consists of a fast opposite transistor turn-off detection.

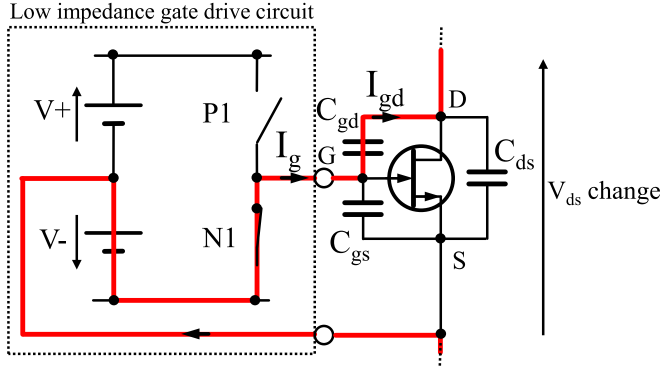


Fig. 7. Schematic of the gate drive circuit and the diode-less WBG transistor in OFF state when a parasitic gate–drain current I_{gd} flows because of a V_{ds} change.

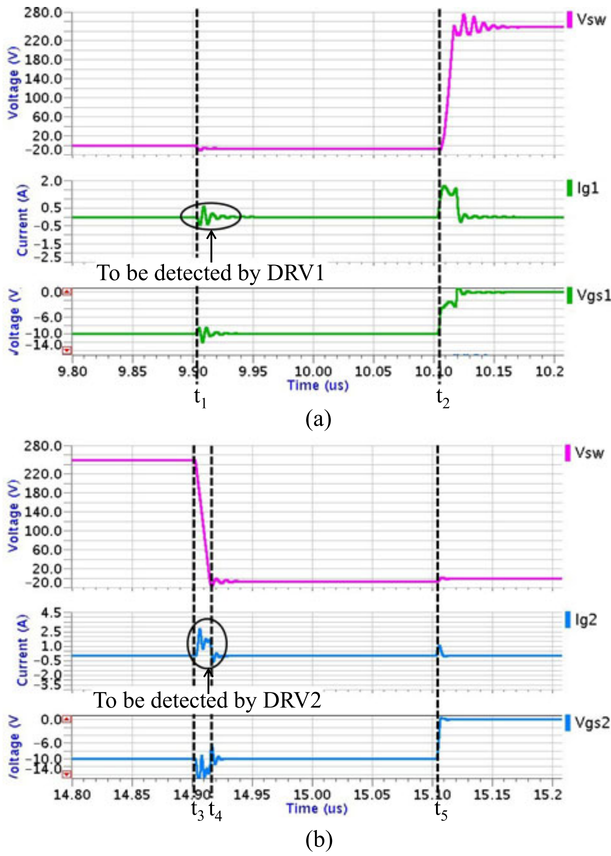


Fig. 8. Voltage and current waveforms of the simulated diode-less SiC JFET-based buck converter operating at 250 V/3 A and 100-kHz switching frequency at (a) Q2 turn-off and (b) Q1 turn-off.

Q1 and Q2 turn-off signals always follow a direct path while Q1 and Q2 turn-on are subject to validation by the opposite transistor turn-off detection. Specific detection circuits shown in Fig. 6 have been developed to be integrated in each gate driver. They are based on previous deadtime detectors presented in [14]–[16] but they do not require additional high-voltage devices or isolation circuits. Indeed they have been designed to detect very small positive and negative changes on the gate but not to detect a zero crossing on high-voltage node $V_{\rm SW}$ as in [14]–[16].

TABLE I
SIMULATION PARAMETERS AND RESULTS FOR PARASITIC GATE TO DRAIN CURRENT CHARACTERIZATION

Parameter	eGaN FETs-based converter	SiC JFETs-based converter
Power supply voltage $V_{\rm BUS}$	45 V	250 V
Switch-node drop during deadtime	−4 V	−5 V
Switched output current I_L	3 A	3 A
Gate–drain parasitic capacitance $C_{\rm gd}$	7 pF	70 pF
Gate–source parasitic capacitance $C_{\rm gs}$	205 pF	223 pF
$V_{\rm ds1}$ variation at Q2 turn-off	+4 V/ns	+5 V/ns
Negative peak current at Q2 turn-off	−0.02 A	−0.5 A
Electric charge associated to $I_{\rm gd1}$ flow	−0.03 nC	−0.4 nC
$V_{\rm ds2}$ variation at Q1 turn-off	−8 V/ns	−20 V/ns
Positive peak current at Q1 turn-off	+0.12 A	+2.5 A
Electric charge associated to $I_{\rm gd2}$ flow	+0.3 nC	+18 nC

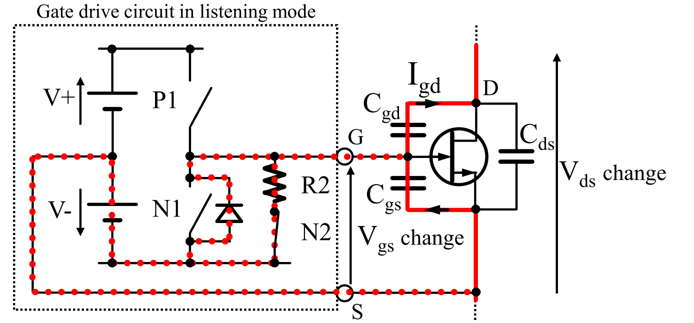


Fig. 9. Schematic of the gate drive circuit in the high-impedance listening mode and the diode-less WBG transistor in OFF state. A $V_{\rm ds}$ change implies a $V_{\rm gs}$ change.

B. Gate-Side Deadtime Management

As can be seen in Fig. 1, the power transistors Q1 and Q2 are surrounded by a number of external and internal parasitic components. For instance, they have an internal parasitic capacitance between each terminal which impacts on their switching performance. For example, the gate–drain capacitance $C_{\rm gd}$ is known to be involved in the parasitic turn-on mechanism during fast $dV_{\rm ds}/dt$ transition [46]–[48]. In our study, we are interested in the gate–source and gate–drain parasitic capacitances coupling during switching not to remove crosstalk as in [48] but to detect the opposite transistor turn-off.

During a switch-node $V_{\rm SW}$ transition, $V_{\rm ds}$ also changes and a current $I_{\rm gd}$ flows through the parasitic gate–drain capacitance $C_{\rm gd}$. If we consider a very low-impedance gate driver applying a constant V– voltage between gate and source as in Fig. 7, the parasitic current $I_{\rm gd}$ can be approximated by (4) for a constant capacitance $C_{\rm gd}$

$$I_{\rm gd} = -C_{\rm gd} \cdot \frac{dV_{\rm dg}}{\rm dt} \approx -C_{\rm gd} \cdot \frac{dV_{\rm ds}}{\rm dt}. \tag{4}$$

For a positive slew rate $dV_{\rm ds}/{\rm dt}$, the capacitance $C_{\rm gd}$ is charged by a negative parasitic current $I_{\rm gd}$ flowing from the

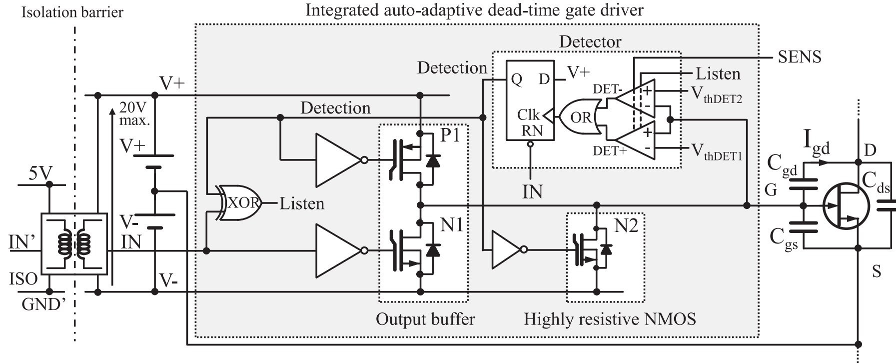


Fig. 10. Circuit schematic of the proposed gate driver.

drain to gate. In the same way for a negative $dV_{\rm ds}/{\rm dt}$ change, the parasitic capacitance $C_{\rm gd}$ is discharged by a positive current $I_{\rm gd}$ flowing from the gate to drain.

Fig. 8(a) and (b) show the voltage and current waveforms obtained by simulation of the diode-less SiC JFET-based buck converter similar to the one in Fig. 1 at Q2 turn-off and Q1 turn-off. A simplified SPICE model has been established matching the parasitic capacitances, conduction, and switching performance of the chosen JFET. The SPICE model provided by the manufacturer has been used for simulation with eGaN FETs. Q1 and Q2 are driven by a 1-Ω low output impedance gate driver similar to the one in Fig. 7. Parasitic inductances are assessed at 5 nH in each gate driver loop and 20 nH in the power loop. Again, we find the four time domains with additional information on currents I_{g1} and I_{g2} flowing through the gate of Q1 and Q2.

Parasitic currents I_g generated by the crosstalk between both sides at Q1 and Q2 turn-off are easily quantifiable by simulation. Simulation parameters and results for this parasitic current study are summarized in Table I. On one hand, simulation results indicate that peak parasitic currents are rather high because of fast Q1 and Q2 turn-off. On the other hand, the quantities of the associated electric charges are small, especially the ones at Q2 turn-off.

In the common buck converter case, DRV1 can be aware of Q2 turn-off by detecting the parasitic current I_{g1} at t_1. It could immediately turn on Q1 in order to virtually eliminate the deadtime dt_1. In the same way at Q1 turn-off, deadtime dt_2 can be eliminated if DRV2 detects the parasitic current flowing through the gate of Q2 at t_3.

C. Parasitic Gate to Drain Current Detection

The first parasitic current $I_{\rm gd}$ to detect is the negative current $I_{\rm gd1}$ flowing through the Q1 gate at time t_1 when Q2 is switched OFF [see Fig. 8(a)]. The second one is the positive current $I_{\rm gd2}$ flowing through the Q2 gate at time t_3 at Q1 turn-off [see Fig. 8(b)]. A specific detector dealing with positive and negative parasitic currents has been developed, and thus, the high-side and low-side gate drivers are the same and output current I_L can change direction without affecting the detection mechanism.

The proposed detection circuit depicted in Fig. 9 puts the gate drive in a high-impedance listening mode to detect opposite transistor turn-off. If the output impedance of the gate driver in this listening state is infinite, parasitic capacitances $C_{\rm gd}$ and $C_{\rm gs}$ constitute a capacitive voltage divider. A $V_{\rm ds}$ variation will charge or discharge the capacitance $C_{\rm gs}$ and change $V_{\rm gs}$ according to (5). In fact, the larger the $C_{\rm gd}/C_{\rm gs}$ ratio and the higher the $\Delta V_{\rm ds}$, then the greater the $\Delta V_{\rm gs}$ change. Characteristics summarized in Table I then suggest a more difficult eGaN FET turn-off detection than the SiC JFET one because of a gate–drain capacitance ten times lower for an almost equal $C_{\rm gs}$. To validate the proposed deadtime management, a first detection circuit has been sized to detect turn-off of the small EPC2007 eGaN FET. If the gate driver is capable of detecting devices with a 7:205 $C_{\rm gd}/C_{\rm gs}$ ratio, it should detect turn-off of WBG devices with a larger $C_{\rm gd}/C_{\rm gs}$ ratio as the chosen SiC JFET because of higher $\Delta V_{\rm gs}$. This first version will not be able to detect the body diode conduction of Si MOSFETs at Q2 turn-off because of too small forward voltage drop and associated $\Delta V_{\rm ds}$.

The gate of the power transistor and the gate driver are protected against overvoltage during fast $V_{\rm ds}$ variation by a high-impedance $R2$ shown on Fig. 9. The $V_{\rm gs}$ variation with this safety impedance is given by (6) during a $V_{\rm ds}$ variation. The maximal $\Delta V_{\rm gs,max}$ change and the minimal $\Delta V_{\rm gs,min}$ change are equal to $\Delta V_{\rm gs}(t_{\rm RV})$ and $\Delta V_{\rm gs}(t_{\rm FV})$, respectively, and approximated by (6) with $t_{\rm RV}$ and $t_{\rm FV}$ the drain–source voltage rise time and fall time. The $\Delta V_{\rm gs,min}$ change is also limited by the threshold voltage $V_{F,N1}$ of the internal diode of NMOS N1

$$\Delta V_{\rm gs} = \Delta V_{\rm ds} \cdot \frac{C_{\rm gd}}{C_{\rm gs} + C_{\rm gd}} \tag{5}$$

$$\Delta V_{\rm gs}(t) = V_{\rm gs}(t) - V_{-} = R2 \cdot C_{\rm gd} \frac{dV_{\rm ds}}{\rm dt} \cdot \left(1 - e^{-\frac{t}{R2(C_{\rm gd}+C_{\rm gs})}}\right), \text{with } \Delta V_{\rm gs} \geq -V_{F,N1}. \tag{6}$$

The impact of the proposed mode on $V_{\rm gs}$ has been studied in the GaN-HEMT-based converter with the same simulation circuit and parameters of Table I with DRV1 and DRV2 in listening mode as in Fig. 9 with a safety high-impedance $R2$ equal to 20 Ω. At Q2 turn-off, the drain–source voltage $V_{\rm ds1}$ rises by 4 V with an additional 4 V transient overvoltage due to the parasitic inductance in the power loop. The negative current $I_{\rm gd1}$ flowing through $R2$ leads to a positive $\Delta V_{\rm gs1}$ change of +230 mV in simulation and +210 mV by calculation of (6). However, at Q1 turn-off, $V_{\rm ds2}$ falls by 49 V, and the positive

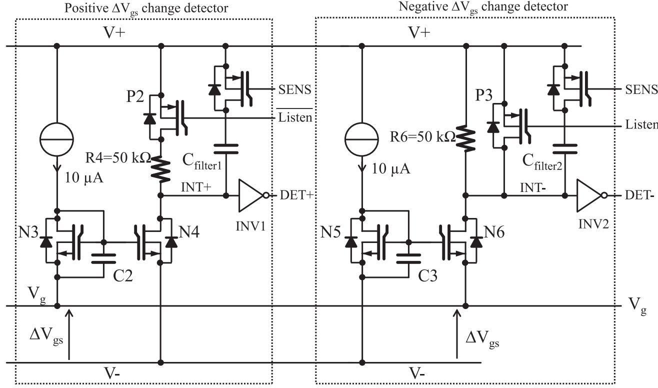


Fig. 11. Detailed circuit schematic of the integrated opposite transistor turn-off detector.

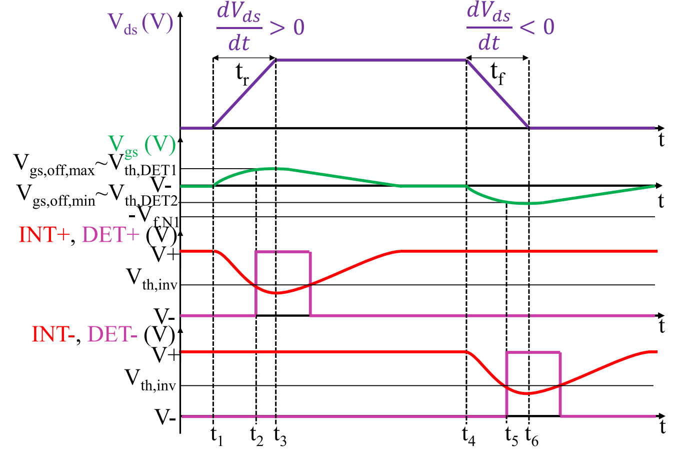


Fig. 12. Typical waveforms of the proposed gate driver in listening mode for a positive and a negative $V_{\rm ds}$ variation.

parasitic current $I_{\rm gd2}$ flows through the body diode of the NMOS N1 generating a negative $\Delta V_{\rm gs2}$ change of -700 mV. Without this diode, $\Delta V_{\rm gs2}$ change could reach -850 mV in the GaN version and -25 V in the SiC version of the converter according to (6) with parameters of Table I.

The detector is reduced to a window detector and in the specific listening mode, it detects if $V_{\rm gs}$ exceeds a positive threshold voltage $V_{\rm th,DET1}$, or a negative threshold voltage $V_{\rm th,DET2}$. According to simulation results, $V_{\rm th,DET1}$ must be below $+230$ mV and $V_{\rm th,DET2}$ above -700 mV to detect eGaN FET turn-off through $\Delta V_{\rm gs}$ change. In the primary detection circuit, these threshold voltages are fixed but they are ideally adjusted as a function of the $C_{\rm gd}/C_{\rm gs}$ ratio, the safety resistance *R*2 and the operating point to ensure proper sensitivity as discussed hereinafter.

V. Gate Drive Circuit

A. Internal Structure

The circuit schematic of the proposed integrated autoadaptive deadtime gate driver is shown in Fig. 10. The driver is made of four main blocks: a buffer, detector, safety 20-Ω on-resistance NMOS N2, and digital control unit. The buffer consists of a common CMOS output buffer but the PMOS P1 is driven by the output signal of the detector.

The detailed analog circuit schematic of the integrated opposite transistor turn-off detector is given by Fig. 11. We can distinguish two symmetrical sub circuits for positive and negative $\Delta V_{\rm gs}$ change detection. Both voltage detectors are based on a specific current mirror N3/N4 or N5/N6, a 10-μA reference current and 50-kΩ pull-up resistance. Waveforms of the gate driver in listening mode are depicted in Fig. 12. In listening steady state, the gate potential V_g is equal to the negative potential V– and the reference current flows through pull-up resistances. Signals INT$-$ and INT+ are equal to V+ -0.5 V and so DET$-$ and DET+ are in low state. When an opposite transistor turns off, at time t_1 or t_4, $V_{\rm ds}$ rises or falls, the resulting parasitic current $I_{\rm gd}$ flow generates a positive or negative $\Delta V_{\rm gs}$ change approximated by (6) and the gate potential V_g is no longer equal to V$-$. The gate–source voltage of N3 and N5 is kept constant by capacitances C2 and C3 but this is no longer the case for N4 and N6. In fact, depending on the sign of the $\Delta V_{\rm gs}$ change the gate–source voltage of N4 or N6 increases. The current mirror is therefore destabilized and signal INT+ or INT$-$ drops to V$-$ according to the transfer functions H_+ and H_- given by (7) and (8) with g_m, $g_{\rm ds}$, and $C_{\rm ds}$ the transconductance, the drain–source conductance, and capacitance of transistors N4, N6, or P3. When signal INT+ or INT– reaches the CMOS inverter switching threshold $V_{\rm th,inv}$ at time t$_2$ or t$_5$, signal DET+ or DET$-$ are set in high state. If we assimilate both detectors to operational amplifiers, then the threshold voltages $V_{\rm th,DET1}$ and $V_{\rm th,DET2}$ approximated by (9) are defined as a positive and a negative systematic input offset voltages. If necessary, these voltages can be slightly adjusted through an independent power supply of the digital part, so an independent switching threshold $V_{\rm th,inv}$ thanks to level-shifters, not depicted in Fig. 10, between analog and digital functions

$$H_+(j\omega) = \frac{\mathrm{INT}_+(j\omega)}{\Delta V_{\rm gs}(j\omega)} = \frac{-\frac{R4 g_{m4}}{1+R4 g_{\rm ds4}}}{1 + j\frac{R4(C_{\rm ds4}+C_{\rm filter1})\omega}{R4 g_{\rm ds4}+1}} = \frac{H(0)}{1 + j\frac{\omega}{\omega_c}} \tag{7}$$

$$H_-(j\omega) = \frac{\mathrm{INT}_-(j\omega)}{\Delta V_{\rm gs}(j\omega)} = \frac{\frac{R6 g_{m6}}{1+R6 g_{\rm ds6}}}{1 + j\frac{R6(C_{\rm ds3}+C_{\rm ds6}+C_{\rm filter2})\omega}{R6 g_{\rm ds6}+1}} = \frac{H(0)}{1 + j\frac{\omega}{\omega_c}} \tag{8}$$

$$V_{\rm th,DET} = \frac{V_{\rm th,inv} - V_+ + V_-}{H(0)}. \tag{9}$$

B. Autoadaptive Deadtime Gate Driver Operation

Fig. 13 shows waveforms of the synchronous buck converter operating with the autoadaptive deadtime gate drivers as in Fig. 14. Signal detection is switched to high when signal IN is high and the gate voltage exceeds $V_{\rm th,DET1}$ or $V_{\rm th,DET2}$ threshold voltage. When signal IN is high but signal detection is low, the signal listen is high:

1) at time t$_1$, the gate drive circuit DRV1 is put into listening mode and is waiting for Q2 turn-off;

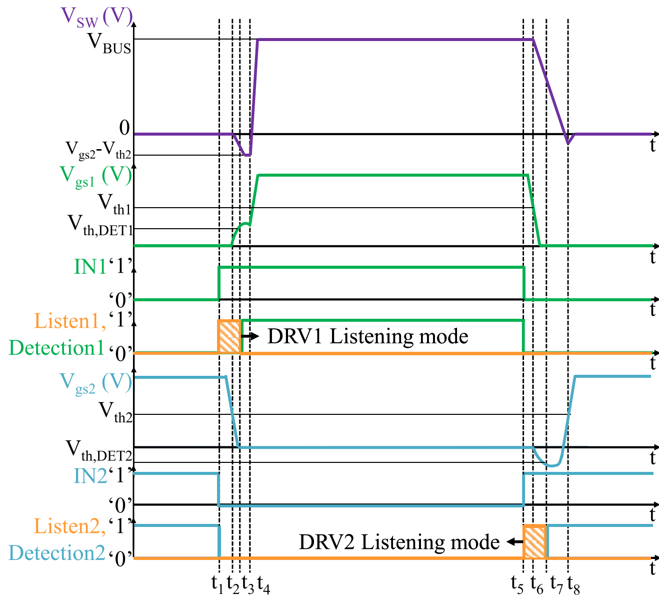


Fig. 13. Waveforms of the diode-less WBG devices-based buck converter operating with the gate driver detecting opposite transistor turn-off on the gate side.

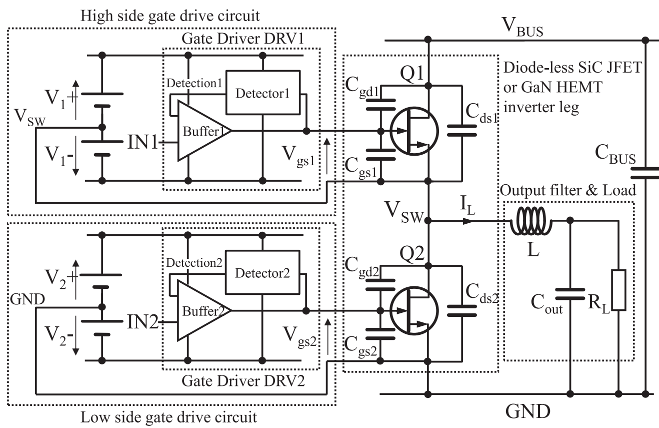


Fig. 14. Circuit schematic of the synchronous buck converter based on diode-less WBG devices driven by the auto-adaptive deadtime gate driver.

2) at time t_2, Q2 is turned OFF, the power node V_{SW} falls and V_{gs1} rises;
3) at time t_3, V_{gs1} is above $V_{\mathrm{th,DET1}}$ and the detection circuit detects Q2 turn-off, the gate drive circuit DRV1 comes back to the normal low impedance mode and turns on Q1 at time t_4;
4) at time t_5, the gate drive circuit DRV2 is in listening mode to detect Q1 turn-off;
5) at time t_6, Q1 is turned OFF, the node V_{SW} and V_{gs2} fall;
6) at time t_7, V_{gs2} being under $V_{\mathrm{th,DET2}}$ the detection circuit detects Q1 turn-off. Q2 is turned ON at time t_8.

Such deadtime management releases timing constraints on input signal generation and propagation. The useful information is now carried by the falling edge of IN1 and IN2 while synchronous switching of Q1 and Q2 are secured by a fast opposite transistor turn-off detection.

C. Preventing Incorrect Detections

We distinguish two types of incorrect detection depending on the sensitivity of detectors. The first can be observed if detectors are too sensitive. In that case, the gate voltage variation is detected too early, at the beginning of the opposite transistor turn-off. Extreme cases, at light load and at heavy load are the most susceptible ones. At light load, when Q1 turns OFF, the time $t_{\mathrm{off},m}$ given by (3) taken by the drain–source voltage of Q1 to reach V_{BUS} is particularly long. The variation dV_{ds1}/dt being lower, the parasitic current I_{gd} given by (4) is also lower and the gate voltage variation is slower. Detections of Q1 turn-off can be so delayed to avoid hard switching with a sufficiently low threshold voltage $V_{\mathrm{th,DET2}}$ or a lower resistance R2. Conversely, at heavy load, the voltage V_{ds1} quickly reached V_{BUS} but drain current can be still flowing through the power device. To prevent shoot-through, the gate driver has a turn-on propagation delay after detection longer than the turn-off one. This extra turn-on delay is initially fixed to 2 ns but a longer delay should be set in accordance with (10) with $t_{d,\mathrm{on}}$ and $t_{d,\mathrm{off}}$, the turn-on and turn-off propagation delays, $t_{\mathrm{FV,Q}}$ and $t_{\mathrm{FI,Q}}$, the drain–source voltage and the drain current fall times of power transistors, $t_{\mathrm{detect,DRV}}$, the opposite transistor turn-off detection delay corresponding to t_3–t_2 and t_7–t_6 times in Fig. 13.

Moreover, a parasitic change of V_{gs} included in the detector bandwidth and higher than $V_{\mathrm{th,DET1}}$ or lower than $V_{\mathrm{th,DET2}}$ happening in the listening mode, t_3–t_1 or t_7–t_5 in Fig. 13, will be detected as an opposite transistor turn-off. To reduce high-frequency sensitivity, a low-pass filter can be added with the SENS signal in Fig. 11. The cutoff frequencies $f_{c,\mathrm{DET}+}$ and $f_{c,\mathrm{DET}-}$ of detectors are given by (11) and (12). With a 4-pF capacitance C_{filter}, the bandwidth of the negative ΔV_{gs} change detector is reduced from 87 to 3.8 MHz and the one of the positive change detector is lowered from 56 to 1.2 MHz. Detector response times to a negative and a positive unit step on ΔV_{gs} are, respectively, 2.5 and 5 ns longer to switch signals DET− and DET+ with these extra capacitances. Therefore, values of C_{filter1} and C_{filter2} must be set in agreement with characteristics of the power transistors and the final application in order to ensure high noise immunity but also short detection delay for minimum reverse conduction loss.

The second incorrect detection occurs when detectors are not sufficiently sensitive. For instance, when the output current is too small, the parasitic current I_{gd} cannot be detected even if the threshold voltages $V_{\mathrm{th,DET1}}$ and $V_{\mathrm{th,DET2}}$ have been correctly adjusted. In order to maintain conversion operations, the listening mode has a finite secure duration. In other words, a long default deadtime is fixed by drivers when opposite transistor turn-off is not detected.

Finally, if fixed values of threshold voltages $V_{\mathrm{th,det1}}$ and $V_{\mathrm{th,det2}}$, safety impedance *R*2 and filter capacitance C_{filter1} and C_{filter1} do not allow to reach proper detections and/or enough performance over wide operating point variations, we propose to assist gate drivers with an MCU or FPGA as in [11], [13], [22]. To keep a fast and cost-effective solution, we think about the same monolithically integrated turn-off detection mechanism but with the sensitivity of detectors managed through the

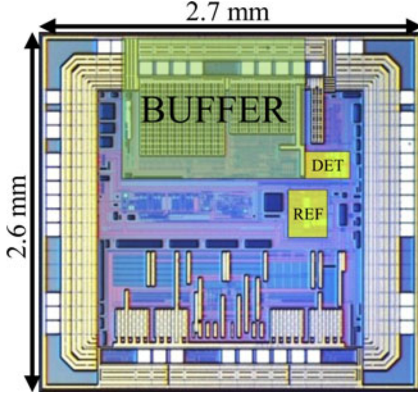


Fig. 15. Specific gate driver die micrograph. The green part is the output buffer and the yellow one the monolithically integrated deadtime controller.

TABLE II
GATE DRIVER ELECTRICAL CHARACTERISTICS FOR A 10-V SUPPLY VOLTAGE

Parameter	Symbol	Test conditions	Value
		OUTPUT	
On resistance V+ to gate	R_{OVH}	$I_g = -500$ mA	1.1 Ω
On resistance V− to gate	R_{OVL}	$I_g = +500$ mA	0.9 Ω
Peak/Continuous output current	I_{PK}	Sourcing, $C_L = 10000$ pF	−9 A/−3.5 A
		Sinking, $C_L = 10000$ pF	11 A/3 A
		SWITCHING CHARACTERISTICS	
Rise time	t_R	$C_L = 1000$ pF	5.4 ns
Fall time	t_F	$C_L = 1000$ pF	5.4 ns
		DEADTIME CONTROLLER CHARACTERISTICS	
Current consumption	I_{ctrl}	$f_{\mathrm{sw}} = 100$ kHz	140 μA
DET1 Threshold Voltage	V_{thDET1}	Listening mode	200 mV
DET2 Threshold Voltage	V_{thDET2}	Listening mode	−250 mV

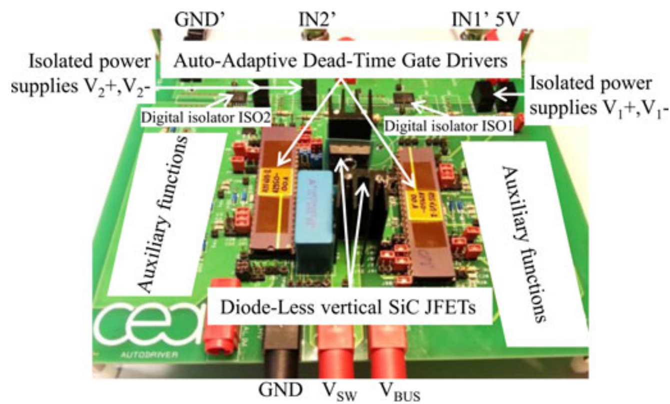


Fig. 16. Picture of the diode-less SiC JFET-based buck converter. The same circuit board is used for the eGaN FETs-based buck converter, thanks to a hybrid footprint.

MCU. We propose to keep fixed values of $V_{\mathrm{th,det}}$ and C_{filter} set in accordance with noise immunity requirements but to online adjust the crosstalk effect on V_{gs} by controlling the value of $R2$ (6) for each gate driver. For a given operating point, MCU will increase $R2$, and thus, sensitivity at each period. When a gate

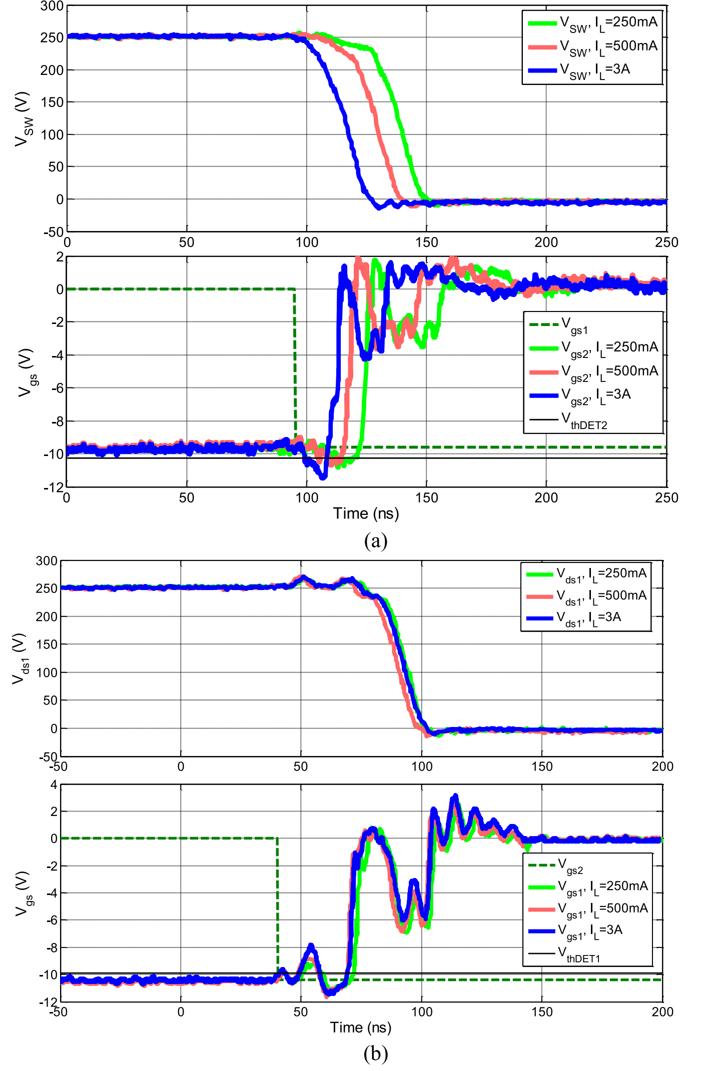


Fig. 17. (a) Q1 and (b) Q2 turn-off waveforms comparison for different output loads of the SiC JFET-based buck converter driven by the autoadaptive deadtime gate driver.

driver correctly detects the opposite switch turn-off before the timeout, it sends back a signal to MCU to hold its optimum $R2$ value. In the same way, when the operating point changes, the average duty cycle is also changing [11] and MCU will search for the new optimum $R2$ value for each gate driver defined as the lower value of $R2$ allowing turn-off detection before the timeout

$$t_{d,\mathrm{on,DRV}} - t_{d,\mathrm{off,DRV}} > t_{F,\mathrm{DRV}} + t_{d,\mathrm{off},Q} + t_{F,Q} - (t_{R,\mathrm{DRV}} + t_{d,\mathrm{on},Q} + t_{\mathrm{detect,DRV}}),\ \text{with}\ t_{F,Q} = \max(t_{\mathrm{FV,Q}}, t_{\mathrm{FLQ}}) \tag{10}$$

$$f_{c,\mathrm{DET+}} = \frac{R4 g_{\mathrm{ds4}} + 1}{2\pi R4\,(C_{\mathrm{ds4}} + C_{\mathrm{filter1}})} \tag{11}$$

$$f_{c,\mathrm{DET-}} = \frac{R6 g_{\mathrm{ds6}} + 1}{2\pi R6\,(C_{\mathrm{ds3}} + C_{\mathrm{ds6}} + C_{\mathrm{filter2}})}. \tag{12}$$

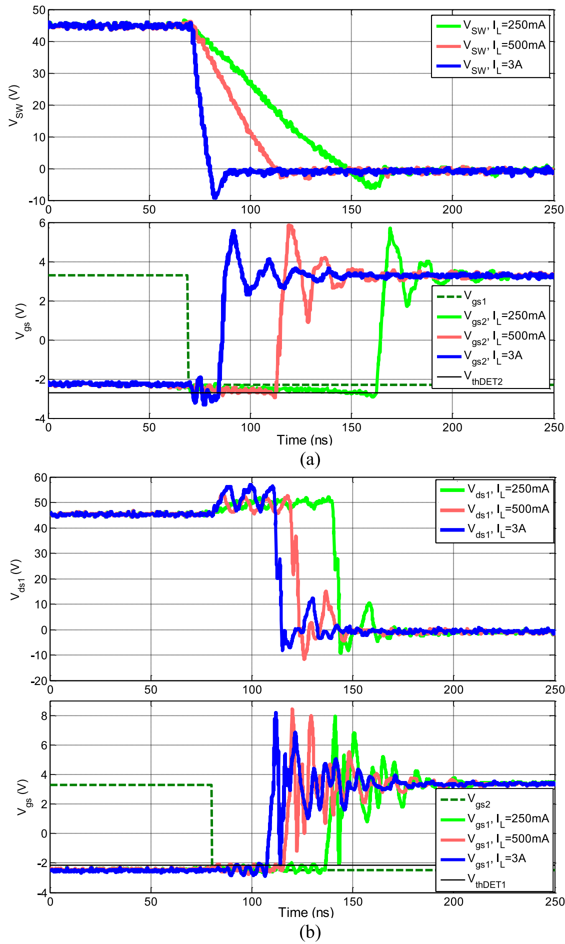
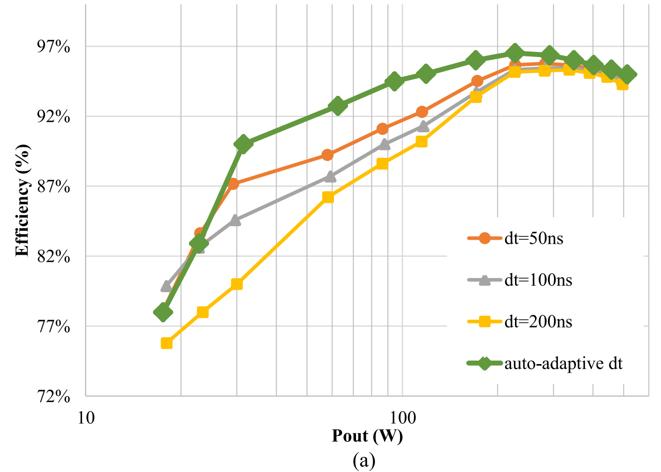


Fig. 18. (a) Q1 and (b) Q2 turn-off waveforms comparison for different output loads of the eGaN FETs-based buck converter driven by the autoadaptive deadtime gate driver.



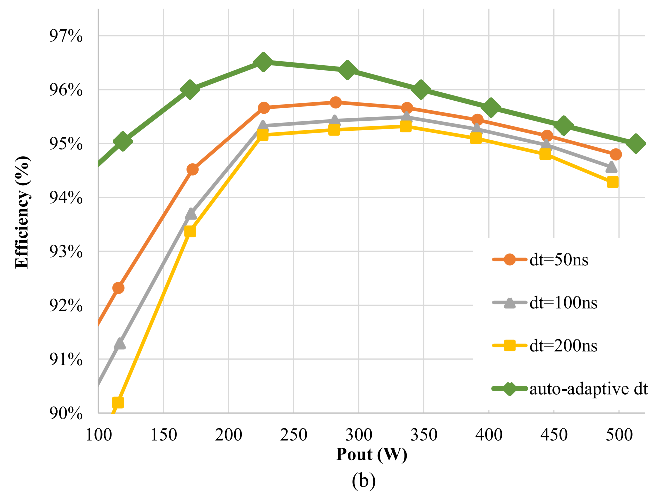


Fig. 19. Efficiency comparison for fixed and autoadaptive deadtime generation in 250-V input, 55-V output, and 100-kHz switching frequency diode-less SiC JFET-based buck converter on a (a) logarithmic scale (b) linear scale.

VI. Experimental Results

A. Specific Gate Driver

The gate driver with the proposed autoadaptive deadtime management has been implemented in an AMS 0.35-μm HV CMOS process which offers NMOSs and PMOSs capable of withstanding 20 V between drain and source, and between gate and source. Fig. 15 shows the gate driver die micrograph with the buffer part in green and its monolithically integrated deadtime controller in yellow. The full chip with other features uses almost 7 mm^2 of silicon area. The gate driver active area is 1.54 mm^2. The output buffer consumes 86% of this active area. The high-speed detector DET, digital control unit, and current reference REF occupy only 0.22 mm^2 of silicon area. The measured electrical characteristics of the gate driver are summarized in Table II. It demonstrates very low output impedances with a 0.9-Ω/1.1-Ω pull-down/pull-up resistance and large output current to strongly and quickly drive transistors.

The integrated detection circuit in listening mode determines whether the gate to V$-$ voltage is higher than $V_{\rm thDET1}$ or lower than $V_{\rm thDET2}$, equal to 200 and -250 mV, respectively. An option has been implemented to turn ON the transistor after a long 250-ns secure time if the $V_{\rm gs}$ change, due to the opposite transistor turn-off, is not detected. The deadtime controller consumes almost 140 μA at 100-kHz switching frequency $f_{\rm SW}$. The quiescent current of the whole gate driver is 800 μA at room temperature which is close to the current consumption of modern 10-V gate driver [43].

B. Improved Synchronous Buck Converter Operations

The proposed gate drive technique has been implemented in two synchronous buck converters based on diode-less 1200-V normally-on SiC trench JFETs or 100-V normally-off eGaN FETs with the same circuit board shown in Fig. 16. Gate driver supply voltages are adjusted in consequence. The autoadaptive deadtime feature has been characterized over a large output load range. Figs. 17 and 18 present Q1 and Q2 turn-off waveforms of the SiC JFET version of the converter and the eGaN FETs one for 0.25 to 3-A output current. In the 250 to 55-V SiC JFET buck converter, Q1 turn-off is detected by DRV2 after 30 ns for the lightest load and in less than 10 ns at 3-A output current. Q2 turn-off is detected by DRV1 in almost 30 ns for any load. Whereas in the 45 to 10 V eGaN FET buck converter, Q1 turn-off is detected by DRV2 after 95 ns for the lightest load and in 10 ns

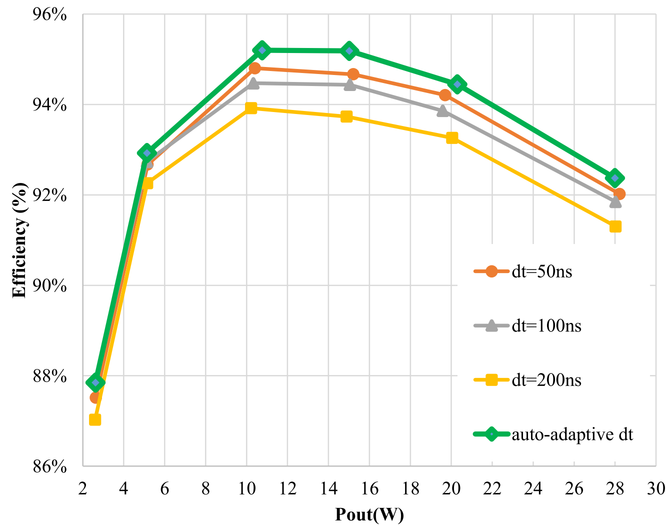


Fig. 20. Efficiency comparison for fixed and autoadaptive deadtime generation in 45-V input, 10-V output, and 100-kHz switching frequency diode-less eGaN FETs-based buck converter.

at 3-A output current. The Q2 turn-off detection delay is from 25 to 55 ns according to the load. After detection, an additional 5 ns delay is necessary to turn on Q1 or Q2. Therefore, as the final deadtime is equal to the detection time plus the turn-on delay, the deadtime controller can safely set deadtimes as short as 15 ns over a large output load range.

Efficiency of the diode-less buck converters based on SiC JFET and GaN FET with the autoadaptive deadtime gate driver has been measured and compared in Figs. 19 and 20 to the same converters operating with the same gate drivers but with the deadtime controller disabled and fixed deadtimes. With the dynamic deadtime scheme, the conversion efficiency is no longer impacted by the reverse conduction losses. In both cases, the converter reaches a better peak efficiency and keeps a high efficiency over a wider output power range than any fixed deadtime. From 10% of the rated load, the SiC JFET-based converter efficiency is over 92% with the adaptive deadtime compared to only 88.7% and 87% with a 50 and 100 ns fixed deadtime, respectively. As shown in Fig. 18(a), the efficiency at light load is lower with autoadaptive deadtime because the threshold voltage $V_{\mathrm{th,DET2}}$ is too high for the chosen SiC JFET. Q1 turn-off is detected too soon and hard switching at Q2 turn-on generates extra losses. On the other hand, the threshold voltage $V_{\mathrm{th,DET2}}$ is properly adapted to the chosen eGaN FETs. The proposed deadtime management ensures at any load level soft-switching at Q2 turn-on and so the best efficiency. Thus, the GaN-based converter reaches 95% peak efficiency and efficiency is over 93% from 5-W output power with the adaptive deadtime.

VII. Conclusion

In half-bridge power converters without additional high-performance diodes in antiparallel, more losses are generated during deadtime because of higher drain-to-source voltage drop. Very short deadtimes are definitely desired but they cannot be safely set in conventional high-voltage isolated converters because of propagation delays mismatching between high side and low side. In this paper, a gate driver with a monolithically integrated deadtime controller is introduced to improve efficiency and reliability of synchronous converters without externally connected diodes. The proposed deadtime management precisely and quickly adjusts the nonoverlap time directly on the gate side. A detection circuit has been implemented to detect the opposite transistor turn-off through the crosstalk between high side and low side by taking advantage of the power transistor gate–drain parasitic capacitance. Once the gate driver is aware of the opposite switch turn-off, it turns on its corresponding transistor thus dealing with very short but safe deadtimes. With such a detection mechanism, additional high-voltage devices are no longer required contrary to previous advanced gate drivers with integrated deadtime management [17], [19], [20], [23]. Therefore, the proposed gate driver has been implemented in a standard 0.35-μm 20-V CMOS process. The monolithically integrated controller consumes only 140 μA for a 10-V supply voltage and 0.22 mm^2 of silicon area. The autoadaptive deadtime management has been validated in two synchronous buck converters without external free-wheeling diodes. In a 500-W 250-V to 55-V diode-less SiC JFET-based converter, the proposed driver deals with deadtimes from only 15 to 35 ns. The converter driven by the autoadaptive deadtime gate driver reaches higher efficiency from 10% of rated load compared to 50 and 100 ns fixed deadtimes. In a 30-W 45-V to 10-V converter based on eGaN FETs, the autoadaptive deadtime management proposes higher efficiency than fixed deadtimes at any load level thanks to lower reverse conduction losses and low-side eGaN FET soft switching.

References

[1] L. Hoffmann, C. Gautier, S. Lefebvre, and F. Costa, “Optimization of the driver of GaN power transistors through measurement of their thermal behavior,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2359–2366, May 2014.

[2] H. Zhang and R. S. Balog, “Loss analysis during dead time and thermal study of gallium nitride devices,” in *Proc. IEEE Appl. Power Electron. Conf.*, 2015, pp. 737–744.

[3] T. Funaki, M. Matsushita, M. Sasagawa, T. Kimoto, and T. Hikihara, “A Study on SiC devices in synchronous rectification of DC-DC Converter,” in *Proc. IEEE Appl. Power Electron. Conf.*, 2007, pp. 339–344.

[4] S.-J. Chee, J. Kim, and S.-K. Sul, “Dead-time compensation based on pole voltage measurement,” in *Proc. IEEE Energy Conv. Congr. Expo.*, 2015, pp. 1549–1555.

[5] B. Zhao, Q. Song, W. Liu, and Y. Sun, “Dead-Time effect of the high-frequency isolated bidirectional full-bridge DC/DC converter: Comprehensive theoretical analysis and experimental verification,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1667–1680, Apr. 2014.

[6] F. Chierchie, L. Stefanazzi, E. E. Paolini, and A. R. Oliva, “Frequency analysis of PWM inverters with dead-time for arbitrary modulating signals,” *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2850–2860, Jun. 2014.

[7] S. Ji, D. Reusch, and F. C. Lee, “High frequency high power density 3-D integrated gallium nitride-based point of load module design,” *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4216–4226, Sep. 2013.

[8] M. K. Song, L. Chen, J. Sankman, S. Terry, and D. Ma, “16.7 A 20V 8.4 W 20MHz four-phase GaN DC-DC converter with fully on-chip dual-SR bootstrapped GaN FET driver achieving 4ns constant propagation delay and 1ns switching rise time,” in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2015, pp. 1–3.

[9] LM5113: 5A, 100V Half-Bridge Gate Driver for Enhancement Mode GaN FETs, TI datasheet. (2016). [Online]. Available: www.ti.com.

[10] XTR26010: High Temperature Intelligent Gate Driver, X-REL Semiconductor datasheet. (2014). [Online]. Available: www.x-relsemi.com.

[11] V. Yousefzadeh and D. Maksimovic, “Sensorless optimization of dead times in DC-DC converters with synchronous rectifiers,” *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 994–1002, Jul. 2006.

[12] D. Han and B. Sarlioglu, “Dead-Time effect on GaN-based synchronous boost converter and analytical model for optimal dead-time selection,” *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 601–612, Jan. 2016.

[13] Z. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, B. J. Blalock, and H. Lu, “Dead-time optimization of SiC devices for voltage source converter,” in *Proc. IEEE Appl. Power Electron. Conf.*, 2015, pp. 1145–1152.

[14] T. Y. Man, P. K. T. Mok, and M. Chan, “An auto-selectable-frequency pulse-width modulator for buck converters with improved light-load efficiency,” in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2008, pp. 440–626.

[15] S. Zhen, B. Zhang, P. Luo, K. Yang, X. Zhu, and J. Li, “A high efficiency synchronous buck converter with adaptive dead time control for dynamic voltage scaling applications,” in *Proc. IEEE Int. Conf. VLSI Syst.-on-Chip*, 2011, pp. 43–48.

[16] W. Yan, C. Pi, W. Li, and R. Liu, “Dynamic dead-time controller for synchronous buck DC-DC converters,” *IEEE Electron. Lett.*, vol. 46, no. 2, pp. 164–165, Jan. 2010.

[17] A. Zhao, A. Shorten, H. Nishio, and W. T. Ng, “An intergrated DC-DC converter with digital one-step dead-time correction,” in *Proc. IEEE Int. Symp. Power Semicond. Devices IC’s*, 2010, pp. 57–60.

[18] S. Mappus (Apr. 2003). Predictive gate drive boosts synchronous DC/DC power converter efficiency, TI application note [Online]. Available: www.ti.com.

[19] L. Chen and F. Z. Peng, “Dead-Time elimination for voltage source inverters,” *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 574–580, Mar. 2008.

[20] J. Xue, K. D. T. Ngo, and H. Lee, “A 99%-efficiency 1-Mhz 1.6-kW zero-voltage-switching boost converter using normally-off GaN power transistors and adaptive dead-time controlled gate drivers,” in *Proc. IEEE Int. Conf. Electron. Devices Solid-State Circuits*, 2013, pp. 1–2.

[21] Y.-K. Lin and Y.-S. Lai, “Dead-time elimination method and current polarity detection circuit for three-phase PWM-controlled inverter,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 83–90.

[22] J. S. Yu, G. Jin, S. L. Cheng, and W. T. Ng, “Digital dead-time control for an integrated tri-mode buck-boost DC-DC converter,” in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, 2015, pp. 1768–1771.

[23] L. Cong, J. Xue, and H. Lee, “A 100V reconfigurable synchronous gate driver with comparator-based dynamic dead-time control for high-voltage high-frequency DC-DC converters,” in *Proc. IEEE Appl. Power Electron. Conf.*, 2015, pp. 2007–2010.

[24] Y. Long, W. Zhang, B. Blalock, L. Tolbert, and F. Wang, “A 10-MHz resonant gate driver design for LLC resonant DC-DC converters using GaN devices,” in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 2093–2097.

[25] W. Zhou, X. Zhong, and K. Sheng, “High temperature stability and the performance degradation of SiC MOSFETs,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2329–2337, May 2014.

[26] M. Alexandru, V. Banu, X. Jorda, J. Montserrat, M. Vellvehi, D. Tournier, J. Millan, and P. Godignon, “SiC integrated circuit control electronics for high-temperature operation,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3182–3191, May 2015.

[27] G. Calderon-Lopez, A. J. Forsyth, D. L. Gordon, and J. R. McIntosh, “Evaluation of SiC BJTs for High-Power DC/DC Converters,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2474–2481, May 2014.

[28] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. R. McNutt, A. B. Lostetter, J. S. Lee, and K. Shiozaki, “A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[29] M. Rodriguez, Y. Zhang, and D. Maksimovic, “High-frequency PWM buck converters using GaN-on-SiC HEMTs,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2462–2473, May 2014.

[30] J. Delaine, P. Olivier, D. Frey, and K. Guepratte, “High frequency DC-DC converter using GaN device,” in *Proc. IEEE Appl. Power Electron. Conf.*, 2012, pp. 1754–1761.

[31] B. Hughes, Y. Y. Yoon, D. M. Zehnder, and K. S. Boutros, “A 95% efficient normally-off GaN-on-Si HEMT hybrid-IC boost converter with 425-W output power at 1 MHz,” in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2011, pp. 1–3.

[32] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, “A survey of wide bandgap power semiconductor devices,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[33] R. Mitova, R. Ghosh, U. Mhaskar, D. Klikic, M.-X. Wang, and A. Dentella, “Investigations of 600-V GaN HEMT and GaN diode for power converter applications,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2441–2452, May 2014.

[34] S. Jahdi, O. Alatise, R. Bonyadi, P. Alexakis, C. A. Fisher, J. A. O. Gonzalez, L. Ran, and P. Mawby, “An Analysis of the switching performance and robustness of power MOSFETs body diodes: A technology evaluation,” *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2383–2394, May 2015.

[35] D. C. Sheridan, K. Chatty, V. Bondarenko, and J. B. Casady, “Reverse conduction properties of vertical SiC trench JFETs,” in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 2012, pp. 385–388.

[36] R. Ouaida, X. Fonteneau, F. Dubois, D. Bergogne, F. Morel, H. Morel, and S. Oge, “SiC Vertical JFET pure diode-less inverter leg,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 512–517.

[37] C. Cai, W. Zhou, and K. Sheng, “Characteristics and application of normally-off SIC-JFETS in converters without antiparallel diodes,” *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4850–4860, Oct. 2013.

[38] Z. Wang, J. Ouyang, J. Zhang, X. Wu, and K. Sheng, “Analysis on reverse recovery characteristic of SiC MOSFET intrinsic diode,” in *Proc. IEEE Energy Conv. Congr. Expo.*, 2014, pp. 2832–2837.

[39] C2M0040120D: 1200V/60A Silicon Carbide Power MOSFET, Cree datasheet. (2015). [Online]. Available: www.cree.com.

[40] IPW90R120C3: 900V/40A Silicon CoolMOS Power Transistor, Infineon datasheet. (2008). [Online]. Available: www.infineon.com.

[41] HCPL-2200: Very High CMR, Wide Vcc Logic Gate Optocouplers, Agilent datasheet. (2007). [Online]. Available: www.agilent.com.

[42] ADUM2400: Quad-Channel Digital Isolator, Analog Devices datasheet. (2015). [Online]. Available: www.analog.com.

[43] LM5114: Single 7.6A Peak Current Low-Side Gate Driver, TI datasheet. (2015). [Online]. Available: www.ti.com.

[44] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, “A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules,” *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3720–3732, Jul. 2014.

[45] K. Fink and S. Bernet, “Advanced gate drive unit with closed-loop control,” *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2587–2595, May 2013.

[46] Q. Zhao and G. Stojcic, “Characterization of Cdv/dt induced power loss in synchronous buck DC/DC converters,” *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1508–1513, Jul. 2007.

[47] E. Velander, A. Lofgren, K. Kretschmar, and H.-P. Nee, “Novel solutions for suppressing parasitic turn-on behaviour on lateral vertical JFETs,” in *Proc. IEEE Energy Conv. Congr. Expo.*, 2014, pp. 1–8.

[48] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, “Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.

Romain Grezaud was born in Thonon, France, in 1987. He received the M.S. degree from the National Institute of Applied Sciences of Lyon INSA, Lyon, France, in 2011. In 2014, he received the Ph.D. degree in electrical engineering from the Grenoble Institute of Technology INPG, Grenoble, France.

He is currently a Research Scientist at the CEA-LETI in the Micro and Nanotechnology Innovation Centre MINATEC, France. His research interests include energy harvesting, power conversion, gate driver, and monolithic integration.

Francois Ayel received the Electronic Engineering Diploma degree from ICPI, Lyon, France, in 1996.

From 1996 to 2005, he was involved in various design activities for microelectronic sensors such as fingerprint and image sensors. From 2005 to 2010, he was technically responsible for ASIC design dedicated to power management for mobile phones in STMicroelectronics. He joined CEA-LETI in 2010 in the Center for Innovation & Nanotechnology (MINATEC). He is in charge of IC design dedicated for high-power and high-temperature applications.

Nicolas Rouger was born in Marseille, France, in 1981. He received the B.Eng. degree from Universite Paris Sud, Orsay, France, and Ecole Normale Superieure de Cachan, Cachan, France. He received the M.Eng. and the Ph.D. degrees in electrical engineering from the Institut National Polytechnique de Grenoble, Grenoble, France.

He was a Postdoctoral Researcher with the MiNa Group, University of British Columbia (UBC, 2008–2009), where he contributed to the modeling, design, and characterization of SOI nanophotonics devices. He is currently a Research Scientist at the French National Center for Scientific Research (CNRS), Paris, France, and the Grenoble Electrical Engineering Lab (G2Elab), Grenoble, France. His main research interests include integration for power transistors and power ICs, WBG power devices, and optical control of novel smart power semiconductor devices.

Jean-Christophe Crebier (M'13) received the bachelor's and master's degrees in electrical engineering in 1995. In 1999, he received the Ph.D. degree in power electronics, EMC for PFC converters from INPG, France.

Since 2001, he is with G2ELab-CNRS (National Center for Scientific Research), France, as a Full Time Researcher. He is a CNRS Senior Scientist in the fields of integrated power electronics. His research interests include system and functional, hybrid and monolithic semiconductor integration for power active devices and converters. Applications of his work are related to the management of multicell distributed systems such as PV or batteries. He is currently a Scientific Advisor at University Grenoble Alpes, Grenoble, France, for electronic and electrical engineering departments and he is the Head of CMP, a support facility for IC and MEMS prototyping.