A 10-MHz Isolated Synchronous Class-Φ_2 Resonant Converter

Xiaoyong Ren, *Member, IEEE*, Yuan Zhou, Dong Wang, Xuewen Zou, and Zhiliang Zhang, *Senior Member, IEEE*

***Abstract*—Because of the forward recovery, the performance of the diodes degrades seriously at multimegahertz, causing extremely high power loss. So, the synchronous rectification (SR) is strongly desired in the multimegahertz resonant converters. This paper proposes a self-driven level-shifted resonant gate driver (RGD) for the SR FET in a 10-MHz isolated class-Φ_2 resonant converter. The proposed RGD provides precise switching timing for the SR so that the body diode conduction loss can be minimized. A control stage is introduced to the proposed RGD to block the circulating current and the low-impedance path in the driver to realize ON–OFF control of the converter with high efficiency. The proposed RGD also generates a tunable dc bias to increase the peak gate voltage and extend the conduction time with the optimal $R_{\mathrm{DS(on)}}$ so that the average $R_{\mathrm{DS(on)}}$ and the associated conduction loss can be reduced significantly. A 10-MHz prototype with 18-V input and 5-V/2-A output was built. At full load of 2 A, the proposed RGD improves the efficiency from 80.2% using the conventional RGD to 82% (an improvement of 1.8%). Compared to the efficiency of 77.3% using the diode rectification, the efficiency improvement is 4.7% at full load.**

***Index Terms*—High frequency, isolated class-Φ_2 resonant converter, level-shift, multimegahertz, ON–OFF control, resonant gate driver, synchronous rectification.**

I. Introduction

RECENTLY, the switching frequency has been pushed up to tens of megahertz, directly reducing the energy storage requirements of the passive components, shrinking the size and weight and allowing faster transient response [1], [2]. Most of the previous research on the multimegahertz resonant converters focuses on the nonisolated applications. For example, the resonant boost converters in [3] and [4] and the resonant SEPIC converters in [5] and [6] have achieved high efficiency and fast dynamic performance. However, the state-of-art monolithic power ICs have realized the nonisolated power conversion with extremely high power density, such as EN23F0QI from ENPIRION, but the isolation still remains a challenge to the power IC solution due to the difficulty of the integration of the magnetic components. This motivates research efforts in the isolated multimegahertz resonant converters, such as the 75-MHz isolated resonant converter proposed in [7]. The converter manages to achieve very high power density. However, the efficiency needs to be further improved, especially the high loss in the diodes, which is 35% of the total power loss.

It is pointed out that the performance of the diodes degrades seriously as the switching frequency increases to tens of megahertz because of the forward recovery [8], [9]. There is a large transient voltage across the diode at the turn-on instant, causing high power loss especially at multimegahertz. Therefore, the multiple diodes are paralleled in [10]–[13] to minimize the conduction loss, resulting in increased component count and cost. However, due to the high-frequency pulse current, the high conduction loss dissipated in the rectifier diodes can still account for 30% $\sim$ 35% of the total power loss [6], [8]. In order to reduce the high conduction loss and the frequency-dependent forward recovery loss, the synchronous rectification (SR) technique is strongly desired for the multimegahertz resonant converters, especially in the application of high output current.

Since the conventional hard-switched gate drivers are too inefficient in multimegahertz low-power applications, the resonant gate drivers (RGDs) are normally needed to reduce high-frequency gate drive loss. However, the RGDs in the previous literatures mostly focus on the control FETs in the multimegahertz resonant converters instead of the SR FETs. The multistage RGD is widely used in the multimegahertz resonant converters [3], [5], [6]. It provides the reliable resonant gate voltage and reduces the high-frequency gate loss by storing the drive energy in the resonant tank. However, since the drive signal is produced by the totem pole, the gate voltage averages a fixed value, typically zero or half the supply voltage V_{CC} [3], [5], [6]. The duty ratio of the MOSFET is also fixed. When applied to the SR, it can hardly provide precise switching timing for the SR FET and induce additional conduction time of the body diode, causing high forward voltage drop and high conduction loss. More importantly, the gate voltage of the RGD is sinusoidal and the slow change of the gate voltage will cause high on-state resistance $R_{\mathrm{DS(on)}}$, especially at turn-on and turn-off instant. Hence, the average $R_{\mathrm{DS(on)}}$ is much higher than that provided in the datasheet. This characteristic of the RGD becomes more serious when employed to the SR and the high average $R_{\mathrm{DS(on)}}$ offsets the benefits of the SR technique seriously. A resonant second harmonic class-E gate driver is proposed in [13], which is a half-wave RGD. It provides a dc bias voltage to shift the gate voltage up and down to control the switch duty ratio. However, it consists of as many as seven passive components, which seriously

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The authors are with the Jiangsu Key Laboratory of New Energy Generation and Power Conversion, Nanjing University of Aeronautics & Astronautics, Nanjing 210016, China (e-mail: renxy@nuaa.edu.cn; zoezy@nuaa.edu.cn; wangdong1989@nuaa.edu.cn; zouxuewen@nuaa.edu.cn; zlzhang@nuaa.edu.cn).

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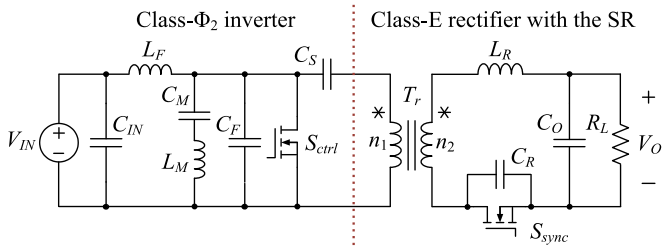

Fig. 1. Isolated synchronous class-Φ_2 resonant converter.

TABLE I
CONVERTER SPECIFICATIONS

V_{IN}	V_O	I_O	P_O	f_s
16~21 V	5 V	2 A	10 W	10 MHz

reduces the power density. Besides, the auxiliary switch also needs additional drive circuit (a CMOS hard-switched inverter driver). The RGDs with tunable dc offset are also proposed in [14] and [15]. However, when applied to the SR FET, the driving logic of the drive signals for the control FET and the SR FET still needs to be solved. Furthermore, the complexity of the drive circuit, consequently, increases the converter size and power loss.

The objective of this paper is to apply the SR technique to the multimegahertz resonant converters. A simple self-driven RGD is proposed for the SR FET in the 10-MHz isolated class-Φ_2 resonant converter. The proposed RGD manages to drive the SR FET with lower $R_{\mathrm{DS(on)}}$ and provides precise switching timing for the SR FET with high efficiency. Section II introduces the problems of the conventional RGD. Section III gives the proposed ON–OFF controlled self-driven RGD for the SR. Section IV gives the simulation results and loss analysis. Section V contains the experimental validation, and finally, Section VI concludes this paper.

II. CHALLENGES FOR THE SR DRIVE IN THE MULTIMEGAHERTZ ISOLATED RESONANT CONVERTERS

A. Multimegahertz Isolated Synchronous Class-Φ_2 Converter

Fig. 1 gives the schematic of the isolated synchronous class-Φ_2 resonant converter and Table I lists the specifications. Because the forward recovery causes high conduction loss in the diodes at multimegahertz, the SR technique is employed to the converter. However, since the SR FETs normally have large total gate charge compared to the control FETs, the gate drive loss at multimegahertz with the conventional hard driver is extremely high and reduces the efficiency seriously.

B. Challenges for the SR Drive and Problems of the Conventional RGD

The challenge of the high-frequency SR drive is that the switching cycle is only 100 ns in this case, which causes problem to obtain the desired phase shift between the drive signals for the control and the SR FETs. The isolation of the drive signal is another problem to be solved.

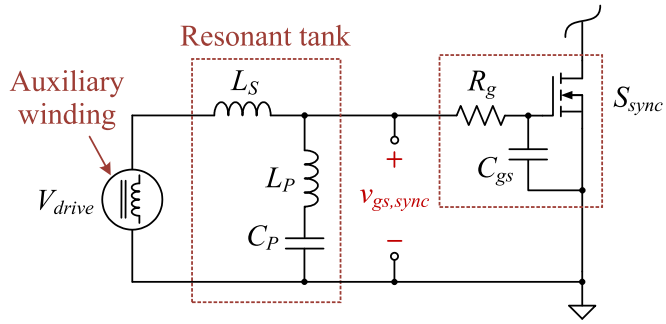

Fig. 2. Conventional RGD with auxiliary winding.

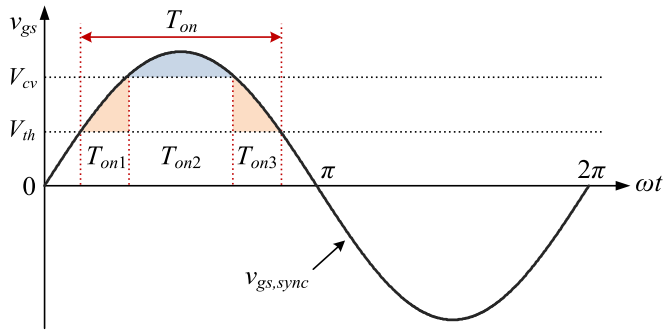

Fig. 3. Resonant drive voltage of the conventional RGD.

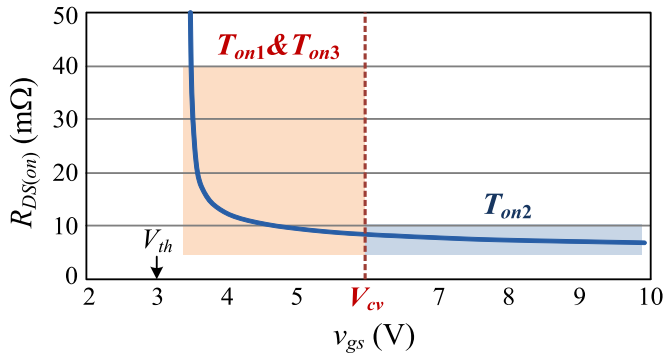

Fig. 4. ON resistance $R_{\mathrm{DS(on)}}$ versus gate voltage v_{gs}.

The multistage RGD is considered for the SR because of its simplicity and efficient gate drive. However, the drive signal of the RGD in previous research is generated by the totem pole. When applied to the SR in this case, the external-driven scheme will induce the propagation delay of the driver ICs (normally tens of nanosecond), which may cause ill effect on the drive signal timing during the switching cycle of 100 ns. Meanwhile, the self-driven SR is a simple drive scheme because the drive signals for the SR FETs are provided by the circuit node voltage inherently without additional controllers and hardware delay problems [16]–[18]. Therefore, as shown in Fig. 2, an auxiliary winding is chosen to provide the drive signal and isolation. Fig. 3 shows the sinusoid gate voltage of the conventional RGD. With the drive signal provided by the auxiliary winding of the transformer, the resonant gate voltage averages zero. There are two main drawbacks of the conventional RGD.

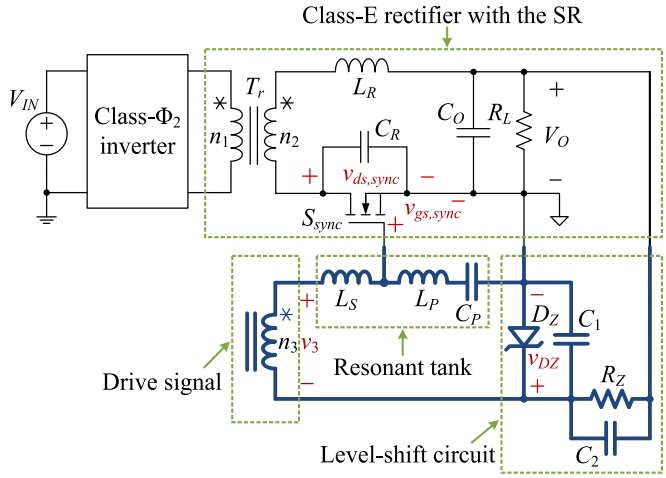

Fig. 5. Proposed self-driven level-shifted RGD.

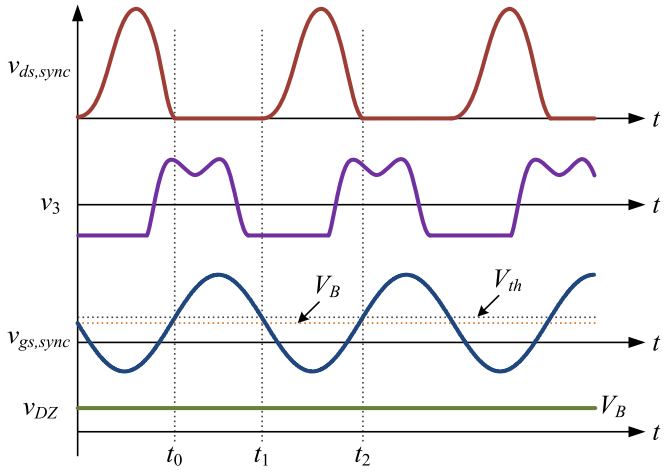

Fig. 6. Key waveforms of the level-shifted RGD.

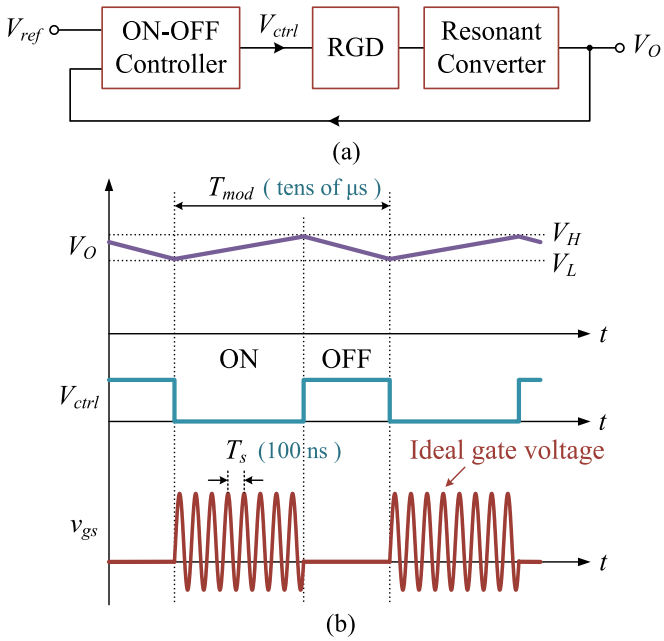

Fig. 7. ON–OFF control for the multimegahertz resonant converters.

1) Fig. 4 shows the typical curve of the on-state resistance $R_{\mathrm{DS(on)}}$ as a function of the gate-to-source voltage v_{gs}, based on the datasheet of a Si MOSFET from Vishay (SiS862DN). It is observed that the $R_{\mathrm{DS(on)}}$ changes significantly with v_{gs}. When v_{gs} just exceeds the threshold voltage V_{th} or declines close to V_{th}, especially at the turn-on and turn-off instant, $R_{\mathrm{DS(on)}}$ is much high. Conversely, when v_{gs} exceeds the critical voltage V_{cv} (typically 5 ∼ 6 V), $R_{\mathrm{DS(on)}}$ is much lower and reduces smoothly.
   Based on the curve of $R_{\mathrm{DS(on)}}$ versus v_{gs}, the conduction time in Fig. 3 is divided into three intervals: the conduction time with a low $R_{\mathrm{DS(on)}}$, T_{on2}, and the conduction time with a high $R_{\mathrm{DS(on)}}$, T_{on1} and T_{on3}. The problem is that T_{on2} is quite short (less than 50% of the total conduction time T_{on}), while T_{on1} and T_{on3} are relatively long (more than 50% of T_{on}). As a result, the average $R_{\mathrm{DS(on)}}$ of the MOSFET is much higher than the rated value in the datasheet, causing high conduction loss in the SR FET.
2) The conduction time of the SR FET can hardly be adjusted flexibly to meet different duty ratio requirement. The duty ratio is always less than 50% and cannot provide precise switching timing for the SR. It will induce the body diode conduction time, which usually causes high voltage drop and conduction loss.

III. Proposed Self-Driven RGD for the SR

A. Self-Driven Level-Shifted RGD for the SR

Fig. 5 gives the proposed self-driven level-shifted RGD for the SR FET. The auxiliary winding n_3 provides the drive signal. The resonant tank provides the desired voltage gain and phase-shift from n_3 to the gate of the SR FET. The level-shift circuit provides a tunable dc bias to increase the peak gate voltage so that the conduction time with the optimal $R_{\mathrm{DS(on)}}$ can be extended and the average $R_{\mathrm{DS(on)}}$ of the MOSFET can be reduced. Moreover, by tuning the phase-shift of the resonant tank and the dc bias, the proposed RGD can provide precise switching timing for the SR FET.

Fig. 6 shows the key waveforms. The voltage across the auxiliary winding, v_3, is transferred through the resonant tank to the ac sine component of the gate voltage $v_{\mathrm{gs,sync}}$. The voltage across D_Z, v_{DZ}, is kept constant at its Zener voltage V_B. So, the dc bias of $v_{\mathrm{gs,sync}}$ also equals V_B. At t_0, the drain voltage $v_{\mathrm{ds,sync}}$ resonates to zero, and $v_{\mathrm{gs,sync}}$ increases in a resonant manner and just exceeds the threshold voltage V_{th} so the SR FET S_{sync} turns ON immediately. At t_1, $v_{\mathrm{gs,sync}}$ decreases below V_{th}, so S_{sync} turns OFF and $v_{\mathrm{ds,sync}}$ begins to rise. After t_1, $v_{\mathrm{gs,sync}}$ resonates always below V_{th} until the next switching cycle.

B. Problems of the Level-Shifted RGD Under ON–OFF Control

The ON–OFF control is normally used in the multimegahertz resonant converters owing to its simple structure and fast transient response [3], [19]. Fig. 7 shows the block diagram

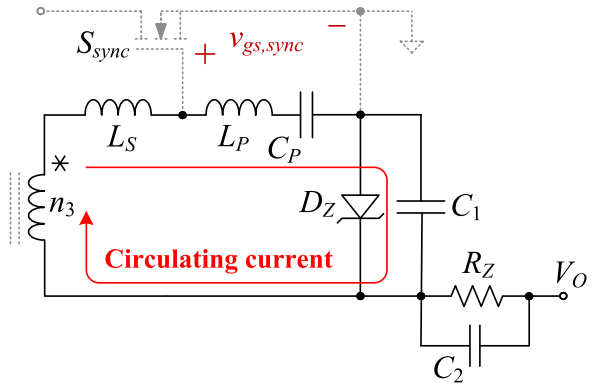

Fig. 8. Circulating current when converter turns OFF.

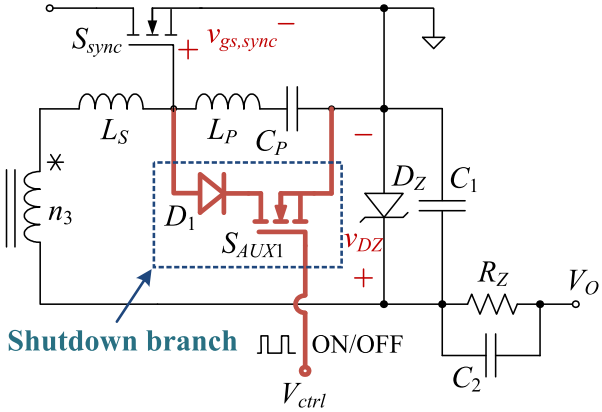

Fig. 9. Self-driven level-shifted RGD with a shutdown branch.

and the key waveforms. The output voltage V_O is compared to the reference $V_{\rm ref}$ by the ON–OFF controller. The output of the controller, $V_{\rm ctrl}$, modulates the converter ON and OFF. The ON–OFF modulation frequency $f_{\rm mod}$ is much lower than the switching frequency f_s. To ensure fast transient response, the ON–OFF control scheme requires that the converter turns ON and OFF quickly. Therefore, for the driver, shown as $v_{\rm gs}$ in Fig. 7, the gate voltage is supposed to achieve fast shutdown and buildup under ON–OFF operation.

The problem of the proposed RGD in Part A is that there is a circulating current and gate energy resonant oscillation in the driver when the converter turns OFF. As shown in Fig. 8, the voltage across the auxiliary winding n_3 drops to zero, and the drive energy stored in the resonant tank induces a circulating current in the *LC* network in the drive circuit, until the drive energy is dissipated by the parasitic resistances. This circulating current will cause the gate voltage resonant oscillation, which may lead to undesired false turn-on of the SR FET and high circulating loss.

To block the circulating current, in Fig. 9, a shutdown branch is added to the drive circuit in parallel with the gate and source. The branch comprises a diode D_1 and an auxiliary switch $S_{\rm AUX1}$ controlled by the control signal $V_{\rm ctrl}$ [3], [5], [6]. However, although the shutdown branch blocks the drive circulating current when the converter turns OFF, it causes another problem when the converter turns ON. There are three operation intervals of the

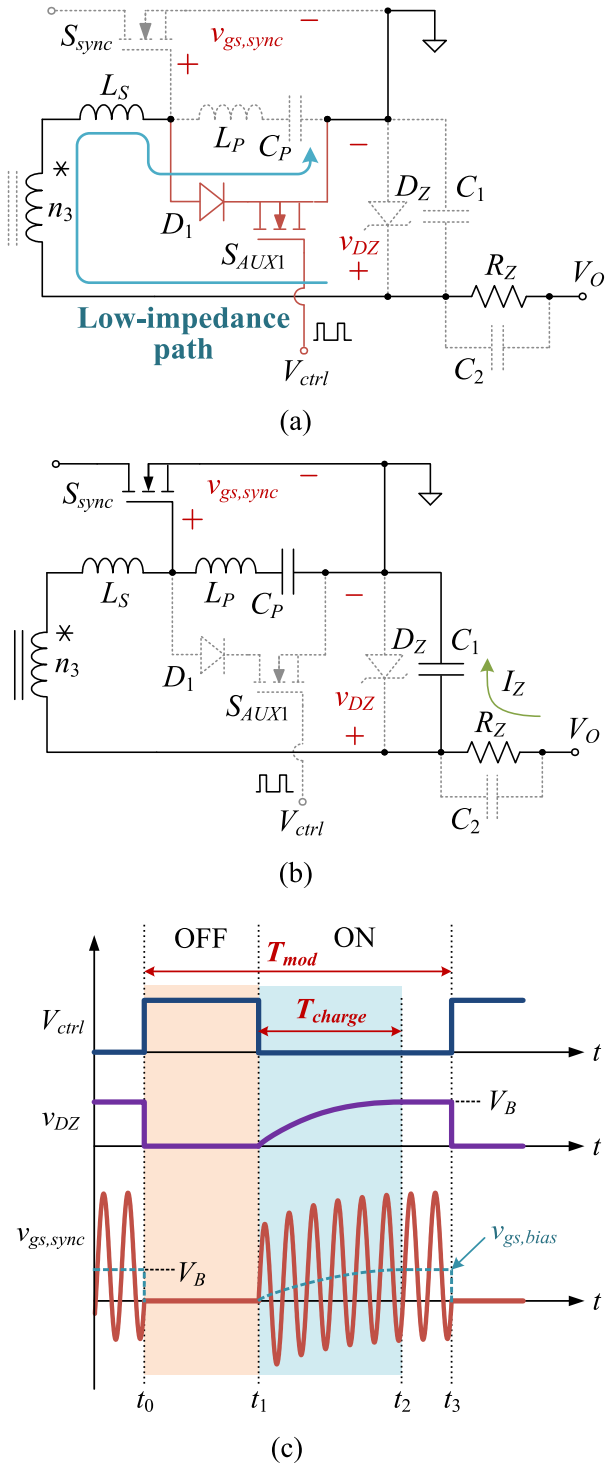

Fig. 10. Equivalent circuits and waveforms of the level-shifted RGD with the shutdown branch.

RGD and Fig. 10 gives the equivalent circuits and the operation waveforms.

1) *Interval 1* $[t_0, t_1]$: $V_{\rm ctrl}$ sets high and the converter turns OFF. In Fig. 10(a), $S_{\rm AUX1}$ turns ON and D_1 conducts to enable the shutdown branch. The auxiliary winding n_3, the inductance L_S, and the shutdown branch form a low-impedance current path. The capacitance C_1 is discharged

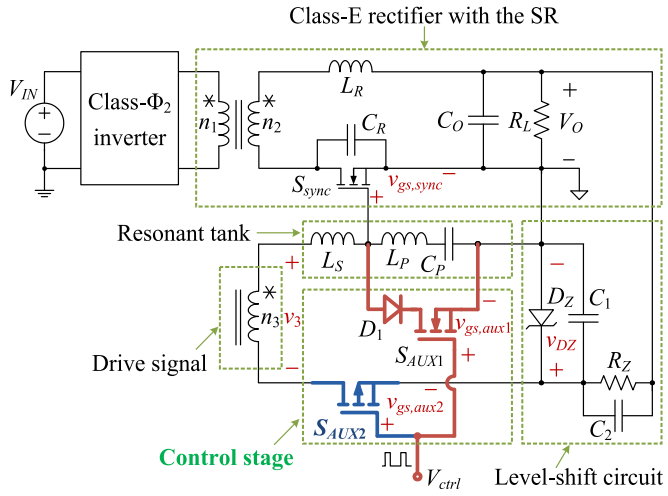

Fig. 11. Proposed ON–OFF controlled level-shifted RGD for the SR.

to zero quickly by this low-impedance path and cannot be charged again because D_1 blocks the reverse charging current. So, in Fig. 10(c), $v_{\mathrm{gs,sync}}$ is clamped to zero from t_0 to t_1. v_{DZ} falls to zero at t_0 and keeps constant at zero from t_0 to t_1.

2) *Interval 2* $[t_1, t_2]$*:* V_{ctrl} sets low and the converter turns ON. S_{AUX1} turns OFF and the shutdown branch is disabled. So, the passive components begin to resonate and C_1 is charged through R_Z by V_O. The voltage across C_1, v_{DZ}, (which is actually the bias voltage of $v_{\mathrm{gs,sync}}$, $v_{\mathrm{gs,bias}}$) increases as

$$\begin{aligned} v_{DZ}(t) &= v_{\mathrm{gs,bias}}(t) \\ &= V_B\left[1-\exp\left(-(t-t_1)/R_Z C_1\right)\right]. \end{aligned} \quad (1)$$

3) *Interval 3* $[t_2, t_3]$*:* v_{DZ} reaches V_{B} and keeps constant. Note that if v_{DZ} cannot reach V_B from t_1 to t_3, this interval does not exist.

During Interval 2, the actual bias voltage $v_{\mathrm{gs,bias}}$ is always lower than the desired bias V_B. From Fig. 10(c), it should be noted that the period of Interval 2, $T_{\mathrm{charge}} = t_2 - t_1$, is too long compared to the modulation cycle T_{mod}. Normally, T_{mod} is several microseconds to tens of microsecond, while the time constant of R_Z and C_1 ($\tau_{RC} = R_Z C_1$) is also in the microsecond range. It means that the bias voltage can hardly reach the desired voltage level during the ON status, seriously offsetting the benefits of the dc bias in the level-shifted RGD under close loop.

C. Proposed ON–OFF Controlled Level-Shifted RGD for the SR

To solve the charging and discharging problem of v_{DZ}, another auxiliary switch S_{AUX2} (P-Channel) is introduced to the driver, as shown in Fig. 11. S_{AUX2} is connected in series between the auxiliary winding n_3 and the level-shift circuit. S_{AUX2} and D_1, S_{AUX1} form the control stage of the proposed ON–OFF controlled level-shifted RGD. Since the control signal V_{ctrl} is a square wave between 0 and V_{CC} (the supply voltage), the gate voltage of S_{AUX2}, $v_{\mathrm{gs,aux2}}$, is a square wave between $-V_B$ and

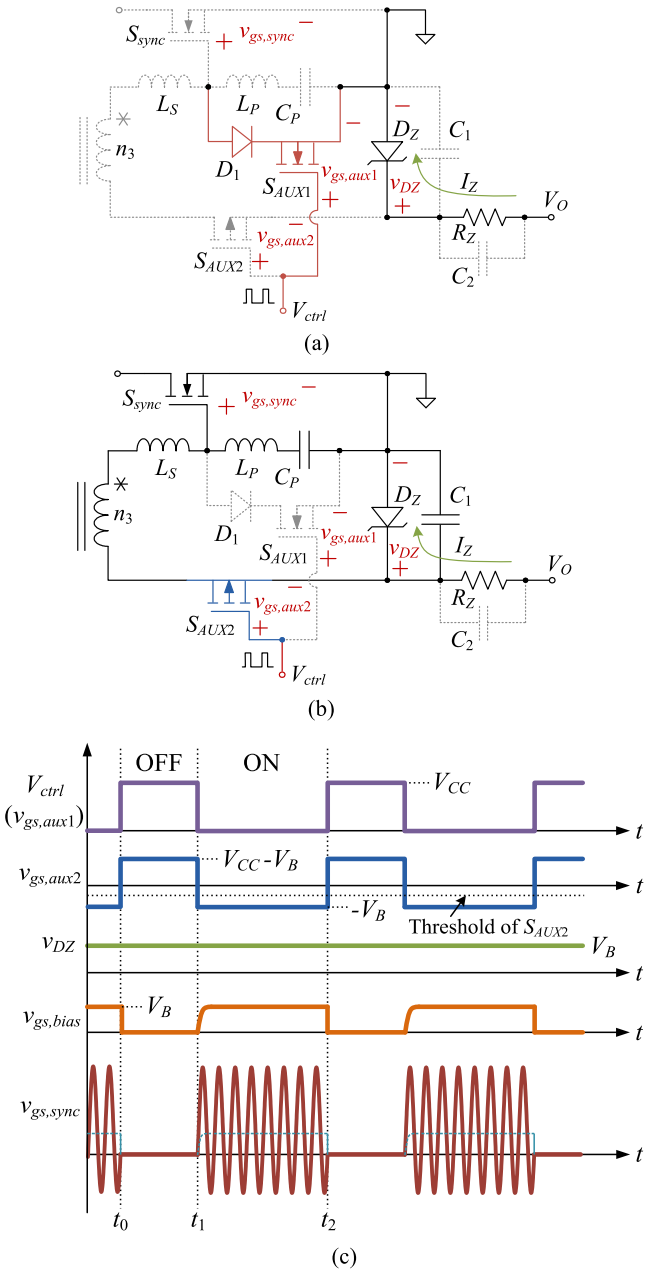

Fig. 12. Equivalent circuits and waveforms of the ON-OFF controlled level-shifted RGD.

$V_{CC} - V_B$. Therefore, S_{AUX1} and S_{AUX2} can share V_{ctrl} as the drive voltage as long as $-V_B$ is lower than the threshold of S_{AUX2}.

Fig. 12 shows the equivalent circuits and the key waveforms of the proposed RGD. In Fig. 12(a), at t_0, V_{ctrl} sets high and S_{AUX1} turns ON to shutdown the gate voltage. $v_{\mathrm{gs,aux2}}$ increases to $V_{CC} - V_B$ to turn OFF S_{AUX2}. The low-impedance path is blocked and the voltage across D_Z will not be discharged. So, in Fig. 12(c), from t_0 to t_1, $v_{\mathrm{gs,sync}}$ is clamped to zero and v_{DZ} is kept stable at V_B. In Fig. 12(b), at t_1, V_{ctrl} sets low and S_{AUX1} turns OFF to disable the shutdown branch. $v_{\mathrm{gs,aux2}}$ falls to $-V_B$ so that S_{AUX2} turns ON to conduct the drive current. The resonant components in the RGD begin to resonate

to provide switching-frequency drive voltage. Since v_{DZ} is not discharged before t_1, there is no charging process from t_1 to t_2. So, in Fig. 12(c), from t_1 to t_2, v_{DZ} still keeps stable at V_B and $v_{\mathrm{gs,bias}}$ increases to V_B as soon as the converter turns ON. Therefore, the benefits of the level-shifted RGD can be maintained under ON–OFF operation.

D. Design of the Level-Shifted RGD

1) Auxiliary Winding: The voltage across the winding n_3 is determined by the output of the inverter and the turns ratio of the primary and the auxiliary windings $n_1 : n_3$. The output of the class-Φ_2 inverter is approximately a square wave between V_{IN} and $-V_{\mathrm{IN}}$. So, the voltage across n_3, v_3, swings between $n_3 V_{IN}/n_1$ and $-n_3 V_{IN}/n_1$. A step-down voltage is preferred so that it is easier to design the resonant tank to generate the desired phase shift and voltage gain. Since the turns ratio of the primary and the secondary windings, $n_1 : n_2$, is 4:1 to balance the voltage and current stress on the SR FET, there are three possible options for $n_1 : n_3$. The final design of $n_1 : n_3$ is 4:1 because if it is set to 4:2 or 4:3, the peak gate voltage would easily be high or even exceed the limits of the device ($\pm$20 V), which results in the over voltage damage of the semiconductor device.

2) Resonant Tank: The capacitance C_P blocks the dc bias voltage. The inductances, L_P and L_S, set the winding to gate (ac component) transfer function, which is

$$H(s) = \frac{V_{\mathrm{gs,ac}}(s)}{V_3(s)} = \frac{sR_g L_P C_{\mathrm{iss}} + L_P}{s^2 L_P L_S C_{\mathrm{iss}} + sR_g C_{\mathrm{iss}}(L_P + L_S) + L_P + L_S}. \quad (2)$$

So, the frequency characteristics are

$$A(\omega) = |H(j\omega)| \quad (3)$$

$$\varphi(\omega) = \arctan\left(\frac{\mathrm{Im}(H(j\omega))}{\mathrm{Re}(H(j\omega))}\right). \quad (4)$$

The inductances need to be designed to obtain the desired voltage gain and phase shift. The phase-shift of the drive signal v_3 to the gate voltage $v_{\mathrm{gs,sync}}$, φ, can be obtained by the simulation of the power train. Replacing the SR FET with an ideal diode, the phase angle difference between the output of the inverter and the ideal conduction time of the diode is the desired φ. In this case, $\varphi \approx -26°$. Substituting φ into (4), the relation between L_P and L_S can be described as $L_S = f(L_P)$.

The resonant frequency of L_P and C_{iss} is below f_s, so an initial point for L_P can be selected as

$$L_P > 1/4\pi^2 f_s^2 C_{\mathrm{iss}}. \quad (5)$$

So, the value of L_S can be determined. Then, the voltage gain $A(\omega) = V_{\mathrm{gs,ac}}/V_3$ needs to be checked, which is supposed to ensure a proper amplitude for the drive voltage, that is, $V_{\mathrm{th}} < V_{\mathrm{gs,ac}} < V_{\mathrm{gs,max}}$, where $V_{\mathrm{gs,max}}$ is the maximum gate voltage of the device.

And the voltage across n_3 is

$$V_3 = \frac{n_3}{n_1} V_{\mathrm{IN}}. \quad (6)$$

TABLE II
SIMULATION PARAMETERS: $V_{\mathrm{IN}} = 18$ V, $V_{\mathrm{O}} = 5$ V, $P_{\mathrm{O}} = 10$ W, AND $f_s = 10$ MHz

L_F	220 nH	C_F	420 pF
L_M	220 nH	C_M	220 pF
L_R	18 nH	C_R	3600 pF
$n_1 : n_2 : n_3$	4:1:1	C_B	1 μF
L_S	560 nH	R_Z	470 Ω
L_P	150 nH	C_1, C_2	1 μF
C_P	100 nF	D_Z	TZS4679 (2 V)

So

$$\frac{n_1 V_{\mathrm{th}}}{n_3 V_{\mathrm{IN,min}}} < A(\omega_s) < \frac{n_1 V_{\mathrm{gs,max}}}{n_3 V_{\mathrm{IN,max}}}. \quad (7)$$

After the voltage gain is checked, the values of L_P and L_S can be determined. Some trial-and-error tuning is still required to make the final design.

3) Level-Shift Circuit: The level-shift circuit provides the desired dc bias V_B for the RGD. The value of V_B is determined by the duty ratio and the threshold voltage of the SR FET. The duty ratio is set to 0.5 to balance the voltage and current stress on the device. So, the dc bias voltage V_B is supposed to be around the threshold voltage, that is, $V_B = V_{\mathrm{th}}$. Since the switch selected for the SR is SiS862DN from Vishay and the threshold voltage is around 2 V, the Zener diode TZS4679 with a Zener voltage of 2 V is selected as D_Z.

IV. SIMULATION AND LOSS ANALYSIS OF THE PROPOSED RGD

A. Simulation Results

The circuit in Fig. 11 is simulated with LTspice and the simulation parameters are listed in Table II.

Fig. 13 gives the SR simulation comparison. The drive voltage of the conventional RGD is a sine wave with 5-V amplitude while the drive of the proposed RGD has a dc bias of 2 V. With both RGDs, the duty ratio of the SR FET is about 0.48 and the peak drain voltage is 20 V. With the conventional RGD, the conduction time of the body diode is 11 ns, more than 22% of the total conduction time. On the contrary, the proposed RGD provides precise switching timing for the SR FET and the conduction time of the body diode is almost zero. Another point is that, the peak gate voltage of the proposed RGD is higher than that of the conventional RGD owing to the 2 V bias. So, the conduction time with optimal $R_{\mathrm{DS(on)}}$ is extended from zero using the conventional RGD to 26 ns (more than 54% of the total conduction time).

Fig. 14 gives the close-loop gate drive simulation comparison. The control signal of the converter V_{ctrl} is set as a square wave with a duty cycle of 20 μs and a duty ratio of 0.2. In Fig. 14(a) without S_{AUX2}, v_{DZ} drops to zero as soon as the converter turns OFF. When the converter turns ON, v_{DZ} and $v_{\mathrm{gs,bias}}$ increase slowly and $v_{\mathrm{gs,bias}}$ does not reach the desired bias of 2 V in the end. On the contrary, with S_{AUX2} in Fig. 14(b), v_{DZ} remains constant at its Zener voltage of 2 V all the time. $v_{\mathrm{gs,bias}}$ and $v_{\mathrm{gs,synnc}}$ are clamped at zero when the converter turns OFF and $v_{\mathrm{gs,bias}}$ increases to 2 V immediately when the converter

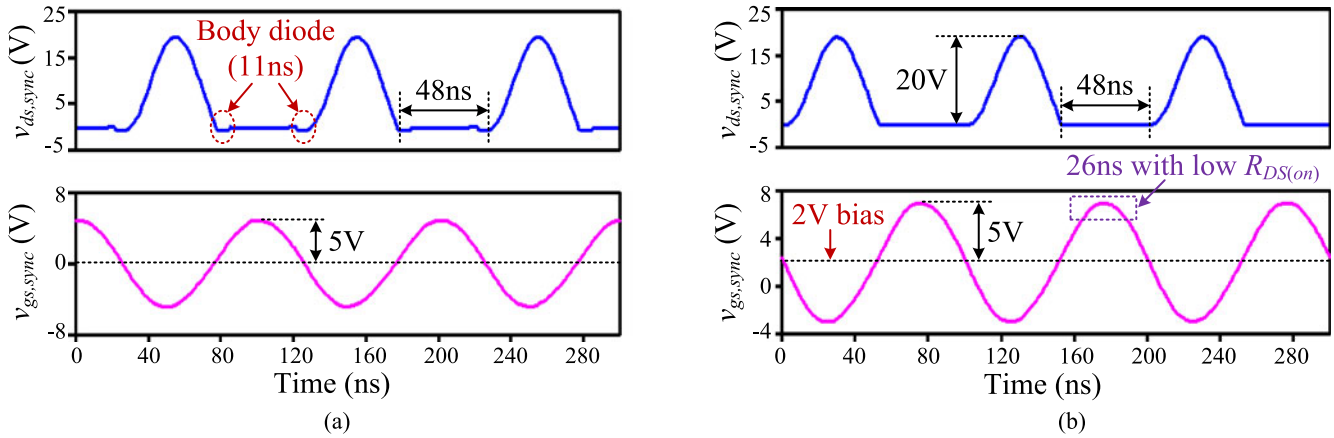

Fig. 13. Simulation of the conventional and the proposed RGDs. (a) Conventional RGD, (b) Proposed RGD.

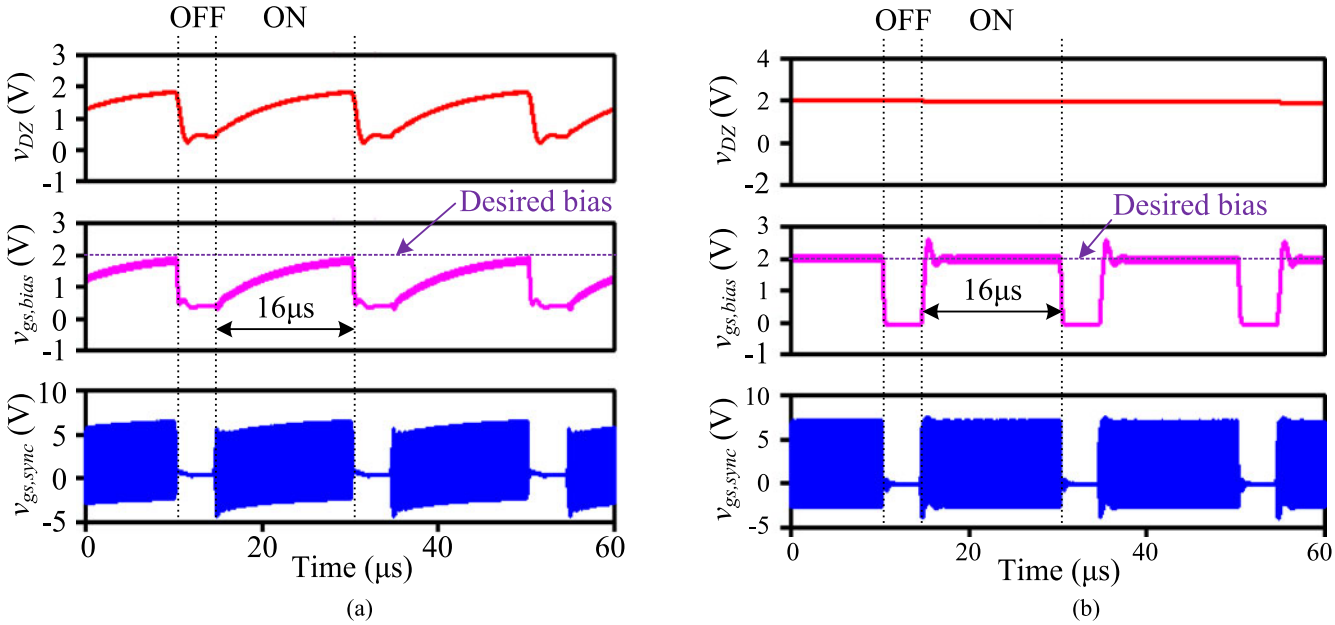

Fig. 14. Simulated close-loop gate drive comparison. (a) Without S_{AUX2}, (b) With S_{AUX2}.

turns ON. So, $v_{\mathrm{gs,sync}}$ is level shifted as desired as soon as the converter turns ON.

B. Loss Analysis of the SR With the Proposed RGD

1) Drive Loss of the SR: Fig. 15 gives the loss model of the proposed RGD when the converter is ON, where R_g is the gate resistance of S_{sync}, R_3 is the ESR of n_3, R_{LS} and R_{LP} are the ESRs of L_S and L_P, respectively, R_{AUX2} is the on-state resistance of S_{AUX2}. To avoid complexity, the ESRs and ESLs of the capacitance are not considered.

In Fig. 15, the gate voltage of the RGD, $v_{\mathrm{gs,sync}}$, is

$$v_{\mathrm{gs,sync}}(t) = V_B + V_{\mathrm{gs,ac}} \sin(2\pi f_s t + \theta). \tag{8}$$

The phase shift between $v_{\mathrm{gs,sync}}$ and the voltage across the input capacitance, $v_{C\mathrm{iss}}$, is

$$\Delta\theta = \arctan 2\pi f_s C_{\mathrm{iss}} \cdot R_g \approx 0. \tag{9}$$

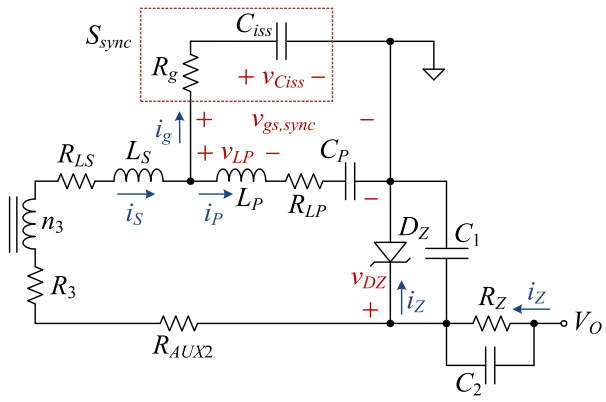

Fig. 15. Loss model of the proposed RGD.

So, the voltage across C_{iss} is

$$v_{C\mathrm{iss}}(t) = v_{\mathrm{gs,sync}}(t) \cdot \cos\Delta\theta \approx v_{\mathrm{gs,sync}}(t). \tag{10}$$

The current through R_g is

$$i_g(t) = i_{C\text{iss}}(t) = C_{\text{iss}} \frac{dv_{C\text{iss}}(t)}{dt} = 2\pi f_s V_{\text{gs,ac}} C_{\text{iss}} \cos(2\pi f_s t + \theta). \quad (11)$$

Therefore, the loss dissipation in R_g is

$$P_{Rg} = I_g^2 R_g = 2\pi^2 f_s^2 V_{\text{gs,ac}}^2 C_{\text{iss}}^2 R_g. \quad (12)$$

The voltage across C_P is V_B. Since the impedance of R_{LP} is quite small compared to L_P, the phase shift between $v_{\text{gs,sync}}$ and v_{LP} can be ignored. So, v_{LP} is

$$v_{LP}(t) = V_{\text{gs,ac}} \sin(2\pi f_s t + \theta). \quad (13)$$

With the integral of v_{LP}, the current through L_P is

$$i_P(t) = \frac{1}{L_P} \int v_{LP}(t)\, dt = -\frac{V_{\text{gs,ac}}}{2\pi f_s L_P} \cos(2\pi f_s t + \theta). \quad (14)$$

The power loss in the ESR of L_P can be calculated as

$$P_{LP} = I_P^2 \cdot R_{LP} = \frac{V_{\text{gs,ac}}^2}{8\pi^2 f_s^2 L_P^2} R_{LP}. \quad (15)$$

Combining (11) and (14), the current through R_3 is

$$i_S(t) = i_g(t) + i_P(t) = \left(2\pi f_s V_{\text{gs,ac}} C_{\text{iss}} - \frac{V_{\text{gs,ac}}}{2\pi f_s L_P}\right) \times \cos(2\pi f_s t + \theta). \quad (16)$$

So, the loss dissipated in R_3, R_{LS}, and R_{AUX2} can be calculated as

$$P_{R3} = I_S^2 \cdot R_3 \quad (17)$$

$$P_{LS} = I_S^2 \cdot R_{LS} \quad (18)$$

$$P_{S\text{AUX2}} = I_S^2 \cdot R_{\text{AUX2}} \quad (19)$$

$$I_S = \sqrt{2}\pi f_s V_{\text{gs,ac}} C_{\text{iss}} - \frac{V_{\text{gs,ac}}}{2\sqrt{2}\pi f_s L_P}. \quad (20)$$

The current flowing through R_Z is

$$i_Z(t) = \frac{V_O - V_B}{R_Z}. \quad (21)$$

Owing to the high resistance of R_Z, the power loss in the level-shift circuit is negligible.

Combining (12), (15), and (17)–(19), the total drive loss of the proposed RGD is

$$P_D = P_{R3} + P_{Rg} + P_{LS} + P_{LP} + P_{S\text{AUX2}}. \quad (22)$$

2) Conduction loss of the SR: The conduction loss of the SR consists of the conduction loss in the MOSFET, $P_{\text{CON,SR}}$, and the conduction loss in the body diode, $P_{\text{CON,BD}}$, which can be calculated as

$$P_{\text{CON,SR}} = I_{\text{SR,rms}}^2 \cdot R_{\text{DS(on),avg}} \quad (23)$$

$$P_{\text{CON,BD}} = V_{F,\text{BD}} \cdot I_{\text{BD,avg}} \quad (24)$$

where $I_{\text{SR,rms}}$ is the RMS current of the MOSFET, $V_{F,\text{BD}}$ is the forward voltage of the body diode (normally 0.7 $\sim$ 0.8 V) and can be found in the datasheet, $I_{\text{BD,avg}}$ is the average current of the body diode.

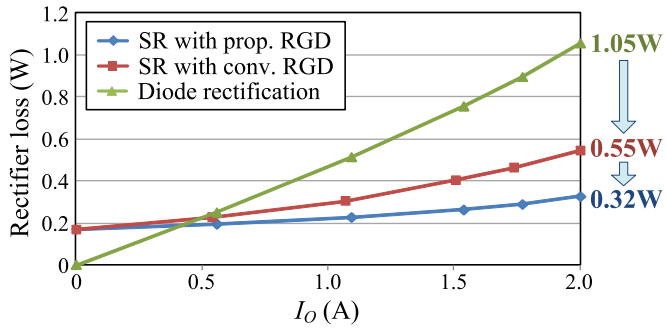

Fig. 16. Rectifier device loss comparison (RGD drive loss included) .

3) Rectifier Loss Comparison Among Different Rectification Schemes: Fig. 16 gives the calculated rectifier loss comparison among three different rectification schemes. The loss of the rectifier diode is calculated based on the recommended formula for STPS3L60 (60 V/3 A, ST) as

$$P_{\text{diode}} = 0.44 \times I_{\text{avg}} + 0.05 \times I_{\text{rms}}^2. \quad (25)$$

From Fig. 16, it is observed that when the output current I_O is below 0.5 A, the power loss of the SR FET is higher than the diode rectification because of the drive loss. When I_O is over 0.5 A, the SR schemes become more efficient than the diode scheme. More importantly, the conduction loss of the SR with the proposed RGD is reduced compared to the conventional RGD. At 5-V/2-A output, the loss of the SR with the proposed RGD is 0.32 W (3.2% of P_O), a reduction of 42% (0.23 W) compared to the SR with the conventional RGD (0.55 W), and a reduction of 72% (0.73 W) compared to the diode rectification (1.05 W).

V. Experimental Verification and Discussion

To verify the proposed circuit, an experimental prototype operating at 10-MHz, 18-V input and 5-V/2-A output was built. Fig. 17 gives the photograph of the prototype. Tables III and IV give the component values and part numbers in the power stage and the proposed RGD, respectively. The inductance in the inverter stage, L_B, is provided by the leakage inductance of the transformer. The values of C_F and C_R in Table III are the external capacitances in parallel with the output capacitance of the MOSFETs.

Fig. 18 shows the drain and gate voltage waveforms of the control FET. It is observed that the drain voltage is approximately half-wave symmetric. The peak drain voltage is 47 V at 18 V input (2.61 times of the input voltage), and the converter provides good zero-voltage switching (ZVS) achievement for the control FET.

Fig. 19 shows the drain and gate voltage waveforms of the SR FET. It is observed that the proposed RGD provides a sinusoidal drive voltage with a dc bias of 2 V and the amplitude of the sine component is 5.8 V, agreeing well with the theoretical analysis and simulation results. The drain and gate oscillation is caused by the parasitic package inductance and the nonlinearity of the parasitic capacitance of the device. The duty ratio of the SR FET is 0.5 and the peak drain voltage is 20 V.

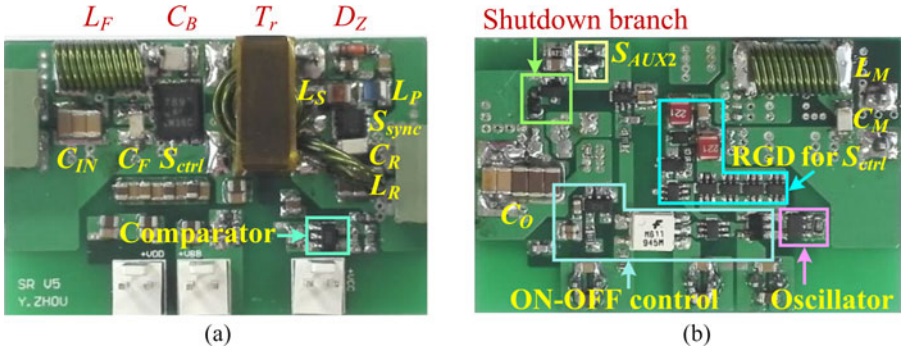

Fig. 17. Photograph of the prototype.

TABLE III
COMPONENTS IN THE POWER STAGE

$S_{\rm ctrl}$	Si7898DP (Vishay) (150 V, N-channel)	$S_{\rm sync}$	SiS862DN (Vishay) (60 V, N-channel)
L_F, L_M	2222SQ-221 (Coilcraft)	L_R	A04T (Coilcraft)
C_F	268 pF	C_R	2940 pF
C_M	247 pF	C_B	15 nF
$C_{\rm IN}$	20 μF	C_O	235 μF
$n_1 : n_2 : n_3$	4:1:1	Core	ER 14.5/3/7 (4F1)

TABLE IV
COMPONENTS IN THE PROPOSED RGD

L_S	680 nH	D_1	BAS170WS (Vishay)
L_P	150 nH	S_{AUX1}	FDV303N (Fairchild)
C_P	0.1 μF	S_{AUX2}	NTA4151P (ON Semi)
R_Z	470 Ω	D_Z	TZS4679 (Vishay)

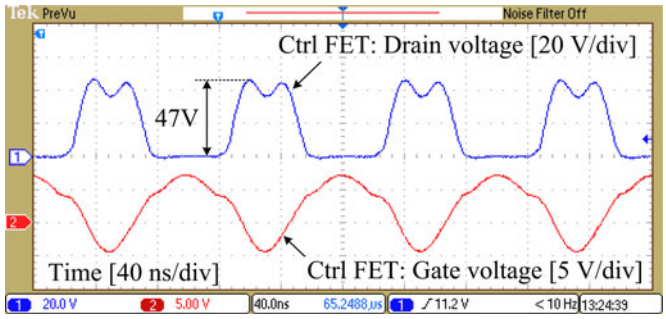

Fig. 18. Waveforms of the ctrl FET: $V_{\rm IN} = 18$ V, $V_O = 5$ V, and $f_s = 10$ MHz.

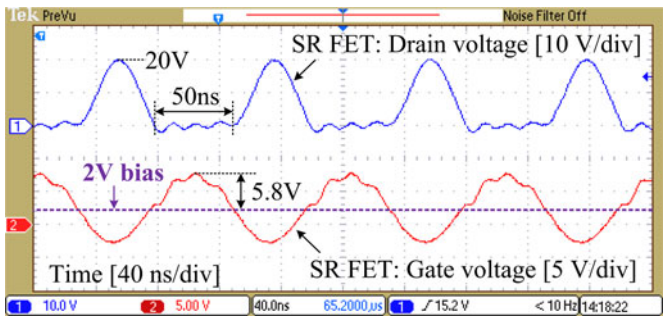

Fig. 19. Waveforms of the SR FET: $V_{\rm IN} = 18$ V, $V_O = 5$ V, and $f_s = 10$ MHz.

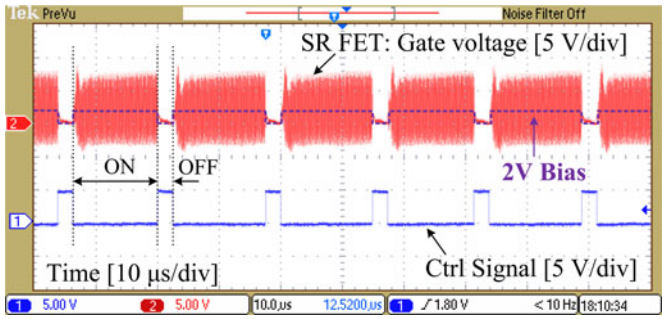

Fig. 20. Gate voltage of the SR and the control signal: $V_{\rm IN} = 18$ V, $V_O = 5$ V, and $P_O = 10$ W.

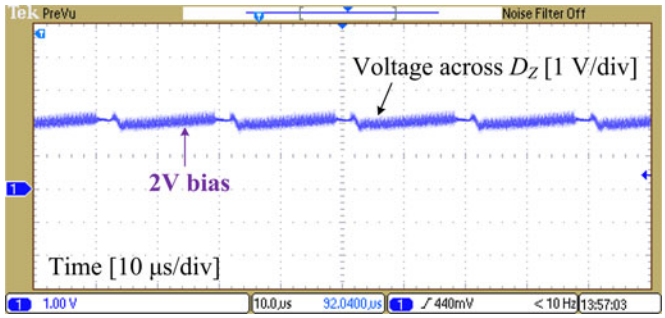

Fig. 21. Voltage across D_Z: $V_{\rm IN} = 18$ V, $V_O = 5$ V, and $P_O = 10$ W.

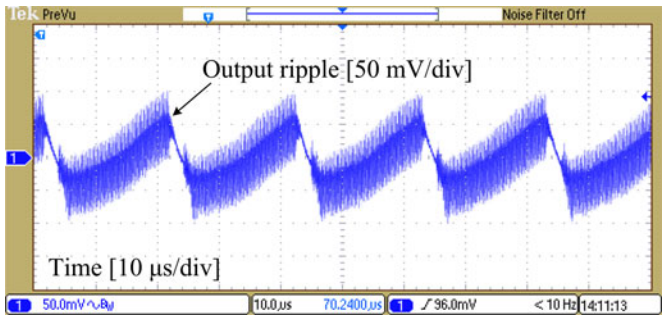

Fig. 22. Output voltage ripple: $V_{\rm IN} = 18$ V, $V_O = 5$ V, and $P_O = 10$ W.

Fig. 20 shows the close-loop gate voltage of the proposed RGD and the control signal. The modulation frequency is 55 kHz at full load. It is observed that when the converter turns OFF, the gate voltage is clamped to zero quickly. When the converter turns ON, the gate voltage begins to resonate, and the bias voltage of

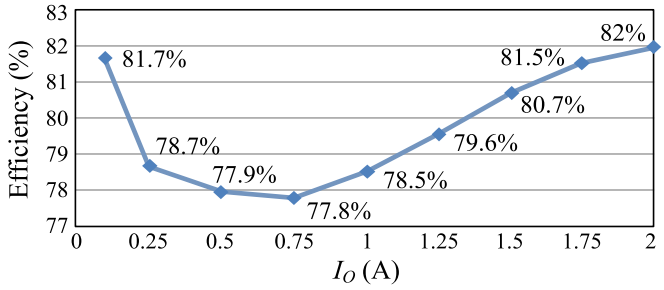

Fig. 23. Close-loop efficiency: $V_{\rm IN} = 18$ V and $V_O = 5$ V.

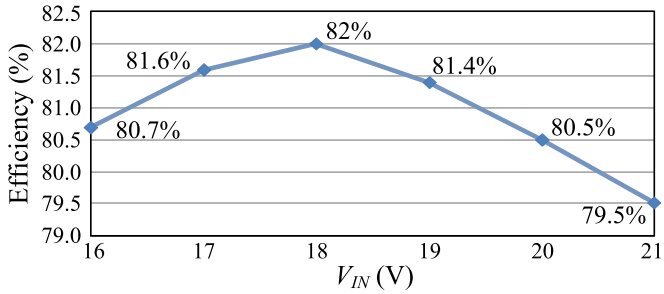

Fig. 24. Close-loop efficiency: $V_O = 5$ V and $P_O = 10$ W.

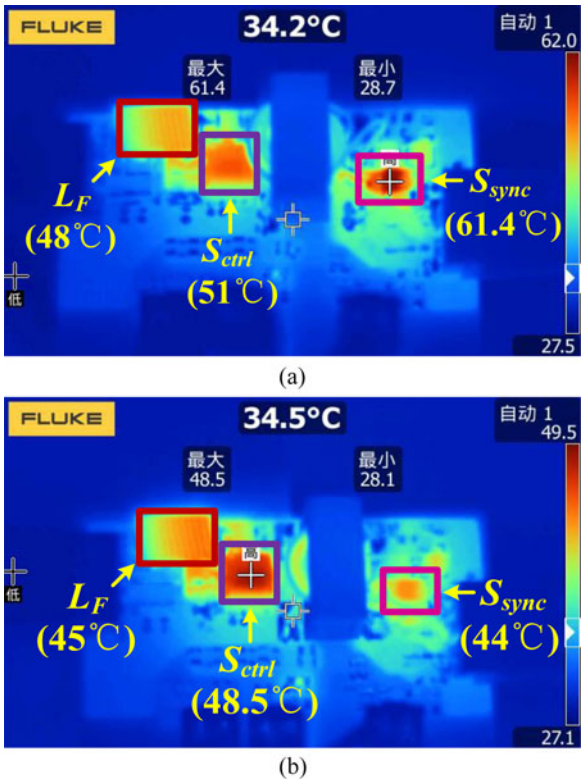

Fig. 25. Thermal imaging comparison: $V_{\rm IN} = 18$ V, $V_O = 5$ V, and $P_O = 10$ W.

the gate voltage reaches the desired Zener voltage (2 V in this case) immediately.

Fig. 21 shows the voltage across the Zener diode D_Z in the proposed RGD. It can be seen that there is no charging and discharging process of v_{DZ} during the ON–OFF operation, and

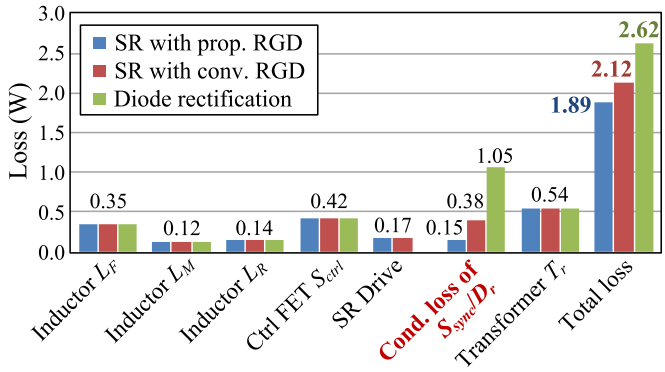

Fig. 26. Loss breakdown: $V_{\rm IN} = 18$ V, $V_O = 5$ V, and $P_O = 10$ W.

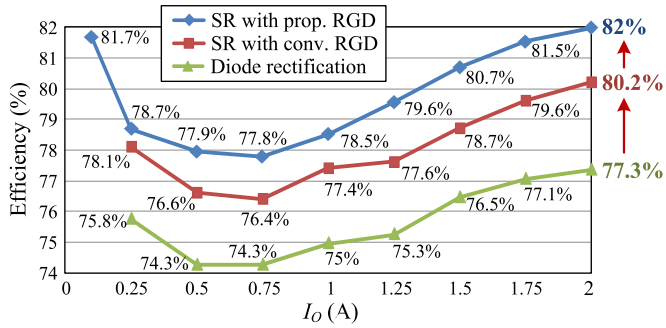

Fig. 27. Efficiency comparison: $V_{\rm IN} = 18$ V and $V_O = 5$ V.

it remains stable at 2 V (the Zener voltage of D_Z), agreeing well with the theoretical analysis in Section III.

Fig. 22 gives the output voltage ripple (20-MHz bandwidth), which is mainly determined by the output capacitance and the hysteresis band of the ON–OFF controller. In this case, the low-frequency output ripple at 5-V output is about 100 mV (5% of V_O), which can be further reduced by narrowing the hysteresis band or increasing the output capacitance.

Fig. 23 gives the close-loop efficiency at the nominal input of 18 V. The peak efficiency is 82% at full load. As I_O decreases, the efficiency decreases from 82% to 77.9% (at 37.5% of full load), and then, increases back to 81.7%, similar to the efficiency curve in [6]. Fig. 24 shows the close-loop efficiency with different input voltages. The converter efficiency maintains above 79.5% within the input range of 16∼21 V. When the input voltage is lower or higher than 18 V, the resonant converter cannot provide good ZVS achievement for the MOSFETs. Besides, the drive loss of the SR increases with the increase of the input voltage owing to the self-driven scheme.

Two additional prototypes rectified by the SR with the conventional RGD and the diodes were built, respectively. For fair comparison, other parameters in the power stage are the same. Two Schottky diodes (PMEG4020ER, 40 V/2 A, NXP) are used in parallel. Since $R_{\rm DS(on)}$ with the RGD varies all the time during one switching cycle and the switching period is only 100 ns, it is difficult to measure $R_{\rm DS(on)}$ directly. However, the conduction loss reduction owing to the reduction of $R_{\rm DS(on)}$ was verified by the temperature rise reduction and the efficiency improvement.

TABLE V
COMPARISON AMONG THE RGD APPLICATIONS IN MEGAHERTZ RESONANT CONVERTERS

RGD applications	V_{IN} (V)	V_O (V)	P_O (W)	Isolation	Device	f_s (MHz)	Efficiency
Trapezoidal self-oscillating RGD for boost [3]	14.4	32.4	23	×	RF LDMOSFET	110	87%
Multistage RGD for boost [3]	14.4	32	17	×	LDMOSFET (hand optimized)	50	78.5%
Multistage RGD for boost [20]	12	33	12	×	LDMOSFET (computer optimized)	50	88%
Resonant second harmonic class-E gate driver [13]	160–200	33	200	×	RF MOSFET	30	83.6%
LC voltage-controlled oscillator gate driver [15]	6	15	5	×	RF LDMOSFET	60	77%
Multistage RGD for SEPIC [5] (two in parallel)	3.6–7.2	7	3	×	Si MOSFET	20	82.3%
Multistage RGD for SEPIC [6]	15	28	14	×	Si MOSFET	30	82.5%
Self-oscillating RGD for ctrl and SR FETs [12]	45	11.2	5	×	Si MOSFET	50	67%
Multistage RGD [7]	12	12	7	√	LDMOSFET (optimized)	75	74%
Two-channel multistage RGD for push–pull [23]	30–36	24	50	√	Si MOSFET	30	73.3%
Proposed RGD for the SR	16–21	5	10	√	Si MOSFET	10	82%

Fig. 25 gives the thermal imaging comparison at steady state under nature air cooling (taken by Ti300 from Fluke IR-Fusion Thermal Imager). The temperature of the SR with the conventional RGD is 61.4 °C while that of the SR with the proposed RGD is only 44 °C. The temperature rise is reduced from 32 °C to 16 °C (a reduction of 50%). With the ZVS achievement and the same thermal resistance, the loss of the SR with the proposed RGD is reduced by 50% compared to the conventional RGD, agreeing well with the loss evaluation. There is some temperature difference in the inverter stage (L_F and S_{ctrl}). It is caused by the slightly different parasitic parameters of the transformer.

Fig. 26 gives the loss breakdown comparison under the nominal condition. Owing to the reduction in the conduction loss, the total power loss of the converter with the proposed RGD is 1.89 W, a reduction of 0.23 W compared with the conventional RGD (2.12 W), and a reduction of 0.73 W compared to the diode rectification (2.62 W).

Fig. 27 gives the close-loop efficiency comparison. Compared to the SR with the conventional RGD and the rectifier diodes, the SR with the proposed RGD achieves significant efficiency improvement in wide load range. At full load of 2 A, the proposed RGD improves the efficiency from 80.2% using the conventional RGD to 82% (an improvement of 1.8%). Compared to the efficiency of 77.3% using the diode rectification, the efficiency improvement is 4.7% at full load.

Table V lists the specifications of megahertz resonant converters using RGDs in the previous literatures. The switching frequency and the power rating are in wide range. Most of the resonant converters above tens of megahertz focus on the nonisolated low output current applications, where the Schottky diodes are used as the rectifiers. The high-performance RF LDMOSFETs are commonly used owing to the low parasitic parameters. From Table V, it noted that these megahertz converters realize high efficiency, however, using expensive custom design LDMOSFETs, and moreover, the application is targeted to nonisolated condition. Compared to these nonisolation converters, the proposed solution is using the commercial low-cost Si power devices to achieve high efficiency of 82% under rated condition and realizes the isolation at the same time.

For the Si-based megahertz converters in the table, it should be pointed out that these converters are basically suitable to nonisolated applications. However, the converter development in this paper is from the evaluation project of the power module products from TI and Mornsun companies, which is a 5-V/2-A low-cost isolated power module [21], [22]. Although it is difficult to do fair comparison because of wide switching frequency range and power rating due to different applications, we achieved slightly better efficiency and isolation using the proposed RGD. Compared to the isolated resonant converters in [7] and [23], the converter efficiency is improved by over 8%.

VI. CONCLUSION

The forward recovery of the diodes causes poor performance and high conduction loss in the multimegahertz resonant converters. The challenge along with the SR is the precise and efficient drive of the SR FET. A simple and efficient self-driven RGD is proposed in this paper. A control stage comprised of a shutdown branch and an auxiliary switch is introduced to the RGD to block the circulating current and the low-impedance path in the drive circuit so that the gate voltage can achieve fast shutdown and buildup under ON–OFF operation to ensure fast transient response. Moreover, the proposed RGD generates a tunable dc bias to increase the peak gate voltage and extend the conduction time with the optimal $R_{\mathrm{DS(on)}}$ so that the average $R_{\mathrm{DS(on)}}$ and the associated conduction loss in the SR FET can be reduced. It also provides precise switching timing for the SR to minimize the body diode conduction loss. A 10-MHz prototype was built with 18-V input and 5-V/2-A output. At full load of 2 A, the SR with the proposed RGD improves the converter efficiency from 80.2% using the conventional RGD to 82% (an improvement of 1.8%), and the temperature rise of the SR FET is reduced from 32 to 16 °C (a reduction of 50%). Compared to the efficiency of 77.3% using the diode rectification, the efficiency improvement is 4.7% at full load.

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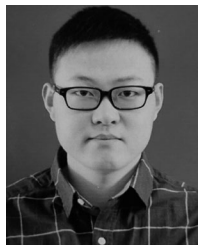
Xiaoyong Ren (S'04–M'11) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2002, 2005, and 2008, respectively.

From 2009 to 2011, he was a Postdoctoral Researcher at the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. He is currently with the Department of Electrical Engineering, NUAA. He has authored and coauthored more than ten technical papers published in international journals and conference proceedings. His current research interests include dc–dc conversion, converter control techniques, GaN device application, and renewable power systems.

Yuan Zhou received the B.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2013, where she is currently working toward the M.S. degree at the Aero-Power Sci-tech Center.

Her research interests include high-frequency dc–dc power conversion.



Dong Wang received the B.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2011, where he is currently working toward the M.S. degree at the Aero-Power Sci-tech Center.

His research interests include battery management system and GaN device application.

Xuewen Zou received the B.S. degree in electrical information engineering from the Nanjing University of Posts and Telecommunications, Nanjing, China, in 2013. He is currently working toward the M.S. degree at the Aero-Power Sci-tech Center, Nanjing University of Aeronautics and Astronautics (NUAA).

His research interests include high-frequency power conversion.

Zhiliang Zhang (S'03–M'09–SM'14) received the B.Sc. and M.Sc. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2002 and 2005, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2009.

In June, 2009, he joined NUAA, where he is currently a Professor at the Aero-Power Sci-tech Center. His research interests include high-frequency power converters and renewable energy power conversion system. He worked as a Design Engineering Intern from June to September, 2007, at Burlington Design Center, VT, Linear Technology Corporation.

Prof. Zhang was a Winner of "United Technologies Corporation Rong Hong Endowment" in 1999. He serves as the Secretary of the PELS Technical Committee on Power and Control Core Technologies since 2013.