Z-Source Matrix Converter: An Overview

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***Abstract*—Conventional matrix converters (MCs) have limited voltage gain that is less than 0.866, whether for direct MC (DMC) or indirect MC (IMC). The Z-source MCs (ZSMCs) overcome the voltage gain limitation of the traditional MC and achieve buck and boost operation with reduced switches count, thereby achieving low cost, high efficiency, and reliability, compared to the back-to-back converter. Furthermore, it will leads to more MC industrial applications. This paper presents an up-to-date comprehensive overview of the different ZSMC topologies and their configurations, circuit analyses, modulation schemes, and applications. This study offers a comprehensive and systematic reference for the future development of the ZSMCs.**

***Index Terms*—Quasi-Z-source (QZS) converter, Z-source (ZS) converter, ZS direct MC (ZSDMC), ZS indirect matrix converter (MC).**

I. Introduction

THERE are two types of ac–ac conversion systems, the traditional ac–dc–ac converter and the matrix converter (MC). The traditional ac–dc–ac converter consists of a pulsewidth modulation (PWM) boost rectifier and a PWM inverter with dc link. A bulky dc-link capacitor and a heavy input filter inductors may lead to high cost, large size, heavy weight, low reliability, and also high losses [1], [2].

The MC directly connects the ac source to the load without any dc-link capacitor. It presents many desirable characteristics: 1) simple and compact power circuit without a dc-link capacitor; 2) output voltages with variable amplitude and variable frequency; 3) sinusoidal input/output currents; and 4) operation with a unity power factor in the input side. The MCs can be divided into two categories: the direct MC (DMC) and the indirect MC (IMC), as shown in Fig. 1. The DMC performs the voltage and current conversion in one stage (direct) power conversion, while the IMC features a two-stage (indirect) power conversion. Both of them have the same behavior, but the latter has simpler commutation stress than the former. The DMC and IMC circuit topologies are equivalent in their basic functionality. The difference in the categories results in a difference in loading of the semiconductors and a different commutation scheme. The IMC has a simpler commutation due to its two-stage structure. However, this is achieved at the expense of more series-connected power devices in the path of high current, which results in a higher semiconductor losses and typically a lower achievable efficiency compared with the DMC. However, the differences between the control performances of DMC and IMC are quite negligible in practice [3].

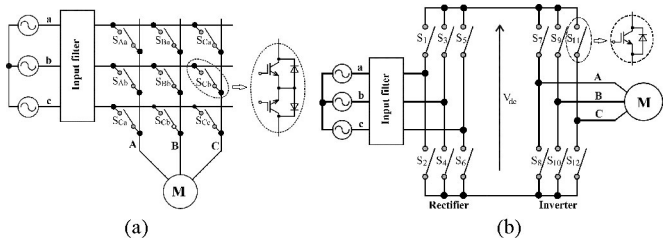

Fig. 1. AC/AC converter topologies: (a) direct and (b) indirect MC topologies.

For all these attractive properties the MC has not yet gained much attention in the industry due to its many unsolved problems. The most critical problem is the reduced voltage transfer ratio, which is defined as the ratio between the output voltage and the input voltage, and has been constrained to 0.866 when using a linear modulation [3]. A lots of research has been done on the overmodulation method to overcome the problem of low voltage transfer ratio. However, the overmodulation can only be achieved at the expense of the quality of both output voltage and input current [4]. Improving the voltage transfer ratio is an important research topic. One easy solution is to connect a transformer between the power supply and the MC. However, a mains transformer is bulky, expensive and it also affects the system efficiency. Another solution is to use a matrix-reactance frequency converter (MRFC), which consists of an MC and an ac chopper, and has a voltage transfer ratio larger than 1. The MRFC is categorized into two groups: the integrated matrix-reactance frequency converter (IMRFC) and the cascaded matrix-reactance frequency converter (CMRFC), as shown in Fig. 2. Unfortunately, the IMRFC topology has several disadvantages. First, the control algorithm is complicated due to the required synchronization between the MC and the AC chopper. Second, the voltage transfer ratio strongly depends on the circuit and the load parameters. Finally, the input power factor is lower than other MCs even for a purely resistive load. The CMRFC topology has less passive components compared by the IMRFC topology; however, it has limited voltage gain, also more complicated damping control of the input current and disturbed output current [5].

The Z-source (ZS) or quasi-Z-source (QZS) converter/inverter can achieve a high voltage gain in a single-stage power conversion due to its boost ability [6], [7], where the ZS/QZS network is inserted between the dc input source and inverter.

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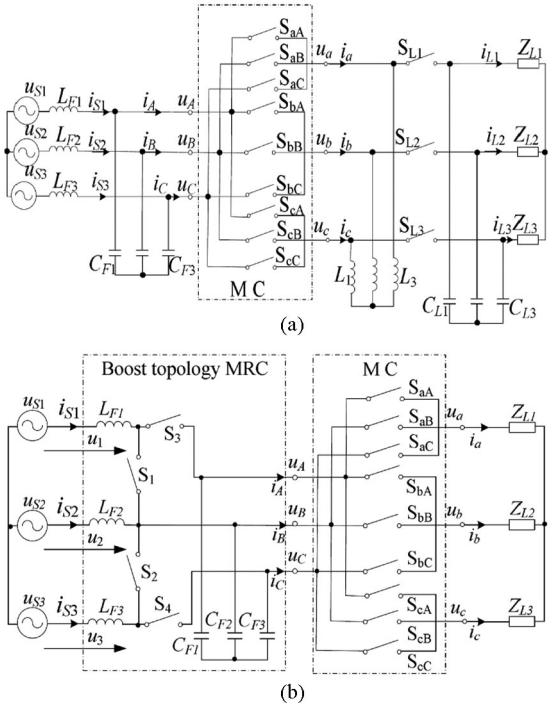

Fig. 2. (a) IMRFC and (b) CMRFC topologies [5].

By introducing the ZS/QZS network into different MC topologies, a novel MC topology called Z-source MC (ZSMC) has been proposed. According to the topology of the MC, they are called Z-source indirect MC (ZSIMC) and Z-source direct MC (ZSDMC). Therefore, it is possible to overcome the low-voltage-gain challenge of the traditional MC; in addition, the ZS/QZS network allows the short circuit, which makes the ZSMC commutation easier. As a result, the ZSMC provides a low-cost, reliable, and highly efficient structure for buck and boost ac/ac conversion. Moreover, there are two different configurations of the ZSIMC topology, depending on the location of the ZS/QZS network. The ZS/QZS network can be located between the rectifier and inverter of IMC at the intermediate dc link, the voltage gain is extended, but it is not all-silicon solution and will cause larger size and heavier weight (it requires large inductors and capacitors in the dc link) than the conventional IMC. The other option, where the ZS/QZS network is inserted between the input ac source and rectifier of the IMC to achieve all-silicon solution. This configuration can achieve high voltage gain with a small ZS/QZS network, but it requires a large number of switches, so it is at the result of higher cost.

This paper will present an updated overview of the different ZSMC topologies, including the ZSIMC with its all-silicon and not all-silicon configurations and also the ZSDMC.

II. ZSIMC (ALL-SILICON SOLUTION)

A. Different Topology Configurations

Fig. 3 shows the recently proposed ZS/QZSIMC topologies [8]–[11], which consists of five parts: three-phase ac source, ZS/QZS network, front-end rectifier, back-end inverter, and ac load. The ZS network includes three inductors

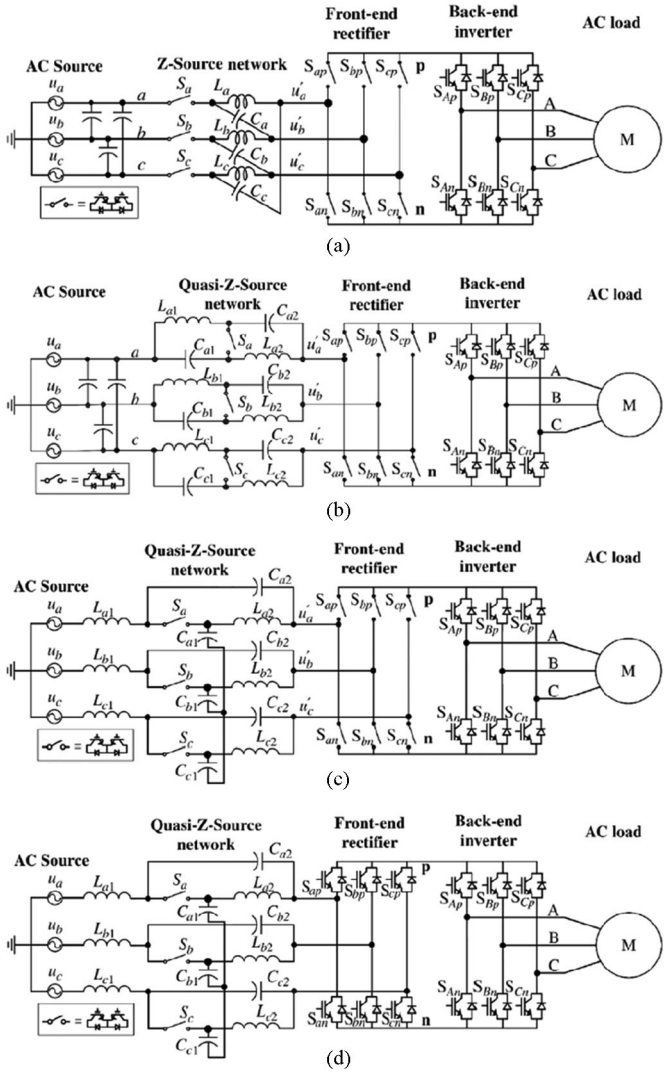

Fig. 3. Different ZSIMC topologies: (a) ZSIMC with discontinuous current mode [11]; (b) QZSIMC with discontinuous current mode [9]; (c) QZSIMC with continuous current mode [8]; (d) simplified QZSIMC [12].

(L_a, L_b, L_c), three capacitors (C_a, C_b, C_c), and three bidirectional switches (S_a, S_b, S_c). However, the QZS network includes six inductors ($L_{a1}, L_{a2}, L_{b1}, L_{b2}, L_{c1}, L_{c2}$), six capacitors ($C_{a1}, C_{a2}, C_{b1}, C_{b2}, C_{c1}, C_{c2}$), and three bidirectional switches (S_a, S_b, S_c). One gate signal S_x can be used to control these three switches because they have the same switching behavior. This unique ZS/QZS network allows the ZS/QZSIMC to work on buck and boost modes. The ZSIMC topology, as shown in Fig. 3(a), has only three inductors and three capacitors compared to the other QZSIMC topologies that have six inductors and six capacitors. However, the ZSIMC topology has a limited voltage boost ratio (voltage gain can only reach 1.15), inherited phase shift caused by the Z network, which makes the control inaccurate, and also discontinuous current in the front of the Z-source network, require additional input filters to reduce input current total harmonic distortion (THD), which may increase the whole system volume and cost and make efficiency reduction [8]. The discontinuous QZSIMC topology, as shown in Fig. 3(b), has been proposed in [9], by adding

TABLE I
COMPARISON OF THREE ZS/QZSIMC (ALL-SILICON SOLUTION) AC/AC CONVERTER TOPOLOGIES [11]

	ZSIMC	Discontinuous QZSIM	Continuous QZSIM
Additional input filter	Yes	Yes	No
Voltage gain	Low	High	High
Current ripples	High	Low	Low
Voltage ripples	Low	High	Middle
Inductor current stress	Low	High	Middle
Capacitor voltage stress	Middle	Low	High
Switch current stress	Low	High	High
Switch voltage stress	Low	Low	High
Input current THD	Middle	High	Low
Output voltage THD	High	Middle	Low
Efficiency	High	Low	High

three more inductors and three more capacitors compared to the ZSIMC topology; however, the voltage gain can go to four to five times or even higher, depending on the voltage rating of the switches. Furthermore, there is no phase shift due to the QZS network. But, it still require additional input filters. The continuous QZSIMC topology, as shown in Fig. 3(c), has been proposed in [8]. The continuous QZSIMC topology does not require input filters, because the QZS network is integrated with the *LC* filter. The three ZS/QZSIMC topologies, shown in Fig. 3, were compared in detail in terms of voltage gain, current ripple, voltage ripple, inductor current and capacitor voltage stresses, ZS/QZS switch current and voltage stresses, filtering function, input current THD, output voltage THD, and also efficiency [12]. Table I summarizes the evaluation of three ZS/QZSMC topologies.

Furthermore, in [10], common-mode voltage (CMV) issue of the QZSIMC with continuous current mode has been investigated and three modulation strategies were developed in order to reduce the CMV for the QZSIMC with the CMV peak value reduction of 42%.

The simplified QZSIMC, which has been proposed in [12], as shown in Fig. 3(d), by modifying the topology shown in Fig. 3(c). This topology requires less power switches, only 12 switches to reduce the system cost, rather than 18 switches, which is the same to back-to-back converter without a dc-link capacitor. The QZS network integrates the *LC* filtering function in order to avoid additional input filter. The simplified QZSIMC has a performance limitation that input current will have high harmonics if no input current closed-loop compensation is used. Therefore, the input current closed-loop control is necessary in order to lower the harmonics of input current.

B. Operating Principle and Equivalent Circuits

Fig. 4 shows the equivalent circuit of the QZSIMC topology with continuous input current at the shoot-through (ST) and non-shoot-through (NST) states. During the NST state, the switches $S_x (x = a, b, c)$ are on ($S = 1$) as shown in Fig. 4(a), the inductors discharge the capacitors, each output phase voltage of QZS network is the sum of two capacitor voltages. On the other hand, during the ST state, switches S_x are off ($S = 0$) as

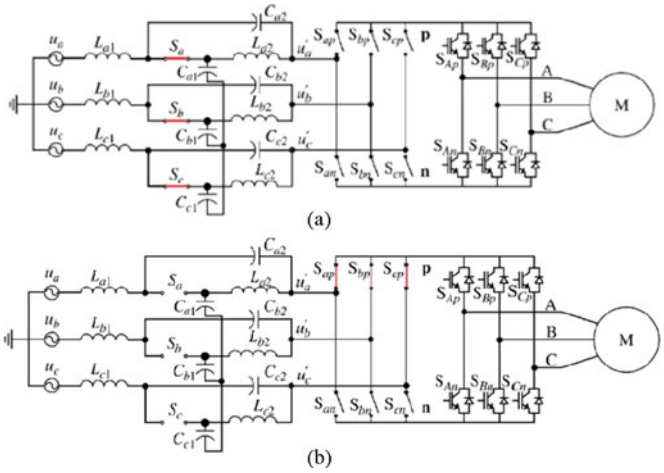

Fig. 4. Equivalent circuit of the QZS-IMC: (a) non-ST state and (b) ST state.

shown in Fig. 4(b), the input side of front-end rectifier is short circuited, and the inductors are charged.

During the NST state, from Fig. 4(a), the following voltage and current equations can be obtained:

$$\begin{bmatrix} u_{Ca2} \\ u_{Cb2} \\ u_{Cc2} \end{bmatrix} = -\begin{bmatrix} u_{La2} \\ u_{Lb2} \\ u_{Lc2} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} u_{La2} \\ u_{Lb2} \\ u_{Lc2} \end{bmatrix} = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} - \begin{bmatrix} u_{Ca1} \\ u_{Cb1} \\ u_{Cc1} \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} u_{La2} \\ u_{Lb2} \\ u_{Lc2} \end{bmatrix} = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} + \begin{bmatrix} u_{Ca2} \\ u_{Cb2} \\ u_{Cc2} \end{bmatrix} - \begin{bmatrix} u'_a \\ u'_b \\ u'_c \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} i_{La1} \\ i_{Lb1} \\ i_{Lc1} \end{bmatrix} - \begin{bmatrix} i_{La2} \\ i_{Lb2} \\ i_{Lc2} \end{bmatrix} = \begin{bmatrix} i_{Ca1} \\ i_{Cb1} \\ i_{Cc1} \end{bmatrix} - \begin{bmatrix} i_{Ca2} \\ i_{Cb2} \\ i_{Cc2} \end{bmatrix}. \tag{4}$$

During the ST state, from Fig. 4(b), the following voltage and current equations can be obtained:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} + \begin{bmatrix} u_{Ca2} \\ u_{Cb2} \\ u_{Cc2} \end{bmatrix} = \begin{bmatrix} u_{La1} \\ u_{Lb1} \\ u_{Lc1} \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} u_{Ca1} \\ u_{Cb1} \\ u_{Cc1} \end{bmatrix} = \begin{bmatrix} u_{La2} \\ u_{Lb2} \\ u_{Lc2} \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} i_{La1} \\ i_{Lb1} \\ i_{Lc1} \end{bmatrix} = -\begin{bmatrix} i_{Ca2} \\ i_{Cb2} \\ i_{Cc2} \end{bmatrix}, \begin{bmatrix} i_{La2} \\ i_{Lb2} \\ i_{Lc2} \end{bmatrix} = -\begin{bmatrix} i_{Ca1} \\ i_{Cb1} \\ i_{Cc1} \end{bmatrix} \tag{7}$$

where u denotes the voltage and i denotes the current and the subscripts C_{x1} and C_{x2} are the capacitors 1 and 2 of phase x; L_{x1} and L_{x2} for the inductors 1 and 2 of phase x, for $x = a, b,$ and c.

For one switching cycle T_s, if the time interval of ST state is T, the ST duty cycle is defined as $D = T_0/T_s$. The inductor average voltages and the capacitor average currents should be zero over one switching period in steady state. From (1) to (7),

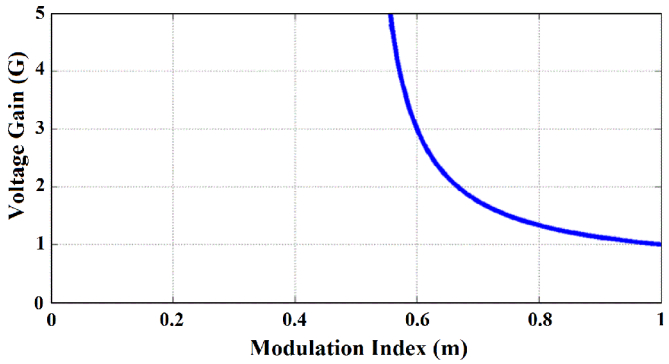

Fig. 5. Voltage gain versus modulation index of the QZSIMC.

it is possible to obtain

$$\begin{bmatrix} i_{La1} \\ i_{Lb1} \\ i_{Lc1} \end{bmatrix} = \begin{bmatrix} i_{La2} \\ i_{Lb2} \\ i_{Lc2} \end{bmatrix} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} u_{Ca2} \\ u_{Cb2} \\ u_{Cc2} \end{bmatrix} = \frac{D}{1-D} \begin{bmatrix} u_{Ca1} \\ u_{Cb1} \\ u_{Cc1} \end{bmatrix} \tag{9}$$

$$\begin{bmatrix} u_{Ca1} \\ u_{Cb1} \\ u_{Cc1} \end{bmatrix} = \frac{1-D}{1-2D} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}. \tag{10}$$

Combining (3) and (10), the following equations can be obtained:

$$\begin{bmatrix} u'_a \\ u'_b \\ u'_c \end{bmatrix} = \frac{1-D}{1-2D} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}. \tag{11}$$

The voltage boost factor *B* is expressed as

$$B = \frac{u_o}{u_i} = \frac{1}{1-2D} \tag{12}$$

where u_i is the amplitude of input voltage source and u_o is the output voltage amplitude of the QZS network. The voltage gain *G* of the proposed QZSIMC will be

$$G = Bm \tag{13}$$

where $m = m_i m_o$ is the modulation index of the IMC, m_i is the modulation index of the front-end rectifier, and m_o is the modulation index of the back-end inverter. Fig. 5 shows the voltage gain versus the modulation index of the QZSIMC. The voltage gain can be greater than 1 through choosing the modulation index and ST duty cycle ($D < 0.5$), which is boost mode. Of course, the buck mode can be achieved through using lower modulation index.

C. Modulation

The IMC consists of a front-end rectifier and a back-end inverter. The input-current space vector modulation (SVM) controls the front-end rectifier to achieve controllable input power factor, and the output-voltage SVM controls the back-end inverter to modulate three-phase output voltage [13]. The rectifier

TABLE II
INPUT CURRENT VECTORS, SWITCHING COMBINATIONS, AND DC-LINK VOLTAGE FOR QZSIMC (ALL-SILICON SOLUTION)

N	U_{dc}	S_{ap}, S_{bp}, S_{cp}	S_{an}, S_{bn}, S_{cn}	Vector
1	u_{ac}	1 0 0	0 0 1	I_1 (active vector)
2	u_{bc}	0 1 0	0 0 1	I_2 (active vector)
3	$-u_{ab}$	0 1 0	1 0 0	I_3 (active vector)
4	$-u_{ac}$	0 0 1	1 0 0	I_4 (active vector)
5	$-u_{bc}$	0 0 1	0 1 0	I_5 (active vector)
6	u_{ab}	1 0 0	0 1 0	I_6 (active vector)
7	0	1 0 0	1 0 0	I_0 (zero vector)
8	0	0 1 0	0 1 0	I_0 (zero vector)
9	0	0 0 1	0 0 1	I_0 (zero vector)
10	0	1 1 1	0 0 0	I_d (ST vector)
11	0	0 0 0	1 1 1	I_d (ST vector)

stage of the QZSIMC shown in Fig. 4 has three operation states: active, zero, and ST states, as indicated in Table II. During the ST state, the three-phase ac power supply is short-circuited to achieve voltage boost. The SVM vector duty ratios are calculated by

$$\begin{aligned} d_\alpha &= m_i \sin\left(\frac{\pi}{3} - \theta_i\right) \\ d_\beta &= m_i \sin\theta_i \\ d_s &= \text{const}(d_s \le 1 - d_\alpha - d_\beta) \\ d_{0r} &= 1 - d_\alpha - d_\beta - d_s \end{aligned} \tag{14}$$

where m_i is the modulation index of the front-end rectifier; θ_i is the input current vector angle; $d_\alpha, d_\beta, d_s,$ and d_{0r} are the duty ratios of different current vectors in one switching period.

The back-end inverter is the same with conventional voltage-source inverter, which includes the six active vectors and two zero vectors, the duty ratios are calculated by

$$\begin{aligned} d_u &= m_o \sin\left(\frac{\pi}{3} - \theta_o\right) \\ d_v &= m_o \sin\theta_o \\ d_{0i} &= 1 - d_u - d_v \end{aligned} \tag{15}$$

where m_o is the modulation index of the back-end inverter; θ_o is the output voltage vector angle; and d_u, d_v, and d_{oi} are the duty ratios of output voltage active vector and zero vector, respectively.

To obtain an effective balance of the input currents and output voltages in the switching period, the modulation pattern should combine both the rectification and inversion switching states, and the switching sequence is shown in Fig. 6. The corresponding duty ratios can be calculated by

$$\begin{aligned} d_{u\alpha} &= d_u \cdot d_\alpha \\ d_{u\beta} &= d_u \cdot d_\beta \\ d_{v\alpha} &= d_v \cdot d_\alpha \\ d_{v\beta} &= d_v \cdot d_\beta \\ d_{oi\alpha} &= d_{oi} \cdot d_\alpha \\ d_{oi\beta} &= d_{oi} \cdot d_\beta \end{aligned} \tag{16}$$

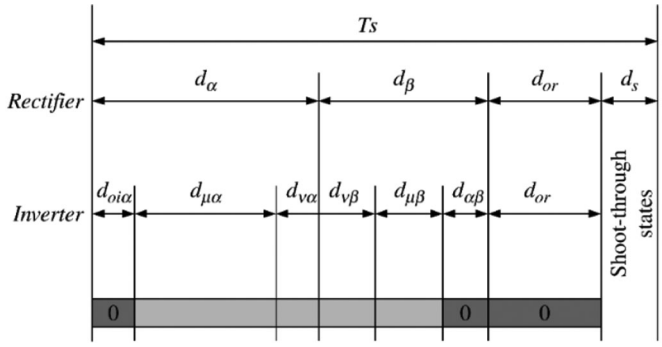

Fig. 6. Switching sequence for the QZSIMC (all-silicon solution).

where T_s is the switching period and $d_{u\alpha}, d_{u\beta}, d_{v\alpha}, d_{v\beta}, d_{oi\alpha}$, and $d_{oi\beta}$ are the duty ratios of different output voltage vectors in one switching period. As shown in Fig. 6, while the front-end rectifier stage is in commutation, the inverter works on zero vector, which indicates that the dc-link current is zero during commutation. Hence, zero-current switching is guaranteed on the rectifier stage during commutation, which simplifies the commutating process even though it is very complicated for conventional MCs.

D. Parameter Design of the QZS Network

The QZS inductor should limit the high-frequency current ripple, and the QZS capacitor should limit high-frequency voltage ripple. From Fig. 4(a), the inductor $L_{x1}(x = a, b, c)$ voltage equals to the difference of the input voltage and the capacitor C_{x1} voltage, the inductor L_{x2} voltage equals to the capacitor C_{x2} voltage, at the NST state, it is possible to obtain [10]

$$\begin{cases} L_{x1} = \dfrac{|u_i - u_{Cx1}|\,(1-D)T_s}{\Delta i_i} \\ L_{x2} = \dfrac{|u_{Cx2}|\,(1-D)T_s}{\Delta i_{L_{x2}}} \end{cases}. \tag{17}$$

If $\Delta i_i = r_L I_s$ and $\Delta i_{L_{x2}} = r_L I_{L_{x2}}$, respectively, the following equations can be obtained:

$$\begin{cases} L_{x1} \geq \dfrac{\left|u_{i_{\max}} - u_{C_{x1\max}}\right|(1-D)T_s}{r_L I_s} = \dfrac{\sqrt{2}V_s D(1-D)T_s}{(1-2D)r_L I_s} \\ L_{x2} \geq \dfrac{\left|u_{C_{x2\max}}\right|(1-D)T_s}{r_L I_{L_{x2}}} = \dfrac{\sqrt{2}V_s D(1-D)T_s}{(1-2D)r_L I_{L_{x2}}} \end{cases} \tag{18}$$

where $I_s, I_{L_{x2}}$, and V_s are the RMS values of input current, inductor L_{x2} current, and input voltage, respectively; r_L is the designed ripple coefficient of inductor currents.

During the ST state, as shown in Fig. 4(b), the capacitor C_{x1} current equals to the inductor L_{x2} current, the capacitor C_{x2} current equals to the input current, and it is possible to obtain [10]

$$\begin{cases} C_{x1} = \dfrac{i_{L_{x2}} DT_s}{\Delta u_{C_{x1}}} \\ C_{x2} = \dfrac{i_i DT_s}{\Delta u_{C_{x2}}} \end{cases}. \tag{19}$$

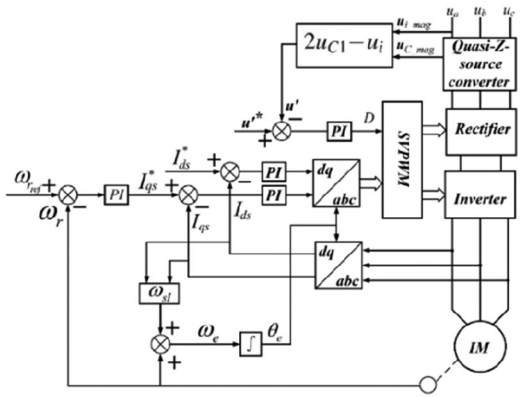

Fig. 7. Block diagram of a vector control-based QZSIMC-fed IM drive system [8].

If $\Delta u_{C_{x1}} = r_C u_{C_{x1}}$ and $\Delta u_{C_{x2}} = r_C u_{C_{x2}}$, respectively, the following equations can be obtained:

$$\begin{cases} C_{x1} \geq \dfrac{i_{L_{x2\max}} DT_s}{\Delta u_{C_{x1}}} = \dfrac{\sqrt{2}I_s D(1-2D)T_s}{(1-D)r_C V_s} \\ C_{x2} \geq \dfrac{i_{i_{\max}} DT_s}{\Delta u_{C_{x2}}} = \dfrac{\sqrt{2}I_s(1-2D)T_s}{r_C V_s} \end{cases} \tag{20}$$

Where $u_{C_{x1}}$ and $u_{C_{x2}}$ are the RMS values of the capacitor C_{x1} and capacitor C_{x2}, respectively; r_C is the designed ripple coefficient of the capacitor voltages and I_s is the RMS values of input current.

E. QZSIMC (All-Silicon Solution) Applications

To demonstrate the application of an all-silicon solution QZSIMC, Fig. 7 shows a vector-control-based QZSIMC fed a 4-kW IM drive system. The q-axis component reference i_{qs}^* of the stator current is the output of the speed closed-loop through a PI controller. The d-axis component reference i_{ds}^* of the stator current is constant, which is equal to the excitation current of the IM. The d-axis and q-axis current component closed loops will ensure an error-free tracking [8].

III. ZSIMC (Not All-Silicon Solution)

A. Topology Different Configurations

A second family of ac–ac Z-source converter based on the IMC has been proposed in [14] and is shown in Fig. 8. Only additional passive components are required without any increase in the number of power semiconductor switches, which can increase the complexity of control algorithm. The main purpose of the proposed topology is to boost the average dc-link voltage in order to provide higher load voltage when required. In Fig. 8(a), the switches in the rectification stage are implemented using four-quadrant switches, and the switches in the inversion stage are implemented with an IGBT and an antiparallel diode. The inductors (L_1, L_2) and capacitors (C_1, C_2) make up a symmetrical Z-source network. Furthermore, two simplified ac–ac Z-source converter topologies are presented in Fig. 8(b) and (c), which are based on the sparse and ultrasparse MC topologies, respectively. Also, in [15]–[17], an additional power switch (S_1)

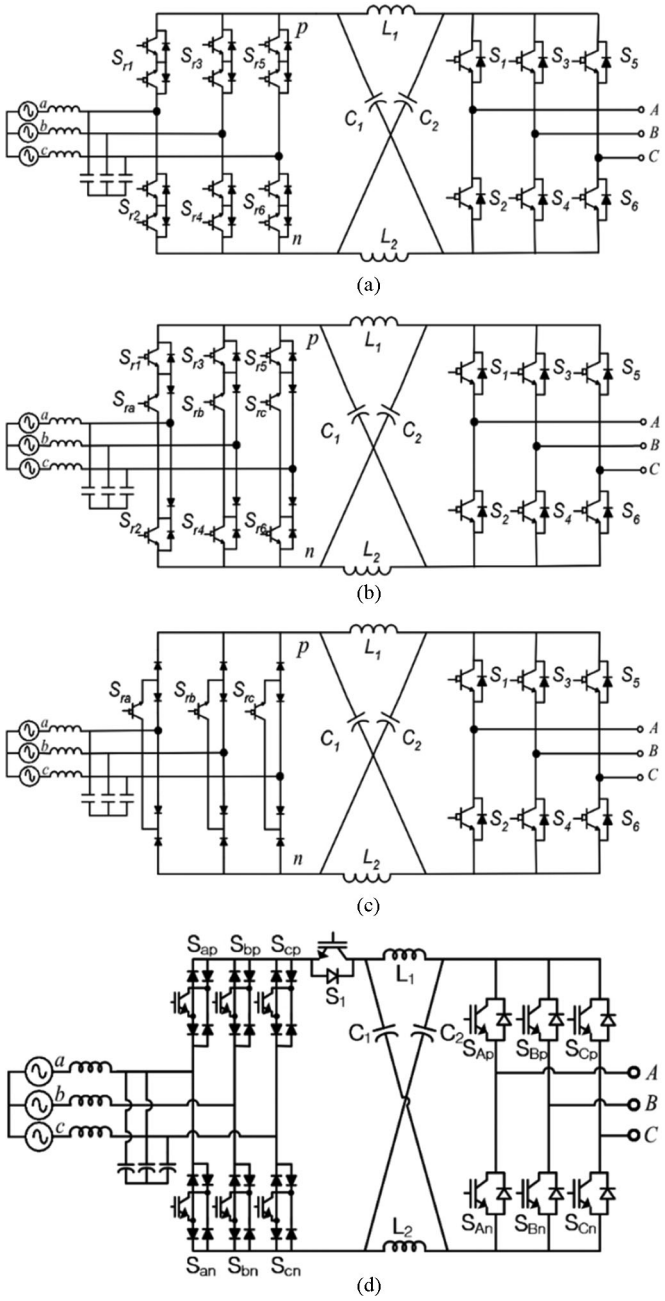

Fig. 8. Different ZSIMC topologies: (a) ZSIMC; (b) Z-source sparse MC; (c) Z-source ultrasparse MC; and (d) bidirectional Z-source sparse MC.

is inserted in the dc link before the Z-source network to ensure the bidirectional power flow, as shown in Fig. 8(d). During operating in a normal motoring mode, the dc-link current can flow through the integrated antiparallel diode of the IGBT and feed the load through the Z-source inverter. On the other hand, during operation in the power regenerative braking mode, the current can flow from the collector to the emitter of the IGBT and feed back to the grid.

In [19] and [20], a three-phase/three-phase ultrasparse MC utilizing a series Z-source, quasi-Z-source, and switched inductor Z-source networks has been proposed, as shown in Fig. 9. Series Z-source, quasi-Z-source, or switched inductor Z-source

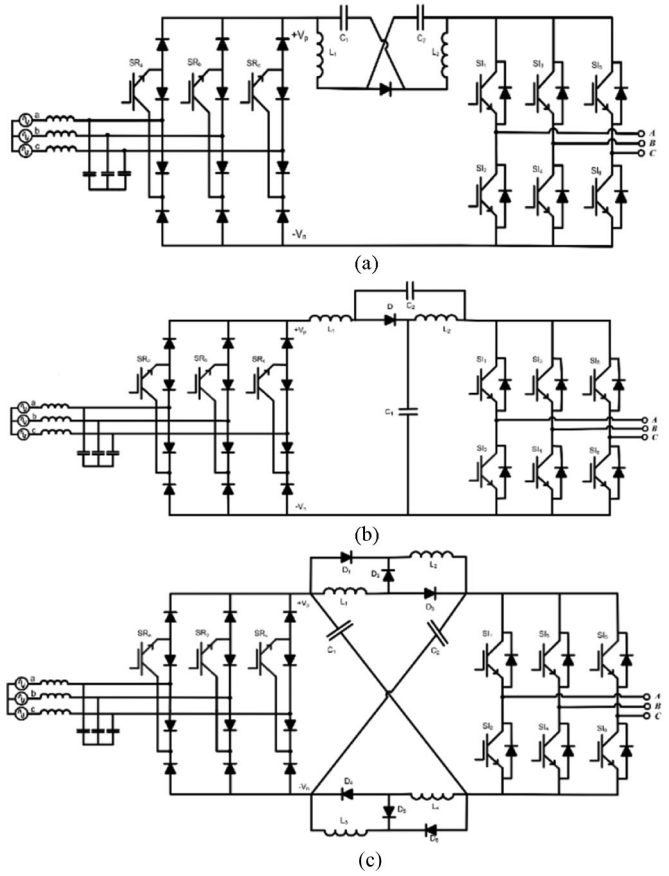

Fig. 9. (a) Series ZSMC, (b) quasi-Z-source MC, and (c) switched-inductor ZSMC topologies.

network is inserted in either rail of the IMC. These converters constitute an improvement over the cascaded ZSMC by reducing the voltage across the Z-source network's capacitor, limiting the inrush current at startup for series Z-source and widening the boost ratio for quasi-Z-source and very high boost ratio for switched inductor ZSMC. The FFT analysis of these converters input/output currents can be carried out [21], [22], indicating a slight superiority of the switched inductor ZSMC over the quasi-Z-source converter and the series Z-source MC over the cascaded Z-source converter with respect to the quality of input currents.

An extension to the existing three-level IMC by inserting a Z-source impedance network between the front-end current-source rectifier (CSR) and rear-end neutral point clamped (NPC) VSI, can obtain buck–boost ac–ac conversion capability, has been proposed in [23] and [24]. The split-dc capacitors used in conventional NPC converter is eliminated and replaced by the filtering capacitors of the front-end CSR. Fig. 10(a) shows the bidirectional topology of the three-level ZSIMC, while Fig. 10(b) shows the unidirectional version.

The Z-source and switched-inductor Z-source networks have been combined with the supersparse MC topology in [25] in order to create a novel three-phase to single-phase MCs (SPMCs), the ZSMC and SIZSMC, with voltage-boosting capability and a unity power factor, as shown in Fig. 11. These converters are suitable for all applications with unidirectional power flow.

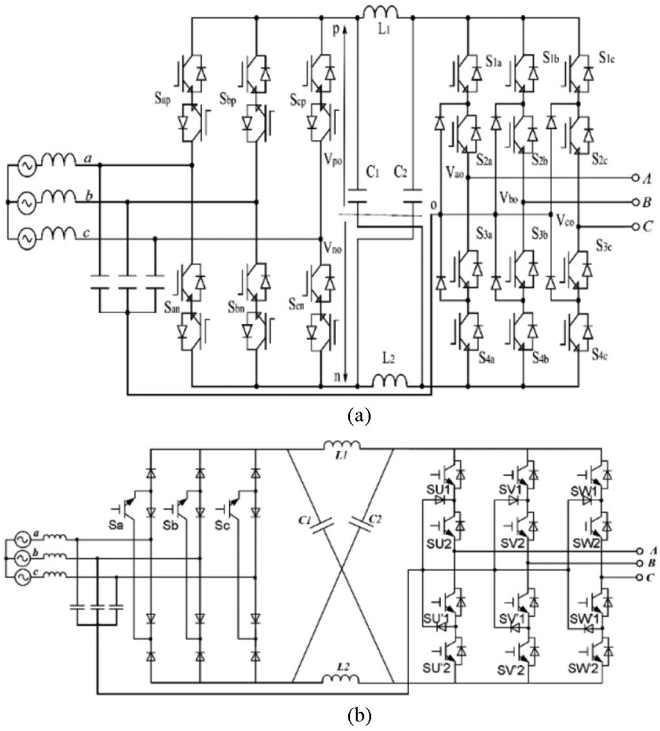

Fig. 10. (a) Bidirectional three-level ZSIMC; (b) unidirectional three-level Z-source indirect sparse MC topologies.

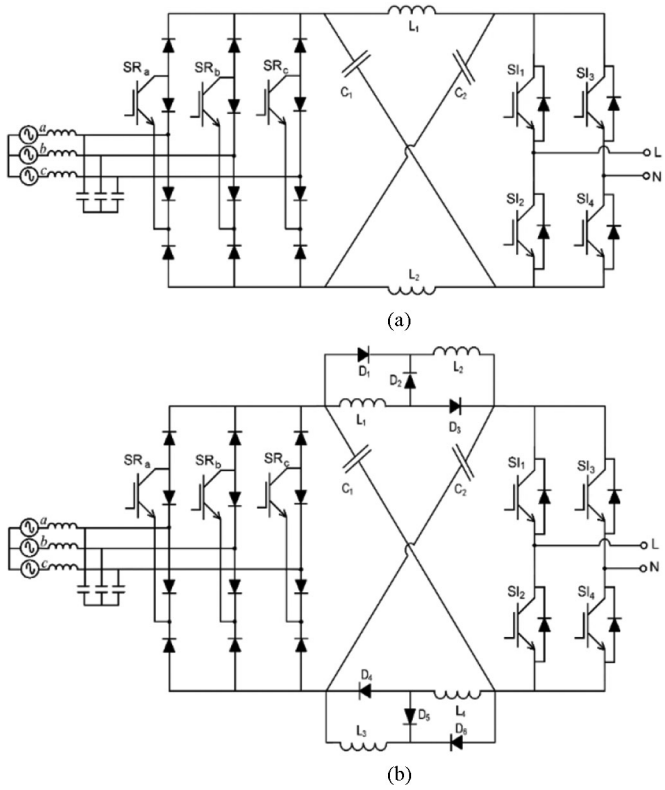

Fig. 11. Three-phase to single-phase super-sparse (a) ZSMC and (b) switched-inductor Z-source MC (SIZMC) topologies.

B. Operating Principle and Equivalent Circuits

Fig. 12 shows the modes of operation of the QZSMC, shown in Fig. 8(a), under the NST and ST conditions. Fig. 12(a) shows situation when diode *D* is on. Capacitors C_1 and C_2 are simultaneously charged by the rectified input voltages. In Fig. 12(b), the converter is operating under the ST condition, boosting the output voltage. Now, the diode *D* is off.

During the NST state, from Fig. 12(a), one can get the following voltage and current equations [27]:

$$\begin{cases} C_1 \dfrac{du_{C1}}{dt} = i_{L1} - i_o, & C_2 \dfrac{du_{C2}}{dt} = i_{L2} - i_o \\ L_1 \dfrac{di_{L1}}{dt} = u_{\text{in}} - u_{C1}, & L_2 \dfrac{di_{L1}}{dt} = -u_{C2} \end{cases} \tag{21}$$

where i_{L1}, i_{L2}, and i_o denote the currents of two inductors and the dc-link bus, respectively, and u_{C1}, u_{C2}, and u_{in} denote the voltages across the two capacitors, and QZS network input voltage, here, u_{in} is the virtual dc-link voltage produced by the rectification state.

During the ST state, from Fig. 12(b), the following equations can be obtained [27]:

$$\begin{cases} C_1 \dfrac{du_{C1}}{dt} = -i_{L2}, & C_2 \dfrac{du_{C2}}{dt} = -i_{L1} \\ L_1 \dfrac{di_{L1}}{dt} = u_{\text{in}} + u_{C2}, & L_2 \dfrac{di_{L1}}{dt} = u_{C1} \end{cases} \tag{22}$$

For one switching cycle T_s, if the time interval of ST state is *T*, the ST duty cycle is defined as $D = T_0/T_s$. The inductor average voltages and the capacitor average currents should be zero over one switching period in steady state. From (18) and (19), it is possible to obtain

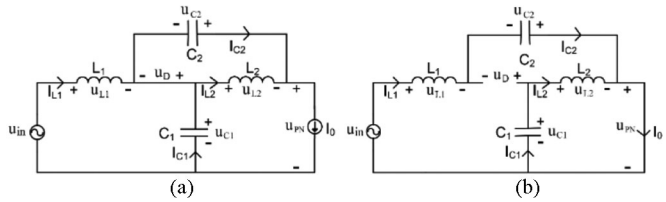

Fig. 12. Modes of operation of the quasi-Z-source MC: (a) non-ST state; (b) ST state.

$$\begin{cases} u_{C1} = \dfrac{1-D}{1-2D} u_{\text{in}} \\ u_{C2} = \dfrac{D}{1-2D} u_{\text{in}} \end{cases}. \tag{23}$$

The output voltage of the QZS network is

$$u_{PN} = u_{C1} + u_{C2} = \frac{1}{1-2D} u_{\text{in}}. \tag{24}$$

The voltage boost factor *B* is expressed as

$$B = \frac{u_{PN}}{u_{\text{in}}} = \frac{1}{1-2D}. \tag{25}$$

The voltage gain *G* of the QZSIMC shown in Fig. 8(a) will be calculated as

$$G = Bm \tag{26}$$

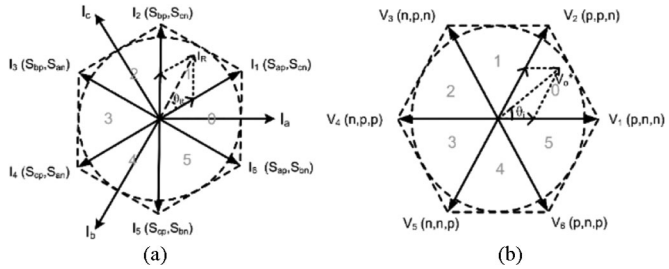

Fig. 13. (a) Front-end rectifier current space vectors; (b) back-end inverter voltage space vectors for the QZSIMC (not all-silicon solution).

where $m = m_i m_o$ is the modulation index of the IMC, m_i is the modulation index of the front-end rectifier, and m_o is the modulation index of the back-end inverter.

C. Modulation

Control of the QZSIMC shown in Fig. 8 is based on the combined space vector rectification (SVR) and space vector inversion (SVI) PWM techniques. Switches of the front-end rectifier are controlled using the SVR technique. Regarding the input-current vectors shown in Fig. 13(a), the reference current vector is synthesized from the adjacent vectors and a zero vector and their duty ratios are calculated from the classic formulas for space vector PWM as

$$\begin{aligned} d_\lambda &= m_o \sin\left(\frac{\pi}{3} - \theta_R\right) \\ d_\delta &= m_o \sin\theta_R \\ d_{0R} &= 1 - d_\lambda - d_\delta \end{aligned} \tag{27}$$

where θ_R denotes the local angle of the reference current, d_λ, d_δ and d_{0R} denote the duty ratios of the active and zero vectors, respectively.

The back-end inverter switches are controlled using the SVI technique. Fig. 13(b) shows the output-voltage vectors where symbols *p* and *n* refer to the upper and lower switches of the inverter. The back-end inverter utilizes 2 zero-voltage vectors, six active voltage vectors, and one ST state, which is forbidden in conventional MCs and inverters. Modulation of the active vectors decides the angular position of the averaged output voltage vector, while a zero vector is employed to adjust its magnitude. The ST state produces the voltage boost. The reference vector of output voltage is defined as

$$\vec{V}_o^* = V_{\text{out}} e^{j\omega_o t} \tag{28}$$

where V_{out} is the desired output line voltage and ω_o is the output radian frequency. Denoting the local angle of the reference voltage by θ_i, the duty ratios of the active vectors d_α, d_β and zero vectors d_{0i} are calculated as

$$\begin{aligned} d_\alpha &= m_v \sin\left(\frac{\pi}{3} - \theta_i\right) \\ d_\beta &= m_v \sin\theta_i \\ d_{ST} &= \begin{cases} \dfrac{B-1}{3B+1}, & \text{for SIZMC} \\ \dfrac{B-1}{2B}, & \text{for QZSM and SZMC} \end{cases} \\ d_{0i} &= 1 - d_\alpha - d_\beta - d_{ST} \end{aligned} \tag{29}$$

where m_v [0,1] is the voltage modulation index and *B* is the boost factor. Values of m_v and d_{ST} are dependent. If m_v is set close to 1, then the voltage gain approaches zero because of the limited zero vectors. The time-averaged power outputs from the three-switch rectifying stage and the inverter stage are equal. This allows combining the two modulation strategies. Assuming the input displacement angle of zero (unity power factor), the combined duty ratios are given by

$$\begin{aligned} d_{\lambda\alpha} &= d_\lambda \cdot d_\alpha = m_o m_v \sin(\pi/3 - \theta_R)\sin(\pi/3 - \theta_i) \\ d_{\lambda\beta} &= d_\lambda \cdot d_\beta = m_o m_v \sin(\pi/3 - \theta_R)\sin(\theta_i) \\ d_{\delta\alpha} &= d_\delta \cdot d_\alpha = m_o m_v \sin(\theta_R)\sin(\pi/3 - \theta_i) \\ d_{\delta\beta} &= d_\delta \cdot d_\beta = m_o m_v \sin(\theta_R)\sin(\theta_i) \end{aligned} \tag{30}$$

The switching ratios are then calculated as

$$\begin{bmatrix} T_{\lambda\alpha} \\ T_{\lambda\beta} \\ T_{\delta\alpha} \\ T_{\delta\beta} \end{bmatrix} = \frac{T_S}{2} \begin{bmatrix} d_{\lambda\alpha} \\ d_{\lambda\beta} \\ d_{\delta\alpha} \\ d_{\delta\beta} \end{bmatrix} \tag{31}$$

$$T_{ST} = T_S \cdot d_{ST}. \tag{32}$$

For minimum number of switching in a switching period, the combined duty ratios must be applied in the $T_{\lambda\alpha}, T_{\lambda\beta}, T_{\delta\beta}, T_{\delta\alpha}, T_{ST}, T_{\delta\alpha}, T_{\delta\beta}, T_{\lambda\beta}, T_{\lambda\alpha}$ sequence.

D. Parameter Design of the QZS Network

The QZS network capacitor value is selected according to the desired voltage ripple and the capacitor current. According to the equations [27]

$$u_L = L\frac{di_L}{dt}, \qquad i_C = C\frac{du_C}{dt}. \tag{33}$$

From (19), we get

$$\begin{aligned} \Delta u_{C1} &= \frac{i_{L2} D T_s}{C_1}, \quad \Delta u_{C2} = \frac{i_{L1} D T_s}{C_2}, \\ \Delta i_{L1} &= \frac{(u_{in} + u_{C2}) D T_s}{L_1}, \quad \Delta i_{L2} = \frac{u_{C1} D T_s}{L_2} \end{aligned} \tag{34}$$

where $\Delta u_C = r_C u_C$ and $\Delta i_L = r_L i_L$ are the peak values of the voltage and current ripples, respectively. Also, r_C is the capacitor voltage ripple ratio and r_L is the inductor current ripple ratio.

Using (20)–(22) and (25), we can get

$$\begin{aligned} C_1 &\geq \frac{PD(1-2D)T_s}{r_C(1-D)u_{\text{in}}^2}, \quad C_2 \geq \frac{P(1-2D)T_s}{r_C u_{\text{in}}^2}, \\ L_1 &= L_2 \geq \frac{u_{\text{in}}^2 (1-2D) D T_s}{P(1-D) r_L} \end{aligned} \tag{35}$$

where *P* is the input power of the system.

E. ZS/QZSIMC (Not All-Silicon Solution) Applications

The ZSIMC (not all-silicon solution) has been used as a part of a variable-speed drive system for a three-phase induction

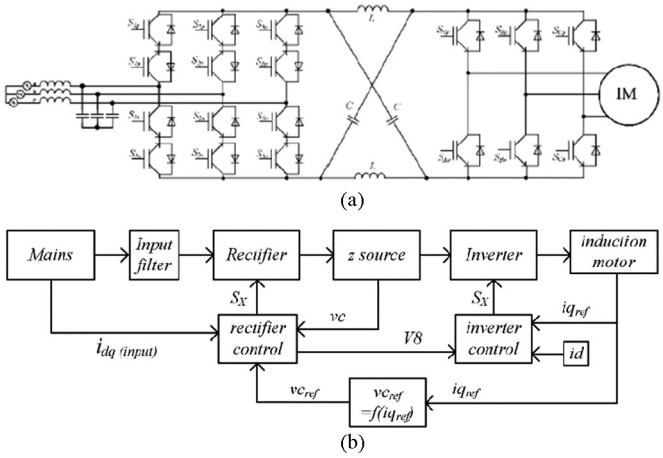

Fig. 14. ZSIMC-based IM drive system: (a) system topology and (b) control algorithm [26].

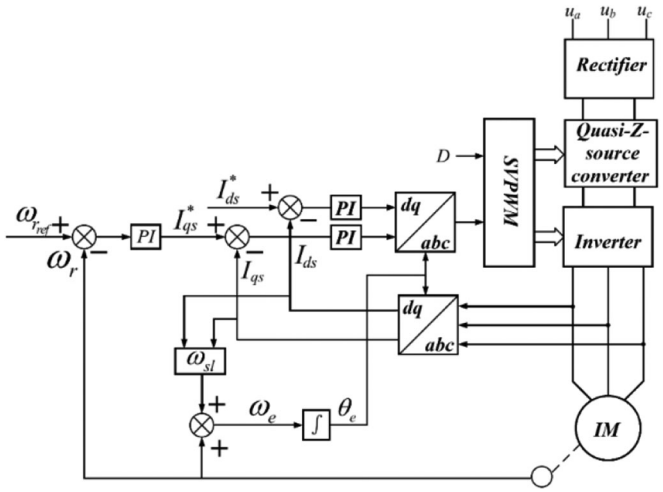

Fig. 15. Block diagram of the quasi-ZSIMC-based induction motor drive [27].

motor, as shown in Fig. 14. A new control method has been proposed to increase the operating voltage range of an IMC-based motor drive system, while at the same time guaranteeing unitary input power factor. The control was separated into two different stages, both depending on the dc-link Z-source capacitor voltage. The rectifier stage is controlled so that the current vectors impose phase and amplitude control, thus guaranteeing near unity power factor. On the other hand, on the inverter side, the inverter stage, along with a closed loop control of the ac three-phase induction motor currents, also enforces specific operation modes, providing the necessary stator voltage, and increasing the power flow from the mains to the load [26].

The quasi-ZSIMC (QZSIMC) has been applied for induction motor drive system, and the indirect field-oriented control has been used, as shown in Fig. 15 [27]. The indirect sparse-matrix topology with inductive–capacitive diode (LCD) networks, as shown in Fig. 16, has been used for gearless wind energy system [28]. The wind power captured by the turbine is converted by a PMSG and transmitted to the grid via an MC. The rectification stage of the converter regulates the power factor and draws sinusoidal currents from the PMSG. The LCD network

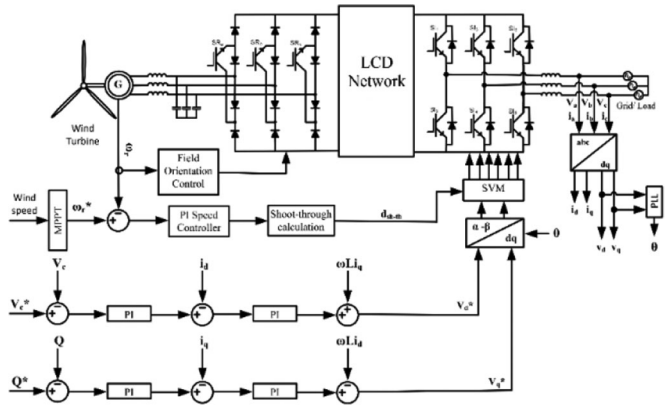

Fig. 16. Wind-energy system with PMSG, MC, and LCD network [28].

TABLE III
COMPARISON OF QZSIMC: ALL-SILICON SOLUTION AND NOT ALL-SILICON-SOLUTION TOPOLOGIES

	SZIMC (All-Silicon-Solution)	SZIMC (Not All-Silicon-Solution)
ZS/QZS network location	Between the input ac source and rectifier	Between the rectifier and inverter at the intermediate dc link
ZS/QZS network components	The ZS network composed of three inductors, three capacitors, and three bidirectional switches. The QZS network composed of six inductors, six capacitors, and three bidirectional switches.	Two inductors and two capacitors
Voltage gain	1.15 for ZS network. Four to five for QZS network.	Two to three times
Disadvantages	The power supply directly connected to the load without an intermediate dc bus will cause noise interference between both sides in each other. Too many components with complicated control.	The voltage across Z-source capacitors is larger than the input voltage. Larger capacitors, which increase the overall cost and volume. The inrush current and resonance in the Z-source network at startup.

and the inversion stage step up the voltage on the grid side. The generator-side control strategy is based on the principle of zero *d*-axis current control. The voltage-oriented control of the rectifier stage allows decoupling of the active and reactive input powers, and the required boost factor is maintained by adjusting the ST duty ratios of the inverter stage.

Table III presents a comparison between the two different configurations of the QZSIMC.

IV. Z-SOURCE DIRECT MC

A. Alternative Topology Configurations

By introducing the Z-source network to the conventional DMC, which has been proposed as a ZSDMC, as shown in Fig. 17 [29]–[33], it is possible to overcome the low voltage gain of the traditional DMC; in addition, the Z-source network allows the short circuit, which makes the ZSDMC commutation easier. The ZSDMC is derived from the traditional DMC by only adding three inductors, capacitors, switches and diodes. However, the ZSDMC has a limited voltage boost ratio (voltage gain can only reach 1.15), inherited a phase shift caused by the Z-source network, which makes the control inaccurate,

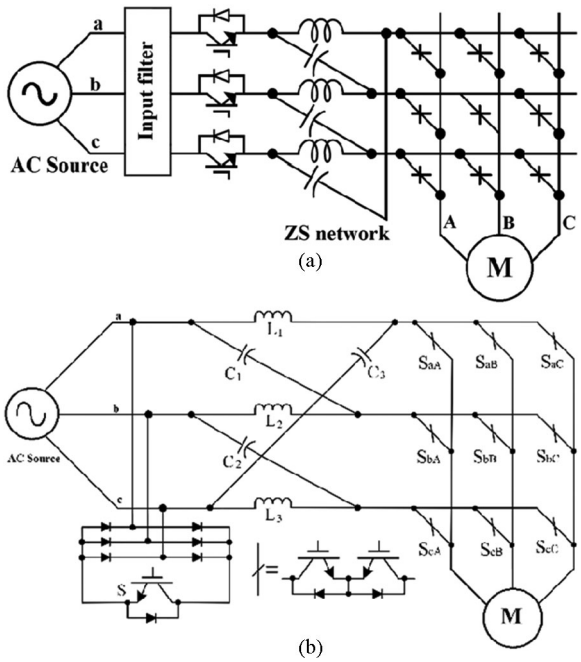

Fig. 17. Different ZSDMC topologies.

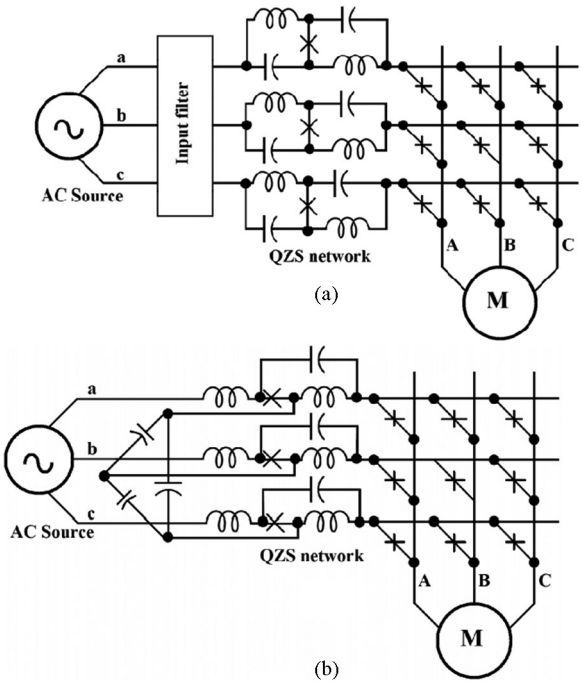

Fig. 18. Quasi-ZSDMC topologies with: (a) discontinuous input current and (b) continuous input current.

and also discontinuous current in the front of Z-source network. However, for the quasi-Z-Source DMC (QZSDMC), as shown in Fig. 18, the voltage gain can go to four to five times or even higher, depending on the voltage rating of the switches, no phase shift, which can cause less error in the control, and lower switch voltage and current stress [34]. In addition, the circuit in Fig. 18(b) has continuous input current [36].

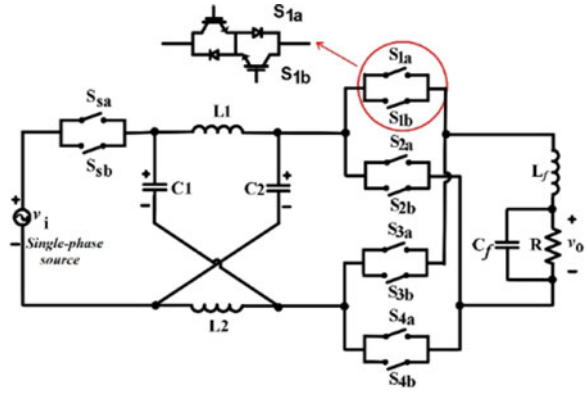

Fig. 19. Single-phase ZSMC topology [37].

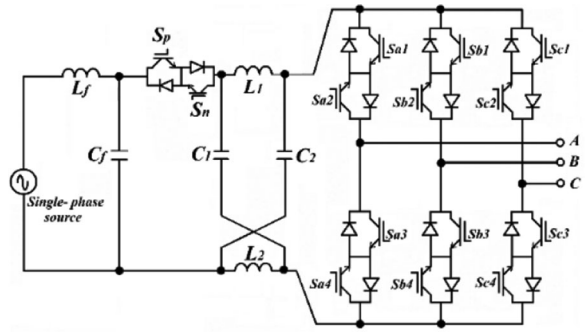

Fig. 20. Single- to three-phase ZSMC [40].

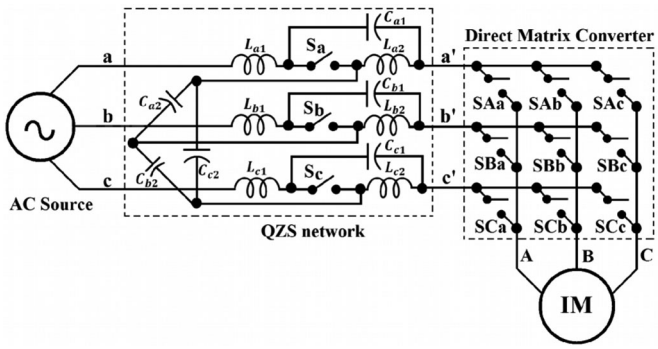

Fig. 21. Quasi-ZSDMC topology.

Compared to the traditional DMC, the ZSDMC and QZS-DMC both can boost the voltage higher than 0.866. The boost ratio depends on the duty cycle of the extra ST state. Also the QZSDMC topology can conduct less voltage/current stress on the switch and passive components, less input and output harmonics and higher power factor than the ZSDMC. Moreover, compared to ZSDMC topology, the QZSDMC is a component less, compact, high efficient, and also wide range voltage buck–boost MC [36].

In [37]–[39], a new family of single-phase ac/ac buck–boost converters based on SPMC and Z-network concept has been proposed, as shown in Fig. 19. The proposed single-phase ZSMC has the merits; the output voltage can be bucked-boosted and in-phase with the input voltage; the output voltage can also be bucked-boosted and out-of-phase with the input voltage.

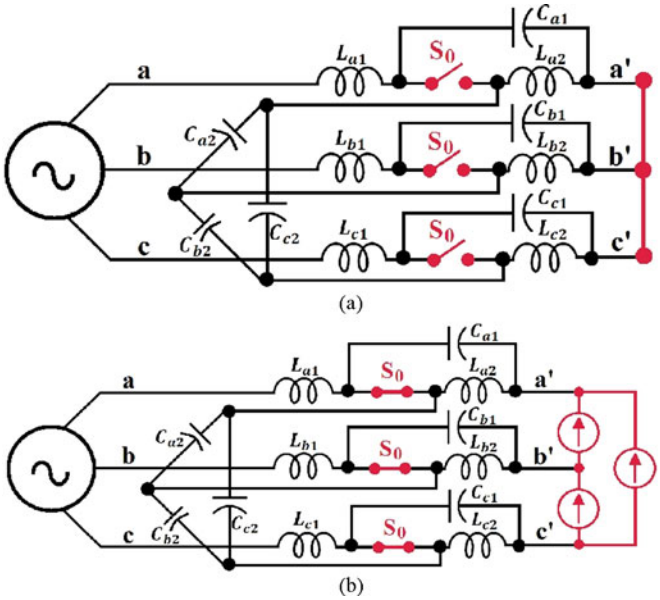

Fig. 22. Equivalent circuit of the QZSDMC: (a) ST state; (b) non-ST state.

In [39], a single-to three-phase ZSMC (STZMC) has been proposed by using the MC theory and Z-source conversion concept, as shown in Fig. 20. The STZMC converters can boost the amplitude of output voltage with the desired frequency. Furthermore, the limitations of single to three-phase MC, such as lower input–output voltage transfer ratio and unbalanced output currents has been improved.

B. Operating Principle and Equivalent Circuits

The main circuit configuration of the QZSDMC is shown in Fig. 21. It consists of two parts, namely, QZS network and DMC. The QZS network includes six inductors ($L_{a1}, L_{a2}, L_{b1}, L_{b2}, L_{c1}, L_{c2}$), six capacitors ($C_{a1}, C_{a2}, C_{b1}, C_{b2}, C_{c1}, C_{c2}$), and three additional bidirectional switches (S_a, S_b, S_c). One gate signal can be used to control these three switches because they have the same switching state. Therefore, the drive signal for S_a, S_b, and S_c can be denoted as S_0.

The operation principle of the QZSDMC can be divided into two switching states: ST and non-ST states. Fig. 22 shows the QZSDMC equivalent circuits during these states. During the ST state, Fig. 22(a), the switch S_0 is off and the output of the QZSDMC is shorted for boost operation. During the NST state, as shown in Fig. 22(b), the switch S_0 is on for normal DMC operation. Due to the symmetry of the system, inductors of QZS network ($L_{a1}, L_{a2}, L_{b1}, L_{b2}, L_{c1}, L_{c2}$) have the same inductance (L), and the capacitors ($C_{a1}, C_{a2}, C_{b1}, C_{b2}, C_{c1}, C_{c2}$) also have the same capacitance (C).

For one switching cycle, T_s, the time interval of the ST state is T_0, and the time interval of the NST state is T_1; hence, $T_s = T_0 + T_1$, and the ST duty ratio is $D = T_0/T_s$. From Fig. 22(a), during the ST state, one can get the following voltage equations:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{La1} \\ v_{Lb1} \\ v_{Lc1} \end{bmatrix} + \begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} - \begin{bmatrix} v_{Cb1} \\ v_{Cc1} \\ v_{Ca1} \end{bmatrix} - \begin{bmatrix} v_{Lb1} \\ v_{Lc1} \\ v_{La1} \end{bmatrix} \quad (36)$$

where v denotes the voltage and the subscripts C_{x1} and C_{x2} are the capacitors 1 and 2 of phase x and L_{x1} and L_{x2} for the inductors 1 and 2 of phase x, $x = a, b, c$. During the NST state, its equivalent circuit is shown in Fig. 22(b), and the following equation can be obtained:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{La1} \\ v_{Lb1} \\ v_{Lc1} \end{bmatrix} + \begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} + \begin{bmatrix} v_{a'b'} \\ v_{b'c'} \\ v_{c'a'} \end{bmatrix} - \begin{bmatrix} v_{Cb1} \\ v_{Cc1} \\ v_{Ca1} \end{bmatrix} - \begin{bmatrix} v_{Lb1} \\ v_{Lc1} \\ v_{La1} \end{bmatrix}. \quad (37)$$

In steady state, the average voltage of the inductors over one switching cycle should be zero, and owing to the symmetric voltages of the three-phase capacitors, it is possible to get [32]

$$\begin{bmatrix} v_{a'b'} \\ v_{b'c'} \\ v_{c'a'} \end{bmatrix} = \frac{1}{1-2D} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix}. \quad (38)$$

Defining B as the boost factor, and it is expressed as

$$B_{\mathrm{QZSDMC}} = \frac{v_o}{v_i} = \frac{1}{1-2D} \quad (39)$$

where v_{i} is the amplitude of input voltage source and v_o is the output voltage amplitude of the QZS network. The voltage gain G of the QZS network in the one switching cycle, is given by

$$G = Bm. \quad (40)$$

C. Modulation

The principle of applying the ST state for the QZSDMC is to replace some of the zero state by the ST state, in order not to affect the output voltage. By using the carrier-based PWM, the zero output voltage state in MC is corresponding to the switching state that all three output phases are connected to the same input phase. It happens when all three-phase output voltages are either higher or lower than the carrier signal. So the ST reference should be either higher than the maximum reference voltage or lower than the minimum reference voltage [34].

All the boost control methods that have been explored for the traditional Z-source converter, such as simple boost, maximum boost, maximum constant boost, and modified SVM [41], can be applied to the QZSDMC with a modification of the carrier envelope. Fig. 23 shows a simple boost PWM control strategy for the QZSDMC. The carrier waveform has the same envelope as the three-phase source voltages v_a, v_b, and v_c. The top envelope consists of the maximum voltage among the three input phase voltages, and the bottom envelope consists of the minimum voltage among them. During each switching period, the modified carrier signal is compared with the output voltage references v_A, v_B, and v_C to produce their PWM switching sequences (S_A, S_B, S_C). The ST pulses are generated by comparing the ST references with the modified carrier waveform, as shown in Fig. 23. The PWM switching sequences S_A, S_B, S_C should be distributed to nine ac switches in order to generate the expected PWM pulses. For this purpose, six additional logical signals are used, as shown in Fig. 24, where S_{x1}, S_{y1}, and S_{z1} denote the

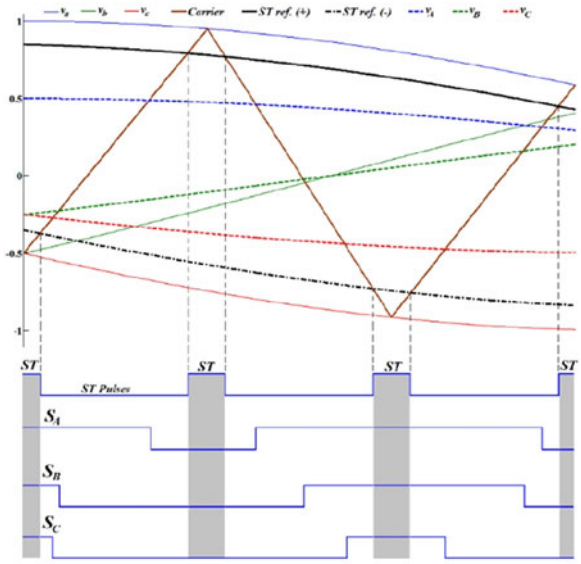

Fig. 23. QZSDMC switching states generation.

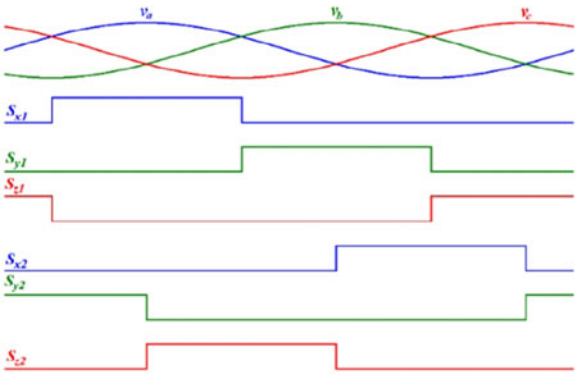

Fig. 24. Voltage envelope indicators.

indicators for their respective phase *a*, phase *b*, and phase *c* of the top voltage envelope. S_{x2}, S_{y2}, and S_{z2} denote the indicators for their respective phase *a*, phase *b*, and phase *c* of the bottom voltage envelope. These six voltage envelope indicators are combined with the three PWM switching sequences to generate nine switching signals according to the following logics:

$$\begin{aligned}
S_{Aa} &= S_{x1}S_A + S_{x2}\bar{S}_A \\
S_{Ab} &= S_{y1}S_A + S_{y2}\bar{S}_A \\
S_{Ac} &= S_{z1}S_A + S_{z2}\bar{S}_A \\
S_{Ba} &= S_{x1}S_B + S_{x2}\bar{S}_B \\
S_{Bb} &= S_{y1}S_B + S_{y2}\bar{S}_B \\
S_{Bc} &= S_{z1}S_B + S_{z2}\bar{S}_B \\
S_{Ca} &= S_{x1}S_C + S_{x2}\bar{S}_C \\
S_{Cb} &= S_{y1}S_C + S_{y2}\bar{S}_C \\
S_{Cc} &= S_{z1}S_C + S_{z2}\bar{S}_C.
\end{aligned} \tag{41}$$

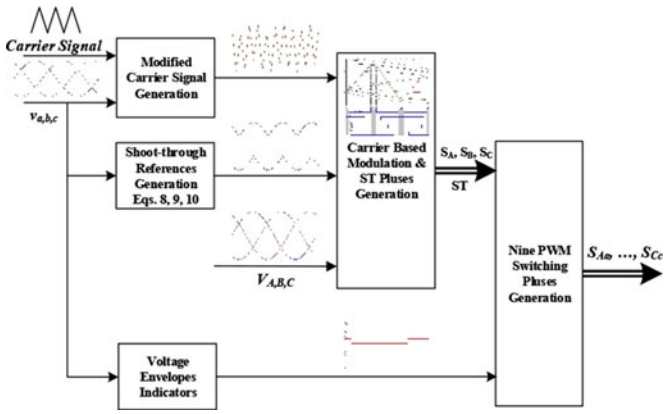

Fig. 25. Block diagram of QZSDMC PWM generation with ST insertion.

The aforementioned logical functions can be used to drive the QZSDMC after inserting the ST states.

A simple boost control is achieved through two ST references, in which both references are related to both envelopes by [32]

$$v_{st,r} = \frac{(y_{\max} - y_{\min})n + y_{\max} + y_{\min}}{2} \tag{42}$$

where *n* will determine the ST duty ratio, and its value has a limitation that the resultant minimum value of the top ST reference should be less than 0.5 p.u. and larger than *M*. Therefore, $1 \geq n \geq (1+4M)/3$ for the top ST reference, and its negative value is (*-n*) for the bottom ST reference. The modulation index should be less than 0.5, given that the output references v_A, v_B, and v_C can be any frequency with any phase angle and with no harmonic injection. $y_{\max}$ and $y_{\min}$ are the top and bottom envelopes of the source voltages, respectively. For the simple boost control, the ST interval from the top reference can be calculated as

$$T_0 = \frac{1-n}{2}T_c \tag{43}$$

where T_0 and T_c are the ST duration per switching cycle and switching time, respectively, and its ST duty ratio in half carrier cycle is

$$D_h = \frac{1-n}{2}. \tag{44}$$

Fig. 25 shows the complete process to generate the switching signals for the QZSDMC. First, the triangle carrier signal is modulated by the input reference signals v_a, v_b, and v_c to generate the modified carrier signal, which is bounded by the maximum and minimum envelopes of the input reference signals. Second, the ST references are generated from the input reference signals and the desired boost ratio using (33), (34), and (35). Then, the switching sequences S_A, S_B, S_C and ST pulses are generated by comparing the output voltage references v_A, v_B, and v_C and the ST references with the modified carrier signal. Furthermore, the voltage envelope indicators are generated from the input reference signals v_a, v_b, and v_c. For example, $S_{x1} = 1$ when phase *a* voltage is the largest value among the three-phase voltages and $S_{x2} = 1$ when phase *a* has the minimum voltage among the three-phase voltages. Finally, these six

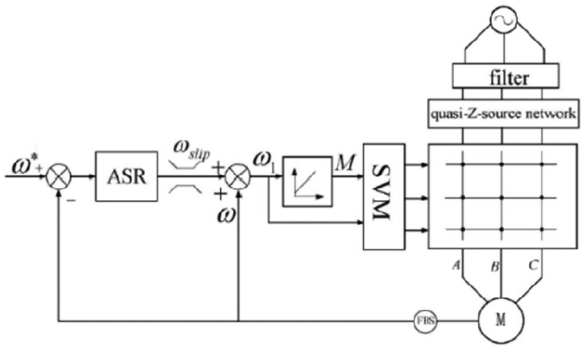

Fig. 26. Block diagram for a QZSDMC-based ASD system.

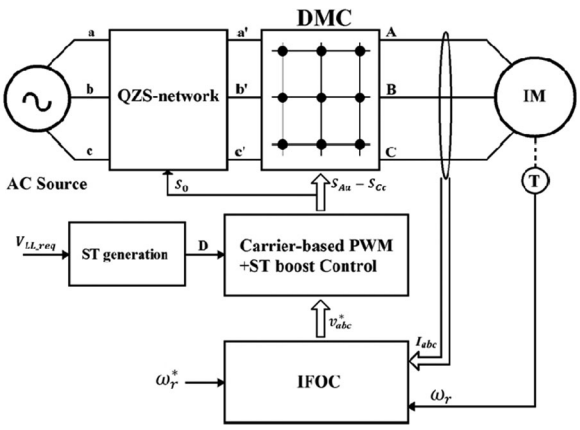

Fig. 27. Block diagram of the QZSDMC-based IM-ASD.

voltage envelope indicators are combined with the three PWM switching sequences S_A, S_B, S_C and the ST pulses to generate nine switching signals.

D. Applications of the QZSDMC

In [33], the quasi-Z-source DMC (QZSDMC) with discontinuous input current has been used for feeding IM as a part of adjustable speed drive (ASD) system. The complete block diagram of the proposed system is shown in Fig. 26. The speed encoder detects the rotor speed to compare with the reference speed. The speed controller deals with the speed error and adjusts the modulation index of the MC, the ST duty ratio is designed according to the corresponding voltage gain and the output voltage can be obtained to meet the desired value.

In [42] and [43], a four-quadrant ASD system based on the QZSDMC feeding a vector-controlled induction motor has been proposed. The proposed system overcomes the reduced voltage transfer ratio limitations of the traditional DMC-based ASD system; therefore, the QZSDMC-IM-based ASD will increase the application of the DMC in different industry fields. The proposed ASD system can operate at full load with small QZS network elements, which are suitable for ASD system. The QZSDMC can achieve buck and boost operation with reduced number of switches, thereby achieving low cost, high efficiency, and reliability, compared to the traditional DMCs. In addition, there is no requirement of dead time with QZS network; hence, commutation of the QZSDMC is easier than the traditional DMC. The proposed closed-loop speed control system can obtain a

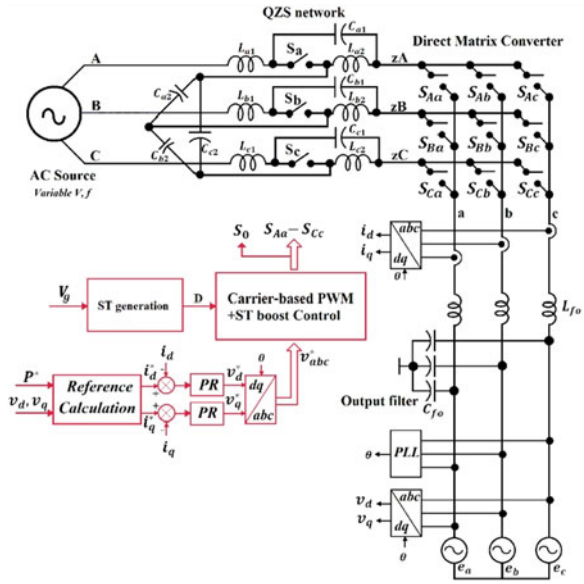

Fig. 28. Grid-connected QZSDMC system.

voltage gain larger than 1 and can operate in motoring and regenerating operation modes with perfect references tracking as verified by MATLAB simulation and dSPACE real-time implementation results. Fig. 27 shows the control block diagram of an induction motor drive system fed with QZSDMC.

The QZSDMC can be used for interfacing renewable energy sources as it is a direct ac/ac converter with a voltage gain greater than unity [44]. The presented simulation results presented are attractive enough to verify the proposed system and to justify additional research work to develop a more efficient QZSDMC grid-connected system. Fig. 28 shows the proposed converter with its control algorithm.

V. Conclusion

This paper outlined a review of the literature on the three ZSMC different topologies, namely, ZSIMC (all-silicon solution), ZSIMC (not all-silicon solution), and Z-source DMC. For each topology, the different topology configurations, circuit analysis, modulation, parameters design, and application had been reviewed. The QZSMC topologies overcomes the voltage gain limitation of the traditional MC and achieves the buck and boost condition with reduced number of switches, therefore achieving low cost, high efficiency, and reliability, compared to back-to-back converter. Furthermore, it will leads to more MC industrial applications.

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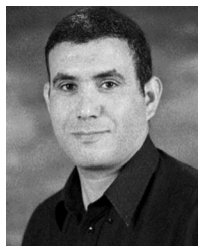

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