Three-Phase Split-Source Inverter (SSI): Analysis and Modulation

Ahmed Abdelhakim, *Student Member, IEEE*, Paolo Mattavelli, *Fellow, IEEE*, and Giorgio Spiazzi, *Member, IEEE*

***Abstract*—In several electrical dc–ac power conversions, the ac output voltage is higher than the input voltage. If a voltage-source inverter (VSI) is used, then an additional dc–dc boosting stage is required to overcome the step-down VSI limitations. Recently, several impedance source converters are gaining higher attentions [1], [2], as they are able to provide buck-boost capability in a single conversion stage. This paper proposes the merging of the boost stage and the VSI stage in a single stage dc–ac power conversion, denoted as split-source inverter (SSI). The proposed topology requires the same number of active switches of the VSI, three additional diodes, and the same eight states of a conventional space-vector modulation. It also shows some merits compared to Z-source inverters, especially in terms of reduced switch voltage stress for voltage gains higher than 1.15. This paper presents the analysis of the SSI and compares different modulation schemes. Moreover, it presents a modified modulation scheme to eliminate the low frequency ripple in the input current and the voltage across the inverter bridge. The proposed analysis has been verified by simulation and experimental results on a 2.0-kW prototype.**

***Index Terms*—DC–AC, pulse-width modulation, single-stage, space vector, split-source inverter, voltage-source inverter (SSI), Z-source inverter (ZSI).**

I. Introduction

VOLTAGE-SOURCE inverters (VSIs) are the most common dc–ac power converters employed in any power electronic system. The VSI embraces only the buck capability with the inversion stage, i.e., the output ac voltage cannot exceed the available dc input voltage. This point is not an issue for many applications with high dc rail. Meanwhile, several applications require the output ac voltage to exceed the input dc voltage. Hence, the use of an additional boosting stage is mandatory for these applications such as fuel cells-based systems, which are characterized by a low and unregulated input voltage [3]–[5]. Recently, dc–ac power converters which embrace the buck-boost capability in a single stage are gaining attention due to their merits compared to the two-stage equivalent in terms of size, cost, weight, and complexity of the whole system [6]–[10]. The most common topology in this power converter category is the conventional Z-source inverter (ZSI) topology, shown in Fig. 1 and introduced in [1]. This inverter exploits an impedance network that comprises four passive elements in addition to a diode that carries the full power to work as a buck-boost stage. Several topologies exist for the so-called ZSI in addition to the conventional one shown in Fig. 1, among them the quasiZSI (qZSI) and the current fed qZSI are introduced in [11]–[14]. Other topologies like the switched-inductor ZSI and the switched-inductor qZSI are discussed in [15], [16]. Moreover, the semiZSI is another ZSI topology introduced as a low cost solution for single-phase photo-voltaic systems [17]. Most of the single stage dc–ac power converter topologies are reviewed in [2], while their different modulation schemes are reviewed in [18].

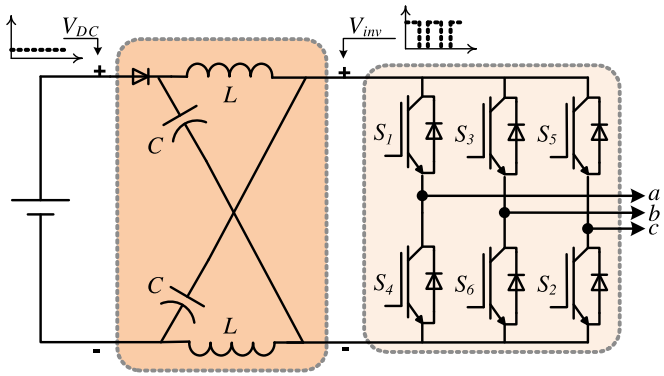

Fig. 1. Z-source inverter.

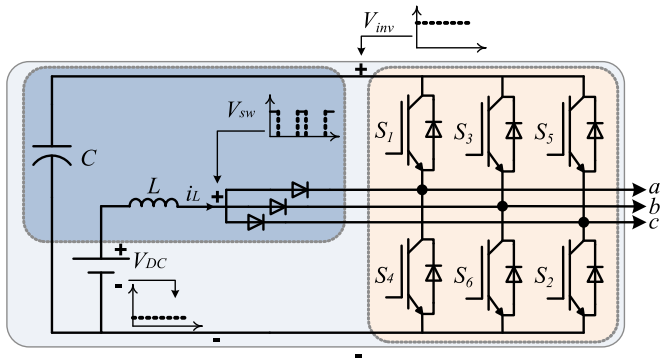

Fig. 2. Proposed three-phase SSI.

The so-called ZSI requires an additional switching state out of the conventional eight states, besides having a discontinuous input current and utilizing four passive elements. Hence, this paper proposes a different topology called the split-source inverter (SSI), shown in Fig. 2. This topology utilizes a reduced passive element count compared with the ZSI, in addition to a diode for each inverter leg. The advantages of the proposed

Manuscript received September 30, 2015; revised November 27, 2015; accepted December 25, 2015. Date of publication December 29, 2015; date of current version June 24, 2016. Recommended for publication by Associate Editor H. A. Abu-Rub.

A. Abdelhakim and P. Mattavelli are with the Department of Management and Engineering, University of Padova, Vicenza 36100, Italy (e-mail: ahmed.a.abdelrazek@ieee.org; mattavelli@ieee.org).

G. Spiazzi is with the Department of Information Engineering, University of Padova, Padova 35131, Italy (e-mail: spiazzi@dei.unipd.it).

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Digital Object Identifier 10.1109/TPEL.2015.2513204

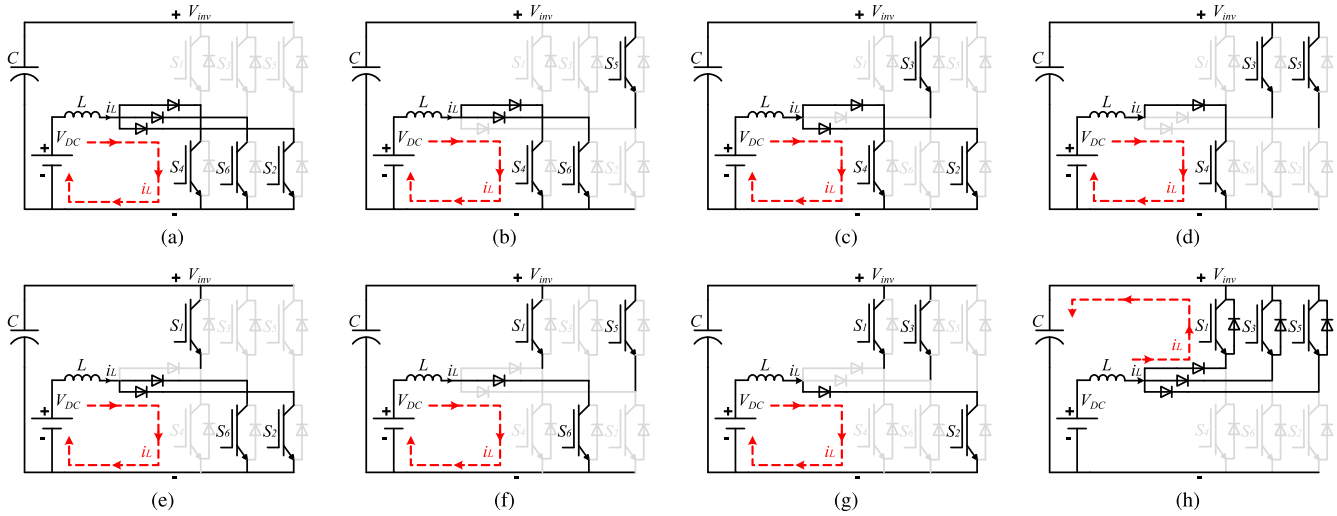

Fig. 3. Switching states of the three-phase SSI neglecting the load conditions (a) State 000 and $V_{\rm sw} = 0$ (b) State 001 and $V_{\rm sw} = 0$ (c) State 010 and $V_{\rm sw} = 0$ (d) State 011 and $V_{\rm sw} = 0$ (e) State 100 and $V_{\rm sw} = 0$ (f) State 101 and $V_{\rm sw} = 0$ (g) State 110 and $V_{\rm sw} = 0$ (h) State 111 and $V_{\rm sw} = V_{\rm inv}$, where "1" means the upper switch is turned ON.

topology, compared with the ZSI, are: a continuous input current, a standard modulation strategy that employs the same eight states of the VSI, and a constant inverter voltage with a low frequency component. This topology is derived by integrating a boost converter into a three-phase VSI, by connecting the boost inductor to the switching nodes of the inverter legs via diodes. The employment of the boost converter in dc–ac power conversion was first studied in [19], [20], where [19] studies the possibility of making a combination from two boost converters to get a sinusoidal output voltage. The work discussed in [20] instead, has introduced the possibility of eliminating the boost converter semiconductor active switch by utilizing the lower semiconductor active switch of a single-phase VSI for power factor correction application.

This paper is organized as follows: the analysis and modulation of the proposed three-phase SSI is discussed in Section II, where the space-vector pulse-width modulation (SVPWM) is utilized in addition to the sinusoidal PWM (SPWM) and the third-harmonic injected PWM (THPWM) schemes. Moreover, Section II introduces a modification of the space-vector modulation scheme to enhance the performance of the SSI, by eliminating the low frequency component in the inverter voltage and the inductor current. In Section III, the conventional ZSI is reviewed using several modulation schemes and compared to the proposed SSI. Finally, a 2.0-kW SSI is designed, simulated, and experimentally tested in Section IV to validate the proposed topology.

II. Three-Phase SSI Topology

A. Operation

The three-phase SSI, shown in Fig. 2, uses the same B6-bridge of the conventional three-phase VSI, considering the same eight states shown in Fig. 3. This inverter uses at least one of the lower semiconductor switches, S_2, S_4, and S_6, to charge the inductor L, where seven different states exist as shown in Fig. 3(a)–(g). Meanwhile, it uses only one state to discharge this inductor and charge the inverter dc link capacitor, as shown in Fig. 3(h). The charging of L can be done considering three semiconductor switches as shown in Fig. 3(a), or two semiconductor switches as shown in Fig. 3(b), (c), and (e), or one semiconductor switch as shown in Fig. 3(d), (f), and (g). Fig. 3 shows that the employed diodes in this topology suffers from different commutations during one switching cycle.

B. Modulation

This section discusses the modulation schemes of the proposed three-phase SSI topology. The SVPWM scheme is considered first, then the standard sinusoidal and third-harmonic injected modulation schemes are analyzed. Moreover, the effect of biasing the reference signals of these modulation schemes is discussed and applied on the third-harmonic injected modulation scheme, to show its merit over the unbiased case in terms of voltage stresses.

1) SVPWM Scheme: The operation of the three-phase SSI described before does not require any special pulses to be generated or modifications of the standard modulation schemes of the VSI for its basic operation. Hence, the same modulation schemes of the VSI are applied to the SSI in this paper, where the SVPWM, whose equivalent reference signals are shown in Fig. 4 [21], [22], is utilized to explain the idea behind the basic modulation of the SSI. In Fig. 4, $\theta = \omega_1 t$, where ω_1 is the fundamental angular frequency.

According to Figs. 3 and 4, the inductor L is charged when at least one of the reference signals is smaller than the carrier signal. The explanation can be simplified by considering a virtual envelope representing the negative peaks of the reference signals, where the operation of the SSI is as follows; when this envelope is smaller than the carrier signal, the inductor is charging as shown in Fig. 3(a) to (g), and when this envelope is larger than the carrier signal, the inductor is discharging and the capacitor is charging as shown in Fig. 3(h).

2) Other PWM Schemes: Other standard PWM schemes, like the SPWM and the THPWM, can be used with the proposed

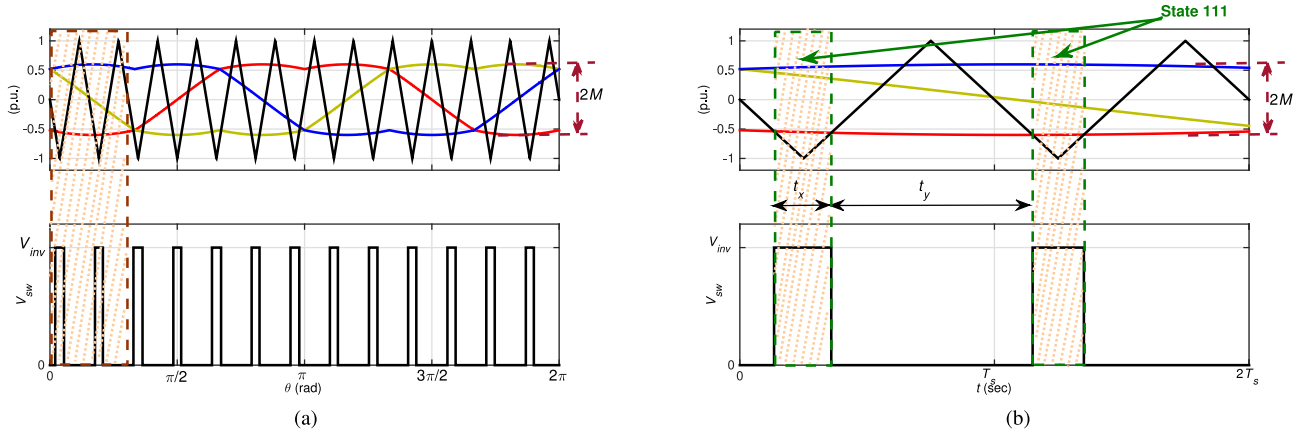

Fig. 4. Equivalent reference signals of the SVPWM scheme (a) Reference and carrier signals for one fundamental cycle (b) Zoom on the reference and carrier signals for two switching cycles, where M=0.6, the frequency modulation index M_f=13, t_x is the inductor discharging time during one switching cycle, and t_y is the inductor charging time during one switching cycle.

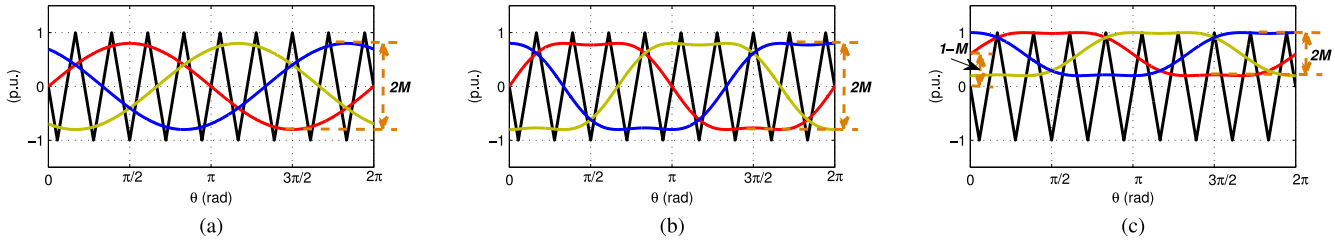

Fig. 5. Other possible modulation schemes for the three-phase SSI (a) Standard SPWM scheme with M=0.8 (b) Standard THPWM scheme with M=0.8 (c) BTHPWM scheme with M=0.4, where the third-harmonic component is 1/6 the fundamental one and the frequency modulation index M_f=9.

inverter topology. Moreover, the effects of biasing the reference signals of any modulation scheme are investigated with reference to the THPWM modulation. Hence, three additional modulation schemes are analyzed in this section: SPWM, THPWM, and the biased THPWM (BTHPWM). The reference signals of these modulation schemes are shown in Fig. 5.

C. Mathematical Derivation

1) SVPWM Scheme: The inductor L of the SSI is charged with a duty cycle D, where $D = t_y/(t_x + t_y)$ being t_x and t_y defined in Fig. 4. For the SVPWM scheme discussed in [21] and [22], considering the modulation index M definition shown in Fig. 4, D is related to M by

$$D(\theta) = \frac{1}{2}\left\{1 - M\sin\left(\theta - \frac{2\pi}{3}\right)\right\} \tag{1}$$

where $0 \le \theta \le \frac{\pi}{3}$. Based on (1) and Fig. 4, the duty cycle D is not constant, as it varies with a low frequency equals to six times the fundamental frequency. This variation is higher in the case of the SPWM scheme, where D varies with a low frequency equals to three times the fundamental frequency with higher amplitude. The duty cycle variation of the SVPWM is bounded by $D_{\min}$ and $D_{\max}$ given by

$$D_{\min} = 0.5 + \frac{\sqrt{3}M}{4} \tag{2}$$

$$D_{\max} = 0.5 + \frac{M}{2}. \tag{3}$$

The inductor is charged with an average duty cycle $D_{\rm av}$ given by

$$D_{\rm av} = 0.5 + \frac{3M}{2\pi}. \tag{4}$$

Based on the inductor flux balance and the capacitor charge balance, the normalized average inverter voltage $\frac{V_{\rm inv}}{V_{\rm DC}}$ is given by

$$\frac{V_{\rm inv}}{V_{\rm DC}} = \frac{1}{1 - D_{\rm av}} \tag{5}$$

where, $V_{\rm DC}$ is the input dc voltage. Substituting (4) in (5) yields

$$\frac{V_{\rm inv}}{V_{\rm DC}} = \frac{2\pi}{\pi - 3M}. \tag{6}$$

From (6), the normalized output fundamental peak phase voltage $\frac{V_{\phi 1}}{V_{\rm DC}}$ is

$$\frac{V_{\phi 1}}{V_{\rm DC}} = \frac{2\pi M}{\sqrt{3}\pi - 3\sqrt{3}M}. \tag{7}$$

Finally, the selection of the inductor should consider the high frequency and the low frequency current components due to the switching and the duty cycle variation, respectively. This is done by finding high-frequency ripple for the inductor current ΔI_{Lh} and the capacitor voltage $\Delta V_{{\rm inv}h}$ given by

$$\Delta I_{Lh} = \frac{DV_{\rm DC}}{f_s L} \tag{8}$$

$$\Delta V_{{\rm inv}h} = \frac{(1-D)I_{\rm DC}}{f_s C}. \tag{9}$$

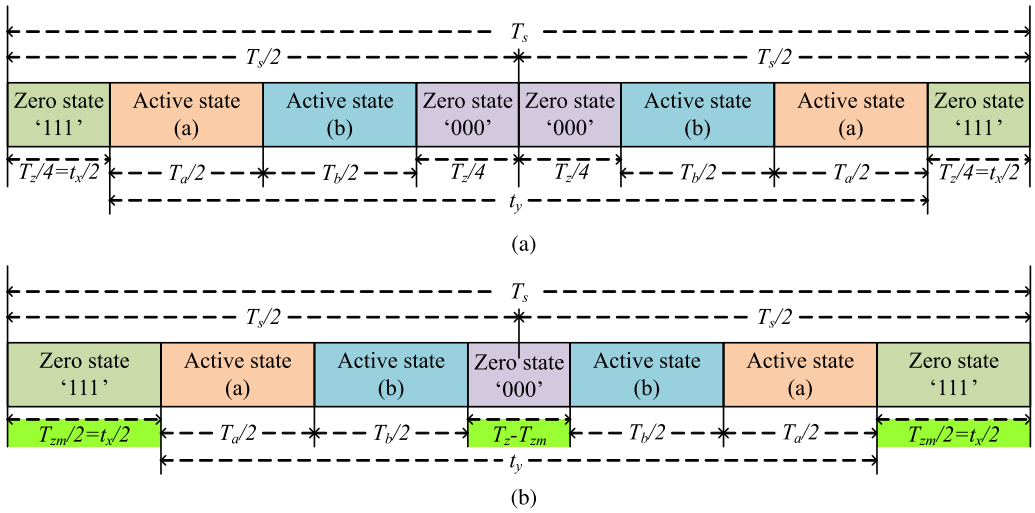

Fig. 6. Switching pattern during any sector (a) Using the conventional SVPWM scheme (b) Using the MSVPWM scheme, where t_x is the inductor discharging time during one switching cycle, and t_y is the inductor charging time during one switching cycle.

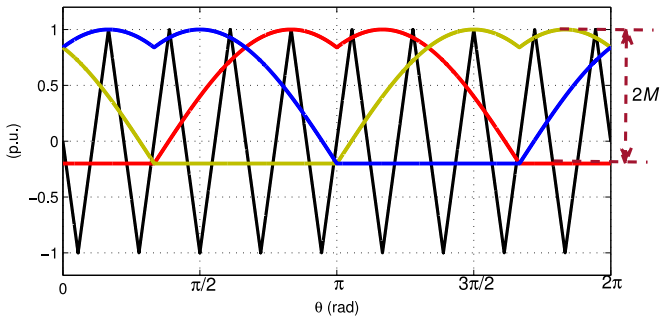

Fig. 7. Equivalent reference signals of the MSVPWM scheme.

The low-frequency terms in both input inductor current and inverter voltage are caused by the duty cycle modulation, given by (1). The low-frequency inductor voltage ripple, assuming constant inverter voltage, is given by $|V_{L_l}| = (1 - D(\theta))V_{\text{inv}}$, while the low-frequency capacitor current ripple, assuming constant inductor current, is given by $|I_{C_l}| = (1 - D(\theta))I_{\text{DC}}$. Now, in order to estimate the low-frequency ripple components, only the fundamental terms of $|V_{L_l}|$ and $|I_{C_l}|$ are considered, which are proportional to the fundamental term of Fourier series of $D(\theta)$

$$D_l = \frac{6M}{35\pi}. \tag{10}$$

Thus,

$$\Delta I_{Ll} \approx \frac{D_l V_{\text{inv}}}{6\omega_1 L} = \frac{M V_{\text{inv}}}{70\pi^2 f_1 L} \tag{11}$$

$$\Delta V_{\text{inv}l} \approx \frac{D_l I_{\text{DC}}}{6\omega_1 C} = \frac{M I_{\text{DC}}}{70\pi^2 f_1 C}. \tag{12}$$

Under worst conditions, the low-frequency ripple is added to the high frequency one; thus, the required inductance and capacitance are given by

$$L \approx \frac{M V_{\text{inv}}}{70\pi^2 f_1 \Delta I_L} + \frac{D_{\max} V_{\text{DC}}}{f_s \Delta I_L} \tag{13}$$

$$C \approx \frac{M I_{\text{DC}}}{70\pi^2 f_1 \Delta V_{\text{inv}}} + \frac{(1 - D_{\min}) I_{\text{DC}}}{f_s \Delta V_{\text{inv}}} \tag{14}$$

where, $\Delta I_L = \Delta I_{Ll} + \Delta I_{Lh}$ and $\Delta V_{\text{inv}} = \Delta V_{\text{inv}l} + \Delta V_{\text{inv}h}$.

2) Other PWM Schemes: The mathematical equations for the SPWM, the THPWM, and the BTHPWM modulation schemes are introduced in this section, where the duty cycle (D) and its average value (D_{av}) of each modulation of these modulation schemes can be determined by

$$D(\theta) = \begin{cases} 0.5 - \dfrac{M}{2}\sin(\theta) & \Rightarrow \text{SPWM} \\ 0.5 - \dfrac{M}{\sqrt{3}}\{\sin(\theta) + \dfrac{1}{6}\sin(3\theta)\} & \Rightarrow \text{THPWM} \\ \dfrac{M}{2} - \dfrac{M}{\sqrt{3}}\{\sin(\theta) + \dfrac{1}{6}\sin(3\theta)\} & \Rightarrow \text{BTHPWM} \end{cases} \tag{15}$$

where $\frac{7\pi}{6} \le \theta \le \frac{11\pi}{6}$, and M is modulation index shown in Fig. 5,

$$D_{\text{av}} = \begin{cases} \dfrac{1}{2} + \dfrac{3\sqrt{3}}{4\pi}M & \Rightarrow \text{SPWM} \\ \dfrac{1}{2} + \dfrac{3}{2\pi}M & \Rightarrow \text{THPWM} \\ \left\{\dfrac{1}{2} + \dfrac{3}{2\pi}\right\}M & \Rightarrow \text{BTHPWM.} \end{cases} \tag{16}$$

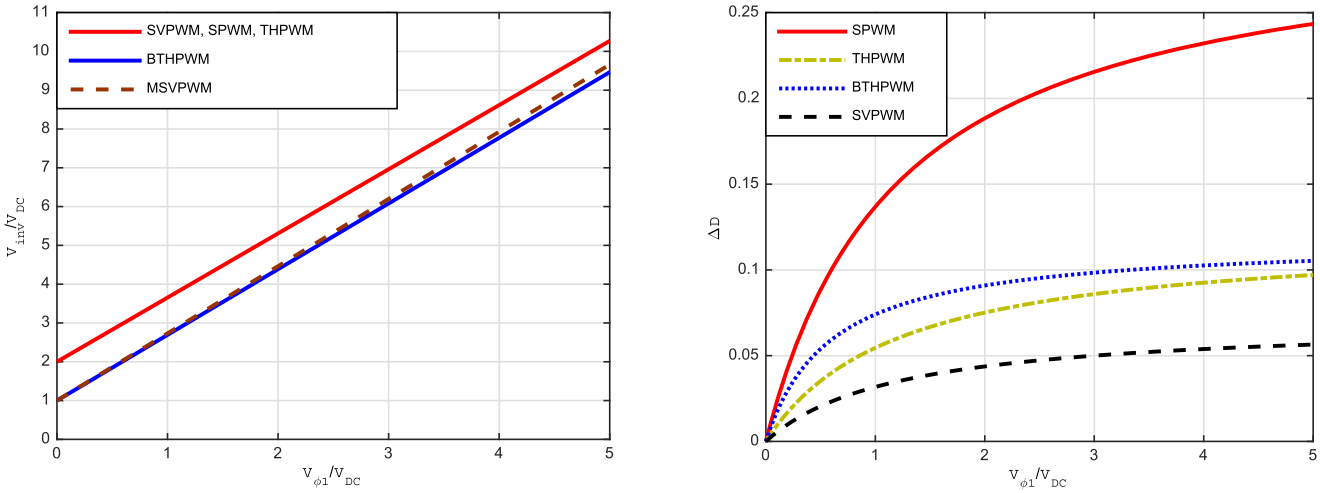

Fig. 8. Comparative figures between the SPWM, the THPWM, the BTHPWM, the SVPWM, and the MSVPWM schemes (a) $V_{\rm inv}/V_{\rm DC}$ versus $V_{\phi 1}/V_{\rm DC}$ (b) ΔD versus $V_{\phi 1}/V_{\rm DC}$.

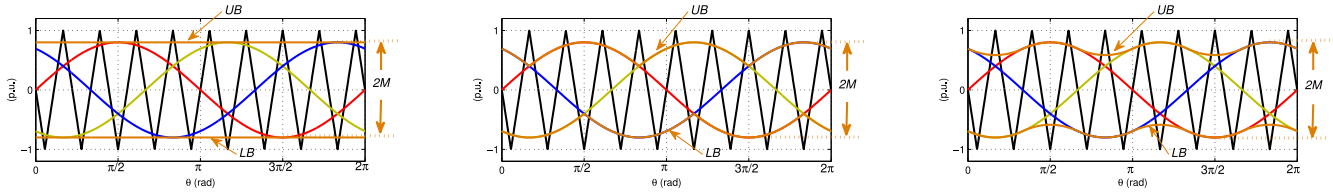

Fig. 9. Reference signals of the ZSI common modulation schemes (a) Simple-boost PWM scheme (b) Maximum-boost PWM scheme (c) Constant-boost PWM scheme, where M=0.8, the frequency modulation index $M_f = 9$.

Meanwhile, the normalized inverter and output fundamental peak phase voltages can be determined by

$$\frac{V_{\rm inv}}{V_{\rm DC}} = \begin{cases} \dfrac{4\pi}{2\pi - 3\sqrt{3}M} & \Rightarrow \text{SPWM} \\ \dfrac{2\pi}{\pi - 3M} & \Rightarrow \text{THPWM} \\ \dfrac{2\pi}{2\pi - (\pi+3)M} & \Rightarrow \text{BTHPWM} \end{cases} \tag{17}$$

$$\frac{V_{\phi 1}}{V_{\rm DC}} = \begin{cases} \dfrac{2\pi M}{2\pi - 3\sqrt{3}M} & \Rightarrow \text{SPWM} \\ \dfrac{2\pi M}{\sqrt{3}\pi - 3\sqrt{3}M} & \Rightarrow \text{THPWM} \\ \dfrac{2\pi M}{2\sqrt{3}\pi - (\pi+3)\sqrt{3}M} & \Rightarrow \text{BTHPWM} \end{cases} \tag{18}$$

for these modulation schemes.

Finally, the inductor and the capacitor values can be calculated considering the same steps as before. The result is

$$L \approx \frac{KMV_{\rm inv}}{6\pi f_1 \Delta I_L} + \frac{D_{\max} V_{\rm DC}}{2 f_s \Delta I_L} \tag{19}$$

$$C \approx \frac{KMI_{\rm DC}}{6\pi f_1 \Delta V_{\rm inv}} + \frac{(1 - D_{\min}) I_{\rm DC}}{2 f_s \Delta V_{\rm inv}} \tag{20}$$

where, K is a constant given by

$$K = \begin{cases} \dfrac{3\sqrt{3}}{8\pi} & \Rightarrow \text{SPWM} \\ \dfrac{27 - 4\pi\sqrt{3}}{36\pi} + \dfrac{3}{35\pi} & \Rightarrow \text{THPWM, BTHPWM} \end{cases} \tag{21}$$

and $D_{\min}$, and $D_{\max}$ are the minimum and the maximum values of the duty cycle given by

$$D_{\min} = \begin{cases} \dfrac{1}{2} + \dfrac{1}{4}M & \Rightarrow \text{SPWM} \\ \dfrac{1}{2} + \dfrac{2\sqrt{3}}{9}M & \Rightarrow \text{THPWM} \\ \left\{\dfrac{1}{2} + \dfrac{2\sqrt{3}}{9}\right\}M & \Rightarrow \text{BTHPWM} \end{cases} \tag{22}$$

$$D_{\max} = \begin{cases} \dfrac{1}{2} + \dfrac{1}{2}M & \Rightarrow \text{SPWM} \\ \dfrac{1}{2} + \dfrac{1}{2}M & \Rightarrow \text{THPWM} \\ M & \Rightarrow \text{BTHPWM.} \end{cases} \tag{23}$$

Note that, the low-frequency ripple components in case of the THPWM and the BTHPWM schemes have been calculated considering the lowest two harmonics of the Fourier series of

TABLE I
INPUT/OUTPUT RELATIONS OF THE ZSI USING THE COMMON MODULATION SCHEMES [1], [23], [24]

	Simple-boost PWM	Maximum-boost PWM	Constant-boost PWM
Normalized shoot-through time $\left(\frac{T_{ST}}{T_s}\right)$	$1-M$	$1-\frac{3\sqrt{3}M}{2\pi}$	$1-\frac{\sqrt{3}M}{2}$
Normalized inverter voltage $\left(\frac{V_{inv}}{V_{DC}}\right)$	$\frac{1}{2M-1}$	$\frac{\pi}{3\sqrt{3}M-\pi}$	$\frac{1}{\sqrt{3}M-1}$
Normalized output peak phase voltage $\left(\frac{V_{\phi 1}}{V_{DC}}\right)$	$\frac{M}{2(2M-1)}$	$\frac{\pi M}{2(3\sqrt{3}M-\pi)}$	$\frac{M}{2(\sqrt{3}M-1)}$

TABLE II
CURRENT STRESSES IN THE DIFFERENT SWITCHES OF THE SSI AND THE ZSI

	SSI	ZSI
Upper IGBTs	$I_{max}=I_{\phi 1}$	$I_{max}=\frac{2I_L+\Delta I_L}{3}+I_{\phi 1}$
Upper freewheeling diodes	$I_{max}=\frac{I_L+\Delta I_L}{3}+I_{\phi 1}$	$I_{max}=I_{\phi 1}$
Lower IGBTs	$I_{max}=I_L+\Delta I_L+I_{\phi 1}$	$I_{max}=\frac{2I_L+\Delta I_L}{3}+I_{\phi 1}$
Lower freewheeling diodes	$I_{max}=I_{\phi 1}$	$I_{max}=I_{\phi 1}$
Additional diode(s)	$I_{max}=I_L+\Delta I_L$ $I_{av}=\frac{I_L}{3}$	$I_{max}=\{I_L\}/\{1-(\frac{T_{ST}}{T_s})\}$ $I_{av}=I_L$

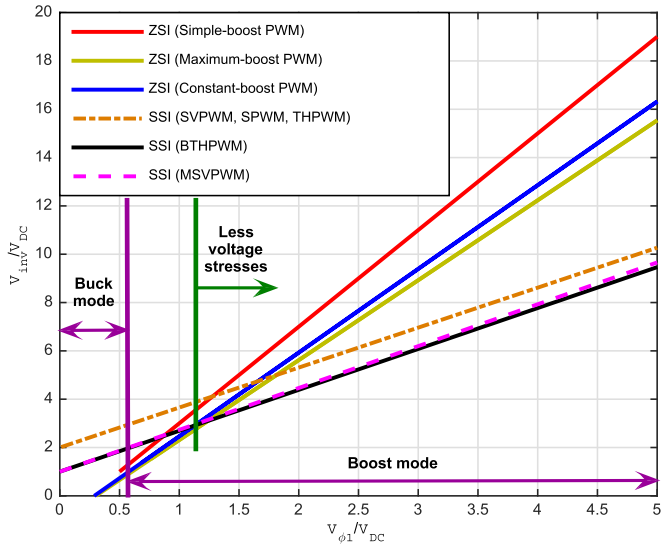

Fig. 10. V_{inv}/V_{DC} versus $V_{\phi 1}/V_{DC}$ for the ZSI and the SSI considering the different modulation schemes of both inverters.

(15) because they have comparable amplitudes. As a worst condition, the two harmonic amplitudes have been simply summed together and they yield the two terms in the K definition of (21).

It is worth noting that the low-frequency component using the SPWM scheme is very high compared with the SVPWM due to two main reasons: the first one is the order of the low-frequency component, which is six times the fundamental component using the SVPWM scheme and three times the fundamental component using the SPWM scheme, while the second reason is the lower duty cycle variations for the SVPWM scheme, which results in a lower low-frequency component amplitude. The ratio between the low-frequency component in the inductor current using the SPWM scheme and its equivalent using the SVPWM scheme can be calculated from the low-frequency terms in (13) and (19) to be 7.58. The same ratio exists for the low-frequency component in the inverter voltage neglecting the high-frequency term.

D. Modified SVPWM (MSVPWM) Scheme

The low-frequency component in the inductor current and the inverter voltage using the aforementioned modulation schemes is important. This low-frequency component can be eliminated by fixing the duty cycle D. This can be done by recalling the switching pattern of the SVPWM scheme during any sector shown in Fig. 6(a), where T_s is the sampling time, T_a and T_b are the two equivalent active states times, and T_z is the zero states equivalent time. Hence, redistributing the zero states equivalent time without affecting the active states time is the key point. The discharging time t_x of the inductor L is fixed to the minimum value of the zero state equivalent time T_{zm}, given by

$$t_x = T_{zm} = T_s\left\{1-2M\sin\left(\frac{\pi}{6}\right)\right\} \tag{24}$$

during any sector as shown in Fig. 6(b), where the remaining zero states time is assigned to the other zero state.

By making $t_x = T_{zm}$, the biasing, discussed before, is automatically achieved as shown in Fig. 7, where the reference signals using this modification are showed. Fig. 7 shows that the lower virtual envelop is constant, where the duty cycle D is now fixed and equal to M.

The normalized inverter and output fundamental peak phase voltages can now be calculated by

$$\frac{V_{inv}}{V_{DC}} = \frac{1}{1-M} \tag{25}$$

$$\frac{V_{\phi 1}}{V_{DC}} = \frac{M}{\sqrt{3}(1-M)}. \tag{26}$$

Finally, the inductor and capacitor values can be calculated, as in the boost converter, by considering only the switching

TABLE III
DESIGN STEPS OF THE 2.0-KW SSI

	V_{DC}	I_{DC}	$V_{\phi 1}$	pf	$I_{\phi 1}$	f_s	f_1	Required M		V_{inv}		D			Required L		Required C	
								Eq.	M	Eq.	(V)	Eq.	D_{min}, D_{max}	D_{av}	Eq.	L (mH)	Eq.	C (μF)
(a)	100 V	20 A	$110\sqrt{2}$ V	0.8 lag	$7.58\sqrt{2}$ A	10.0 kHz	50 Hz	(7)	0.5892	(6)	457	(1), (2), (3), (4),	0.7551, 0.7946	0.7813	(13)	3.1	(14)	86.6
(b)								(18)	0.6804	(17)	457	(16), (22), (23)	0.6701, 0.8402	0.7813	(19)	15.3	(20)	380
(c)									0.5892		457		0.7268, 0.7946	0.7813		4.2		152.22
(d)									0.7415		363		0.6562, 0.7415	0.7248		4.0		241
(e)								(26)	0.7293	(25)	369	–	0.7293	0.7293	(27)	1.46	(28)	73.3

(a) SVPWM (b) SPWM (c) THPWM (d) BTHPWM (e) MSVPWM

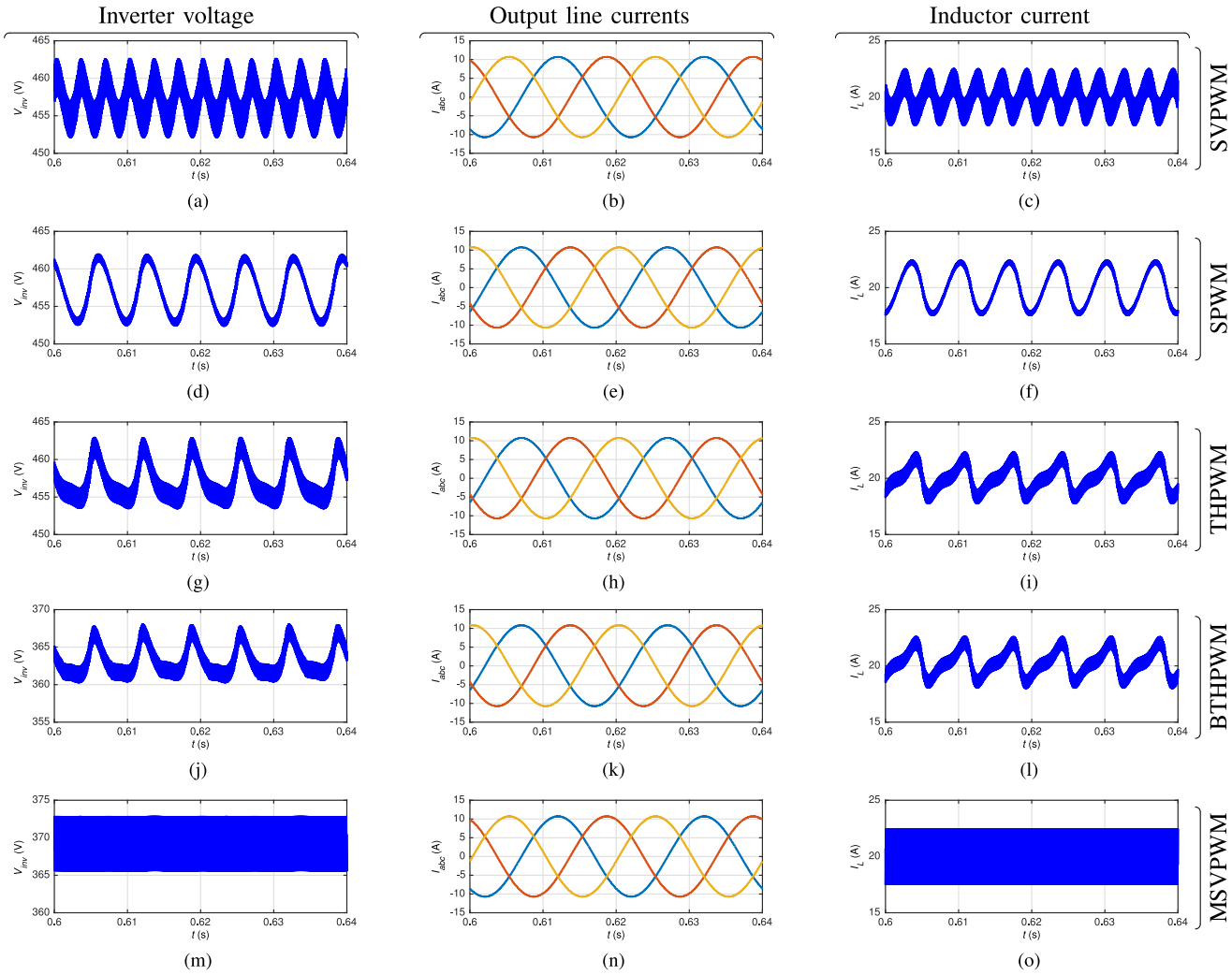

Fig. 11. MATLAB/Simulink model results with different modulation schemes. From left to right: inverter voltage, output line currents, and inductor current waveforms. From top to bottom: SVPWM, SPWM, THPWM, BTHPWM, and MSVPWM.

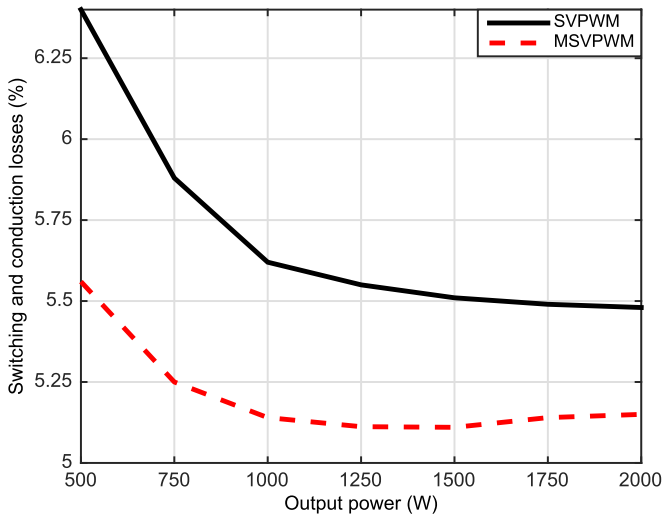

Fig. 12. Simulated switching and conduction losses of the proposed SSI switches using PLECS toolbox.

frequency ripple given by (8) and (9) with D = M, i.e.,

$$L = \frac{MV_{\rm DC}}{f_s \Delta I_L} \tag{27}$$

$$C = \frac{(1-M)I_{\rm DC}}{f_s \Delta V_{\rm inv}}. \tag{28}$$

E. Modulation Schemes Comparison

To compare between these different modulation schemes, the normalized inverter voltage $V_{\rm inv}/V_{\rm DC}$ is shown versus the normalized output fundamental peak phase voltage $V_{\phi 1}/V_{\rm DC}$ in Fig. 8(a). Meanwhile, the duty cycle variation ΔD is shown in Fig. 8(b) versus the normalized output fundamental peak phase voltage $V_{\phi 1}/V_{\rm DC}$ for four modulation schemes out of five, as the MSVPWM scheme has no duty cycle variations. ΔD is calculated based on the minimum duty cycle ($D_{\rm min}$) and the maximum duty cycle ($D_{\rm max}$).

Fig. 8 shed the light upon two important points: the first one is the higher duty cycle variation for the SPWM compared to the other modulation schemes, which calls for higher values of the passive elements for the same inductor current and inverter voltage low-frequency components, and the second point is the reduced switch voltage stress using the BTHPWM and the MSVPWM schemes, which is the main merit behind the biasing. The less voltage stresses using the BTHPWM and the MSVPWM schemes is the result of a reduced zero state interval shown in Fig. 3(a) as this state increases the charging time of the inductor. Hence, the active states, which controls the output voltage are mainly controlling the inverter voltage with negligible contribution of this zero state.

III. Current and Voltage Stresses Comparison

This section shows the current and voltage stresses of the proposed topology using the SVPWM scheme versus the corresponding stresses of the conventional ZSI considering its commonly used PWM schemes. The boosting function in the ZSI is accomplished using the impedance network, shown in Fig. 1, which requires an extra zero state, called the shoot-through state, added to the conventional eight states of the VSI to add the boosting capability. This extra state is achieved by gating the same semiconductor switches on the same leg simultaneously, which could be fulfilled using seven methodologies; gating one leg per time, gating two legs simultaneously, and gating the three legs simultaneously [1]. If the shoot-through state is fulfilled by gating the three legs simultaneously, the current through all the switches is two times the inductor current that equals the dc average current. Hence, each semiconductor device of the B6 bridge should withstand a current of $(\frac{2I_L}{3} + I_{\phi 1})$. Meanwhile, the bottom switches in the SSI should carry a current of $(I_L + I_{\phi 1})$, while the upper switches of the SSI should carry a current of $(\frac{I_L}{3} + I_{\phi 1})$.

There are three common PWM schemes employed for the ZSI introduced in [1], [23], and [24]. These modulation schemes use additional envelops to generate the shoot-through state as shown in Fig. 9, where the difference between these modulation schemes is the shape of the employed envelop. The first modulation scheme introduced in [1], called the simple boost PWM scheme, has the reference signals shown in Fig. 9(a). This PWM scheme has the two constant envelops equals the peaks of the sinusoidal reference signals. The second modulation scheme introduced in [23], called the maximum-boost PWM scheme, uses the positive and the negative peaks of the sinusoidal reference signals to generate the desired envelops as shown in Fig. 9(b). Finally, the third modulation scheme introduced in [24], called the constant-boost PWM scheme, uses the equations given by (29) and (30) to generate the desired envelops as shown in Fig. 9(c). The normalized output fundamental peak phase voltage and the normalized inverter voltage as a function of the modulation index M are summarized in Table I for the three modulation schemes

$$UB = \begin{cases} M\left(\sqrt{3} + \sin\left(\theta - \dfrac{2\pi}{3}\right)\right) & 0 \le \theta \le \dfrac{\pi}{3} \\ M\sin(\theta) & \dfrac{\pi}{3} \le \theta \le \dfrac{2\pi}{3} \end{cases} \tag{29}$$

$$LB = \begin{cases} M\sin\left(\theta - \dfrac{2\pi}{3}\right) & 0 \le \theta \le \dfrac{\pi}{3} \\ M(\sin(\theta) - \sqrt{3}) & \dfrac{\pi}{3} \le \theta \le \dfrac{2\pi}{3}. \end{cases} \tag{30}$$

Finally, the current stresses in the different switches of the SSI and ZSI are summarized in Table II, where, $I_{\rm max}$ and $I_{\rm av}$ are the maximum and average currents in each single switch respectively, while $T_{\rm ST}$ is the shoot-through state equivalent time.

The normalized inverter voltage $V_{\rm inv}/V_{\rm DC}$ against the normalized output fundamental peak phase voltage $V_{\phi 1}/V_{\rm DC}$ is shown in Fig. 10 for the ZSI and the proposed topology considering different modulation schemes for both topologies. This figure shows an important merit for the proposed topology over the ZSI, which is the reduced voltage stresses for voltage gains higher than 1.15.

TABLE IV
PARAMETERS OF THE EXPERIMENTAL 2.0-KW SSI

	V_{DC}	L_{filter}	C_{filter}	R_{load}	f_s	f_1	M	$L\ (mH)$	$C\ (\mu F)$
SVPWM scheme							0.5892	3.2	120
SPWM scheme							0.6804	7.9	590
THPWM scheme	100.0 V	1.0 mH	60.0 μF	13.5 Ω	10.0 kHz	50.0 Hz	0.5892	4.3	170
BTHPWM scheme							0.7415	4.3	170
MSVPWM scheme							0.7293	1.6	120

IV. 2.0-KW SSI: SIMULATIONS AND EXPERIMENTAL RESULTS

A. Design Procedure

This section shows the design steps of a 2.0-kW SSI, where the SSI is assumed to be fed from a fuel cell stack with a nominal voltage of 100 V. The design steps are elucidated in Table III. The selection of the inductor and the capacitor of the SSI is accomplished based on the desired current and voltage ripples in both elements, respectively, using (13) and (14) for the SVPWM and using (19) and (20) for the remaining PWM schemes, considering an inductor current ripple of 25% and a capacitor voltage ripple of 2%. The same table shows that the use of the MSVPWM scheme reduces the switch voltage stresses while maintaining the same output voltage amplitude, and requires lower passive component values compared with the other modulations schemes, where the selection of the passive elements is accomplished based on the desired current and voltage ripples as before using (27) and (28).

B. Simulation Results

A MATLAB/Simulink model has been built to simulate the operation of the designed 2.0-kW system using the analyzed modulation schemes. The simulation results are shown in Fig. 11, where the inverter voltage, the output line currents, and the inductor current waveforms are reported. These simulation results verify the analysis of the proposed topology using the different PWM schemes and shed the light upon the merit of the MSVPWM, in terms of reduced passive elements as well as reduced switch voltage stress.

The proposed SSI is simulated using the PLECS toolbox to calculate the switching and conduction losses of the semiconductor devices, where the modeled IGBTs are FGW50N60HD for the lower devices, and IRGIB15B60KD1P for the upper devices, and the modeled diode is VS-30EPH06PbF for the additional input diodes.

The obtained switching and conduction losses of the switches as a percentage of the output power, for different output power values using the SVPWM and the MSVPWM schemes, are showed in Fig. 12, while SPWM and THPWM modulation schemes revealed almost the same losses as the SVPWM one and the BTHPWM gives almost the same losses as the MSVPWM. This figure shows the advantage of using the MSVPWM modulation scheme also from the conversion efficiency point of view.

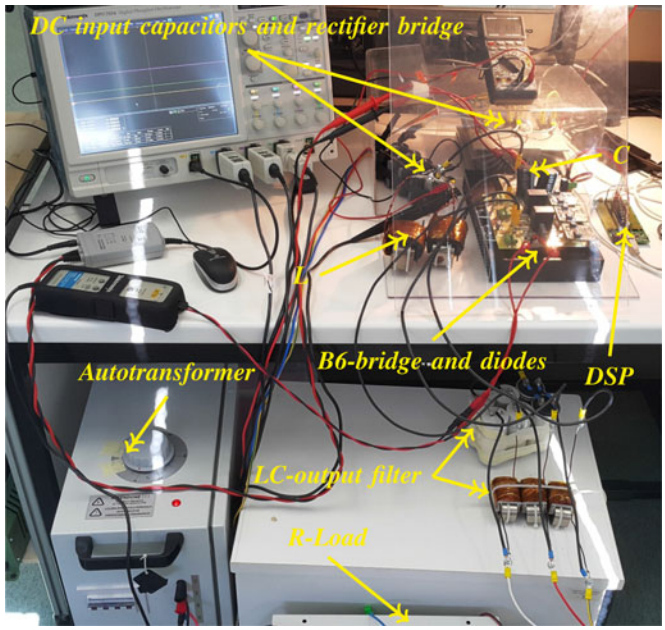

Fig. 13. SSI Experimental Prototype.

C. Experimental Results

This section reports the experimental measurements taken on a 2.0-kW prototype designed according to the presented procedure. The inverter feeds a star-connected resistive load through an *LC* filter, whose parameters are summarized in Table IV. The same table reports the values of the input inductor and the inverter capacitor employed with each investigated modulation scheme together with the modulation index used to obtain the same output phase voltage of 110VRMS.

Fig. 13 shows the experimental setup, while Figs. 14 and 15 report the main waveforms recorded with the different modulation schemes. Comparing the measurements with the theoretical expectations, we observe a lower inverter voltage (roughly 10%) in the prototype, which is caused by both converter losses and the large deadtime used in the switch driving signals. Moreover, the residual low-frequency oscillation in both inductor current and inverter voltage visible in the MSVPWM waveforms can be ascribed to an input voltage ripple.

The experimental results shown in Figs. 14 and 15 shed the light on the value of the low-frequency component in the inductor current and the inverter voltage using the conventional modulation schemes. This low-frequency component is very

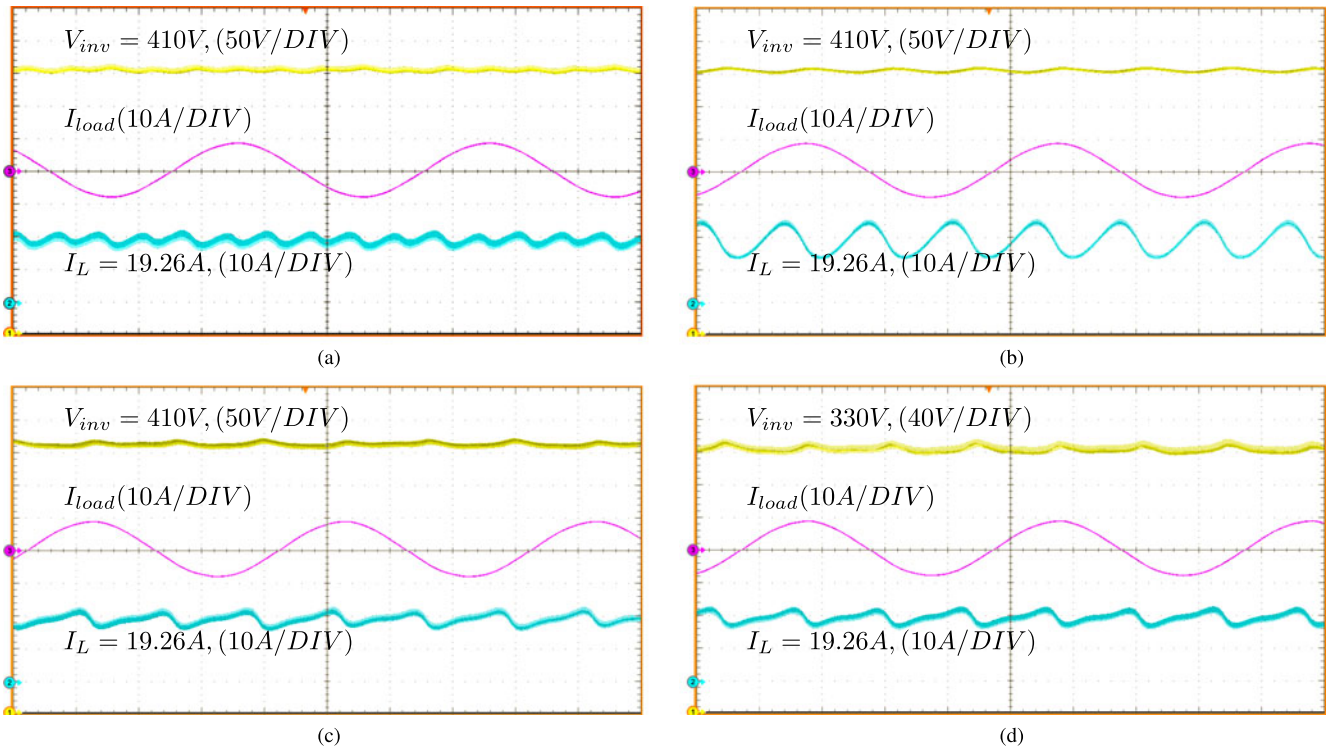

Fig. 14. Experimental results of the proposed SSI with a time scale of 5 ms/DIV (a) SVPWM scheme (b) SPWM scheme (c) THPWM scheme (d) BTHPWM scheme.

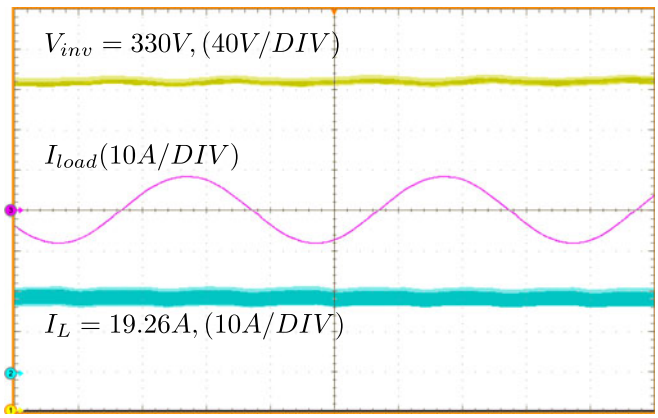

Fig. 15. Experimental results of the proposed SSI using the MSVPWM scheme with a time scale of 5 ms/DIV.

high in the SPWM scheme compared with the other modulation schemes, which makes it practically difficult to use the SPWM scheme due to the high passive components requirements using this scheme. On the other hand, this undesired component is eliminated using the MSVPWM scheme, where much lower passive elements are required compared with the other modulation schemes.

V. Conclusion

This paper proposes a different single-stage dc–ac power converter called SSI. This inverter has some merits compared with the other single-stage dc–ac power converters, which can be summarized as follows:

a) shorter commutation path compared with the ZSI;
b) the same standard modulation schemes of the VSI;
c) the same eight switching states of the VSI;
d) the same number of active switches as the VSI;
e) continuous input current.

Moreover, this paper showed the different modulation schemes for the proposed SSI, in addition to introducing a modified modulation scheme to enhance its performance by eliminating the low-frequency component in the inductor current and the capacitor voltage through a different allocation of the zero state of the SVPWM modulation. This provision, automatically causes the biasing of the modulation signals that proved to be helpful in reducing the switch voltage stress. On the other hand, the proposed SSI suffers from higher diode commutations.

The proposed SSI has been theoretically analyzed and verified using a MATLAB/Simulink model. A 2.0-kW experimental prototype has been implemented to validate the theoretical analysis.

References

[1] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar. 2003.
[2] Y. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. Town, "Impedance-source networks for electric power conversion part i: A topological review," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 699–716, Feb. 2015.
[3] L. Zhang, D. Xu, G. Shen, M. Chen, A. Ioinovici, and X. Wu, "A high step-up dc to dc converter under alternating phase shift control for

fuel cell power system," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1694–1703, Mar. 2015.
[4] V. Samavatian and A. Radan, "A high efficiency input/output magnetically coupled interleaved buck-boost converter with low internal oscillation for fuel-cell applications: CCM steady-state analysis," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5560–5568, Sep. 2015.
[5] P. Cossutta, M. Aguirre, A. Cao, S. Raffo, and M. Valla, "Single-stage fuel cell to grid interface with multilevel current-source inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 5256–5264, Aug. 2015.
[6] M.-K. Nguyen, Y.-C. Lim, and S.-J. Park, "A comparison between single-phase quasi-z-source and quasi-switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6336–6344, Oct. 2015.
[7] J. Cai and Q.-C. Zhong, "An asymmetrical γz-source hybrid power converter with space vector pulse-width modulation," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2014, pp. 344–349.
[8] M. Mohr, W. Franke, B. Wittig, and F. Fuchs, "Converter systems for fuel cells in the medium power range: A comparative study," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2024–2032, Jun. 2010.
[9] A. Hakeem, A. Elserougi, A. El Zawawi, S. Ahmed, and A. Massoud, "A modified capacitor voltage control algorithm for suppressing the effect of measurement noise on grid-connected z-source inverters controllers," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2013, pp. 204–209.
[10] A. Abdelhakim, "Analysis and modulation of the buck-boost voltage source inverter (BBVSI) for lower voltage stresses," in *Proc. IEEE Int. Conf. Ind. Technol.*, Mar. 2015, pp. 926–934.
[11] A.-V. Ho, T.-W. Chun, and H.-G. Kim, "Extended boost active-switched-capacitor/switched-inductor quasi-z-source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5681–5690, Oct. 2015.
[12] Q. Lei, D. Cao, and F. Z. Peng, "Novel loss and harmonic minimized vector modulation for a current-fed quasi-z-source inverter in HEV motor drive application," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1344–1357, Mar. 2014.
[13] I. Roasto and D. Vinnikov, "New voltage mode control method for the quasi-z-source-based isolated dc/dc converters," in *Proc. IEEE Int. Conf. Ind. Technol.*, Mar. 2012, pp. 644–649.
[14] D. Vinnikov, I. Roasto, R. Strzelecki, and M. Adamowicz, "Step-up dc/dc converters with cascaded quasi-z-source network," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3727–3736, Oct. 2012.
[15] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, "Generalized multi-cell switched-inductor and switched-capacitor z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 837–848, Feb. 2013.
[16] H. Ahmed, H. Cha, S.-H. Kim, and H.-G. Kim, "Switched-coupled-inductor quasi-z-source inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1241–1254, Feb. 2016.
[17] T. Ahmed and S. Mekhilef, "Semi-z-source inverter topology for grid-connected photovoltaic system," *IET Power Electron.*, vol. 8, no. 1, pp. 63–75, 2015.
[18] Y. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. Town, and S. Yang, "Impedance-source networks for electric power conversion part ii: Review of control and modulation techniques," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1887–1906, Apr. 2015.
[19] R. Caceres and I. Barbi, "A boost dc–ac converter: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, Jan. 1999.
[20] J. Alves, A. Perin, and I. Barbi, "An electronic ballast with high power factor for compact fluorescent lamps," in *Proc. 31st IAS Annu. Meet., Conf. Rec. IEEE Ind. Appl. Conf.*, Oct. 1996, vol. 4, pp. 2129–2135.
[21] B. Sakthisudhursun, J. Pandit, and M. Aware, "Simplified three-level five-phase SVPWM," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2429–2436, Mar. 2016.
[22] H. Fang, X. Feng, W. Song, X. Ge, and R. Ding, "Relationship between two-level space-vector pulse-width modulation and carrier-based pulsewidth modulation in the over-modulation region," *IET Power Electron.*, vol. 7, no. 1, pp. 189–199, Jan. 2014.
[23] F. Z. Peng, M. Shen, and Z. Qian, "Maximum boost control of the z-source inverter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 833–838, Jul. 2005.
[24] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. Tolbert, and D. Adams, "Constant boost control of the z-source inverter to minimize current ripple and voltage stress," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 770–778, May 2006.

Ahmed Abdelhakim (S'15) was born in Matrouh, Egypt, on April 1, 1990. He received the B.S. and the M.S. (Hons.) degrees in electrical engineering from Alexandria University, Alexandria, Egypt, in 2011 and 2013, respectively. He is currently working toward the Ph.D. degree at the University of Padova, Padua, Italy, where he is working under the supervision of Prof. Mattavelli.

From 2011 till 2014, he was a Demonstrator in Alexandria University then a Lecturer Assistant, where he helped in teaching some power electronics courses for the undergraduate students. Moreover, he was a Cosupervisor for several graduation projects. In 2012, he was involved in Spiretronics Company's research and developments team in Alexandria, Egypt, for nine months, then he was a Visiting Scholar with Texas A&M university, Qatar, working on some research activities for two months. In 2015, he was a Research Fellow with the University of Padova, Padova, Italy, where he was involved in some research activities led by Prof. Paolo Mattavelli. His major research interest includes the analysis, modeling, and control of power converters in islanded and grid-connected modes of operation for renewable energy systems.

Paolo Mattavelli (S'95–A'96–M'00–SM'10–F'14) received the Ph.D. (Hons.) degree in electrical engineering from the University of Padova, Padova, Italy, in 1995.

From 1995 to 2001, he was a Researcher with the University of Padova. From 2001 to 2005, he was an Associate Professor with the University of Udine, where he led the Power Electronics Laboratory. In 2005, he joined the University of Padova in Vicenza with the same duties. From 2010 to 2012, he was a Professor and a Member of the Center for Power Electronics Systems, Virginia Tech. He is currently a Professor with the University of Padova. His major research interest includes analysis, modeling and analog and digital control of power converters, grid-connected converters for renewable energy systems and microgrids, high-temperature, and high-power density power electronics. In these research fields, he has been leading several industrial and government projects.

Dr. Mattavelli was an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2003 to 2012. From 2005 to 2010, he was the Industrial Power Converter Committee Technical Review Chair for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. For terms 2003–2006, 2006–2009, and 2013–2015, he has been a Member-at-Large of the IEEE Power Electronics Society's Administrative Committee. He also received the Prize Paper Award in the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2005, 2006, 2011, and 2012 and the Second Prize Paper Award at the IEEE Industry Application Annual Meeting in 2007.

Giorgio Spiazzi (S'92–M'95) received the Graduate degree (*cum laude*) in electronic engineering, in 1988, and the Ph.D. degree in industrial electronics and informatics from the University of Padova, Padova, Italy, in 1993.

He is currently working as an Associate Professor in the Department of Information Engineering, University of Padova. His main research interests include the fields of dc–dc converters for renewable energy sources, soft-switching techniques, solid-state lamp ballasts, and electromagnetic compatibility in power electronics.