On the Design Process of a 6-kVA Quasi-Z-inverter Employing SiC Power Devices

Mariusz Zdanowski, *Member, IEEE*, Dimosthenis Peftitsis, *Senior Member, IEEE*, Szymon Piasecki, *Member, IEEE*, and Jacek Rabkowski, *Senior Member, IEEE*

***Abstract*—This paper presents the design process of a 6-kVA quasi-Z-source inverter built with SiC power devices, in particular, employing SiC MOSFETs and SiC Schottky diodes. The main design target is to find the optimal parameters and a good agreement between the efficiency and power density of the converter. The performance of the system may be influenced not only by the switching frequency but also from the specific pulsewidth modulated (PWM) method or type of SiC MOSFET, and, therefore, various design cases are analyzed. At a final step, the 6 kVA/3 × 400 VAC inverter employing the 80 mΩ SiC MOSFETs and operating at 100 kHz with the minimum switching number method is chosen for investigation and a laboratory prototype is built. From experiments, the high performance of the designed system is confirmed. More specifically, it is shown that an efficiency above 95.6% (at 400 VDC, $B = 1.9$) and a power density higher than 2 kW/dm^3 have been reached. Last but not least, the obtained results, which can be recognized as leading in the area of impedance source converters, show the great benefits gained by employing the new power semiconductor devices.**

***Index Terms*—DC-AC power converters, design optimization, pulse width modulation, silicon carbide.**

I. Introduction

THE quasi-Z-source inverter [1] is one of the most popular topologies among impedance source converters due to relatively simple structure and, especially, continuous input current. A basic topology presented in Fig. 1 [1] was deeply investigated in many applications [2] such as electric vehicles [3] and wind turbines [4], but the most popular area is definitely photovoltaic energy conversion systems [2], [5]–[8]. Moreover, several modifications have also been introduced to quasi-Z-source inverters over the years. In order to improve the boost ability, the use of a modified impedance network [9], [10] or a transformer [11], [12] has been proposed. Current-fed [13] and multilevel converters with quasi-Z-source network have also been studied in the literature [14], including systems combining PV panels with energy storage systems [15].

Manuscript received October 14, 2015; revised December 09, 2015; accepted January 26, 2016. Date of publication February 19, 2016; date of current version June 24, 2016. Recommended for publication by Associate Editor M. Adamowicz.

M. Zdanowski S. Piasecki and J. Rabkowski are with the Institute of Control and Industrial Electronics, Warsaw University of Technology, Warsaw 00-662, Poland (e-mail: mariusz.zdanowski@ee.pw.edu.pl; szymon.piasecki@ee.pw.edu.pl; jacek.rabkowski@isep.pw.edu.pl).

D. Peftitsis is with the Lab for High Power Electronics Systems, Department of Information Technology and Electrical Engineering, Swiss Federal Institute of Technology (ETH Zürich), Zürich 8092, Switzerland (e-mail: peftitsis@hpe.ee.ethz.ch).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2527100

Most of the presented laboratory models are based on the state-of-the-art Silicon IGBT technology. However, the potential benefits of employing new wide band gap devices have been shown by employing such semiconductor devices in various power electronics applications [16]–[18]. It is very likely that the better switching performance and lower on-state losses of silicon carbide (SiC) and Gallium Nitride (GaN) transistors compared to the silicon counterparts may also be utilized to improve the performance of the impedance source converters. The first attempt was made in 2011 with employing normally on SiC JFETs in order to increase the switching frequency of 2xiZ inverter to 100 kHz [19]. Nevertheless, the obtained efficiency was rather poor due to the relatively high on-state resistance of the early-generation SiC JFETs. Additionally, in [20], low-voltage GaN HEMTs were used in a single-phase quasi-Z-source inverters to improve the efficiency of a PV conversion system to 98%. Recently, the application of SiC diodes and SiC transistors has been shown in a three-level, three-phase quasi-Z-source neutral-point-clamped inverter [21], [22], where a significant increase of the system efficiency was also achieved. These examples show that the design of an impedance source converter with wide band-gap devices is not a trivial issue. From one side, high frequency is very tempting due to the seriously limited size of the passive elements. On the other hand, high switching frequency leads to efficiency reduction due to power losses in semiconductors and also in passive elements. Thus, a fundamental question, which is addressed in this paper, is how to find the optimal operation parameters of the impedance source inverter in terms of efficiency and power density. The authors propose to use a design procedure based on circuit simulations, calculations, and volume estimation, which leads to an optimization surface. After providing basic information about quasi-Z-source inverter in Section II, the design procedure using an optimization surface is presented in Section III. Then, the design and building process of the laboratory prototype of the 6 kVA inverter is described in Section IV and experimentally investigated in Section V. Last but not least, conclusions are given in Section VI.

II. Basic Parameters of the Quasi-Z-Source Inverter

This section presents a set of basic information, mathematical formulas, and parameters regarding the designed quasi-Z-source converter based on suitable literature references. The authors assume that the system under investigation is a three-phase quasi-Z-source converter rated at 6 kVA and operating as an interface between a dc source (i.e., PV panels) varying from $V_{\mathrm{dc}} = 400$ to 550 V and a three-phase grid having a voltage of 3×400 V rms.

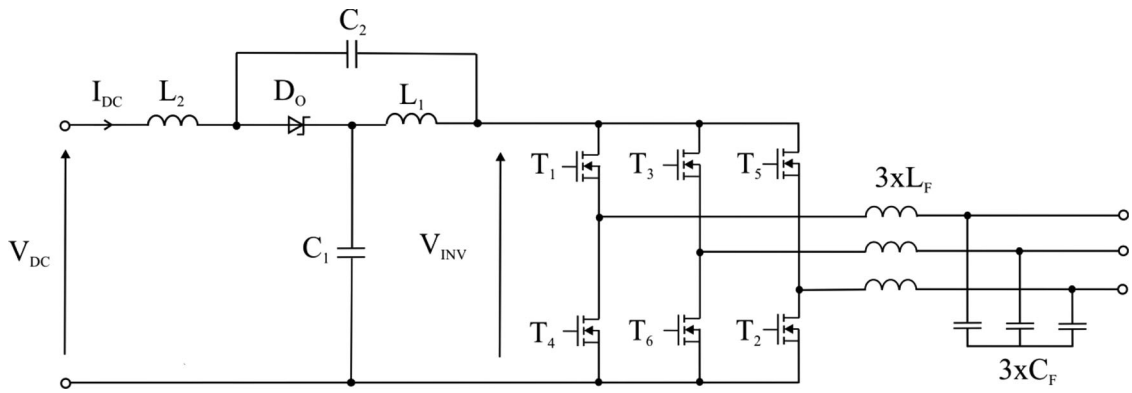

Fig. 1. Schematic diagram of a three-phase quasi-Z-source inverter employing SiC power devices.

A. Passive Elements

In reference to the input voltage $V_{\rm dc}$, the voltage across the inverter bridge $V_{\rm INV}$ is expressed as [1]

$$V_{\rm INV} = BV_{\rm DC} \tag{1}$$

where B is the boost factor. In this case, the boost factor is varying between $B = 1.2$ ($V_{\rm dc} = 550\,{\rm V}$) and 1.9 ($V_{\rm dc} = 400\,{\rm V}$) in order to ensure a sufficiently high amplitude of the output ac voltage. It must be noted that $B = 1.9$ corresponds to the worst case where the maximum voltage across inverter equals $V_{\rm INV} = 760\,{\rm V}$. This means that 1200 V class power semiconductor devices such as SiC MOSFETs and SiC Schottky diodes are suitable for the discussed design. The average voltage across the capacitor C_1 is equal to

$$V_{C_1} = \frac{B+1}{2} V_{\rm dc}. \tag{2}$$

And assuming the worst-case boost factor (i.e., $B = 1.9$), V_{C_1} is not higher than 580 V, while the capacitor C_2 operates at a lower voltage given by

$$V_{C_2} = \frac{B-1}{2} V_{\rm dc}. \tag{3}$$

In the presented design case, V_{C_1} is not higher than 180 V.

The average input current $I_{\rm dc}$, which is equal to the inductor current (see Fig. 1), can be calculated from the input voltage and power. In the worst case, the average input current is equal to 15 A. Current ripples are related to the inductance values $L = L_1 = L_2$, the frequency f_S, the boost factor B, the input voltage $V_{\rm dc}$, and the number of the shoot-through (ST) states per switching period $n_{\rm ST}$

$$\Delta i_L = \frac{t_{\rm st}}{2n_{\rm ST}L}(V_{C_1} - V_{\rm dc}) = \frac{B^2-1}{8Bf_S n_{\rm ST} L} V_{\rm dc}. \tag{4}$$

An *LC* filter operates under similar conditions as in the voltage-source inverters (VSIs). The parameters of this filter are determined on the basis of standard equations under the assumption that the resonant frequency should be at least four times lower than the switching frequency.

B. Semiconductor Power Losses and PWM Methods

In the discussed quasi-Z-source inverter, the two dominant semiconductor power loss (P_S) contributions are the conduction P_C and switching $P_{\rm SW}$ power losses

$$P_S = P_C + P_{\rm SW}. \tag{5}$$

The conduction power losses P_C are rather constant while the switching frequency varies. For the standard carrier-based PWM, as presented in [1], switching power losses can be divided into two substantial parts: the first part, which is caused by the switching process in a similar way as in the VSI, and the second part, which is related to the ST states [23]. In the first case, the phase current is switched between the transistors and diodes of the same inverter leg and the equation is the same as for the VSI

$$P_{\rm SW\_VSI} = \frac{6}{\pi} f_S (E_{\rm ON} + E_{\rm OFF} + E_{\rm REC}) \frac{V_{\rm INV}}{V_N} \frac{I_M}{I_N} \tag{6}$$

where $E_{\rm ON}$, $E_{\rm OFF}$, and $E_{\rm REC}$ are the datasheet values of the switching energies obtained at voltage V_N and current I_N, and I_M is the peak value of the phase current. The second component of the switching power losses is mostly influenced by the input current $I_{\rm dc}$, voltage across the inverter bridge $V_{\rm INV}$, and the number of ST states per switching period $n_{\rm ST}$. In the case of the widely applied maximum constant boost control method [24], where the ST states are introduced with all six transistors, it can be described as

$$P_{\rm SW\_ST} = n_{\rm ST} f_S (E_{\rm ON} + E_{\rm OFF} + E_{\rm REC}) \frac{V_{\rm INV}}{V_N} \frac{2I_{\rm dc}}{I_N}. \tag{7}$$

Over the years, several PWM methods for impedance source converters have been proposed [2], [24]–[28]. In this paper, however, only two essential methods affecting the switching power losses will be considered. The first one, namely, MCBC has already been mentioned earlier. The corresponding power losses using MCBC are described by (6) and (7) under the assumption that $n_{\rm ST} = 2$ [23], [27]. The second method is the so-called minimum switching number (MSN) [27], [28]. According to this method, a reduction of the VSI-alike switching power losses is applied by means of discontinuous PWM using a minimum loss approach [29]. This type of the modulation selects to not switch the phase leg with the maximum current

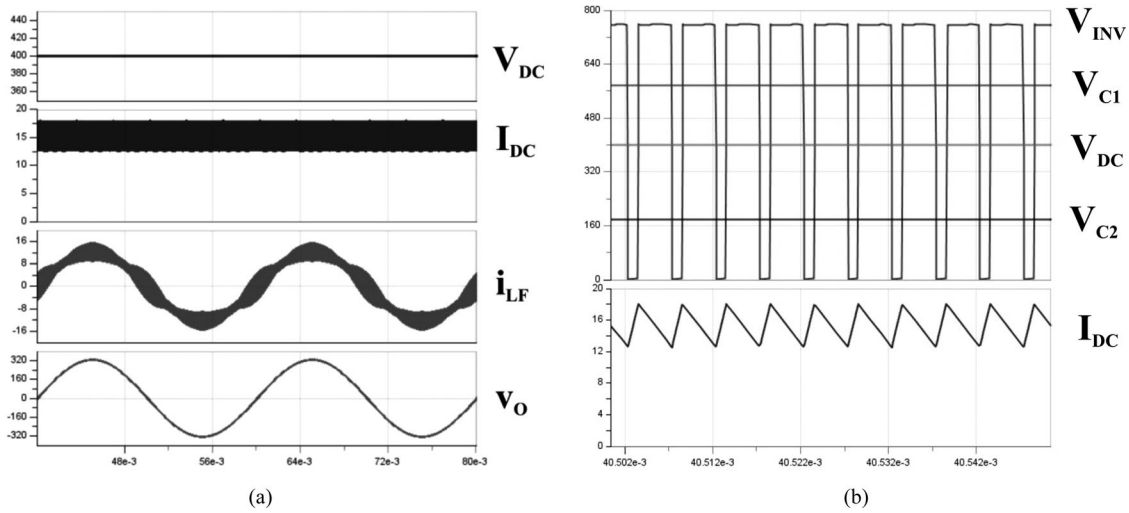

Fig. 2. Simulation results from Gecko for case G (6 kVA, $B = 1.9$, $V_{\rm dc} = 400\,{\rm V}$): (a) input ($I_{\rm dc}$, $V_{\rm dc}$) and output variables (v_O, $i_{\rm LF}$) when two fundamental periods are visible; (b) internal variables (voltage across the inverter $V_{\rm INV}$, capacitor voltages V_{C_1}, V_{C_2}, and input current $I_{\rm dc}$) in several switching periods scale.

value, which corresponds to the elimination of one of the zero states (000 or 111) from the switching pattern. In the case of Z-source inverters, only one type of the zero states (000 or 111) should be kept inactive in order not to introduce low-frequency components to the currents of L_1 and L_2. Thus, the inactive phase leg is not always with the maximum current, and this is a reason why the maximum reduction factor applied to (6) is slightly lower than in the VSI case (0.5). Another possibility to influence the switching power losses is to apply the ST state only once per switching period, which means that $n_{\rm ST} = 1$. The disadvantage of the MSN method is the reduced frequency of the quasi-Z-network, which means that the current ripples will be higher or, alternatively, if the same current ripple should be maintained, the inductances L_1 and L_2 must be increased.

III. Design with the Use of an Optimization Surface

In this section, a simple design procedure for the quasi-Z-inverter is shown. In particular, several different design cases are considered in order to find the optimal design parameters for achieving a certain amount of power losses and keeping the volume of the system below specific limits [30], [31]. Taking into account the 6 kVA converter, there are two design constraints that have been set for the optimization procedure. The first one is a targeted efficiency higher than 95% (for the worst-case conditions: $B = 1.9$, $V_{\rm dc} = 400\,{\rm V}$), and the second one is a targeted power density above 2 kW/dm^3. A set of additional constraints has also been defined: peak-to-peak current ripples Δi_L must be kept lower than 20% (3 A) and the total harmonic distortion (THD) of the output current to be less than 2%. Therefore, the input parameters which should be properly adjusted are the switching frequency (varies between 10 and 150 kHz), the selection of a PWM method (MCBC or MSN) and the type of transistors (SiC MOSFETs: 40 and 80 mΩ). The output variables of the optimization procedure are the power losses $P_{\rm TOT}$ and the volume of the converter $V_{\rm TOT}$.

At the first step of the optimization procedure, the passive elements of the Z-network (i.e., L_1, L_2, C_1, C_2) and *LC* filter (i.e., L_F, C_F) are determined on the basis of the input parameters (i.e., switching frequency, PWM method, and transistor type) in order to meet the considered design requirements. The ripple of the input current Δi_L influences the size of the Z-network inductors and capacitors, while the THD of the output current and voltage impacts the parameters of the *LC* filter. The parameters of the passive elements are inserted to a circuit simulation model developed in Gecko, and simulations were performed for the worst-case conditions in order to verify the quality of the waveforms (input current ripples and THD of the output voltage). An example of these simulation results is shown in Fig. 2, where the input and output waveforms are presented for one of the examined cases. The verified parameters of the passive elements are summarized in Table I. Moreover, the volume ($V_{\rm LZ}$, $V_{\rm LF}$) and the expected power losses ($P_{\rm LZ}$, $P_{\rm LF}$) of all inductor cases are also estimated. It must be noted that for simplicity only ferrite cores were considered and that the effects of the ac resistance were neglected. The detailed design process of the aforementioned inductors is presented in Appendix B. Based on manufacturers data, the volume of the capacitors was also determined and the results are shown in Table IV (see Appendix A). The next design step focuses on the estimation of the semiconductor power losses. Using simulation results for the power semiconductor devices performed in Gecko (parameters in Table III, Appendix A) and assuming a fixed junction temperature $T_j = 125^{\circ}{\rm C}$ (worst case), Table V summarizes the power loss results. A proper and efficient cooling system for the quasi-Z-inverter must also be chosen. The choice of the thermal resistance and the size of the heatsink were made under the assumption that the Cooling System Performance Index (CSPI) [32] is equal to 3. Finally, all obtained data for the examined cases A to H (from Tables IV and V) are plotted on the graphs shown in Fig. 4. This figure shows the obtained optimization surfaces (power losses versus volume) for the semiconductor devices [see Fig. 4(a)], the Z-network

TABLE I
VARIOUS DESIGN CASES OF THE QUASI-Z-SOURCE INVERTER (THE CONSIDERED DIODE IN ALL CASES IS C4D20120D)

Case	f_S (kHz)	PWM Method	Transistor Type	Z-Network	*LC* Filter
A	10	MCBC	40 mΩ	2 × 1.25 mH, 2 × 220 μF	$L_f = 1$ mH, $C_f = 4.7$ μF, $f_r = 2.3$ kHz
B	10	MSN	40 mΩ	2 × 2.5 mH, 2 × 220 μF	
C	10	MCBC	80 mΩ	2 × 1.25 mH, 2 × 220 μF	
D	100	MCBC	40 mΩ	2 × 125 μH, 2 × 15 μF	$L_f = 100$ μH, $C_f = 0.47$ μF, $f_r = 23$ kHz
E	100	MSN	40 mΩ	2 × 250 μH, 2 × 30 μF	
F	100	MCBC	80 mΩ	2 × 125 μH, 2 × 15 μF	
G	100	MSN	80 mΩ	2 × 250 μH, 2 × 30 μF	
H	150	MSN	80 mΩ	2 × 180 μH, 2 × 20 μF	$L_f = 70$ μH, $C_f = 0.22$ μF, $f_r = 40$ kHz

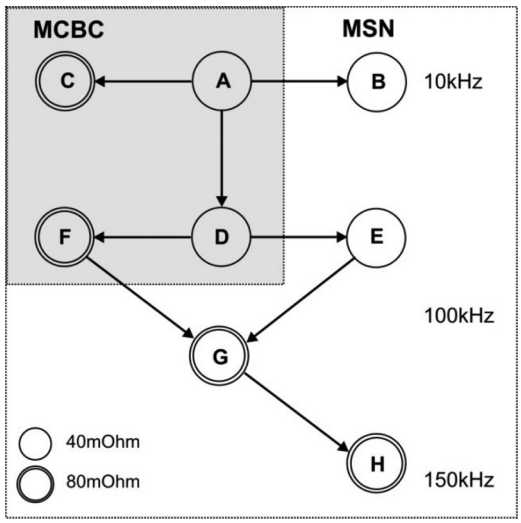

Fig. 3. Flowchart of the performed optimization process.

[see Fig. 4(b)], and the substantial parts of the 6 kVA inverter [see Fig. 4(c)].

A. Design Cases

For the optimization procedure, the path shown in Fig. 3 is taken into consideration, where the optimization starts assuming case A. This case was chosen in reference to a standard silicon-IGBTs-based converter and corresponds to operation at a switching frequency of 10 kHz and using the MCBC PWM method. The only difference is found on the type of the power semiconductor devices. In particular, 40 mΩ SiC MOSFETs (C2M0040120D) and 20 A Schottky diodes are employed. On the contrary, the required passive elements are in the same range as for the Si-IGBTs-based converter (inductors 1.25 mH in Z-network and 1 mH in *LC* filter, Table I). However, when SiC power devices are employed, the corresponding power losses are lower and, in result, the volume of the heatsink is also smaller. According to the results presented in Table V (Appendix A), the most loaded device is the diode due to the dominant conduction losses ($P_{\mathrm{CD}} = 27.6$ W), while less than 10 W of the total power losses per SiC MOSFET are also obtained from Gecko simulations.

The next case B is analyzed for the same switching frequency, as in case A, but with utilizing the MSN pulsewidth modulation (PWM) method ($n_{\mathrm{ST}} = 1$). As mentioned earlier, the MSN PWM minimizes the semiconductor power losses but the required values of the passive elements in the Z-network are doubled compared to case A (see Table I). Consequently, the total efficiency obtained in case B is the maximum among all the discussed cases. Nevertheless, the volume of the converter is the maximum, as shown in Fig. 4(c).

According to the graph depicted in Fig. 3, the third case, namely C, is similar to case A, but instead 80 mΩ SiC MOSFETs are employed. The increase of the conduction power losses due to the higher on-state resistance ($r_{\mathrm{DS(ON)}}$) is not compensated by the better switching performance (see Table II), and, therefore, the total losses are 5 W higher than in case A (see Table V). Thus, case C is slightly worse than A on the optimization surface shown in Fig. 4(c).

Considering the case D, the converter operation is moved toward higher frequencies compared to cases A–C (see Fig. 3). More specifically, in case D, the switching frequency equals $f_S = 100$ kHz and the MCBC method are used which leads to a significant reduction of the volume of the passive elements. All inductances are ten times lower (see Table I), and the volume of the Z-network is the minimum among all examined cases (see Fig. 4). On the other hand, the power losses caused in the semiconductors are increasing to 7% of the rated power, and an extremely bulky heatsink is needed in order to meet the thermal constraints of the system [see Fig. 4(a)].

If the MSN PWM pattern is utilized, a reduction of the semiconductor power losses is possible as analyzed in the next case E (see Fig. 3). In this case, the corresponding power losses drop to 3.9% of the rated power of the converter as shown in Table V and Fig. 4(a). Nevertheless, both inductors in the Z-network have to be increased by a factor of 2 (see Table I). A way to reduce the power losses is to replace the 40 mΩ MOSFETs by the 80 mΩ counterparts, which also show a better switching performance (see Table II). In contrast to the cases with a switching frequency of 10 kHz (i.e., A and C), over 2% of power losses caused in transistors is saved by switching from case D to case F.

Both cases E and F are combined in the next case, namely G, where the MSN method and 80 mΩ transistors are used at the same time. The increase of the Z-network inductors is compensated by using a smaller heatsink (0.75 dm^3), and in comparison to case D, the power losses are reduced to approximately 4% of the rated power. According to Fig. 4(c), this case seems to be the optimal one in terms of obtained total power losses and volume of the converter.

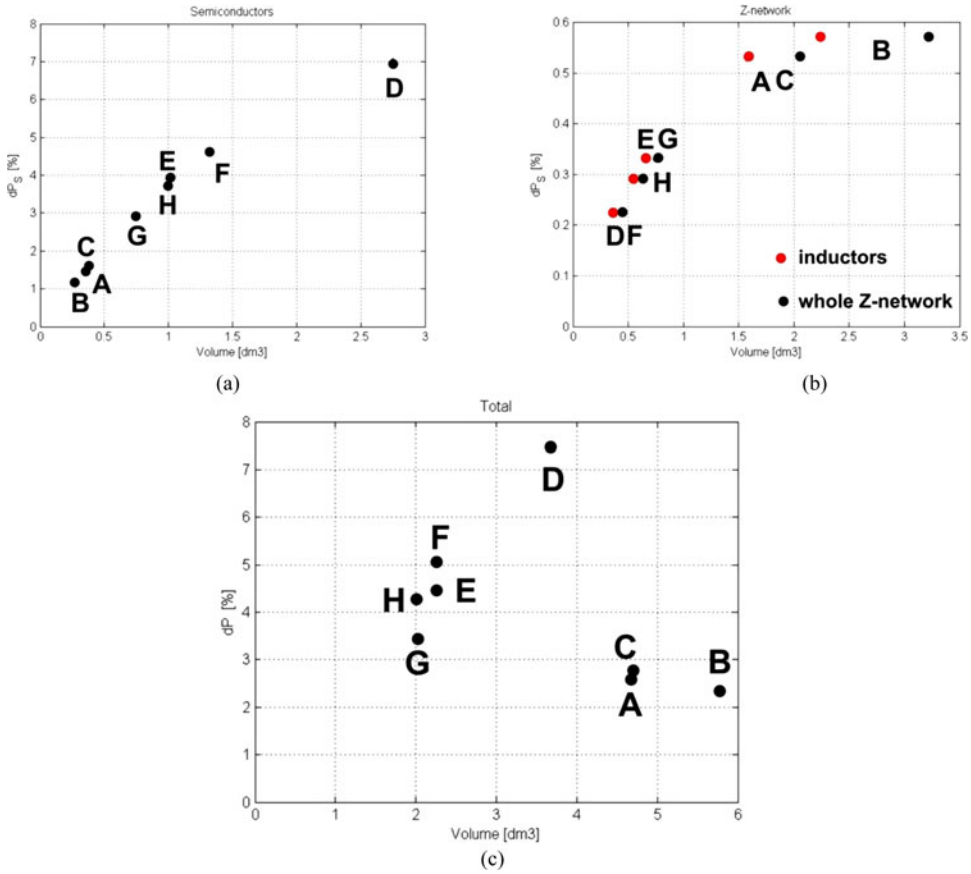

Fig. 4. Simulated and calculated power losses versus volume of the designed quasi-Z-source inverter: (a) semiconductors, (b) Z-network, and (c) semiconductor devices, Z-network, and *LC* filter.

Last but not least, the switching frequency increased to 150 kHz and the MSN PWM method is utilized (case H in Fig. 3). Even though a reduction of the size of passive elements is observed, the increase of the total power losses is more dominant (see Fig. 4).

IV. Laboratory Prototype of the 6 kVA Quasi-Z-Source Inverter

A laboratory prototype of the quasi-Z-source inverter rated at 6 kW (see Fig. 5) was designed and constructed using the design parameters of the case G, as these were determined from the optimization process. The parameters of the inverter are presented in Table II. The main bridge contains six 1200 V/80 mΩ SiC MOSFETs without external antiparallel diodes and single SiC Schottky diode (C4D20120D) is applied in the Z-network. All switches are controlled using the MSN modulation method at $f_S = 100$ kHz by employing a digital-signal-processor (DSP) of the type TMS320F28335. The gate drivers are supplied from special isolated dc/dc converters (+20/−5 V), while the signals to the gate drivers are provided using the optocouplers ACPL-W-347. The power semiconductor devices (i.e., transistors and diode) are mechanically mounted on a heatsink of the type LA 6 with forced air-cooling. The Z-network contains two inductors designed using ferrite cores (250 μH/25 A, litz wire) and two 30 μF capacitors from Vishay with the ratings of 700 and 500 V for C_1 and C_2, respectively. Additionally, a capacitor of 3 μF/700 V is connected to the input to filter out the high-frequency ripples appeared on the inductor current. The *LC* filter consists of three 100 μH/25 A inductors designed on 42 mm Sendust powder cores and three 0.47 μF/450 V film capacitors. The total dimensions of the prototype (without the controller

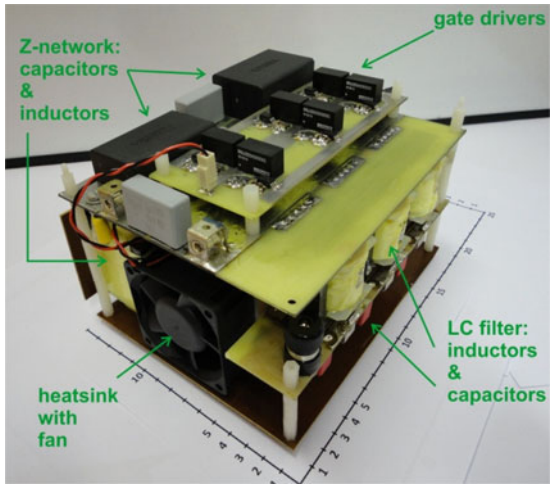

Fig. 5. Laboratory model of the 6 kVA quasi-Z-source inverter.

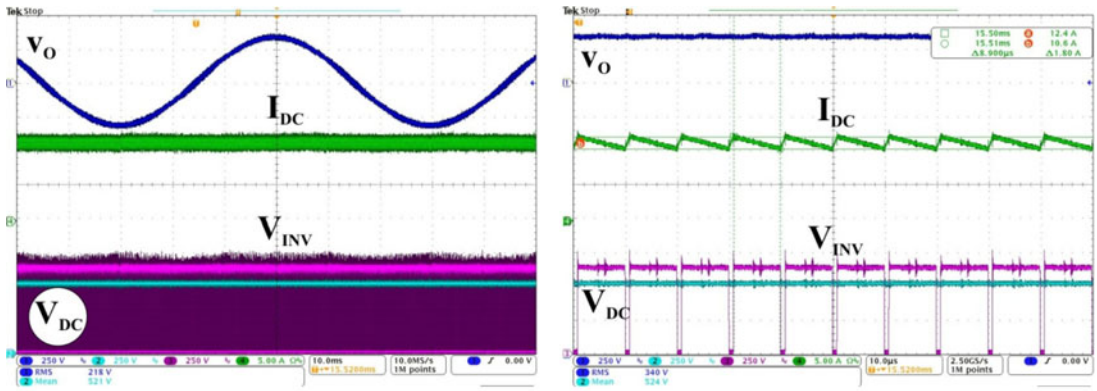

Fig. 6. Recorded oscillograms for $B = 1.2$, $V_{\rm dc} = 525$ V, $I_{\rm dc} = 12$ A, and 3 × 400 V rms on the output for the (a) 10 ms/div scale and (b) 10 μs/div scale. From the top: output voltage v_O, input current $I_{\rm dc}$, voltage across inverter $V_{\rm INV}$, and input voltage $V_{\rm dc}$.

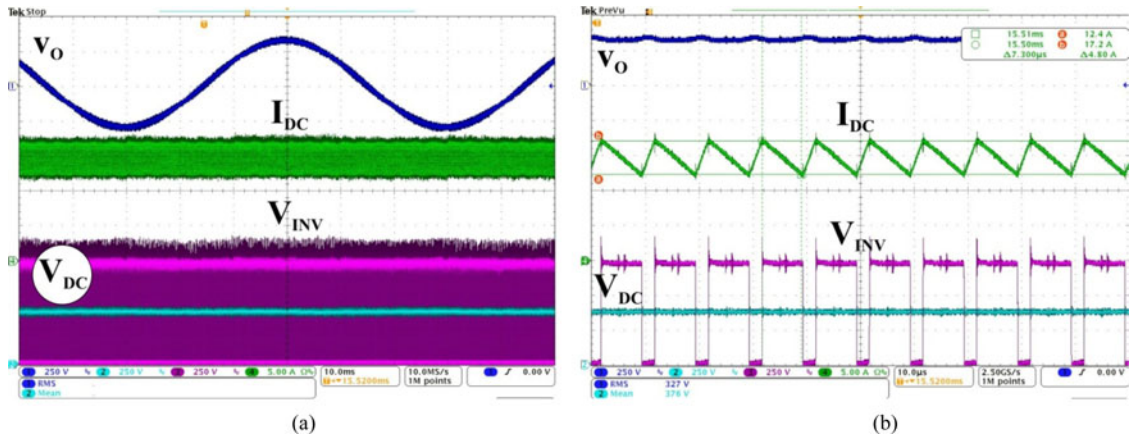

Fig. 7. Recorded oscillograms for $B = 1.9$, $V_{\rm dc} = 400$ V, $I_{\rm dc} = 15$ A, and 3 × 400 V rms on the output for the (a) 10 ms/div scale and (b) 10 μs/div scale. From the top: output voltage v_O, input current $I_{\rm dc}$, voltage across inverter $V_{\rm INV}$, and input voltage $V_{\rm dc}$.

TABLE II
PARAMETERS OF THE 6 KVA LABORATORY MODEL

Rated power P_N	6 kVA
Output voltage $V_{O\,(\rm rms)}$	230 V
Input voltage range	400–550 V
Switching frequency, f_s	100 kHz
Semiconductors	6 × SiC transistors (1200 V / 80 mΩ)
Semiconductors	and 1 × SiC diode (1200 V/34 A)
Z-network components	2 × ferrite inductors (250 μH/25 A)
Z-network components	2 × capacitors (30 μF/700 V and 500 V)
LC filter components	3 × inductors (100 μH/25 A)
LC filter components	3 × capacitors (0.47 μF/450 V)
Dimensions of prototype	145 × 175 × 110 mm
Volume	2.8 dm^3

and auxiliary supply) are 145 × 175 × 110 mm, which results in a volume of approximately 2.8 dm^3. This volume is higher than the estimated one of 2 dm^3 for case G [see Fig. 4(c)] as the laboratory prototype also contains other components (e.g., gate-driver circuits, connectors, etc.). It must, however, be noted that most of the converter's volume is occupied by the elements taken into account during the design process: the heatsink with the fan (26% of the total volume, 0.73 dm^3) and inductors (Z-network: 21% of the total volume and *LC* filter 11% of the total volume).

V. EXPERIMENTS

The designed prototype of the 6 kVA quasi-Z-source converter was experimentally tested under various operating conditions in order to verify the desired performance of the system. A programmable dc power source supplies the required direct voltage to the input of the converter, while the three-phase output voltage is fed to a three-phase resistive load. Key waveforms at various operating points of the quasi-Z-source inverter were recorded with a digital oscilloscope, while the input and output powers of the converter were monitored using a high-precision power analyzer (Yokogawa W1800). Figs. 6 and 7 show two oscillograms recorded at two different operating points of the converter, which confirm the proper operation of the designed prototype at nominal power and a switching frequency of 100 kHz. More specifically, the waveforms shown in Fig. 6 corresponds to an operation with $B = 1.2$ where the input voltage is boosted from 525 to 630 V. Similarly, Fig. 7 depicts the case when $B = 1.9$ and the input voltage is boosted from 385 to 750 V. The implemented MSN PWM method

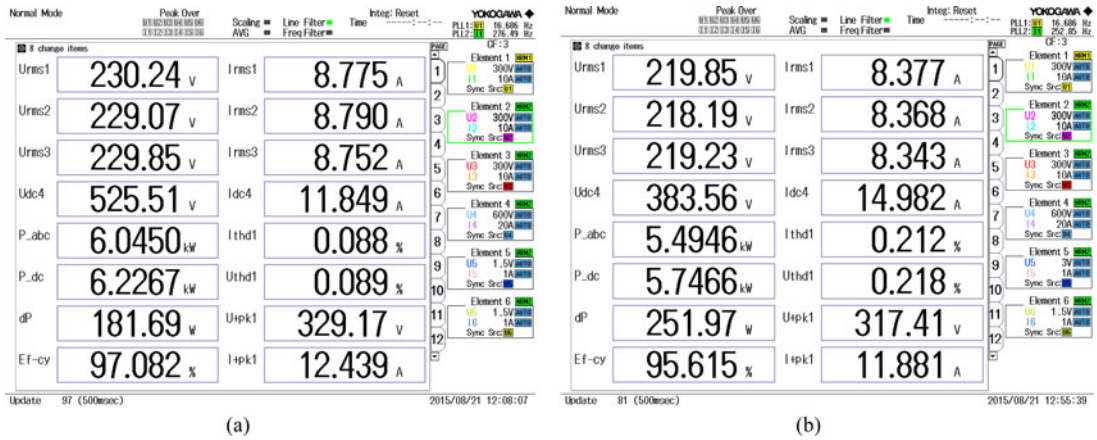

Fig. 8. Recorded screenshots of the power analyzer for efficiency measurements: (a) $B = 1.2$ and (b) $B = 1.9$.

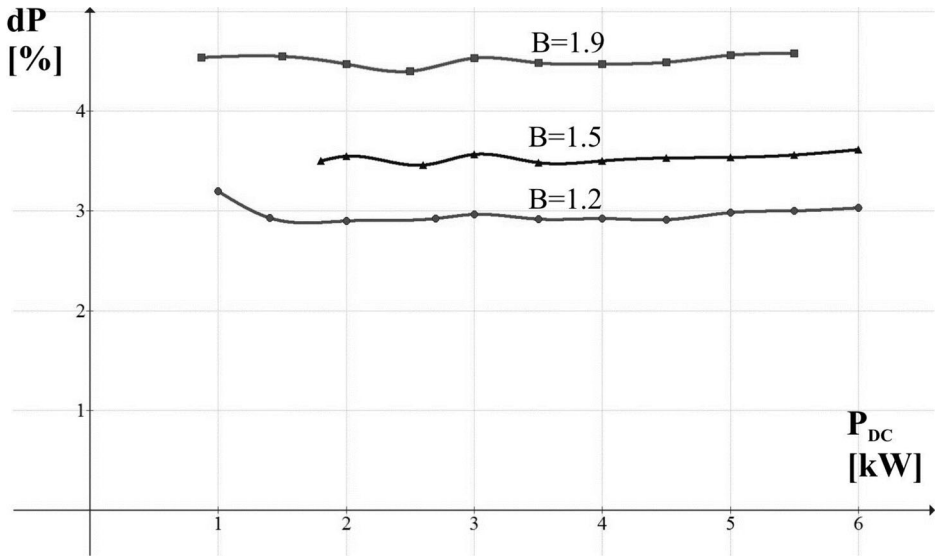

Fig. 9. Measured power losses (dP) as a function of the input power ($P_{\rm dc}$) for three different values of the boost factor B.

introduces a single ST state per switching period, and thus the frequency of the voltage across the inverter $V_{\rm INV}$ equals to switching frequency (100 kHz). The same frequency is visible in the current of the Z-network inductors. However, the peak-to-peak value of the current ripple is higher for the boost factor $B = 1.9$ ($2\Delta i_L = 4.8$ A) than for $B = 1.2$ ($2\Delta i_L = 1.8$ A). In terms of the average input current $I_{\rm dc}$, the obtained amplitudes of the current ripples Δi_L equals 16% and 7.6% of $I_{\rm dc}$, respectively.

As already mentioned earlier, power loss measurements were also performed on the experimental prototype. Fig. 8(a) and (b) shows the screenshots of the power analyzer for operation with $B = 1.2$ and $B = 1.9$, respectively. The total power losses as a function of the output power at three different values of the boost factor *B* are presented in Fig. 9. From this figure, it is clear that the power losses increase with the boost factor, and, in particular, they are the highest for $B = 1.9$ (4.4% of the nominal power). This is basically due to the increased commutation voltage $V_{\rm INV}$ and input current $I_{\rm dc}$. On the contrary, operating the converter with a boost factor of $B = 1.5$, the power losses drop to 3.5% of the nominal power, while a further decreasing of the total power losses (<3% of the nominal power) is observed for $B = 1.2$. Moreover, from Fig. 9, it is also visible that the obtained power losses of the quasi-Z-source inverter are proportional to the input power and that the efficiency is almost constant for a given value for the boost factor *B*. In addition, the obtained results come in very good agreement with the required design constraints that an efficiency higher than 95% is targeted. On the other hand, it seems that the calculated power losses summarized in Tables IV and V are lower than the corresponding measured losses on the laboratory model. The authors believe that the reason to this is the ac resistance of the inductor windings, which was neglected for the theoretical estimation of the losses, additional losses in the capacitors, resistive losses in the tracks of the power printed circuit board (PCB), and, especially, the switching performance of the SiC devices. Note that the switching energies

TABLE III
BASIC PARAMETERS OF THE SIMULATED SiC DEVICES

C2M0040120D	$r_{\mathrm{DS(ON)}}(125\,^{\circ}\mathrm{C}) = 62\,\mathrm{m}\Omega$ $E_{\mathrm{ON}} + E_{\mathrm{OFF}} = 1.4\,\mathrm{mJ}(800\,\mathrm{V}/40\mathrm{A})$	$R_{\mathrm{TH}} = 0.38 + 0.15 = 0.53\,\mathrm{K/W}$
C4D20120D	$V_{\mathrm{FO}} = 0.75\,\mathrm{V}$, $r_F = 50\,\mathrm{m}\Omega$ (two dies in parallel) $Q_c = 104\,\mathrm{nC}$ $E_{\mathrm{REC}} = 83.2\,\mu\mathrm{J}$	$R_{\mathrm{TH}} = 0.43 + 0.15\,\mathrm{K/W}$
C2M0080120D	$r_{\mathrm{DS(ON)}}(125\,^{\circ}\mathrm{C}) = 128\,\mathrm{m}\Omega$ $E_{\mathrm{ON}} + E_{\mathrm{OFF}} = 400\,\mu\mathrm{J}(20\,\mathrm{A}, 800\,\mathrm{V})$	$R_{\mathrm{TH}} = 0.65 + 0.15\,\mathrm{K/W}$

TABLE IV
POWER LOSSES AND VOLUME OF THE PASSIVE ELEMENTS (LZ, Z-NETWORK INDUCTORS; CZ, Z-NETWORK CAPACITORS; LF, FILTER INDUCTORS; CF, FILTER CAPACITORS)

Case	P_{LZ} (%)	P_{LF} (%)	V_{LZ} (dm^3)	V_{CZ} (dm^3)	V_{LF} (dm^3)	V_{CF} (dm^3)	V (dm^3)
A and C	0.53	0.6	1.57	0.494	2.05	0.215	4.329
B	0.57	0.6	2.24	0.988	2.05	0.215	5.493
D and F	0.226	0.23	0.382	0.049	0.48	0.022	0.933
E and G	0.33	0.23	0.66	0.093	0.48	0.022	1.255
H	0.29	0.18	0.56	0.067	0.37	0.016	0.68

TABLE V
POWER LOSSES SIMULATED IN GECKO FOR THE WORST CASE $B = 1.9$ AND $V_{\mathrm{dc}} = 400\,\mathrm{V}$ (P_{CT}, TRANSISTOR CONDUCTION; $\mathrm{P_{SWT}}$, TRANSISTORS SWITCHING; P_T, TRANSISTORS; P_{CD}, DIODE D_0 CONDUCTION; P_{SWD}, DIODE D_0 SWITCHING; P_S, TOTAL SEMICONDUCTORS), REQUIRED THERMAL RESISTANCE R_{THCA}, AND VOLUME OF THE COMMON HEATSINK V_H

Case	P_{CT} (W)	P_{SWT} (W)	P_{T} (W)	P_{CD} (W)	P_{SWD} (W)	P_{D} (W)	P_S (W)	dP_S (%)	R_{THCA} (K/W)	V_H (dm^3)
A	22.4	35.3	57.7	27.6	2.1	29.7	87.4	1.46	0.942	0.354
B	22.4	17.7	40.1	27.6	1.1	28.7	68.8	1.15	1.211	0.275
C	45.6	18.4	64	27.4	2.1	29.5	93.5	1.56	0.9	0.37
D	22.5	347.4	369.4	27.5	21.1	48.6	418	7	0.121	2.75
E	22.5	173.7	196.2	27.5	10.5	38	234.2	3.9	0.333	1
F	45.4	183.4	228.8	27.4	21	48.4	277.2	4.62	0.25	1.33
G	45.4	91.71	137.1	27.4	10.5	37.9	175	2.91	0.446	0.75
H	45.4	136.8	182.5	27.6	16.4	44	226.5	3.78	0.334	1

obtained from the manufacturer datasheets of SiC MOSFETs (see Table II) are determined using a double-pulse test circuit under a constant direct voltage. The devices in quasi-Z-source inverter, however, are switching without a real direct voltage (Z-network inductor and capacitor in series), and, therefore, the switching performance may be worse than the expected from datasheets.

VI. SUMMARY

A 6-kVA quasi-Z-source inverter equipped with SiC power semiconductor devices was designed using an optimization procedure based on simulations, calculations, and system volume estimations. Several cases were analyzed in terms of power losses and power density in order to find the optimal parameters of the system. It is shown that the optimal design parameters are a switching frequency of 100 kHz, the MSN PWM modulation method with a single ST per switching period and employing 80 mΩ SiC MOSFETs. Using the optimal design parameters, a laboratory prototype of the quasi-Z-source inverter was built. The resulting power density of the whole system was found to be slightly higher than 2 kW/dm^3. This number for the power density of the converter, as well as an efficiency of approximately 95.6% measured at the worst-case conditions (boost factor $B = 1.9$), fulfill the initial design constraints. Moreover, when the input voltage increases to 525 V ($B = 1.2$), the power losses drop below 3% of the nominal power, which correspond to an efficiency well above 97%. Last but not least, all presented results confirm the beneficial influence of SiC power devices on the performance of the quasi-Z-source inverter. It is very possible that the same effects may be achieved for other topologies from the family of impedance source converters, as, for example, other modifications of the quasi-Z-source inverter aiming in an extended voltage regulation range.

APPENDIX A

See Tables III–V.

APPENDIX B: DESIGN OF THE Z-SOURCE INDUCTORS

Based on the information shown in Table I, five cases for the Z-source inductors were considered. These are listed as follows:

1) $L = 2.5\,\mathrm{mH}$ at $f = 10\,\mathrm{kHz}$
2) $L = 1.25\,\mathrm{mH}$ at $f = 20\,\mathrm{kHz}$
3) $L = 250\,\mu\mathrm{H}$ at $f = 100\,\mathrm{kHz}$
4) $L = 180\,\mu\mathrm{H}$ at $f = 150\,\mathrm{kHz}$
5) $L = 125\,\mu\mathrm{H}$ at $f = 200\,\mathrm{kHz}$

TABLE VI
DESIGN PARAMETERS OF THE CONSIDERED FIVE CASES OF INDUCTORS EMPLOYED IN THE Z-NETWORK

Inductor	Number of Stacked Cores and Core Shape	Core Losses (W)	Copper Losses (W)	Number of Turns	Number of Parallel-Connected Litz Wires	Air Gap (mm)	Temperature at Full Current (Steady State)	Volume (L)
$L = 2.5\,\mathrm{mH}$ at f = 10 kHz	Three stacked cores Magnetics, 0P49928EC (EE-core 100.3 mm)	3.03	14.15	74	6	6	108 °C	1.12
$L = 1.25\,\mathrm{mH}$ at $f = 20\,\mathrm{kHz}$	Two stacked cores Magnetics, 0P49928EC (EE-core 100.3 mm)	2.02	14.4	64	5	6	104.9 °C	0.785
$L = 250\,\mu\mathrm{H}$ at $f = 100\,\mathrm{kHz}$	Magnetics, 0P48020EC (EE-core 80 mm)	1.45	8.6	39	4	3	78.08 °C	0.333
$L = 180\,\mu\mathrm{H}$ at $f = 150\,\mathrm{kHz}$	Magnetics, 0P46527EC (EE-core 80 mm)	1.59	7.3	33	4	3	73.97 °C	0.28
$L = 125\,\mu\mathrm{H}$ at $f = 200\,\mathrm{kHz}$	Magnetics, 0P46527EC (EE-core 65 mm)	3.16	3.6	19	4	2	64.33 °C	0.191

Various design parameters of the Z-source inductors were calculated assuming ferrite EE-shape cores. Table VI summarizes the detailed design parameters for each of the aforementioned Z-source inductors.

Moreover, in order to have a fair comparison litz wire even considered for the two low-frequency designs. For all cases, litz wire having 120 strands of 0.1 mm diameter each considered (0.94 mm^2 of cross-section area). In all cases, the temperature rise in the core was considered to be lower than (or approximately) 100 °C. Thus, in the case of $L = 1.25\,\mathrm{mH}$ and $L = 2.5\,\mathrm{mH}$, respectively, six and five parallel-connected litz wires are required in order to meet the temperature design constraints. However, in the rest of the cases, four parallel-connected litz wires are used, so that the rated current can safely flow and hence the temperatures in those cases are relatively lower.

The first set of calculations was performed assuming EE shape cores. In particular, for the case of 1.25 and 2.5 mH inductors, and due to the thermal design of the inductor, ferrite cores in EE-shape might not be available from manufacturers. Thus, the largest EE-shape ferrite cores, which were stacked, were assumed in these two cases.

Regarding the core losses, a few conclusions can also be drawn. First, it must be noted that the core losses depend on the induction level and the frequency, as well as the volume of the core. In the case of $L = 2.5\,\mathrm{mH}$ and $L = 1.25\,\mathrm{mH}$, three and two cores were stacked, respectively, in order to meet the desired temperature rise and to fit the number of turns within the core window. This means that for the same flux density level, the core losses are relatively high, regardless of the fact that the targeted frequency is low. On the other hand, comparing cases 3 and 4 with the case 5, it reveals that even though a smaller core is used in case 5, the corresponding core losses are higher. This is due to the higher frequency (200 kHz) in case 5.

The copper losses are basically governed by the length of the winding and the cross-section area. In cases 1 and 2, for instance, the windings are long and, thus, the copper losses are also higher compared to cases 3, 4, and 5. Another important loss contribution is the eddy-current losses. These depend on the thickness of the winding and the frequency (material as well, but copper is used in all cases). However, since litz wire is considered in all five cases, the associated eddy-current losses are negligible.

REFERENCES

[1] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE Power Electron. Spec. Conf.*, June 15–19, 2008, pp. 2743–2749.

[2] Y. Liu, H. Abu Rub, and G. Baoming, "Z-source/quasi-Z-source inverters: Derived networks, modulations, controls and emerging applications to photovoltaic conversion," *IEEE Ind. Electron. Mag.*, vol. 8, no. 4, pp. 32–44, Dec. 2014.

[3] F. Guo, L. X. Fu, C. H. Lin, C. Li, W. Choi, and J. Wang, "Development of an 85-kW bidirectional quasi-Z-source inverter with DC-link feed-forward compensation for electric vehicle applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5477–5488, Dec. 2013.

[4] Y. Liu, B. Ge, F. Z. Peng, A. R. Haitham, A. T. de Almeida, and F. J. T. E. Ferreira, "Quasi Z-source inverter based PMSG wind power generation system," in *Proc. 2011 IEEE Energy Conversion Congress Expo.*, Sep. 17–22, pp. 291–297.

[5] Y. Li, J. Anderson, F. Z. Peng, and D. Liu, "Quasi-Z-source inverter for photovoltaic power generation systems," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 15–19, 2009, pp. 918–924.

[6] Y. Zhou, L. Liu, H. Li, "A high-performance photovoltaic module-integrated converter (MIC) based on cascaded quasi-z-source inverters (qZSI) using eGaN FETs," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2727–2738, Jun. 2013.

[7] B. Ge, H. Abu-Rub, F. Peng, Q. Lei, A. de Almeida, F. Ferreira, D. Sun, and Y. Liu, "An energy stored quasi-Z-source inverter for application to photovoltaic power system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4468–4481, Oct. 2013.

[8] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "An effective control method for quasi-Z-source cascade multilevel inverter based grid-tie single-phase photovoltaic power system," *IEEE Trans. Ind. Informat.*, vol. 10, no. 1, pp. 399–407, Feb. 2014.

[9] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, and L. K. Siow, "Extended-boost Z-source inverters," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2642–2652, Oct. 2010.

[10] M. K. Nguyen, Y. C. Lim, and G. B. Cho, "Switched-inductor quasi-Zsource inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3183–3191, Nov. 2011.

[11] D. Vinnikov and I. Roasto, "Quasi-Z-source based isolated DC/DC converters for distributed power generation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 192–201, Jan. 2011.

[12] D. Vinnikov, I. Roasto, R. Strzelecki, and M. Adamowicz, "Step-up DC/DC converters with cascaded quasi-Z-source network," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3727–3736, Oct. 2012.

[13] S. Yang, F. Z. Peng, Q. L. Inoshita, and R. Z. Qian, "Current-fed quasi-Z-source inverter with voltage buck–boost and regeneration capability," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 882–892, Mar./Apr. 2011.

[14] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and S. Stepenko, "Single phase three-level neutral-point-clamped quasi-Z-source inverter," *IET Power Electron.*, vol. 8, no. 1, pp. 1–10, 2015.

[15] D. Sun, B. Ge, W. Liang, H. Abu-Rub, and F. Z. Peng, "An energy stored quasi-Z-source cascade multilevel inverter-based photovoltaic power generation system," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5458–5467, Sep. 2015.

[16] J. Milan, P. Gondignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[17] J. Rabkowski, D. Peftitsis, and H. P. Nee, "SiC power transistors—A new era in power electronics is initiated," *IEEE Ind. Electron. Mag.*, vol. 6, no. 2, pp. 17–26, Jun. 2012.

[18] A. Bindra, "Wide-bandgap power devices: Reshaping the power electronics landscape," *IEEE Power Electron. Magazine*, vol. 2, no. 1, pp. 42–47, Mar. 2015.
[19] J. Rąbkowski, M. Zdanowski, and R. Barlik, "Silicon carbide inverter with two series Z-networks," in *Proc. 20th IEEE Int. Symp. Ind. Electron.*, Gdańsk, Poland, Jun. 27–30, 2011, pp. 372–377.
[20] Y. Zhou, L. Liu, and H. Li, "A high-performance photovoltaic module-integrated converter (MIC) based on cascaded quasi-z-source inverters (qZSI) using eGaN FETs," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2727–2738, Jun. 2013.
[21] O. Husev, C. Roncero-Clemente, D. Vinnikov, and T. Jalakasa, "Three-level three-phase quasi-Z-source neutral-point-clamped inverter with novel modulation technique for photovoltaic application," *Electric Power Syst. Res.*, vol. 130, pp. 10–21, Jan. 2016.
[22] O. Husev, S. Stepenko, C. Roncero-Clemente, E. Romero-Cadaval, and R. Strzelecki, "Experimental investigation of high frequency 3L-NPC qZS inverter for photovoltaic application," in *Proc. 39th Annual Conf. IEEE Ind. Electron. Society*, Nov. 2013, pp. 5969–5974.
[23] W.-T. Franke, M. Mohr, and F. W. Fuchs, "Comparison of a Z-source inverter and a voltage-source inverter linked with a DC/DC-boost-converter for wind turbines concerning their efficiency and installed semiconductor power," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 15–19, 2008, pp. 1814–1820.
[24] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 770–778, May/Jun. 2006.
[25] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "Overview of space vector modulations for three-phase Z-source/quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2098–2108, Apr. 2014.
[26] Y. Tang, S. Xie, and J. Ding, "Pulsewidth modulation of Z-source inverters with minimum inductor current ripple," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 98–106, Jan. 2014.
[27] J. Rabkowski, M. Nowak, and R. Barlik, "Pulse width modulation methods for bidirectional/high-performance Z-source inverter," in *Proc. Power Electron. Spec. Conf.*, June 15–19, pp. 2750–2756.
[28] J. Rabkowski, "Improvement of Z-source inverter properties using advanced PWM methods," in *Proc. 13th Eur. Conf. Power Electron. Appl.-EPE'09*, p. 1–9.
[29] D.-W. Chung, S.-K. Sul, "Minimum-loss PWM strategy for 3-phase PWM rectifier," in *Proc. Power Electron. Specialists Conf.*, 1997, vol. 2, pp. 1020–1026.
[30] M. Kasper, C.-W. Chen, D. Bortis, J. W. Kolar, and G. Deboy, "Hardware verification of a hyper-efficient (98%) and super-compact (2.2kW/dm3) isolated AC/DC telecom power supply module based on multi-cell converter approach," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 65–71.
[31] D. Boillat, F. Krismer, and J. Kolar, "Design space analysis and ρ-η Pareto optimization of LC output filters for switch-mode AC power sources," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6906–6923, Dec. 2015.
[32] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical converter power density limits for forced convection cooling," in *Proc. Int. PCIM Europe 2005 Conf.*, Nuremberg, Germany, Jun. 7–9, pp. 608–619.

Mariusz Zdanowski (S'09–M'16) was born in Milanowek, Poland, in 1985. He received the M.Sc. degree in electrical engineering and the Ph.D. degree in electrical engineering from the Institute of Control and Industrial Electronics, Warsaw University of Technology, Warsaw, Poland, in 2009 and 2015, respectively.

In 2011, he spent four months at the Laboratory of Electrical Energy Conversion, KTH Royal Institute of Technology, Stockholm, Sweden, where he was involved in research on the parasitic capacitance of inductors cooperating with fast switching silicon carbide devices. His current research interests include power electronic converters, silicon carbide devices and magnetic components for high-frequency operation.

Dimosthenis Peftitsis (S'03–M'13–SM'15) was born in Kavala, Greece, in 1985. He received the Diploma (Hons.) in electrical and computer engineering from the Democritus University of Thrace, Xanthi, Greece, in 2008, and the Ph.D. degree from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2013.

In 2008, he was with the ABB Corporate Research, Västerås, Sweden, for six months, where he was involved in the diploma thesis. From 2013 to 2014, he was a Postdoctoral Researcher involved in the research on SiC converters in the Department of Electrical Energy Conversion, KTH Royal Institute of Technology. Since 2014, he has been working as a Postdoctoral Fellow at the Lab for High Power Electronics Systems, ETH Zurich, where he is currently involved in dc breakers for multiterminal HVDC systems. In May 2016, he will be with the Norwegian University of Science and Technology in Trondheim, Norway, as an Associate Professor of Power Electronics in the Department of Electrical Power Engineering. His current research interests include SiC power converters design, gate and base driver design for SiC JFETs and BJTs, as well as dc-breaker concepts for HVDC systems.

Szymon Piasecki (S'10–M'16) was born in Nidzica, Poland, in 1985. He received the M.Sc. degree in automatics and robotics from the Faculty of Electrical Engineering, Warsaw University of Technology, Poland, in 2009, where he is currently working toward the Ph.D. degree.

In 2009, he spent five months in Mondragon University, Mondragon, Spain, working on the diploma thesis. In 2011, he was in Polytechnic University of Catalonia, Barcelona, Spain, for five months, where he was involved in SEER Research Group activities. His current research interests include problems of power quality, grid connected converters design, advanced topologies of the grid filters and, recently, multi-objective optimization in power electronics.

Jacek Rabkowski (M'10–SM'14) received the M.Sc. and Ph.D. degrees both in electrical engineering from Warsaw University of Technology, Warsaw, Poland, in 2000 and 2005, respectively.

In 2004, he joined the Institute of Control and Industrial Electronics, Warsaw University of Technology, where he is currently a Professor in Power Electronics. During the years 2010–2013, he was also with the Laboratory of Electrical Energy Conversion at KTH Royal Institute of Technology in Stockholm, Sweden. His current research interests include power converters based on wide band-gap devices (SiC and GaN): topologies, design aspects, pulsewidth modulation techniques, control systems but also design of base and gate drivers.

Dr. Rabkowski was a Chairman of the Joint Industrial Electronics Society/Power Electronics Society Chapter in the frame of the IEEE Poland Section in 2012–2015. He has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2015.