Novel Family of Single-Phase Modified Impedance-Source Buck-Boost Multilevel Inverters With Reduced Switch Count

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***Abstract*—This paper describes novel single-phase solutions with increased inverter voltage levels derived by means of a nonstandard inverter configuration and impedance source networks. Operation principles based on special modulation techniques are presented. Detailed component design guidelines along with simulation and experimental verification are also provided. Possible application fields are discussed, as well as advantages and disadvantages. Finally, future studies are addressed for the new solutions.**

***Index Terms*—Impedance-source inverters, multilevel systems, switching harmonics.**

I. Introduction

RECENT solutions based on the impedance networks are applied in various fields. Z-source inverters (ZSIs) [see Fig. 1(a)] and quasi-Z-source inverters (qZSIs) [see Fig. 1(b)] were proposed for low-voltage energy sources grid integration in [1] and [2]. ZSIs overcome the limitation of the conventional grid-connected inverters: they have a buck, a boost, and do not suffer from shoot-through (ST) states. ZSIs and qZSIs utilize the cross-conduction states to boost the input dc voltage by switching on both the top and bottom switches of at least one inverter branch. The main advantage of the qZSI over the ZSI is the continuous input current from the input source; moreover, it shares a common ground with a dc source, which is suitable for renewable energy sources and other applications [3]–[13]. These inverters are capable of performing maximum power point tracking with no need for an extra dc–dc converter stage.

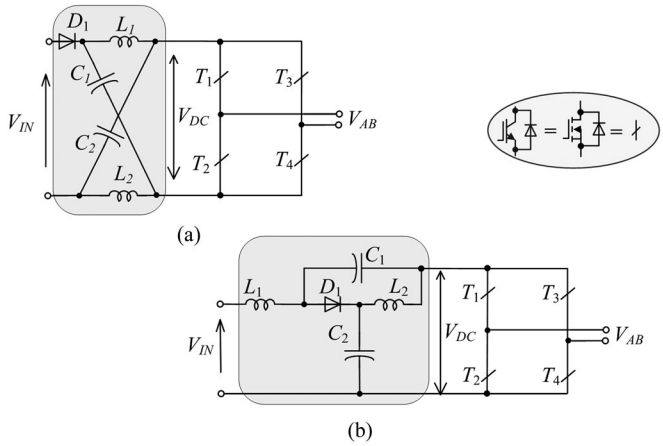

Fig. 1. Conventional (a) two-level ZSI and (b) qZSI.

At the same time, a novel trend in power electronics lies in the modular and multilevel converter applications. Multilevel converters have major advantages over the conventional and very well-known two-level converters. These advantages consist in the improvements of the output power quality or reduced size of the output filter. Typically, multilevel solutions belong to the larger nominal power in the converter [14]–[17]. At the same time, today's multilevel converters are becoming a good solution for low-power and low-voltage applications as well. Reduced voltage stress allows using fast MOSFET semiconductors in the industrially verified Si technologies.

The single-stage buck–boost multilevel inverter was proposed in [18] as a logical extension of the two-level inverter and the ZSI. The combination of any impedance source (IS) networks with multilevel or cascaded inverters gives a single-stage energy conversion with the buck–boost capability. By the introduction of the high-frequency transformer and two additional capacitors, the Z-source neutral-point-clamped (NPC) inverter with a single IS network could be supplied from a single dc source [19]–[23]. Moreover, by a transformer with a turns ratio different from 1:1, an input voltage gain higher than that with the conventional Z-source network could be achieved. Comprehensive studies of the multilevel ZSIs are reported in [24]–[32]. In [32] and [33], a comprehensive study of the Trans-Z-source and Γ-source NPC

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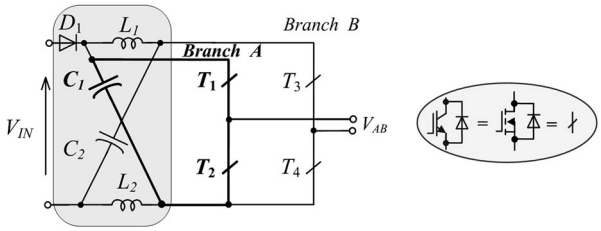

Fig. 2. Single-phase MZSI.

inverters has been reported, where the discontinuous input current during the boost conversion mode is a common drawback of the abovementioned solutions. It could have a negative influence on the input voltage source, especially by using it in the renewable energy sources.

Several papers have covered the comprehensive studies of three-level (3L) NPC qZSI [34]–[37]. The proposed solution combines the above mentioned advantages along with continuous input current.

At the same time, the use of a pure dc link is the main problem of ZSI and qZSI. In order to overcome this problem, IS networks based on coupled inductors have been proposed. Moreover, 3L NPC solutions have already been reported in [38]–[40]. The common drawback of any IS solution based on the coupled inductors lies in the leakage inductance, which leads to current and voltage spikes across the semiconductors [41]. Along with the drawbacks mentioned, the ZSI and qZSI have some hidden capabilities for output quality improvement.

This paper presents several novel single-phase solutions with increased inverter voltage levels derived by means of a nonstandard inverter configuration and IS networks. The first attempts were made in [42] where a general idea is presented. Also, it is patented in [43] and [44]. The hypothesis about the improvement of the output voltage quality was proved by means of a theoretical and simulation study. This paper provides detailed component design guidelines and also an experimental verification.

II. Proposed Novel Single-Phase IS Multilevel Inverters

The proposed single-phase modified ZSI (MZSI) is shown in Fig. 2. It is based on the full-bridge (FB) inverter and single ZS network. Branch A is connected in parallel with the capacitor C_1, while branch B is connected to the terminals of the ZS networks. In this solution, only branch B is in response to the ST generation. Branch A operates in the conventional voltage source inverter (VSI) mode, where the ST state is forbidden.

It is well known that the peak dc-link voltage along with the capacitor voltage is defined as [1]–[3]

$$V_C = V_{C1} = V_{C2} = \frac{(1 - D_S)}{(1 - 2 \cdot D_S)} \cdot V_{\mathrm{IN}} \tag{1}$$

$$V_{\mathrm{DC}} = \frac{1}{1 - 2 \cdot D_S} \cdot V_{\mathrm{IN}} \tag{2}$$

where D_S is the ST duty cycle, V_{DC} is a peak dc-link voltage, V_{IN} is a dc input voltage,V_{C1}, V_{C2} are the capacitor voltages.

It is revealed that the difference lies in the ST duty cycle. In the modified solution, the dc-link voltage applied to the output ac side has a higher peak value and a zero state value, which should be taken into account in the modulation technique. On the other hand, the capacitor voltage has a lower peak value but can be applied continuously. It means that the dc-link voltage and the capacitor's voltage have an equal average value and can be applied in turn.

Another conclusion is that such an approach can be extended to any IS network, which has the same ratio between the dc-link voltage and one of the capacitor's voltage.

Fig. 3 shows the family of the modified qZSIs (MqZSIs). The first single-phase qZS-based solution is illustrated in Fig. 3(a). It has a single qZS network and one FB in the nonstandard configuration. Branch A is connected in parallel with the capacitor C_2 while branch B is connected to the positive terminal of the capacitor C_1 and the negative terminal of the capacitor C_2. Branch B is in response to ST generation. Branch A operates in conventional VSI mode where ST states are forbidden. The next derivation is described in Fig. 3(b). Since it has a symmetrical configuration, it can be titled as a single-phase symmetrical MqZSI. Fig. 3(c) shows a single-phase NPC MqZSI solution. The single-phase NPC MqZSI has two qZS networks and one single-phase NPC inverter.

The first branch A is connected in parallel with the capacitors C_2 and C_3, while branch B is connected to the positive terminal of the capacitor C_1 and the negative terminal of the capacitor C_4. Branch B is in response to ST generation. Branch A operates in the conventional VSI mode, where ST states are forbidden. As mentioned above, such an approach of the derivation can be applied for any kind of IS network, where the average dc-link voltage and average capacitor's voltage are equal.

Similarly to Fig. 3, other types of the family of the buck–boost modified IS inverters (MISI) can be obtained; Fig. 4 shows some of them. In particular, Fig. 4(a) shows the asymmetrical modified T-source inverter (MTSI). It is well known that the peak dc-link voltage along with the capacitor voltage for the T-source network are defined as [20] and [38]

$$V_{C1} = \frac{1 - D_S}{1 - (1 + n)D_S} \cdot V_{\mathrm{IN}} \tag{3}$$

$$V_{\mathrm{DC}} = \frac{1}{1 - (1 + n)D_S} \cdot V_{\mathrm{IN}} \tag{4}$$

where *n* is the turns ratio between the coupled inductors.

The LCCT Z-source circuit is an inductor–capacitor–capacitor–transformer Z-source circuit. LCCT Z-source and quasi-Z-source have been presented in [45] and [46]. Despite on different configurations the boost factor of the LCCT Z-source and quasi-Z-source circuits is similar to the T-source network [see Fig. 4(b)].

Γ-Z-source network [47] contains a coupled inductor as well. The peak dc-link voltage and the capacitor voltage are different

$$V_{C1} = \frac{1 - D_S}{1 - \frac{n}{n-1} \cdot D_S} \cdot V_{\mathrm{IN}} \tag{5}$$

$$V_{\mathrm{DC}} = \frac{1}{1 - \frac{n}{n-1} \cdot D_S} \cdot V_{\mathrm{IN}}. \tag{6}$$

Because of equal average dc-link voltage and average capacitor's voltage the asymmetrical modified Γ-Z-source inverter is

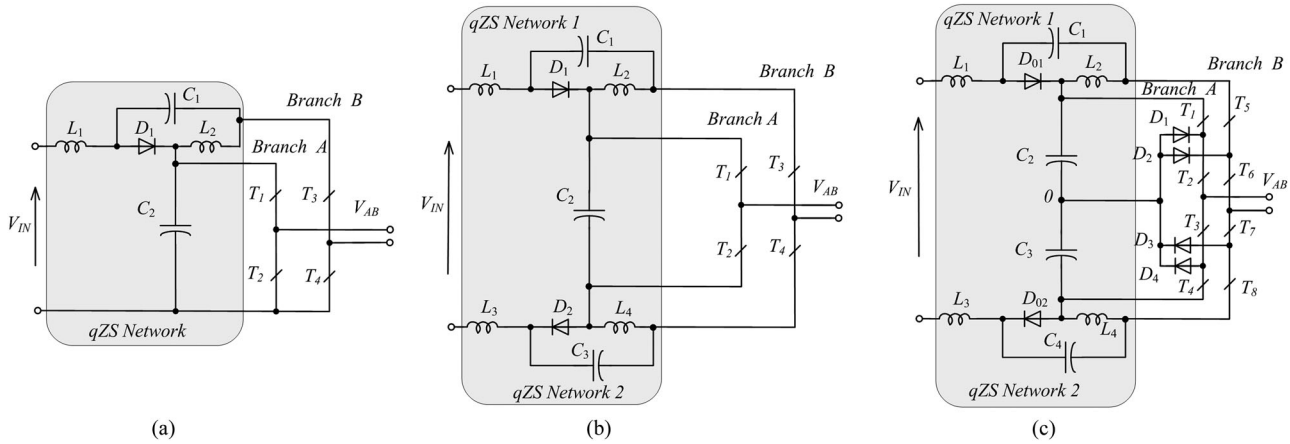

Fig. 3. Family of the single-phase MqZSI: (a) Asymmetrical MqZSI; (b) symmetrical MqZSI; and (c) NPC MqZSI.

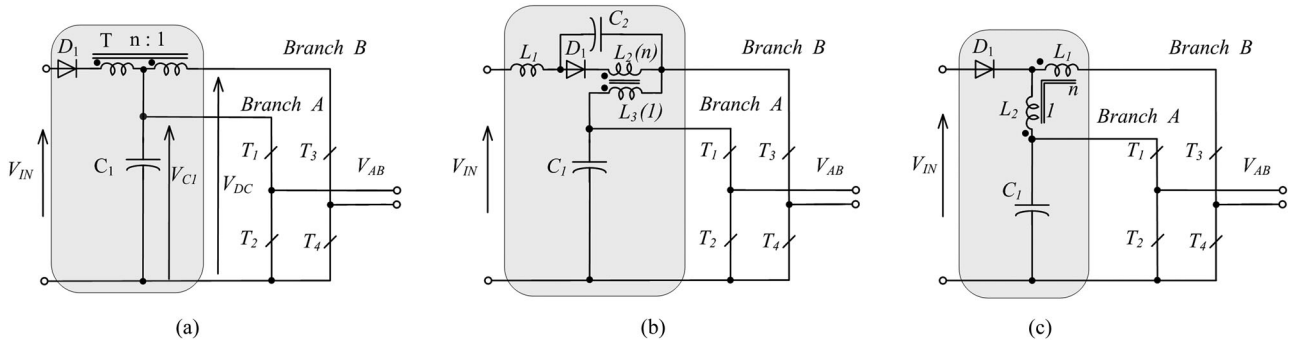

Fig. 4. Single-phase asymmetrical MISIs: (a) MTSI; (b) modified LCCT Z-source inverter; and (c) modified Γ-Z-source inverter.

shown in Fig. 4(c). It is evident that symmetrical and NPC modified inverters based on the above presented solutions can be obtained as well.

Next sections of the paper are devoted to the modulation techniques and component design guidelines. MZSI and MqZSI are under a detailed study. However, it can be extended to any other similar modifications.

III. Special Modulation Techniques and THD Estimation

In order to perform simulation and experimental verifications, special modulation techniques were chosen to involve all switching states and to achieve the best output voltage quality. Fig. 5 shows a sketch of the proposed modulation techniques that can cover all the solutions presented above.

In particular, the modulation technique illustrated in Fig. 5(a) can be used for all four-switch symmetrical and asymmetrical solutions. Reference signal *Ref A* is in response to branch A voltage generation. Modulation index M_A can vary from 0 up to 1. Reference signal *Ref B* is in response to branch B voltage generation. Modulation index M_B can vary from 0 up to 1–D_S. Carrier signal *Carrier1* is in response to the switching generation. The simple example of T_1 and T_3 transistor switching is also illustrated in Fig. 5(a). ST is generated by means of two envelope lines $1 - D_S$, $D_S - 1$ and the signal *Carrier1*.

Table I shows all possible levels of the inverter voltage in the case of the asymmetrical MZSI or MqZSI [see Figs. 2 and 3(a)]. It has four levels instead of three in the traditional FB configuration. At the same time, the positive and the negative level are different. The ST states are outlined in Table I. Also, the forbidden states are illustrated in Table I. It is evident that branch A works like in the conventional VSI mode and applies a restriction to the switching states.

The same modulation technique can be applied for the symmetrical MqZSI [see Fig. 3(b)]. It is evident that due to the symmetrical structure symmetrical six levels of the inverter voltage can be derived. These levels are summarized in Table II. However, the traditional classification of the number of levels per branch is not useful since the inverter has a modified configuration.

Analysis of reveals that there is no zero voltage level. The smallest inverter voltage level corresponds to the ST states. The overall amount of levels is six, which is larger than in the conventional FB solution. At the same time, ST immunity is lost in such a topology since branch A works in the VSI mode.

In conclusion, the symmetrical case has three levels in advance, while the asymmetrical case has only one. Moreover, in the asymmetrical case, the positive and the negative voltage waveforms are formed by a different set of levels. The modulation technique depicted in Fig. 5(b) can beTable IIused for the NPC MqZSI solution [see Fig. 3(c)] or any other NPC MISI.

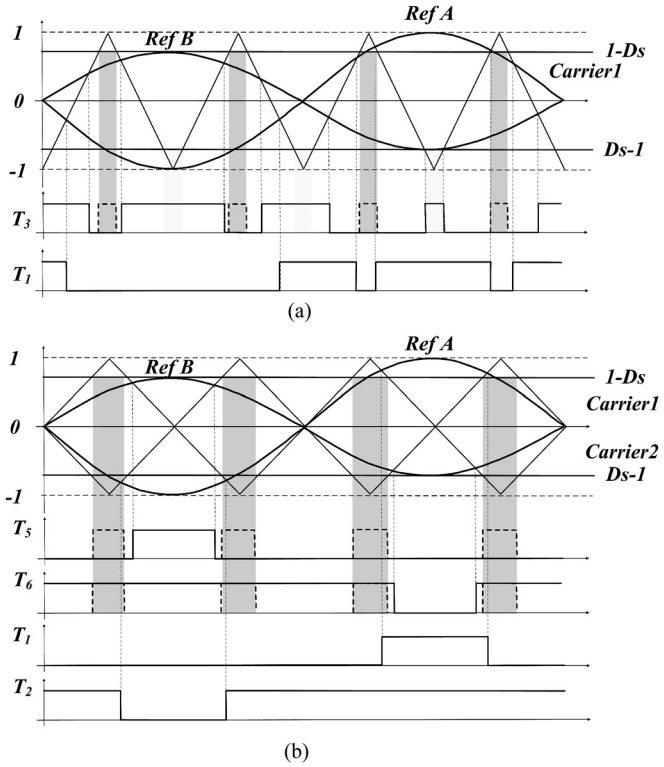

Fig. 5. Modulation technique for single-phase buck–boost MISI family: (a) Four-switch symmetrical and asymmetrical solutions; and (b) NPC MqZSI solution.

TABLE I
SWITCHING STATES FOR A SINGLE-PHASE ASYMMETRICAL MZSI AND MQZSI

N	T_1	T_2	T_3	T_4	Voltage level V_{AB}
1	1	0	0	1	V_{C2}
2	0	1	0	1	0
3	1	0	1	1	$\mathrm{V_C}$
4	0	1	1	1	0
5	1	0	1	0	$-(V_{\mathrm{DC}}-V_{C2})$
6	0	1	1	0	$-V_{\mathrm{DC}}$
7	1	1	x	X	Forbidden state

Finally, Table III shows all the possible levels of the inverter voltage. It has nine levels instead of five in the conventional 3L (three levels per single branch) NPC configuration. At the same time, the positive and the negative levels are different.

IV. COMPONENT DESIGN GUIDELINES

Any single-phase inverter has low-frequency current ripple because of power fluctuating. In order to provide component design guidelines, high-frequency with low-frequency current and voltage ripples should be taken into account. Therefore, the steady-state analysis along with small-signal averaging method is presented.

Fig. 6 shows the equivalent circuit of the asymmetrical MqZSI. It should be mentioned that this model includes a resistor *R,* which represents losses in the IS network.

TABLE II
SWITCHING STATES FOR SINGLE-PHASE SYMMETRICAL MQZSI

N	T_1	T_2	T_3	T_4	Voltage level V_{AB}
1	1	0	0	1	$V_{C3}+V_{C2}$
2	0	1	0	1	V_{C3}
3	1	0	1	1	$V_{C2}/2$
4	0	1	1	1	$-V_{C2}/2$
5	1	0	1	0	$-V_{C1}$
6	0	1	1	0	$-(V_{C1}+V_{C2})$
7	1	1	x	X	Forbidden state

TABLE III
SWITCHING STATES FOR A SINGLE-PHASE NPC MQZSI

N	T1	T2	T5	T6	Voltage level V_{AB}
1	1	1	0	0	$V_{C2}+V_{C3}+V_{C4}$
2	0	1	0	0	$V_{C3}+V_{C4}$
3	1	1	0	1	V_{C2}
4	0	0	0	0	V_{C4}
5	0	1	0	1	0
6	1	1	1	1	$-V_{C1}$
7	0	0	0	1	$-V_{C3}$
8	0	1	1	1	$-(V_{C1}+V_{C2})$
9	0	0	1	1	$-(V_{C1}+V_{C2}+V_{C3})$
10	1	1	1	1	V_{C2}
11	0	1	1	1	0
12	0	0	1	1	$-V_{C3}$

All the states strictly correspond to the states revealed in Table I. The output side of the inverter is represented by means of dc and ac current sources. It models the power flow from the input to the grid or load through the dc link.

It has constant and variable components, which is the characteristic of a single-phase system

$$i_{\mathrm{AB}} = I_{\mathrm{AB}} + \tilde{i}_{\mathrm{AB}}, \quad \tilde{i}_{\mathrm{AB}} = I_{\mathrm{MAX}} \cdot \sin(m\omega t) \tag{7}$$

where I_{AB} is a constant component of the load current, $\tilde{i}_{\mathrm{AB}}$ is a variable component, I_{MAX} is the peak value of the variable component. Both I_{AB} and $\tilde{i}_A B$ will have influence on the state variables of the system, including i_{IN}, i_{L2}, v_{C1}, and v_{C2}, all of which consist of two parts: the dc component and the number of $m\omega$ components

$$\begin{aligned} i_{\mathrm{IN}} = \; & I_{\mathrm{IN}} + \tilde{i}_{\mathrm{IN}}, i_{L2} = I_{L2} + \tilde{i}_{L2} v_{C1} = V_{C1} \\ & + \tilde{v}_{C1}, v_{C2} = V_{C2} + \tilde{v}_{C2}. \end{aligned} \tag{8}$$

Fig. 7 illustrates the inverter voltage $V_{\mathrm{AB}i}$ for only one switching period. Fig. 7(a) shows the positive inverter voltage generation, while Fig. 7(b) shows the negative voltage generation. As it can be seen, in the case of the asymmetrical qZS inverter, the voltage of the positive and the negative cycle contains positive and negative components and differs in shape.

In the positive generation, *a*, *b,* and *e* circuits (see Fig. 6) are involved in the positive voltage distribution, while *c* and *d* are in response to the ST generation. Similarly, in the negative output voltage generation, *b, f* and *e* circuits (see Fig. 6) are involved, while *c* and *d* are in response to the ST generation. Correspondent labels are shown in Fig. 7.

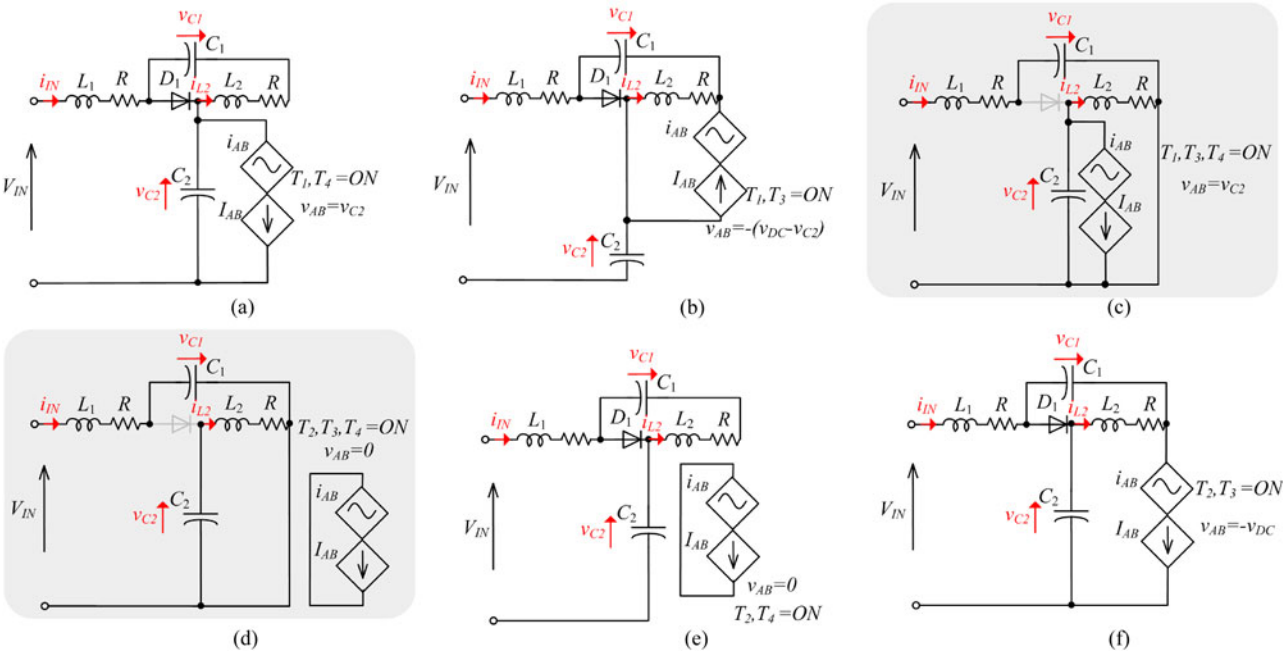

Fig. 6. Equivalent circuits of the asymmetrical single-phase MqZSI.

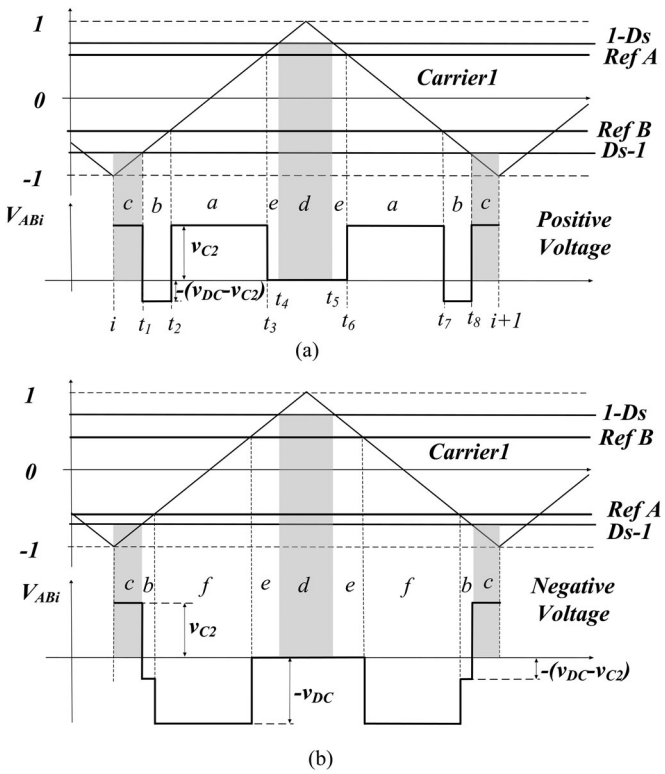

Fig. 7. Inverter voltage $V_{\mathrm{AB}i}$ for one switching cycle of the asymmetrical single-phase MqZSI: (a) Positive voltage; and (b) negative voltage.

A. Steady-State Analysis

The high-frequency ripple is estimated by means of steady-state analysis, when only constant dc current source component of the output side of the inverter is taking into account.

The voltage balance across the inductors and current balance across the capacitors are considered. It means that the average voltage across the inductors and the average current across the capacitors are equal to zero

$$\frac{1}{T}\int v_{\mathrm{L1}}(\mathrm{t})dt = 0, \quad \frac{1}{T}\int i_{C1}(\mathrm{t})dt = 0. \tag{9}$$

The sum of the capacitor voltages defines the peak value of the dc-link voltage

$$V_{\mathrm{DC}} = V_{C1} + V_{C2} \tag{10}$$

where V_{C1}, V_{C2} are the average voltages across the capacitors over one fundamental period.

The capacitor voltages can be found from the voltage balance across the inductors

$$V_{L1} = \left(V_{C2} - \frac{V_{\mathrm{IN}}}{2}\right) D_A - \left(V_{C1} + \frac{V_{\mathrm{IN}}}{2}\right) D_S = 0 \tag{11}$$

$$V_{L2} = V_{C1} \cdot D_A - V_{C2} \cdot D_S = 0 \tag{12}$$

where t_A is time interval of the active state (opposite to ST), t_S—time interval of the ST state, D_A and D_S—the correspondent duty cycles. Despite of different active and ST states in terms of the voltage applied to the output side, the voltage applied to the inductors is the same as in the conventional configurations.

Taking into account the conditions presented above, the voltages across the capacitors can be obtained as

$$V_{C1} = \frac{D_S \cdot V_{\mathrm{IN}}}{2 - 4 \cdot D_S} \tag{13}$$

$$V_{C2} = \frac{V_{\mathrm{IN}} \cdot (1 - D_S)}{2 - 4 \cdot D_S}. \tag{14}$$

It can be seen that it corresponds to the conventional configuration as well as dc-link voltage V_{DC}(2). As a result the

high-frequency current ripple through the inductors remains the same as in conventional configuration. Similar conclusions are valid for voltage ripple across the capacitors. At the same time, the main difference lays in the low-power oscillation, which is flowing in different ways compared to the conventional configuration. In order to estimate low-frequency ripple components the averaging method in Laplace domain is applied. A similar approach has been applied in [48] and [49].

B. Small-Signal Average AC Model

In order to generalize the analysis, $m\omega$ is taken as any component of the variable part of the dc-link current. It is assumed that $C_1 = C_2 = C, L_1 = L_2 = L$. In terms of variable components, the input dc power supply keeps the voltage constant and it does not contain the $m\omega$ component. As it can be seen from Fig. 7, several equivalent circuits are involved in the switching process. At the same time, the duty cycle of certain state strictly depends on the phase of the output voltage. A small-signal model will be created by means of maximum value of the output inverter voltage along with ac component of the output inverter current. As a result, the dynamic model during the positive output voltage generation can be presented by means of two equivalent circuits *a* [see Fig. 6(a)] for active state and *c* [see Fig. 6(c)] for ST state. In the active state with circuit *a* [see Fig. 6(a)], the dynamic equations are

$$\begin{cases} L\dfrac{d\tilde{i}_{\rm IN}}{dt} = -\tilde{v}_{C2} + \tilde{i}_{\rm IN}\cdot R \\ L\dfrac{d\tilde{i}_{L2}}{dt} = -\tilde{v}_{C1} + \tilde{i}_{L2}\cdot R \\ C\dfrac{d\tilde{v}_{C1}}{dt} = \tilde{i}_{L2} \\ C\dfrac{d\tilde{v}_{C2}}{dt} = \tilde{i}_{\rm IN} - \tilde{i}_{\rm AB} \end{cases}. \tag{15}$$

The dynamic equations for ST state [see Fig. 6(c)], can be written as

$$\begin{cases} L\dfrac{d\tilde{i}_{\rm IN}}{dt} = \tilde{v}_{C1} - \tilde{i}_{IN}\cdot R \\ L\dfrac{d\tilde{i}_{L2}}{dt} = \tilde{v}_{C2} - \tilde{i}_{L2}\cdot R \\ C\dfrac{d\tilde{v}_{C1}}{dt} = -\tilde{i}_{\rm IN} \\ C\dfrac{d\tilde{v}_{C2}}{dt} = -\tilde{i}_{L2} - \tilde{i}_{\rm AB} \end{cases}. \tag{16}$$

As $\tilde{x}$ is an $m\omega$ component, the average value of the variables $\tilde{x}$ over one switch cycle T is not zero and as a result, it can be expressed as

$$\begin{cases} L\dfrac{d\langle\tilde{i}_{\rm IN}\rangle_T}{dt} = D_S\cdot(\tilde{v}_{C1} - \tilde{i}_{\rm IN}\cdot R) - D_a(\tilde{v}_{C2} - \tilde{i}_{\rm IN}\cdot R) \\ L\dfrac{d\langle\tilde{i}_{L2}\rangle_T}{dt} = D_S\cdot(\tilde{v}_{C2} - \tilde{i}_{L2}\cdot R) - D_a(\tilde{v}_{C1} - \tilde{i}_{L2}\cdot R) \\ C\dfrac{d\langle\tilde{v}_{C1}\rangle_T}{dt} = D_a\tilde{i}_{L2} - D_S\cdot\tilde{i}_{\rm IN} \\ C\dfrac{d\langle\tilde{v}_{C2}\rangle_T}{dt} = D_a\tilde{i}_{\rm IN} - D_S\cdot\tilde{i}_{L2} - \tilde{i}_{\rm AB} \end{cases}. \tag{17}$$

In order to complete dynamic model, the negative output voltage generation is considered as well. This case is different due to the zero output voltage $v_{\rm AB}$ generation and can be represented by means of two main equivalent circuits *f* [see Fig. 6(f)] for active state and *d* [see Fig. 6(d)] for ST state. In the active state with circuit *f*, the dynamic equations are

$$\begin{cases} L\dfrac{d\tilde{i}_{\rm IN}}{dt} = -\tilde{v}_{C2} + \tilde{i}_{IN}\cdot R \\ L\dfrac{d\tilde{i}_{L2}}{dt} = -\tilde{v}_{C1} + \tilde{i}_{L2}\cdot R \\ C\dfrac{d\tilde{v}_{C1}}{dt} = \tilde{i}_{L2} - \tilde{i}_{\rm AB} \\ C\dfrac{d\tilde{v}_{C2}}{dt} = \tilde{i}_{\rm IN} - \tilde{i}_{\rm AB} \end{cases}. \tag{18}$$

The ST state corresponds to the equivalent circuit *d* [see Fig. 6(d)] and this state can be written as

$$\begin{cases} L\dfrac{d\tilde{i}_{\rm IN}}{dt} = \tilde{v}_{C1} - \tilde{i}_{\rm IN}\cdot R \\ L\dfrac{d\tilde{i}_{L2}}{dt} = \tilde{v}_{C2} - \tilde{i}_{L2}\cdot R \\ C\dfrac{d\tilde{v}_{C1}}{dt} = -\tilde{i}_{\rm IN} \\ C\dfrac{d\tilde{v}_{C2}}{dt} = -\tilde{i}_{L2} \end{cases}. \tag{19}$$

It can be seen that the difference consists in the current $i_{\rm AB}$ flow direction. As a result, the average value of the variables $\tilde{x}$ over one switching cycle *T* for negative voltage generation can be expressed as

$$\begin{cases} L\dfrac{d\langle\tilde{i}_{\rm IN}\rangle_T}{dt} = D_S\cdot(\tilde{v}_{C1} - \tilde{i}_{\rm IN}\cdot R) - D_a(\tilde{v}_{C2} - \tilde{i}_{\rm IN}\cdot R) \\ L\dfrac{d\langle\tilde{i}_{L2}\rangle_T}{dt} = D_S\cdot(\underset{C2}{\tilde{v}} - \tilde{i}_{L2}\cdot R) - D_a(\underset{C1}{\tilde{v}} - \tilde{i}_{L2}\cdot R) \\ C\dfrac{d\langle\tilde{v}_{C1}\rangle_T}{dt} = D_a(\tilde{i}_{L2} - \tilde{i}_{\rm AB}) - D_S\cdot\tilde{i}_{\rm IN} \\ C\dfrac{d\langle\tilde{v}_{C2}\rangle_T}{dt} = D_a(\tilde{i}_{\rm IN} - \tilde{i}_{\rm AB}) - D_S\cdot\tilde{i}_{L2} \end{cases}. \tag{20}$$

Using (17) and (20), dependences $i_{\rm IN}$, i_{L2}, v_{C1} , $v_{C2} = f(I_{\rm MAX}, D_S, R, C, m, \omega, L)$can be obtained. Because these equations are long, they are not shown directly in this paper. It should be mentioned that derived model is valid for certain operation point where ST duty cycle is averaged.

At the same time, the dependencies obtained are illustrated in Figs. 8 and 9. Since the dynamic equations for positive and negative voltage generation are different, the input current waveform will be different as well. Fig. 8 shows the positive output voltage generation, while Fig. 9 shows the negative output voltage generation.

Fig. 8(a) shows the dependence of the input current $I_{\rm IN}$ as a function of the inductance *L* with a different value of *R*. It can be seen that it is close to the resonance frequency as the amplitude of the input current increases. The peak value strongly depends on the value of the losses resistor in *R*. Larger values of *R* lead to damping of the oscillation and the decreasing of peak value.

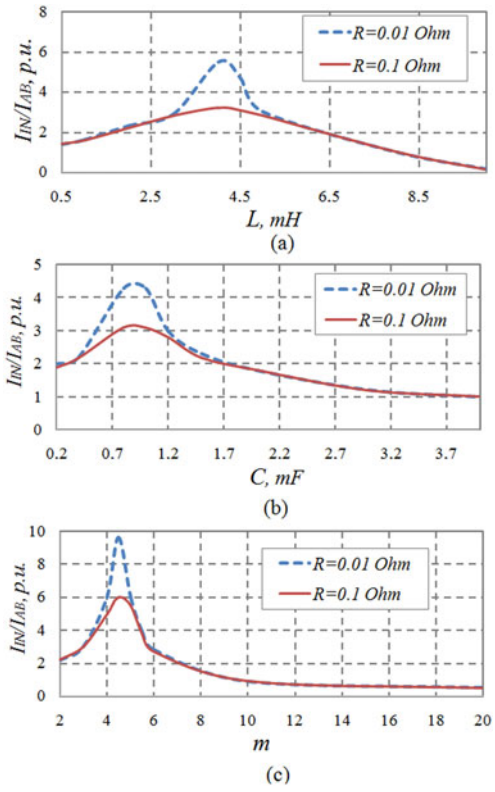

Fig. 8. Dependencies of the input current I_{IN} in case of positive voltage generation as a function of resistance R and of the: (a) Inductance $L(m = 2, C = 0.4$ mF); (b) capacitance $C(m = 2, L = 1.8$ mH); and (c) the harmonic frequency m ($C = 0.4$ mF, $L = 1.8$ mH).

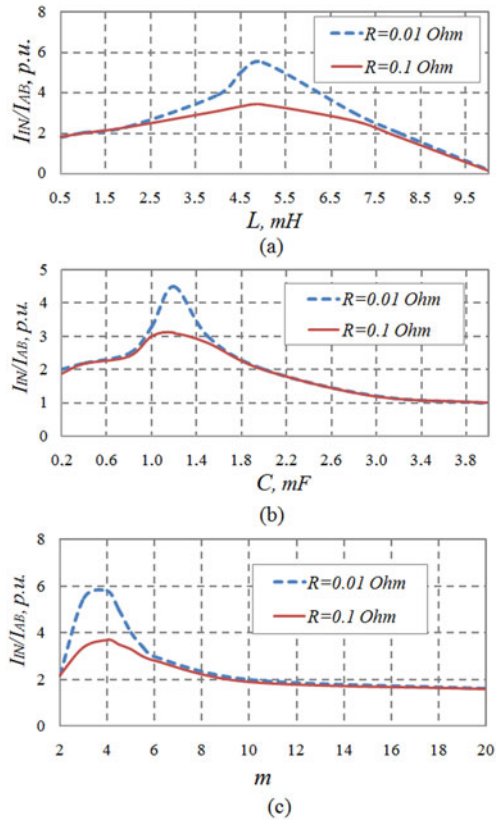

Fig. 9. Dependencies of the input current I_{IN} in case of negative voltage generation as a function of resistance R and of the: (a) Inductance $L(m = 2, C = 1$ mF); (b) capacitance $C(m = 2, L = 1$ mH); and (c) harmonic frequency m ($C = 1$ mF, $L = 1$ mH).

At the same time, similar results are obtained when the capacitance is changing [see Fig. 8(b)]. As it can be seen, the increasing R decreases the amplitude of the peak input current at the resonance frequency. The results obtained show that the resonance frequency may lead to significant current and voltage ripple increase and should be taken into account during the passive component design. In the nonresonance mode (right side after resonance in Fig. 8), the passive component value increase leads to the mitigation of the current and voltage ripples in the inverter.

Finally, Fig. 8(c) demonstrates dependence of the input current I_{IN} as a function of the harmonic frequency m under constant passive elements. It can be seen, that resonance phenomena will happen on the self-resonance frequency defined by passive elements. In all other regions, the harmonic increase leads to decreasing input current ripple. This figure can be used for second harmonic estimation, which is the most significant.

Fig. 9 shows similar results for negative output voltage generation. It can be seen that the results are quite similar, the resonance frequencies are the same for each figures, but the peak values are slightly higher. It should be mentioned that the negative voltage generation is quite similar to the conventional configuration.

As a result, it can be concluded that, in order achieve predefined input current ripple in the modified configurations the passive elements must be the same as in the conventional configurations. The difference lies in the spectrum distribution. Taking into account, the steady-state analysis along with small-signal model it is concluded that the main difference consists in the voltage applied to the semiconductors.Table IV shows the voltage and current stresses of semiconductors. It is assumed that circuits are ideal without any parasitic.

TABLE IV
VOLTAGE AND CURRENT STRESS ON THE SEMICONDUCTORS

Semiconductor	Voltage stress (peak value)	Current stress (peak value)
D1	$\frac{1}{1-2\cdot D_S}\cdot \mathrm{V_{IN}}$	Maximum ST current
T1, T2	$\frac{1-D_S}{1-2\cdot D_S}\cdot V_{\mathrm{IN}}$	Maximum output current
T3 . . . T4	$\frac{1}{1-2\cdot D_S}\cdot V_{\mathrm{IN}}$	Maximum ST current

The difference between traditional and modified solution consists of the voltage stress across transistors T_1 and T_2 which is lower than across T_3 and T_4. Also, the current spike across transistors T_3 and T_4 during ST states is higher since only one branch is involved.

V. Output Voltage Quality Estimation

Increased amount of voltage levels used for output voltage generation reveals the main benefit of the discussed topologies, which lies in the improved output voltage quality. In order to

prove this statement, the output voltage spectrum is estimated and compared analytically.

The attention is paid to the inverter voltage spectrum of the conventional qZSI solution [see Fig. 1(b)] versus asymmetrical MqZSI as depicted in Fig. 3(a). Fig. 7 illustrates the inverter voltage $V_{\mathrm{AB}i}$ for only one switching cycle of the asymmetrical MqZSI. As it was mentioned above, the shape of the positive [see Fig. 7(a)] and the negative [see Fig. 7(b)] inverter voltage is different.

The main idea for further analysis lies in the direct calculation of the Fourier coefficients in the following way. First of all, it is assumed that the reference voltages are constant within each *i* time interval

$$\mathrm{Re}\ f\,A(i) = \sin\left(\frac{2\pi\cdot f_0\cdot i}{N}\right) \tag{21}$$

$$\mathrm{Re}\ f^{*}A(i) = -\sin\left(\frac{2\pi\cdot f_0\cdot i}{N}\right)\cdot(1-D_S) \tag{22}$$

$$\mathrm{Re}\ f\,B(i) = -\sin\left(\frac{2\pi\cdot f_0\cdot i}{N}\right)\cdot(1-D_S) \tag{23}$$

where f_0 is a fundamental frequency, N is the number of switching cycles in the fundamental period. As a result, the switching frequency can be expressed as

$$f_{\mathrm{SW}} = N\cdot f_0. \tag{24}$$

The voltage V_{AB} can be expressed as a function of each time switching interval *i* because the duration of the time intervals shown in Fig. 7 strictly depends on *i*.

In the case of the positive inverter voltage generation

$$t_1 = i+\frac{1}{4}D_S \tag{25}$$

$$t_2 = i+\frac{1}{4}\left(1-(1-D_S)\cdot\sin\left(\frac{2\pi\cdot f_0\cdot i}{N}\right)\right) \tag{26}$$

$$t_3 = i+\frac{1}{4}\left(1+\sin\left(\frac{2\pi\cdot f_0\cdot i}{N}\right)\right) \tag{27}$$

$$t_4 = i+\frac{1}{2}-\frac{1}{4}D_S \tag{28}$$

$$t_5 = i+\frac{1}{2}+\frac{1}{4}D_S \tag{29}$$

$$t_6 = i+\frac{1}{2}+\frac{1}{4}\left(1-\sin\left(\frac{2\pi\cdot f_0\cdot i}{N}\right)\right) \tag{30}$$

$$t_7 = i+\frac{3}{4}+\frac{1}{4}(1-D_S)\cdot\sin\left(\frac{2\pi\cdot f_0\cdot i}{N}\right) \tag{31}$$

$$t_8 = i+1-\frac{1}{4}D_S. \tag{32}$$

Similar equations can be derived for negative voltage generation from Fig. 7(b). Each time interval corresponds to some constant voltage that is defined by the voltage across the capacitors and is shown in Fig. 7.

TABLE V
SWITCHING HARMONIC SPECTRUM

k	Conventional (% of fundamental)	Asymmetrical (% of fundamental)	Symmetrical (% of fundamental)
1	0	3	3
2	54	32	39
3	0	1	14
4	8	5	5
5	0	1	13
6	7	5	0
7	0	0	10
8	1	1	0
9	0	0	5
10	0	1	0

TABLE VI
COMPONENTS AND PARAMETERS USED FOR SIMULATION AND EXPERIMENTAL SETUP

Circuit	Conventional qZSI	Asymmetrical MqZSI	Symmetrical NPC MqZSI
L_1, mH	1.8	1.8	0.9
L_2, mH	1.8	1.8	0.9
L_3, mH			0.9
L_4, mH			0.9
C_1, mF	0.4	0.4	0.2
C_2, mF	0.4	0.4	0.2
C_3, mF			0.2
C_4, mF			0.2
Input power, W		300	
Input voltage, V		255	
Output RMS voltage, V		230	
R, Ω (*losses model*)		0.05	
Switching frequency, kHz		100	

Finally, in order to estimate the inverter voltage harmonics, it can be expressed the Furrier coefficients

$$a_k = \frac{1}{\pi}\cdot\sum_{i=1}^{N}\int_0^{\frac{1}{N\cdot f_0}} V_{\mathrm{AB}i}(t)\cos(2\pi\cdot f_0\cdot N\cdot k\cdot t)\cdot dt \tag{33}$$

$$b_k = \frac{1}{\pi}\cdot\sum_{i=1}^{N}\int_0^{\frac{1}{N\cdot f_0}} V_{\mathrm{AB}i}(t)\sin(2\pi\cdot f_0\cdot N\cdot k\cdot t)\cdot dt \tag{34}$$

where $k=1,2,\ldots,\infty$ are the number of switching harmonics.

Taking into account the equations presented above, the calculation of the Fourier coefficients (33) and (34) is performed by means of Maple software. Similar analysis has been performed for symmetrical MqZSI [see Fig. 3(b)]. Table V shows the first ten switching harmonics multiples of the fundamental harmonics of the V_{AB} voltage for all three cases.

It should be noted that the harmonic spectrum strictly depends on the ST duty cycle D_S. This table corresponds to the $D_S = 0.18$.and *N* is 200. In the case of ST duty cycle reduction, the difference of the harmonic spectrum will not be so evident. The modified solutions have a better harmonic spectrum due to the larger amount of the inverter voltage levels. In particular, the lower switching harmonics are significantly reduced. At the same time, advanced modulation techniques will mitigate the switching harmonic spectrum even more.

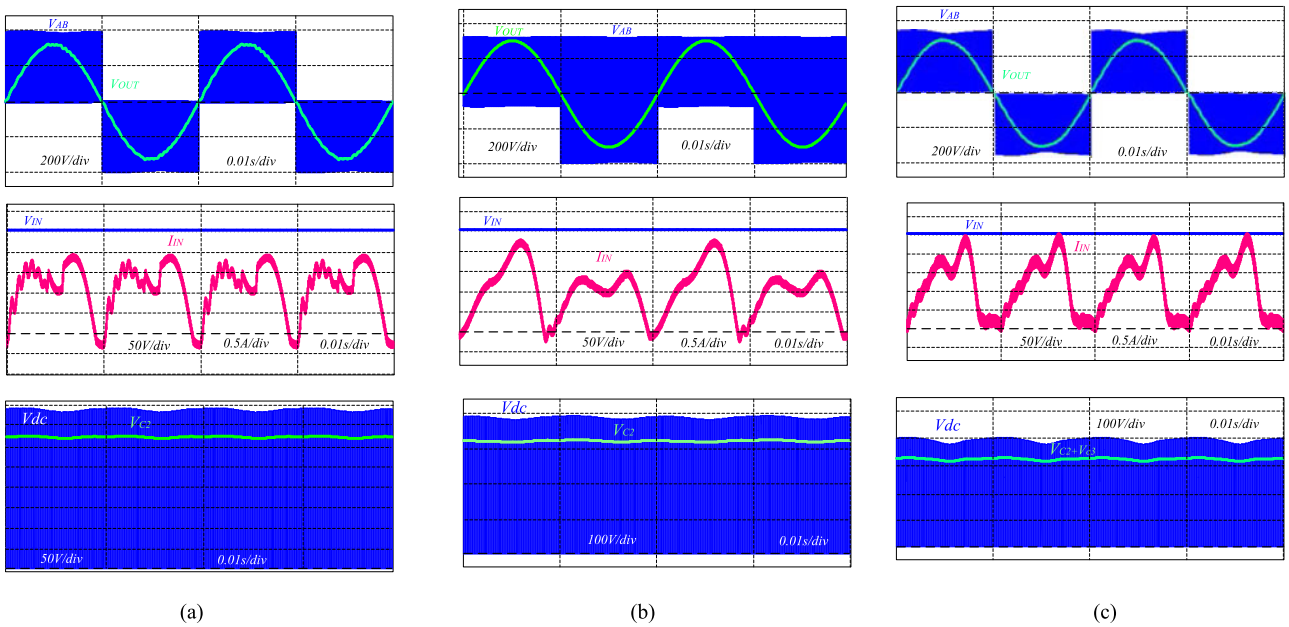

Fig. 10. Simulation results of the single-phase MISIs: (a) Conventional qZSI; (b) asymmetrical MqZSI; and (c) symmetrical NPC qZSI.

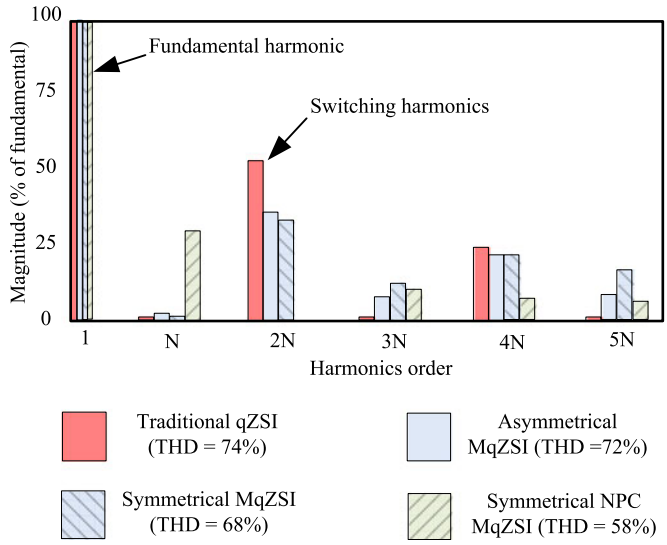

Fig. 11. Simulation harmonic spectrum of the conventional qZSI, asymmetrical MqZSI, symmetrical qZSI, and symmetrical NPC qZSI.

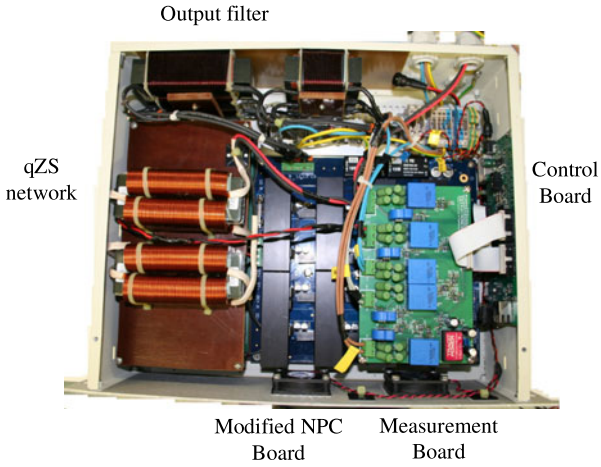

Fig. 12. Photo of the experimental prototype.

TABLE VII
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Control unit (FPGA)	Cyclone IV EP4CE22E22C8
Transistors Driver Chip	ACPL-H312
Transistors $T_1 - - T_{12}$	C2M0080120
qZS network and NPC diodes $D_1 - - D_6$	C3D10065A
$C_1 - - C_4$ —capacitors,	200 μF
L_1 –L_4 —inductors	0.9 mH
L_I—output filter inductor on the inverter side	1 mH
L_L—output filter inductor on the load side	0.4 mH
C_F—output filter capacitor	2 μF

VI. Simulation Results

In order to prove all novel solutions and compare them with conventional counterparts, simulations have been performed. The first simulated converter is an asymmetrical single-phase MqZSI. The next novel solution selected for simulation is a symmetrical single-phase NPC MqZSI. A comparative solution selected to the simulation is the conventional single-phase qZSI [34].

The parameters for the simulation determined by the terms obtained in the Section IV are summarized in Table VI. All the parameters are used for all the solutions studied. Fig. 10 shows the simulation waveforms for the chosen solutions.

Fig. 10(a) showsthe waveforms of the conventional qZSI [see Fig. 1(b)]. Fig. 10(b) shows the waveforms of the asymmetrical MqZSI [see Fig. 3(a)], and finally, Fig. 10(c) shows the waveforms of the symmetrical NPC qZSI [see Fig. 3(c)]. For each

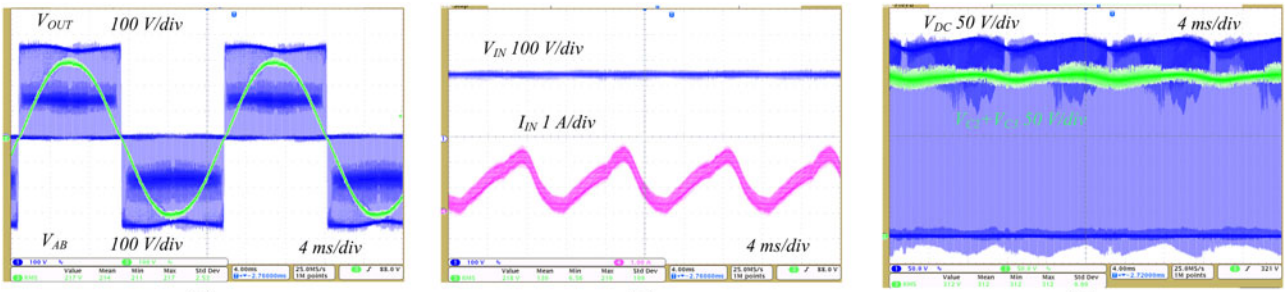

Fig. 13. Experimental results of the single-phase NPC MqZSI: (a) Output voltage before V_{AB} and after V_{OUT} filter; (b) input voltage V_{IN} along with input current I_{IN}; and (c) dc-link voltage V_{DC} along with sum of inner capacitor voltages $V_{C2} + V_{C3}$.

study, from top to bottom, the following can be revealed: the output inverter voltage after the output filter V_{OUT} and before filter V_{AB}, the input voltage V_{IN} along with the input current I_{IN} and dc-link voltage along with the inner (V_{C2}) capacitor voltage.

The main difference lies in the waveform of the input current. It can be seen that the asymmetrical modified solution has a more complex harmonic spectrum of the input current. The fundamental harmonics as well as the double fundamental harmonic are also present in the waveform. At the same time, the peak values are almost the same.

It confirms the conclusion that component design guidelines are the same as for the conventional solutions. The suggested modification of the inverter branch connection has no significant influence on the peak value of the voltage and current ripples, and as a result, on the value of the passive components.

Finally, the inverter voltage spectrum along with THD before filter is shown for all solutions in Fig. 11. In all case study points, the output power was 300 W for all topologies. It can be seen, that the output voltage quality (THD) before filter corresponds to the theoretical results shown in Table V. The worst result belongs to the conventional qZSI.

VII. Experimental Results

To confirm the solutions described, this section presents the experimental results of one of the proposed topologies. Fig. 12 shows the experimental prototype, which was finally assembled in a 3U box. It consists of four main PCB boards with external conventional *LCL* output filters. One of the boards is an assembled qZS network.

For the experimental study, the aim was to confirm the simulation results of the single-phase symmetrical NPC MqZSI. The presented experimental diagrams are in full accordance with the simulation results. The parameters of the passive components are the same as in the simulation results as well. Specifications of the experimental prototype are presented in Table VII. The measurements were made by a digital oscilloscope Tektronix MDO4034B-3, using current probes Tektronix TCP0150, and voltage probes Tektronix TPA-BNC.

The control system is based on the FPGA board with EP4CE22E22C8 from Altera. The FPGA makes it easier to implement nontraditional modulation techniques with the ST states that is important for the given topology. The ACPL-H312 chosen is a cheap high-frequency unidirectional driver. High switching frequency SiC MOSFETs with fast body diodes, SiC NPC, and qZS network diodes allow the switching frequency to be raised up to 100 kHz, which in turn reduces the size of the passive components. Passive resistors served as a load. A regulated dc power supply was used as an input voltage source.

Fig. 13 shows the experimental results by means of the output voltage before V_{AB} and after V_{OUT} filter, the input voltage V_{IN} along with the input current I_{IN} and the dc-link voltage V_{DC} along with the sum of inner capacitor voltages $V_{C2} + V_{C3}$. As it can be seen, the experimental results are very similar to the simulation results.

The measured efficiency of the experimental prototype was in the range 96–98%. The maximum efficiency corresponds to the *VSI* mode without the ST states and where the modulation index is equal to 1. The introduction of the ST states decreases the efficiency. The measured THD of the output voltage before the output filter is about 60%, while after output filter is about 3%.

VIII. Conclusion

This paper describes novel single-phase solutions with increased inverter voltage levels derived by means of a nonstandard inverter configuration and IS networks. Operation principles based on special modulation techniques are presented. Detailed component design guidelines along with simulation and experimental verification are provided.

The main benefits of the proposed solutions lie in the increased amount of levels with all possible merits: reduced THD or reduced size of the output filter. A further advance is the voltage stress on the transistors working in traditional VSI mode is reduced as well.

Also, the switching flexibility changes the current and the voltage spectrum on the passive components. At the same time, such influence is not significant on the peak value of the voltage and current ripples, and as a result, either on the value of the passive components. In the future, special SVM control techniques with much more improved THD of the output voltage can be designed.

At the same time drawbacks like increased conduction losses during ST states generation, lost cross-conduction immunity of the inverter branches that do not have the ST states generation should be taken into account.

The fields of application may be the same as in the case of conventional IS-based inverters. At the same time, a reduced output voltage THD is an important advantage, especially at a low switching frequency of the semiconductors.

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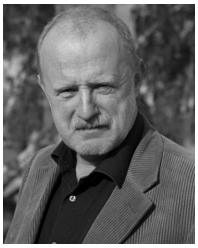

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