Low-Frequency Input Current Ripple Reduction Based on Load Current Feedforward in a Two-Stage Single-Phase Inverter

Youjie Shi, Bangyin Liu, *Member, IEEE*, and Shanxu Duan

***Abstract*—A large amount of ripple at twice the output frequency will emerge in the input current due to the pulsating output power in a two-stage single-phase inverter. To reduce the low-frequency input current ripple, a control strategy is presented in this paper based on the front-end dc–dc converter load current feedforward. It intends to control the dc bus voltage to swing properly at twice the output frequency, making the dc bus capacitor supply nearly all the pulsating power. The implementation method is illustrated, and the operation performance analysis as well as the key parameter design principle is provided. Introducing the proposed feedforward path is able to significantly suppress the input current ripple with little impacts on the original system stability, steady-state tracking accuracy, and dynamic response. Finally, experimental results performed on a buck-type stand-alone two-stage single-phase inverter prototype verify the validity of proposed method and the correctness of analysis.**

***Index Terms*—Current ripple reduction, load current feedforward (LCFF), low-frequency ripple, single-phase inverter.**

I. Introduction

THE two-stage single-phase inverter, consisting of a front-end dc–dc converter and a downstream dc–ac inverter as shown in Fig. 1, has been widely utilized in the distribution systems [1]–[5] such as PV system, fuel cell generator, ship-electric power system, uninterruptible power supply etc. The downstream inverter is responsible for dc-to-ac power conversion. The front-end dc–dc converter can not only achieve voltage matching when the dc input has a great voltage varying range or a large difference with the output in voltage level [5], [6], but also realize the electrical isolation [4] between the input and output with high-frequency transformer when an isolated-type dc–dc converter is adopted.

Due to the pulsating output power of the single-phase inverter, the dc input current of the downstream dc–ac inverter, namely the load current of the front-end dc–dc converter hereinafter, contains a large amount of ripple at twice the output frequency [7]. Once without effective reduction methods, the second harmonic current will be injected into the dc input source as shown in Fig. 1. In some applications, such as the fuel cell or battery power generators and dc microgrids, the low-frequency input ripple will cut down the lifetime and efficiency of dc sources [8], and increase the input filter size. Hence, it is necessary to avoid the pulsating current flowing into the dc sources.

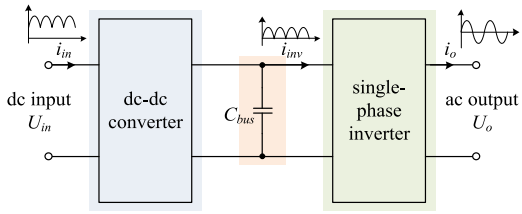

Fig. 1. Circuit configuration of a two-stage inverter.

Both boost- and buck-derived converter can be used as the front-end stage in different application backgrounds. In the boost-derived converter, there exists an input filter inductor which can filter the harmonics and smooth the current, and the input current can be controlled directly. However, there is no inductor in the input side of a buck-derived converter which will further make the input current ripple problem more difficult to solve. Therefore, a buck-derived converter is chosen as the front-end stage for research in this paper.

Basically, the low-frequency input ripple reduction techniques in the literature can be classified into following two categories. The first category is realized by adding auxiliary circuit. To absorb the pulsating power, Schenck *et al.* [9] increase the intermediate dc bus capacitor, and Fukushima *et al.* [10] insert an *LC* circuit to the dc bus. However, it is difficult to optimize the size and weight of system. A bidirectional dc–dc converter is adopted in parallel with the dc bus and acts as a dc active power filter in [11]–[13], and some novel dc–dc converter circuits embedded with ripple port are reported in [14] and [15]. A phase leg is added to the downstream single-phase inverter in [16] and [17]. By properly controlling the amplitude and phase angle of the additional phase leg output current, the total power from dc input can maintain constant. Although these methods can suppress the input current ripple effectively, the extra power switches and circuits may lead to a raise in cost, power losses, and system complexity.

As an alternative, the second category is adopting a proper control strategy to force the intermediate dc bus capacitor to undertake nearly all the ripple in the load current, leaving the input current ripple-free. Without extra circuits, this category has advantages over the former approaches on the efficiency

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and circuit design. Thus, it is more preferred in this paper. The early ripple reduction control method is realized by introducing an inner inductor current loop to form a dual-loop control [6]. However, the voltage-loop crossover frequency must be far below twice the output frequency $2f_o$ [18] which will lead to a slow dynamic response. Then some modified methods are proposed based on dual-loop control. Inserting a notch filter or moving average filter (MAF) to the feedback path [19], [20] or forward path [21]–[24] of the dc bus voltage loop can dramatically increase the voltage-loop bandwidth, meanwhile adopting the resonant control for the input current/voltage loop [23], [24] can improve the open-loop gain at $2f_o$. For further improvement of dynamic performance, Wang *et al.* [20] and Zhang *et al.* [25] add a bandpass filter (BPF) to the inner inductor current feedback path, Zhu *et al.* [26] bring in a load current feedforward (LCFF) path along with a notch filter to the dual-loop control, and then Zhang *et al.* [27] compare their input ripple suppression effect and dynamic performance from an output impedance perspective. Nevertheless, the additional controller for ripple reduction (a notch filter or BPF) in these methods is inserted into the close loop. It will introduce a large negative phase shift at the frequencies lower than its characteristic frequency, and may reduce the system phase margin. The voltage-loop parameter design will become more complex.

Apart from those dual-loop-based methods above, Kwon *et al.* [28] derive the mathematic relationship between the ripple voltage on the dc bus capacitor and the ripple current supplied by it, and adds corresponding second harmonic component to the duty ratio of the front-end dc–dc converter. However, the voltage-loop crossover frequency must be designed low adequately to attenuate the interaction between voltage control and ripple reduction control. Wang *et al.* [29] add pulsating component to the dc bus voltage reference based on the second harmonic content in load current, while the input current ripple cannot be greatly reduced if the voltage-loop bandwidth is lower than $2f_o$.

To reduce the low-frequency input current ripple without the need for auxiliary circuit, this paper proposes a control based on the front-end dc–dc converter LCFF. This method intends to modify the dc bus voltage reference and control the dc bus voltage to pulsate properly at $2f_o$, making the dc bus capacitor supply nearly all the pulsating power. The rest of this paper is organized as follows: In Section II, a control structure illustrating the proposed ripple reduction based on LCFF is given. In Section III, the analysis of system steady-state and dynamic performance as well as the controller parameter design method is presented. Section IV gives experimental verifications on a two-stage single-phase inverter prototype. Finally, conclusion is drawn in Section IV.

II. Input Current Ripple Reduction Strategy Based on LCFF Control

Voltage mode control (VMC) has been frequently adopted for the front-end dc–dc converter to maintain the intermediate dc bus voltage because of its lower system complexity and cost. The traditional control scheme for a buck-derived converter under digital implementation is illustrated in Fig. 2, where L and

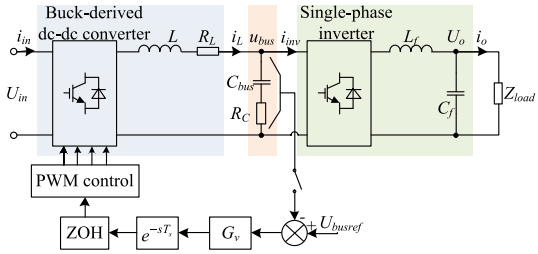


Fig. 2. Traditional VMC scheme for the front-end buck-derived converter.

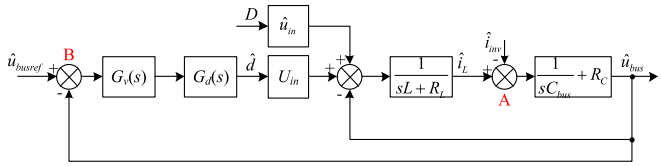


Fig. 3. Small-signal model of the front-end buck-derived dc–dc converter.

R_L are dc filter inductor and its equivalent series resistor (ESR); $C_{\rm bus}$ and R_C are the intermediate dc bus capacitor and its ESR; L_f and C_f are the ac output filter inductor and capacitor; and $Z_{\rm load}$ represents the load impedance. G_v is the voltage controller, and a common PI regulator expressed as

$$G_v(s) = K_p + K_i/s. \tag{1}$$

In a digitally controlled system, there will be computation and pulse width modulation (PWM) delays. In Fig. 2, e^{-sT_s} stands for the one-sampled computation delay, and the sampler can be represented by $1/T_{\rm s}$ [30] in the s-domain where T_s is sampling period, and the zero-order hold (ZOH) can be approximated to [31]

$$G_h(s) = \frac{1-e^{-sT_s}}{s} \approx T_s e^{-0.5sT_s}. \tag{2}$$

Hence, the one-sampled computation delay, the sampler, and ZOH together are equivalent to a delay effect which can be derived as

$$G_d(s) = e^{-sT_s} \cdot \frac{1}{T_s} \cdot G_h(s) = e^{-1.5sT_s}. \tag{3}$$

Fig. 3 shows the small-signal model for the front-end buck-derived converter. When operating with a load, the load current $\hat{i}_{\rm inv}$ of dc–dc converter mainly contains amount of second-order and high-frequency harmonics. It is obvious that the low-frequency component is introduced to the voltage loop by $\hat{i}_{\rm inv}$ at Location A, thus generating ripple in the inductor current $\hat{i}_L$ and further input current $\hat{i}_{\rm in}$.

The most direct and useful approach to eliminate the load current $\hat{i}_{\rm inv}$ disturbance to the voltage loop is to add a component which has the same amplitude but opposite sign, namely $-\hat{i}_{\rm inv}$, to Location A. By moving the feeding node from the output of $1/(sL+R_L)$ to the input of the loop, namely from Location A to B, an equivalent block diagram is derived as shown in Fig. 4(a).

Since we only care about the second harmonics component in the load current $i_{\rm inv}$ which contains the dc component and

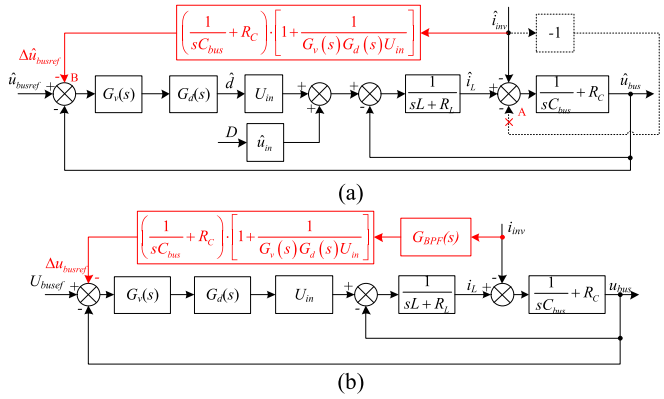


Fig. 4. Control block diagram derivation for realizing ripple reduction: (a) Introducing $-i_{\rm inv}$ to the small-signal model; (b) using BPF for low-frequency ripple extraction in a large-signal model.

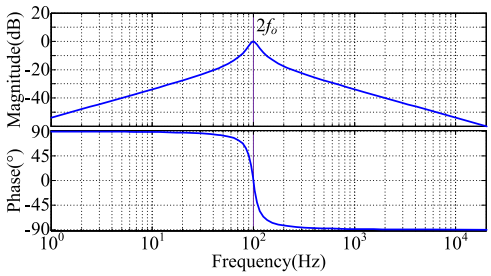


Fig. 5. Bode diagram of BPF with bandwidth $f_{\rm b} = 20$ Hz.

high-frequency harmonics as well, a BPF with characteristic frequency of $2f_o$ is adopted here to extract the second harmonics in $i_{\rm inv}$. The large-signal model is shown in Fig. 4(b). The expression of BPF is

$$G_{\rm BPF}\left(s\right) = \frac{\left(2\pi f_b\right)s}{s^2 + \left(2\pi f_b\right)s + \left(2\pi \cdot 2f_o\right)^2} \tag{4}$$

where f_b is BPF bandwidth, and take $f_b = 20$ Hz as an example, the bode plot is shown in Fig. 5. The BPF bandwidth f_b is a key controller parameter whose design method will be offered later. As the magnitude of BPF is equal to 0 dB at $2f_o$, relatively lower at other frequencies, and the phase angle at $2f_o$ equals 0°, it can extract the second harmonics completely, filtering out other components well.

Compared with traditional VMC in Fig. 3, an extra LCFF path is introduced in Fig. 4(b) whose feeding node is located at the input of voltage loop. This path offers a slight regulation to the dc bus voltage reference. It implies that the voltage reference is no longer a constant value which is expressed as $U_{\rm busref}$ here anymore, but a combination of dc component $U_{\rm busref}$ and a ripple component $\Delta u_{\rm busref}$, and the LCFF controller transfer function is

$$\frac{\Delta u_{\rm busref}}{i_{\rm inv}} = \left(\frac{1}{sC_{\rm bus}} + R_C\right)\cdot G_{\rm BPF}\left(s\right) \cdot\left[1 + \frac{1}{G_v\left(s\right)G_d\left(s\right)U_{\rm in}}\right] = G_{\rm LCFF0}\left(s\right). \tag{5}$$

However, the controller expressed in (5) is not suitable for practical implementation, thus some simplifications and modifications are made as follows.

A. Remove the Delay Function $G_d(s)$.

It can be found that (5) is not easy to realize in the physical world because there is a delay function $G_d(s)$ in the denominator. As the sampling and control frequency is generally much higher than $2f_o$ in most power systems, the lagging phase angle at $2f_o$ produced by the delay function $G_d(s)$ is very small. For example, the phase angle of $G_d(s)$ at $2f_o$ is only 3.4° according to (3) in the prototype illustrated in Table V where the control frequency f_s and output frequency f_o are respectively 15.9 kHz and 50 Hz. Thus the impacts of $G_d(s)$ on the second harmonic component are negligible. On the other hand, although $G_d(s)$ will bring in large phase angle changes at high frequencies, the-high frequency harmonic contents are quite small after filtered by BPF. Therefore, $G_d(s)$ in (5) can be removed directly, and a new LCFF controller is obtained as shown in (6) which can be implemented easily. Next section will prove that this simplification has little impacts on LCFF performance

$$\frac{\Delta u_{\rm busref}}{i_{\rm inv}} \approx \left(\frac{1}{sC_{\rm bus}} + R_C\right)\cdot G_{\rm BPF}\left(s\right)\cdot\left[1 + \frac{1}{G_v\left(s\right)U_{\rm in}}\right] = G_{\rm LCFF1}\left(s\right). \tag{6}$$

B. Simplify the Function $1 + 1/[G_v(s)U_{\rm in}]$

The frequency characteristic of function $1 + 1/[G_v(s)U_{\rm in}]$ in (6) is totally determined by the input voltage $U_{\rm in}$ and voltage-loop controller $G_v(s)$. When the controller parameters have been determined and the input dc voltage approximately remains constant, then its frequency characteristic can be decided. Further, second frequency harmonic is the main component of the signal which will be fed into the function $1 + 1/[G_v(s)U_{\rm in}]$ after filtered by BPF, thus only the frequency characteristic at $2f_o$ is the our concern.

In order to obtain adequate system phase margin, the corner frequency f_L of $G_v(s)$ is generally designed not larger than the resonant frequency $f_{\rm res}$ of the *LC* filter in the front-end dc–dc converter, where the frequencies f_L and $f_{\rm res}$ are, respectively, defined as

$$f_L = K_i \,/\, \left(2\pi K_p\right) \tag{7}$$

$$f_{\rm res} = 1 \,/\, \left(2\pi\sqrt{LC_{\rm bus}}\right). \tag{8}$$

If the resonant frequency $f_{\rm res}$ is lower than $2f_o$, then f_L is smaller than $2f_o$ as well. Actually, $f_{\rm res}$ is not exceeding $2f_o$ in many two-stage single-phase systems [20], [25], [26]. As shown in Fig. 6, when the corner frequency f_L of $G_v(s)U_{\rm in}$ is less than $2f_o$, the magnitude of $1 + 1/[G_v(s)U_{\rm in}]$ at and around $2f_o$ holds constant which is denoted as K_v here, and its phase angle is close to 0°. It indicates that the function $1 + 1/[G_v(s)U_{\rm in}]$ can be replaced by a proportional element K_v due to its frequency

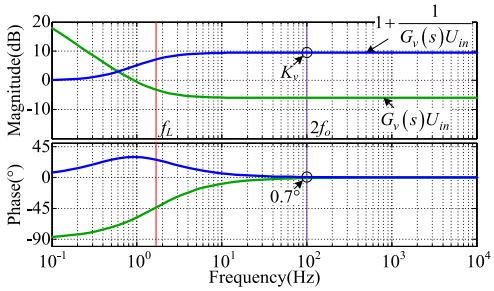


Fig. 6. Frequency characteristic of function $1 + 1/[G_v(s)U_{\rm in}]$.

characteristic, then (6) can be simplified as

$$\frac{\Delta u_{\rm busref}}{i_{\rm inv}} \approx \left(\frac{1}{sC_{\rm bus}} + R_C\right) \cdot G_{\rm BPF}(s) \cdot K_v = G_{\rm LCFF2}(s) \quad (9)$$

$$K_v = {\rm Mag}\left[1 + \frac{1}{G_v(j2\pi \cdot 2f_o)\, U_{\rm in}}\right] \quad (10)$$

where K_v can be calculated through (10). Note that this simplification is not an indispensable step. If the corner frequency f_L is higher than $2f_o$, or the input voltage $U_{\rm in}$ varies greatly, leading to the consequence that the function $1 + 1/[G_v(s)U_{\rm in}]$ cannot be equivalent to a proportional element, then this step can be skipped, and $1 + 1/[G_v(s)U_{\rm in}]$ should be kept unchanged. Simplifying or not will not influence the input ripple suppression effect.

C. Introduce a High-Pass Filter (HPF) $G_{\rm HPF}(s)$

A little amount of dc or very-low-frequency disturbance may be involved in LCFF control by the process of signal sampling or load step change. However, through the continuous integral action of $1/(sC_{\rm bus})$ element, the dc bias will grow rapidly in LCFF controller output, leading to a large steady-state tracking error in the intermediate-dc-bus voltage. In order to suppress the undesirable dc bias, an HPF is suggested to add at the end of LCFF controller.

Considering that the MAF structure can perform as an ideal low-pass filter, and it has the advantage of easy implementation in digital controller, an MAF-based HPF is utilized in this paper. A MAF expressed in s-domain is shown in (11) [32] where N_s is the number of samples taken by the filter in a period. An HPF based on MAF is derived as (12), and its implementation block diagram is illustrated in Fig. 7(a). To eliminate dc and very low-frequency components and meanwhile keep the second harmonic component unaffected, the sample number is set as $N_s = f_s/(2f_o)$ which yields to a moving window of $T_{\rm MAF} = 1/(2f_o)$

$$G_{\rm MAF}(s) = \frac{1}{N_s}\frac{1 - e^{-sN_sT_s}}{1 - e^{-sT_s}} \quad (11)$$

$$G_{\rm HPF}(s) = 1 - G_{\rm MAF}(s) = 1 - \frac{1}{N_s}\frac{1 - e^{-sN_sT_s}}{1 - e^{-sT_s}}. \quad (12)$$

Fig. 7(b) shows the bode plot of MAF and HPF. It can be seen that the HPF has a cutoff frequency of nearly 24 Hz, thus

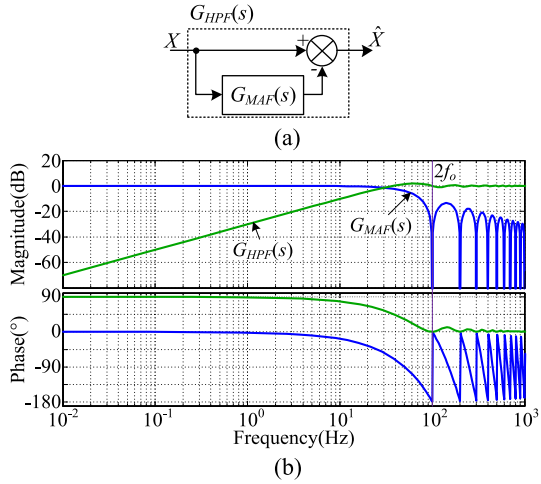


Fig. 7. Block diagram and bode plots of HPF: (a) Block diagram of HPF; (b) bode plot of $G_{\rm MAF}(s)$ and $G_{\rm HPF}(s)$.

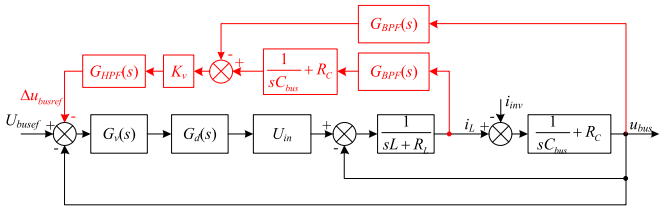


Fig. 8. Implementation block diagram of low-frequency current ripple reduction based on LCFF.

it possesses a good ability of suppressing dc and very low-frequency components without attenuating the component at $2f_o$. Consequently, the LCFF controller can finally be simplified as

$$\frac{\Delta u_{\rm busref}}{i_{\rm inv}} = \left(\frac{1}{sC_{\rm bus}} + R_C\right) \cdot K_v \cdot G_{\rm BPF}(s) \cdot G_{\rm HPF}(s) = G_{\rm LCFF}(s). \quad (13)$$

D. Implement the LCFF Control

Most systems may not be equipped with the dc–dc converter load current sensor. In this condition, one can utilize the filter inductor current i_L and dc bus voltage $u_{\rm bus}$ to calculate the instantaneous value of load current based on (14), and replace the actual load current value $i_{\rm inv}$ in (13) by the estimated one $i'_{\rm inv}$. Moreover, in order to avoid the differential items, the LCFF controller output can be calculated by (15), and the final implementation block diagram of low-frequency input current ripple reduction based on LCFF is obtained as shown in Fig. 8

$$i'_{\rm inv} = i_L - \frac{1}{1/(sC_{\rm bus}) + R_C} U_{\rm bus} \quad (14)$$

$$\Delta u_{\rm busref} = \left[i_L \cdot G_{\rm BPF}(s) \cdot \left(\frac{1}{sC_{\rm bus}} + R_C\right) - U_{\rm bus} \cdot G_{\rm BPF}(s)\right] \cdot K_v \cdot G_{\rm HPF}(s). \quad (15)$$

The physical implication of the proposed LCFF control can be explained as follows: Since we expect that the intermediate dc bus capacitor undertakes nearly all the low-frequency current which will further generate corresponding ripple voltage on the dc bus, it is unreasonable to set a constant reference for the instantaneous dc bus voltage control. The proposed method can solve the conflict by introducing a new path to add a proper ripple to the voltage reference. Namely, the dc bus voltage is controlled to pulsate at $2f_o$ actively which can make the dc bus capacitor supply the corresponding low-frequency ripple, thus preventing the pulsating power flowing into the front-end stage and leaving the input current ripple-free. Hence, the control strategy of this proposed method is quite different from those in [20] and [25]–[27], and the operation performance will be analyzed in the following section.

III. Operation Performance Analysis and Controller Design

The goal is to decrease the low-frequency input current ripple meanwhile remain other performances of the original system unaffected when adopting a ripple reduction method. This section is devoted to analyzing system operation characteristics, including stability, steady state, and dynamic performances.

Since the introduced LCFF path is not located in the close loop, the system characteristic equation is not changed which indicates that LCFF has no impacts on stability of the original system. This property further brings in such superiority: the design method of voltage regulator $G_v(s)$ can be conventional and easy, for it will not be influenced by LCFF controller. Other performance analysis will be presented in the following part.

On the other hand, the LCFF control parameters are crucial to the system performance. Section II has offered most of the parameter design methods. For example, HPF $G_{\rm HPF}(s)$ in Fig. 8 can be referred to (12) where $N_s = f_s/(2f_o)$, and proportion parameter K_v can be obtained by (10). They can be determined once the circuit and voltage control parameters have been designed. While the key parameter of the BPF $G_{\rm BPF}(s)$ expressed in (4), namely the bandwidth f_b, is not determined yet. This section will also discuss about the influence of f_b and its design principle.

A. Input Current Low-Frequency Ripple Reduction Effect

Define back current gain $A_i(s)$ as a transfer function from the input current $i_{\rm in}$ to the load current $i_{\rm inv}$, and its magnitude can be used to evaluate input current ripple reduction effect [20]. The back current gain transfer functions of the front-end dc–dc converters without and with the proposed LCFF are derived respectively in (16) and (17). For simplification and clarity, an appoint is made here that the variable with subscript "0" represents the one performed under traditional VMC, e.g., $A_{i0}(s)$; while the one with subscript "1" is obtained with the proposed LCFF, e.g., $A_{i1}(s)$. The key transfer functions and their physical implications are shown in Table I, and $G_{\rm LCFF}(s)$ is derived as (13)

$$A_{i0}(s) = \frac{\hat{i}_{\rm in0}}{\hat{i}_{\rm inv}} = A_i(s) - \frac{Z_o(s)\,G_v(s)\,G_d(s)\,G_{id}(s)}{1 + G_v(s)\,G_d(s)\,G_{vd}(s)} \quad (16)$$

TABLE I
Some Transfer Functions of the Back Current Gain Model for the Front-End DC–DC Converter

Definition	Physical implication	Transfer function
$A_i(s) = \hat{i}_{\rm in}/\hat{i}_{\rm inv}$	open-loop back current gain	$\frac{DR}{R+R_L}\cdot\frac{sR_C C_{\rm bus}+1}{G(s)}$
$Z_o(s) = \hat{u}_{\rm bus}/\hat{i}_{\rm inv}$	open-loop output impedance	$-\frac{R}{R+R_L}\cdot\frac{(sR_C C_{\rm bus}+1)(sL+R_L)}{G(s)}$
$G_{id}(s) = \hat{i}_{\rm in}/\hat{d}$	duty ratio to input current transfer function	$\frac{U_{\rm in}D}{R+R_L}\cdot\left[1+\frac{s(R_C+R)C_{\rm bus}+1}{G(s)}\right]$
$G_{vd}(s) = \hat{u}_{\rm bus}/\hat{d}$	Duty ratio to output voltage transfer function	$\frac{U_{\rm in}R}{R+R_L}\cdot\frac{sR_C C_{\rm bus}+1}{G(s)}$

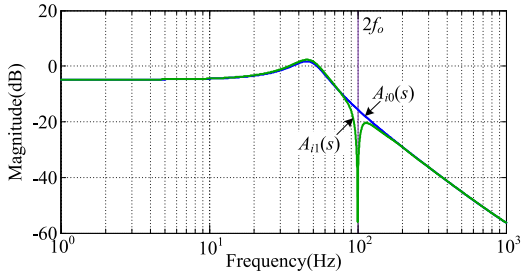


Fig. 9. Magnitude–frequency curves of back current gain without and with LCFF path.

$$A_{i1}(s) = \frac{\hat{i}_{\rm in1}}{\hat{i}_{\rm inv}} = A_i(s) - \frac{[Z_o(s) + G_{LCFF}(s)]\,G_v(s)\,G_d(s)\,G_{id}(s)}{1 + G_v(s)\,G_d(s)\,G_{vd}(s)}. \quad (17)$$

Here, D is the front-end dc–dc converter duty ratio, R is the equivalent load resistance at dc bus, $U_{\rm in}$ is the input voltage, and $G(s)$ expression is $G(s) = s^2\frac{LC_{\rm bus}(R+R_C)}{R+R_L} + s\frac{RC_{\rm bus}(R_L+R_C)+R_L R_C C_{\rm bus}+L}{R+R_L} + 1$.

Based on (16) and (17), Fig. 9 shows the magnitude-frequency curves of the back current gain for the systems without and with LCFF path. Take the system illustrated in Table V as an example, the cut-off frequency of the filter composed of inductor L and dc bus capacitor $C_{\rm bus}$ is 39 Hz. For the system without LCFF control, the amplitude of the back current gain $A_{i0}(s)$ at $2f_o$ is -15.6 dB which is not adequately low to attenuate the input low-frequency ripple. With the introduction of LCFF path, the magnitude of the back current gain $A_{i1}(s)$ is reduced to -44 dB at $2f_o$, and remains unchanged at other frequencies. It suggests that the proposed method has a strong ability of low-frequency ripple attenuation theoretically.

To get a further understanding of the reason why LCFF control can work, the approximate magnitude expressions of the back current gain at $2f_o$ for the systems without and with LCFF are, respectively, derived as (18) and (19) where $\omega_o = 2\pi f_o$. By comparing them, some analysis and explanations are made as follows.

1) According to (18), before introducing the LCFF control, the back current gain $A_{i0}(s)$ magnitude at $2f_o$ is greatly influenced by the parameters of voltage regulator $G_v(s)$. The greater the $G_v(s)$ magnitude at $2f_o$ is, the higher the input current ripple will be. It is because that when the PI controller parameters increase, the dynamic response grows faster, thus the equivalent output impedance of the dc–dc converter decreases, leading to a higher current ripple flowing into the dc–dc converter.
2) Equation (19) indicates that after introducing LCFF path, that item about $G_v(s)$ is cancelled which means the current ripple amplification by voltage regulator has been removed. Since $|sL + R_L| \ll R$ at $2f_o$, $|G_d(j2\omega_o)| = 1$ and $\angle G_d(j2\omega_o)$ is close to 0°, the magnitude value of $A_{i1}(s)$ at $2f_o$ in (19) is relatively small. It means that the low-frequency ripple reduction ability is greatly improved by adding LCFF control. However, it is influenced by the delay function $G_d(s)$. The smaller the delay phase angle introduced by $G_d(s)$ at $2f_o$ is, the better the input current ripple reduction effect will be.
3) Equation (19) does not involve the parameter f_b which is BPF bandwidth. It implies that the low-frequency reduction ability is not influenced by bandwidth f_b.
4) The magnitude value of $A_{i1}(s)$ at $2f_o$ in (19) cannot equal zero. It is because that there always exists low-frequency ripple in the intermediate dc bus voltage, and as a parallel branch, the front-end dc–dc converter must absorb a little amount of pulsating power. As a result, LCFF control can only greatly reduce the low-frequency ripple in the input current, but cannot completely eliminate it

$$\mathrm{Mag}\left[A_{i0}\left(j2\omega_o\right)\right] \approx \mathrm{Mag}\left\{\frac{D}{s^2LC_{\mathrm{bus}} + sC_{\mathrm{bus}}R_L + G_vG_dU_{\mathrm{in}} + 1} \times \left[1 + G_vG_dU_{\mathrm{in}}\left(1 + \frac{sL + R_L}{R}\right)\right]\Big|_{s=j2\omega_o}\right\} \tag{18}$$

$$\mathrm{Mag}\left[A_{i1}\left(j2\omega_o\right)\right] \approx \mathrm{Mag}\left\{\frac{D}{s^2LC_{\mathrm{bus}} + sC_{\mathrm{bus}}R_L + G_vG_dU_{\mathrm{in}} + 1} \times \left[\left(1 - G_d\right) - G_d \cdot \frac{sL + R_L}{R}\right]\Big|_{s=j2\omega_o}\right\} \tag{19}$$

$$\mathrm{Mag}\left[A_{i1\_\mathrm{with}Gd}\left(j2\omega_o\right)\right] \approx \mathrm{Mag}\left\{\frac{D}{s^2LC_{\mathrm{bus}} + sC_{\mathrm{bus}}R_L + G_vG_dU_{\mathrm{in}} + 1} \cdot \left[-\frac{sL + R_L}{R}\right]\Big|_{s=j2\omega_o}\right\}. \tag{20}$$

Actually, there is a delay function $G_d(s)$ in the denominator of the original LCFF controller as shown in (5). But when implementing LCFF to a physical circuit, $G_d(s)$ in LCFF controller can be directly removed by performing the step 1) in Section II. Here is some analysis about the influence of not compensating $G_d(s)$ in LCFF. Equation (5) is the original LCFF controller in which $G_d(s)$ is compensated in LCFF path. The back current gain for the system with $G_d(s)$ compensation in LCFF path, namely $A_{i1\_\mathrm{with}Gd}(s)$, can be obtained by substituting (5) into (17), and the approximate magnitude expression at $2f_o$ is derived as (20). It can be seen that when $G_{\mathrm{d}}(s)$ is compensated in the LCFF, $\mathrm{Mag}[A_{i1\_\mathrm{with}Gd}(j2\omega_o)]$ in (20) mainly depends on the circuit parameters and the voltage close-loop gain at $2f_o$, and is less related to $G_d(s)$. It means that compensating $G_d(s)$ in LCFF can make the ripple reduction effect less influenced by $G_d(s)$. By comparing (19) and (20), it can be found that if the control and sampling frequency is much higher than $2f_o$, $G_d(j2\omega_o)$ is trending to 1, and (19) is extremely close to (20). Thus, for the general systems, the ripple reduction ability without $G_d(s)$ compensation in LCFF is not quite different from the one with compensation.

TABLE II
INPUT RIPPLE REDUCTION PERFORMANCE COMPARISON BETWEEN WITH AND WITHOUT $< sc1 > G_d(s) < /sc1 >$ COMPENSATION IN LCFF CONTROL

	Magnitude of back current gain at $2f_o$	Theoretical value of the second harmonic in i_{in}
With $G_d(s)$ compensation	−44.45 dB	1.048%
Without $G_d(s)$ compensation	−44.42 dB	1.051%

Take the prototype described in Table V as an example, the values of $\mathrm{Mag}[A_{i1\_\mathrm{with}Gd}(j2\omega_o)]$, $\mathrm{Mag}[A_{i1}(j2\omega_o)]$, and the corresponding theoretical predictions of the second harmonic ripple in the input current i_{in} are respectively calculated and shown in Table II. Since the difference is quite small between the two rows of the data in Table II, it can be concluded that not compensating $G_d(s)$ in LCFF only has a little impact on ripple attenuation performance theoretically, and the impact can be accepted. Since the performance improvement is not quite evident and the controller will become much more complex when $G_d(s)$ is compensated in LCFF, not compensating $G_d(s)$ in LCFF is more appropriate and suggested.

B. Parameter sensitivity analysis of LCFF performance

From the final implementation block diagram of LCFF control as shown in Fig. 8, it is found that the values of circuit parameter C_{bus} and R_C, namely the dc bus capacitor and its ESR, must be known when applying LCFF. Thus it is necessary to analysis the sensitivity of LCFF control to the circuit parameters.

1) The influence of R_C to LCFF performance can be ignored, and the reasons are given as follows.
   The dc bus capacitor ESR value can be reduced by connecting several capacitors in parallel. Besides, the product of capacitance and its ESR, namely $C_{\mathrm{bus}} \cdot R_C$ here, tends to be constant for the electrolytic capacitor which is usually used as the dc bus capacitor, and it ranges from 50 to 80×10^{-6} Ω·F [33]. Since in (15) and (17), the parameter R_{C} always appears in the form of "$1 + sC_{\mathrm{bus}}R_C$" and $C_{\mathrm{bus}}R_C$ value is far less than 1, it is the reasonable to ignore the influence of $C_{\mathrm{bus}}R_C$ and simplify the item

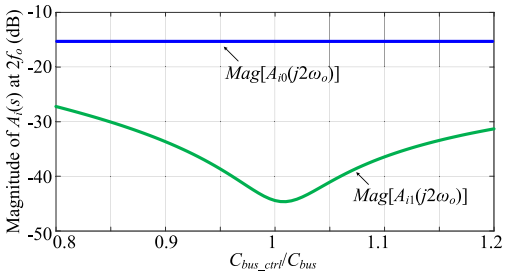


Fig. 10. Relation curve of capacitance error versus $\mathrm{Mag}[A_i(j2\omega_o)]$.

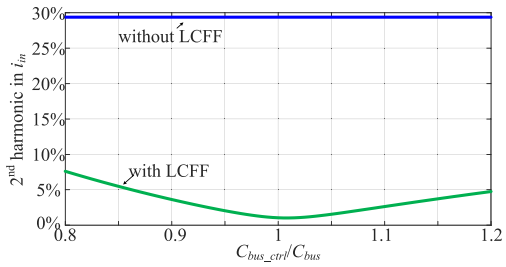


Fig. 11. Relation curve of capacitance error versus the second harmonic in input current i_{in}.

"$1 + sC_{\mathrm{bus}}R_C$" to "1." As the parameter R_C can be neglected in the equations, the influence of R_C to LCFF performance is quite small, and whether the R_C value is accurate or not is not very important when designing the LCFF controller.

2) The accuracy of parameter C_{bus} has an impact on the LCFF performance. However, this impact is acceptable.

Define C_{bus} is the dc bus capacitance in practical circuit, and $C_{\mathrm{bus\_ctrl}}$ is the dc bus capacitance which is used in the LCFF controller. In some conditions, $C_{\mathrm{bus\_ctrl}}$ may not be exactly equal to C_{bus}. Considering that the capacitance error ranges within $\pm 20\%$, the value of $C_{\mathrm{bus\_ctrl}}/C_{\mathrm{bus}}$ ranges from 0.8 to 1.2.

Fig. 10 shows the relation curve of the capacitance error versus the magnitude of the back current gains at $2f_o$. Before using LCFF, the magnitude of $A_{i0}(s)$ at $2f_o$ is only -15.6 dB; and after using LCFF, $\mathrm{Mag}[A_{i1}(j2\omega_o)]$ equals -44 dB when $C_{\mathrm{bus\_ctrl}} = C_{\mathrm{bus}}$. As $C_{\mathrm{bus\_ctrl}}/C_{\mathrm{bus}}$ deviates from 1, the value of $\mathrm{Mag}[A_{i1}(j2\omega_o)]$ is increased and the low-frequency ripple reduction performance will be degraded. When $C_{\mathrm{bus\_ctrl}}/C_{\mathrm{bus}} = 0.8, \mathrm{Mag}[A_{i1}(j2\omega_o)]$ reaches a maximum, namely -27.2 dB. Nevertheless, $\mathrm{Mag}[A_{i1}(j2\omega_o)]$ is still much smaller than $\mathrm{Mag}[A_{i0}(j2\omega_o)]$ which means adding LCFF control can still greatly improve the input ripple reduction performance.

To be more visible, Fig. 11 shows the relationship between capacitance error and the second harmonic component in the input current. When $C_{\mathrm{bus\_ctrl}} = C_{\mathrm{bus}}$, the input current ripple is nearly 29.1% before using LCFF, while it falls to 1.05% after adopting LCFF. The ripple component in i_{in} will increase as $C_{\mathrm{bus\_ctrl}}/C_{\mathrm{bus}}$ is not equal to 1. When $C_{\mathrm{bus\_ctrl}}/C_{\mathrm{bus}} = 0.8$, the ripple reduction effect is worst, and ripple component is 7.60%. Even so, this value is much smaller than the one without LCFF. Liu and Lai [6] suggest that the ripple current should be limited to less than 10%, and it can totally meet this requirement.

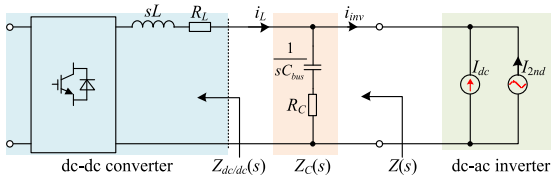


Fig. 12. Equivalent circuit of the two-stage single-phase inverter.

Thus, the accuracy of the capacitance used in controller indeed has an impact on LCFF performance. However, even when the capacitance error reaches -20%, the system with LCFF can still have a good ability of ripple reduction. Besides, $\pm 20\%$ capacitance error is very large, and the practical condition will be much better than this.

In conclusion, LCFF control has some dependence to the parameter accuracy; however, the control performance is acceptable in most applications. The parameters of C_{bus} and R_C can be directly obtained from the datasheet, since the parameter accuracy impact is not so strong. The precision LCR meter can also be used if better ripple reduction performance is required.

C. Output DC Voltage Tracking Accuracy

The dc bus voltage can be expressed as

$$U_{\mathrm{bus}} = G_c(s)\, U_{\mathrm{busref}} - Z(s)\, i_{\mathrm{inv}} \tag{21}$$

where

$$G_c(s) = \frac{(1 + sC_{\mathrm{bus}}R_C)\, G_v G_d U_{\mathrm{in}}}{B(s)} \tag{22}$$

$$Z_0(s) = \frac{(1 + sC_{\mathrm{bus}}R_C)\,(sL + R_L)}{B(s)} \tag{23}$$

$$Z_1(s) = \frac{(1 + sC_{\mathrm{bus}}R_C)\,(sL + R_L + G_{\mathrm{LCFF}}G_v G_d U_{\mathrm{in}})}{B(s)} \tag{24}$$

and $B(s) = s^2 LC_{\mathrm{bus}} + sC_{\mathrm{bus}}(R_C + R_L) + G_v G_d U_{\mathrm{in}}(1 + sC_{\mathrm{bus}}R_C) + 1$. $G_c(s)$ is the close-loop transfer function from voltage reference U_{busref} to the dc bus voltage U_{bus}, and it does not change after using LCFF control. $Z(s)$ can be viewed as the equivalent impedance of the parallel branches composed of the front-end dc–dc converter and the dc bus capacitor C_{bus} as shown in Fig. 12 [25]. $Z_0(s)$ and $Z_1(s)$ are the impedance expressions for the systems without and with LCFF, respectively. Hence, the dc bus voltage steady-state tracking accuracy may be affected by LCFF through the impedance $Z(s)$.

As there is an integral element $1/(sC_{\mathrm{bus}})$ in LCFF controller $G_{\mathrm{LCFF}}(s)$, the dc component may be accumulated continuously and added to the voltage reference during the transient response, resulting in a steady-state error in dc bus voltage. The dynamic process is most violent when the load current steps up from 0 to 100% or steps down from 100% to 0, thus in this situation the voltage error is largest

$$E_{\max} = \lim_{s \to 0} \left| s \cdot Z_1(s) \cdot \frac{I_{\mathrm{dc}}}{s} \right|. \tag{25}$$

TABLE III
LARGEST OUTPUT DC VOLTAGE ERROR UNDER DIFFERENT LCFF IMPLEMENTATIONS

LCFF implementation methods	LCFF controller expression	Largest dc voltage error $E_{\max}$
Step 1)	Equation (6)	$\frac{2\pi f_b}{(2\pi \cdot 2f_o)^2 C_{\rm bus}} \cdot \frac{I_{\rm dc}}{U_{\rm bus}}$
Step 2)	Equation (9)	$\frac{2\pi f_b}{(2\pi \cdot 2f_o)^2 C_{\rm bus}} \cdot \frac{I_{\rm dc}}{U_{\rm bus}} \cdot K_v$
Last step	Equation (13)	0

The largest voltage error $E_{\max}$ can be calculated according to (25), where $I_{\rm dc}$ is the dc component of the rated load current. Table III gives the largest dc voltage tracking errors under different LCFF implementations which have been derived in Section II. It can be concluded that in the first two steps, the converter will have a certain tracking error in its output dc voltage, and the error is proportional to BPF bandwidth f_b; while the error is totally eliminated at the last step after the HPF is introduced. It is because that the HPF which is the last stage of LCFF controller can get rid of the dc bias in the LCFF output, and guarantee that there is no dc bias added to the dc bus voltage reference. Then, the dc component of voltage reference always equals $U_{\rm busref}$, and will not be altered by LCFF output, thus making the dc output voltage error-free. Hence, the HPF is of great importance which can ensure the output voltage accuracy.

D. Low-Frequency Ripple in Intermediate DC Bus Voltage

Since LCFF control forces the dc bus capacitor supply all the pulsating power, the second harmonic voltage ripple on dc bus will also change after ripple reduction, and the downstream single-phase inverter may suffer a distorted output waveform once there are too much second harmonics in dc bus voltage. This part will discuss about the change trends of the low-frequency voltage ripple on dc bus between before and after using LCFF.

Under traditional VMC without LCFF, the front-end dc–dc converter output impedance is derived as

$$Z_{\rm dc/dc0}(s) = \frac{Ls + R_L}{G_v G_d U_{\rm in} + 1}. \tag{26}$$

Further, $Z_{\rm dc/dc0}(s)$ at the frequency of $2f_o$ can be expressed as

$$\begin{aligned} Z_{\rm dc/dc0}(j2\omega_o) &= \frac{j2\omega_o L + R_L}{G_v G_d(j2\omega_o) U_{\rm in} + 1} \\ &\approx \frac{j2\omega_o L + R_L}{K_v/(K_v - 1)} = j2\omega_o L_{eq0} + R_{eq0} \end{aligned} \tag{27}$$

where K_v can be referred to (10). Equation (27) reveals that the dc–dc converter at $2f_o$ under traditional VMC without LCFF can be equivalent to a branch consisting of an inductor with its ESR from the impedance–frequency characteristic perspective. Thus, the physical equivalent circuit model for the dc–dc converter under VMC can be obtained as shown in Fig. 13 where only second harmonic components are considered.

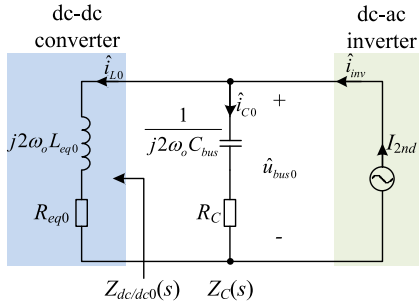


Fig. 13. Physical equivalent circuit model for the dc–dc converter at $2f_o$ under VMC without LCFF.

For the system without LCFF, the amplitudes and directions of current vector $\hat{i}_{L0}$, $\hat{i}_{C0}$, and $\hat{i}_{\rm inv}$ greatly depend on the resonant frequency $f_{\rm res0}$ of the *LC* circuit, where $f_{\rm res0} = 1/(2\pi\sqrt{L_{eq0}C_{\rm bus}})$, and different *LC* parameters can generate various phasor diagrams. Basically, the phasor diagram can be divided into three conditions according to the value of $f_{\rm res0}$ as illustrated in Table IV. The current reference directions have been marked in Fig. 13.

After applying LCFF, the dc–dc converter impedance at $2f_o$ is significantly increased and much larger than the dc capacitor impedance which will be validated in Section III-E. Hence, $|\hat{i}_{L1}|$ is close to zero; $\hat{i}_{C1}$ is considered approximately equal to $\hat{i}_{\rm inv}$. The current phasor diagrams for the system with LCFF are also shown in Table IV.

Case 1: When resonant frequency $f_{\rm res0}$ is less than $2f_o$, the impedance of the dc–dc converter at $2f_o$ is larger than the one of dc bus capacitor, thus the second harmonic currents flowing through them have following relationship:

$$\begin{aligned} &f_{\rm res0} < 2f_o \Rightarrow \frac{1}{2\pi \cdot 2f_o \cdot C_{\rm bus}} < 2\pi \cdot 2f_o \cdot L_{eq0} \\ &\Rightarrow |Z_C(j2\omega_o)| < \left|Z_{\rm dc/dc0}(j2\omega_o)\right| \Rightarrow \left|\hat{i}_{C0}\right| > \left|\hat{i}_{L0}\right|. \end{aligned} \tag{28}$$

Since the directions of currents $\hat{i}_{L0}$ and $\hat{i}_{C0}$ are completely opposite before ripple reduction, three currents meet

$$\hat{\mathbf{i}}_{\mathbf{inv}} = \hat{\mathbf{i}}_{\mathbf{C0}} + \hat{\mathbf{i}}_{\mathbf{L0}} \Rightarrow \left|\hat{i}_{\rm inv}\right| = \left|\hat{i}_{C0}\right| - \left|\hat{i}_{L0}\right| \Rightarrow \left|\hat{i}_{C0}\right| > \left|\hat{i}_{\rm inv}\right|. \tag{29}$$

Equation (29) indicates that for the system under traditional VMC without LCFF, ... It means that not only the downstream dc–ac stage requires second harmonic current, but also the front-end dc–dc converter needs amount of pulsating current due to the ripple voltage on dc bus. Consequently, the pulsating power offered by the dc bus capacitor is quite large, and $|\hat{i}_{C0}| > |\hat{i}_{\rm inv}|$.

Since LCFF control is able to cut down the pulsating current flowing through the front-end dc–dc converter, the dc bus capacitor only needs to offer ripple power to dc–ac stage, namely

$$\left|\hat{i}_{C1}\right| \approx \left|\hat{i}_{\rm inv}\right|. \tag{30}$$

It can be found that $|\hat{i}_{C0}| > |\hat{i}_{C1}|$ by comparing (29) and (30) which means the ripple current flowing through the dc bus capacitor is lowered after applying LCFF. Hence, the voltage

TABLE IV
CHANGE TRENDS OF $\hat{i}_C$ AND $\hat{u}_{\rm bus}$ UNDER VARIOUS CONDITIONS WITH DIFFERENT RESONANT FREQUENCIES

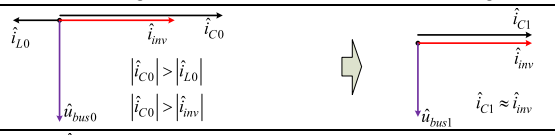
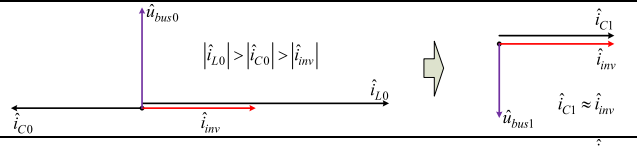
No.	Different f_{res0} of LC circuit	Phasor diagram		Change trends of $\hat{i}_C$ and $\hat{u}_{bus}$
		Before using LCFF	After using LCFF	
Case 1	$f_{res0} < 2f_o$			$\lvert\hat{i}_{C0}\rvert > \lvert\hat{i}_{C1}\rvert$ $\lvert\hat{u}_{bus0}\rvert > \lvert\hat{u}_{bus1}\rvert$
Case 2	$2f_o < f_{res0} < 2\sqrt{2}f_o$			$\lvert\hat{i}_{C0}\rvert > \lvert\hat{i}_{C1}\rvert$ $\lvert\hat{u}_{bus0}\rvert > \lvert\hat{u}_{bus1}\rvert$
Case 3	$f_{res0} > 2\sqrt{2}f_o$			$\lvert\hat{i}_{C0}\rvert < \lvert\hat{i}_{C1}\rvert$ $\lvert\hat{u}_{bus0}\rvert < \lvert\hat{u}_{bus1}\rvert$

TABLE V
SPECIFICATIONS AND PARAMETERS OF THE PROTOTYPE

	Parameters	Values
Specifications	Input voltage $U_{\rm in}$	700 V
	Intermediate dc bus voltage $U_{\rm bus}$	400 V
	Output ac voltage U_o/f_o	230 Vrms/50 Hz
	Control frequency f_s	15.9 kHz
Front-end dc–dc converter	Filter inductor L	4 mH
Intermediate dc bus	DC bus capacitor $C_{\rm bus}$	4.08 mF
Downstream dc–ac inverter	Filter inductor L_f	0.6 mH
	Filter capacitor C_f	20 μF

ripple on dc bus is also decreased after ripple reduction in this condition. Note that the prototype in this paper described in Table V belongs to case 1 because its resonant frequency $f_{\rm res0}$ is less than $2f_o$.

Case 2: When $f_{\rm res0}$ is greater than $2f_o$, then it has $|Z_C(j2\omega_o)| > |Z_{\rm dc/dc0}(j2\omega_o)|$ and $|\hat{i}_{C0}| < |\hat{i}_{L0}|$ before ripple reduction. The currents meet

$$\hat{\mathbf{i}}_{\mathbf{inv}} = \hat{\mathbf{i}}_{\mathbf{C0}} + \hat{\mathbf{i}}_{\mathbf{L0}} \Rightarrow \left|\hat{i}_{\rm inv}\right| = \left|\hat{i}_{L0}\right| - \left|\hat{i}_{C0}\right|. \tag{31}$$

Thus, it is the front-end dc–dc converter that supplies the pulsating power for both intermediate dc bus capacitor and downstream inverter before ripple reduction. Besides, the magnitude relationship between $|\hat{i}_{\rm inv}|$ and $|\hat{i}_{C0}|$ is various when the resonant frequency $f_{\rm res0}$ is different. If $|\hat{i}_{inv}| < |\hat{i}_{C0}|$ before ripple reduction, it can be derived from (31) as

$$\begin{aligned}&\left|\hat{i}_{L0}\right| - \left|\hat{i}_{C0}\right| < \left|\hat{i}_{C0}\right| \Rightarrow \left|\hat{i}_{L0}\right| < 2\left|\hat{i}_{C0}\right| \\ &\Rightarrow \left|Z_{\rm dc/dc0}\left(j2\omega_o\right)\right| > \left|Z_C\left(j2\omega_o\right)\right|/2 \Rightarrow f_{\rm res0} < 2\sqrt{2}f_o.\end{aligned} \tag{32}$$

It can be deduced that when $2f_o < f_{\rm res0} < 2\sqrt{2}f_o$, namely for the case 2 in Table IV, the currents have $|\hat{i}_{L0}| > |\hat{i}_{C0}| > |\hat{i}_{\rm inv}|$. As $|\hat{i}_{C1}| \approx |\hat{i}_{\rm inv}|$, the ripple current provided by dc bus capacitor will be lowered after ripple reduction, i.e., $|\hat{i}_{C1}| < |\hat{i}_{C0}|$. As a result, the ripple voltage on dc bus is also decreased after ripple reduction in this condition.

Case 3: On the contrary, when $f_{\rm res0} > 2\sqrt{2}f_o$, namely for the case 3 in Table IV, three currents meet $|\hat{i}_{L0}| > |\hat{i}_{\rm inv}| > |\hat{i}_{C0}|$. Therefore, only under this condition, it has $|\hat{i}_{C1}| > |\hat{i}_{C0}|$, and the ripple voltage on dc bus is increased after ripple reduction.

However, the resonant frequency $f_{\rm res}$ of the *LC* filter in the front-end dc–dc converter is lower than $2f_{\rm o}$ [20], [25], [26] in many systems which makes it very probable to meet $f_{\rm res0} < 2\sqrt{2}f_o$ belonging to case 1 or 2. Then, the change trend of dc bus voltage ripple will be decreased after ripple reduction. As a result, there is no need to worry that the LCFF control may mount the low-frequency ripple in dc bus voltage or deteriorate the ac output waveforms.

Note that Fig. 13 is a physical equivalent circuit model for helping to understand the ripple current propagation before ripple reduction, and those possible cases listed above are just assisted to provide some insight into how the dc bus voltage ripple changes before and after using LCFF. The exact dc bus voltage ripple proportion can be calculated as follows: the magnitudes of dc component and second harmonics in the front-end dc–dc converter load current $i_{\rm inv}$ have following mathematical relationship [26]:

$$I_{\rm dc} = I_{\rm 2nd}\cos\varphi \tag{33}$$

where $\cos\varphi$ is output power factor. Therefore, the dc bus voltage ripple proportion is derived as (34), where S_o is output apparent power, and impedance expression $Z(s)$ can be referred to (23) and (24)

$$\frac{\hat{u}_{\rm bus}}{U_{\rm bus}} = \frac{\left|Z\left(j2\omega_o\right)\right| \cdot I_{\rm 2nd}}{U_{\rm bus}} = \frac{\left|Z\left(j2\omega_o\right)\right|}{U_{\rm bus}^2/S_o}. \tag{34}$$

It should be noted that the low-frequency voltage ripple on dc bus after ripple reduction depends on the dc bus capacitor impedance for a system at rated power. Hence, to ensure the ac power quality, the intermediate dc bus capacitor design should follow this constraint: the voltage ripple on dc bus must be lower

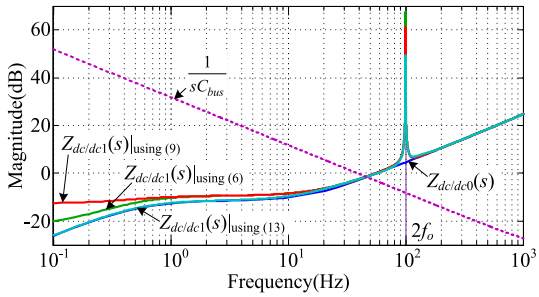


Fig. 14. DC–DC converter equivalent output impedance comparison between without and with LCFF control.

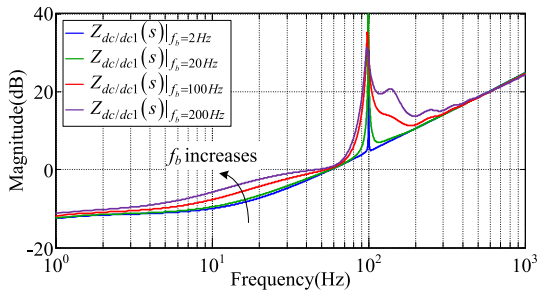


Fig. 15. DC–DC converter output impedances with LCFF under different BPF bandwidths.

than a certain value, such as 2.5% in [26], when $C_{\rm bus}$ supplies all the second harmonics drawn by the downstream dc–ac stage.

E. Dynamic Performance and BPF Design

Dynamic performance includes the characteristics of voltage reference tracking and load-disturbance rejection which are respectively determined by the transfer function $G_c(s)$ and $Z(s)$ in (21). As analyzed above, after introducing LCFF, only impedance $Z(s)$ is altered because of the changed front-end dc–dc converter output impedance $Z_{\rm dc/dc}(s)$, while $G_c(s)$ stays unchanged. Hence, $Z_{\rm dc/dc}(s)$ is chosen to test and compare their dc–dc converter dynamic characteristics. Without and with LCFF, the expressions of dc–dc converter output impedance are respectively derived as (26) and

$$Z_{\rm dc/dc1}(s) = \frac{(1+sC_{\rm bus}R_C)(Ls+R_L+G_vG_dG_{\rm LCFF}U_{\rm in})}{(1+sC_{\rm bus}R_C)(G_vG_dU_{\rm in}+1)-sC_{\rm bus}G_vG_dG_{\rm LCFF}U_{\rm in}}. \tag{35}$$

Fig. 14 shows the front-end dc–dc converter equivalent output impedance comparison between without and with LCFF path. Without LCFF path, the dc–dc converter impedance is only determined by the voltage regulator parameters. After LCFF controller is employed, only the impedance at $2f_o$ is increased dramatically which can obtain a better input second harmonic ripple rejection ability. However, under different LCFF implementation methods, the impedance magnitudes at very low frequency are quite different. When the HPF is used [see (13)], the impedance curve at low frequency decreases obviously, and it is extremely close to the curve of the original system impedance $Z_{\rm dc/dc0}(s)$. It reveals that the HPF in LCFF path can not only eliminate the steady-state voltage error, but also weaken the impacts on the dynamic response speed brought in by LCFF controller. It also proves that with the LCFF controller shown in Fig. 8, the system dynamic performance basically remains unchanged.

As the BPF $G_{\rm BPF}(s)$ is utilized to exact the component which swings at twice the output frequency, the bandwidth f_b should cover twice the output frequency variation range under normal condition no matter whether the downstream single-phase inverter is grid connected or stand-alone. Thus, the bandwidth design principle is that f_b value must be greater than twice the output frequency range. For example, if an inverter is tied to a 60 Hz power grid where the normal frequency range is $-0.7 \sim +0.5$ Hz [34], then f_b should be set at least as 2.8 Hz. Fig. 15 shows several impedance magnitude-frequency curves of the dc–dc converter with LCFF control under different BPF bandwidths. It is easy to find that as the bandwidth f_b increases, the impedance grows larger at very low frequency, slowing down the dynamic response. Hence, the value of f_b is not recommended to

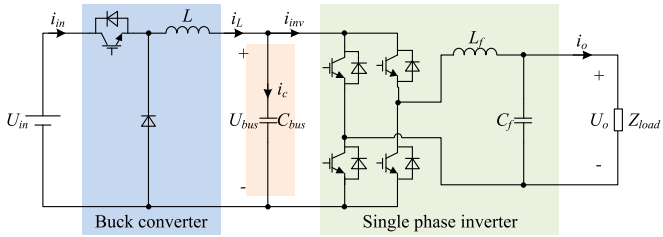


Fig. 16. Main circuit of the two-stage single-phase inverter.

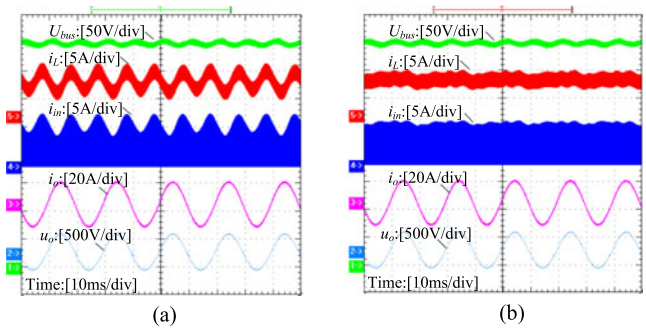


Fig. 17. Steady-state experimental waveforms *at 2.5 kW*: (a) Without LCFF. (b) With LCFF.

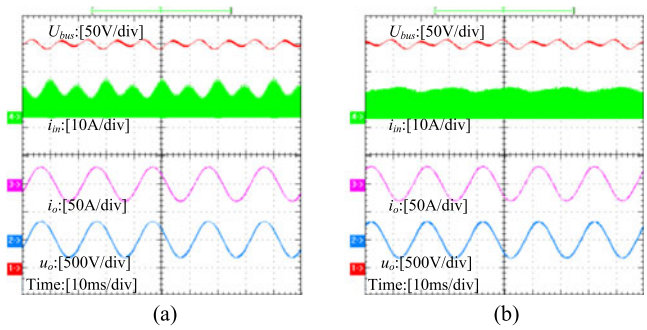


Fig. 18. Steady-state experimental waveforms *at 5 kW*: (a) Without LCFF. (b) With LCFF.

TABLE VI
KEY HARMONIC COMPONENTS COMPARISON AT 2.5 KW BETWEEN THEORETICAL AND EXPERIMENTAL RESULTS IN THE SYSTEM WITHOUT AND WITH LCFF

		DC bus voltage $U_{\rm bus}$		Input current $i_{\rm in}$	
		dc component	second harmonics	dc component	second harmonics
Without LCFF control	Experimental results	399.8	0.84%	3.73	27.35%
	Theoretical results	400.0	0.83%	3.61	29.14%
With LCFF control	Experimental results	399.6	0.68%	3.83	1.83%
	Theoretical results	400.0	0.64%	3.61	1.05%

TABLE VII
KEY HARMONIC COMPONENTS COMPARISON AT 5 KW BETWEEN THEORETICAL AND EXPERIMENTAL RESULTS IN THE SYSTEM WITHOUT AND WITH LCFF

		DC bus voltage $U_{\rm bus}$		Input current $i_{\rm in}$	
		dc component	second harmonics	dc component	second harmonics
Without LCFF control	Experimental results	400.5	1.65%	7.23	24.93%
	Theoretical results	400.0	1.53%	7.14	25.09%
With LCFF control	Experimental results	400.5	1.42%	7.20	0.84%
	Theoretical results	400.0	1.22%	7.14	0.65%

set too large in consideration of the dynamic behavior. Whereas when the bandwidths are too small, the changes of impedances at very low frequency are not quite obvious, such as the conditions in which f_b equals 2 and 20 Hz. In the system illustrated in Table V, bandwidth f_b is designed as 20 Hz.

IV. EXPERIMENTAL VERIFICATION

To demonstrate the performances of the proposed method, VMC without and with LCFF control have been tested on a two-stage single-phase inverter which is shown in Fig. 16. Actually, the inverter is working in a 700-V dc network on a ship, and the ship-electric-power system is similar to the one presented in [35]. The key specifications and parameters of the prototype are given in Table V. The basic control parameters of the front-end dc–dc converter are:

1) the voltage regulator parameters are: $K_pU_{\rm in} = 0.5$ and $K_iU_{\rm in} = 5$;
2) the LCFF controller is implemented based on (15) which is without compensating $G_d(s)$, and the key parameters are: $N_s = f_s/(2f_o) = 159$, $f_b = 20$ Hz, and $K_v = 3.0$.

A. Steady-State Verification

Figs. 17 and 18, respectively, show the steady-state experimental waveforms at 2.5 and 5 kW in the systems without and with LCFF. Here, $U_{\rm bus}$ represents the intermediate dc bus voltage; i_L is the dc–dc converter inductor current; $i_{\rm in}$ stands for the input current; and i_o and u_o are, respectively, the ac output current and voltage. The high-frequency noises in $U_{\rm bus}, i_L$, and $i_{\rm in}$ are the switching frequency harmonics. Based on the experimental waveforms in Figs. 17 and 18, some key harmonic components at 2.5 and 5 kW power levels are, respectively, extracted and listed in Tables VI and VII, and for a clear comparison, the corresponding theoretical results are also given.

At 2.5 kW, for the intermediate dc bus voltage $U_{\rm bus}$, the dc components remain unchanged before and after using LCFF, and the steady-state errors are always less than 1%. It proves that the LCFF control with HPF will not generate the tracking error in dc bus voltage. On the other hand, since $f_{\rm res0} < 2f_o$, this system belongs to case 1. In theory, the second harmonic component in $U_{\rm bus}$ will be reduced after ripple reduction according to the analysis in Section III-D. The theoretical values of second harmonics in $U_{\rm bus}$ is calculated based on (34). In steady-state experiments, the second ripple in $U_{\rm bus}$ is slightly reduced from 0.84% to 0.68% after applying LCFF, and they are basically consistent with the theoretical predictions. For the input current $i_{\rm in}$ under the same load condition, the dc components remain the same before and after ripple reduction which means that the LCFF will not influence power delivery. The low-frequency ripple proportion of $i_{\rm in}$ is 27.35% in the system without LCFF which far exceeds the limitations in [20], while the proportion falls to below 2% after introducing LCFF. The theoretical predictions are derived from (16) and (17). Even though there are slight differences between experimental and theoretical results, the differences are acceptable, and the change trends are same. It can also imply that the input ripple current can still be reduced significantly even if $G_d(s)$ is not compensated in LCFF path. Similarly, the input current ripple can also be suppressed greatly when operating at 5 kW, and the experimental results basically match with the predictions. From the steady-state experimental results, it can be seen that the second harmonic ripple components in both of $U_{\rm bus}$ and $i_{\rm in}$ are changed after the feedforward path is introduced. The input current ripple reduction is realized by controlling the dc bus voltage to swing properly at $2f_o$ and making the dc bus capacitor supply nearly all the pulsating power.

By comparing the data in Tables VI and VII, it can be found that the input current ripples after using LCFF are, respectively, 1.83% and 0.84% at 2.5 and 5 kW in the experiments. It indicates

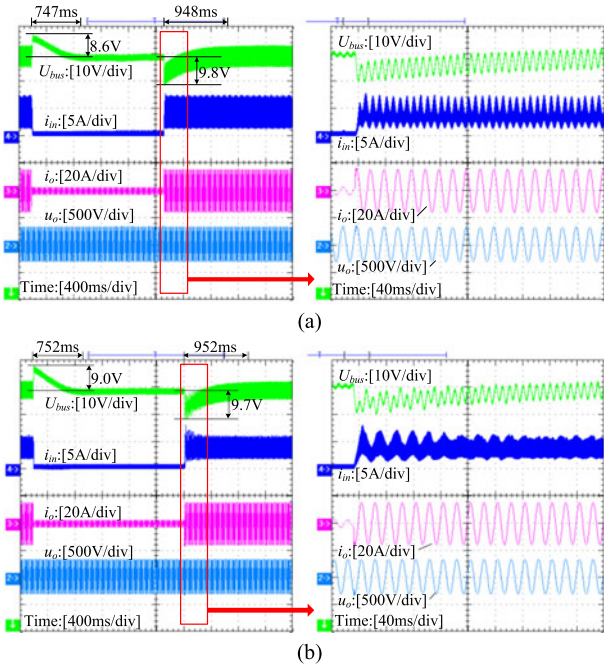


Fig. 19. Load transient response between 0.4 and 2.5 kW: (a) Without LCFF. (b) With LCFF.

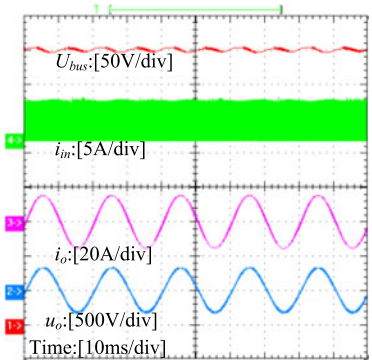


Fig. 20. Steady-state experimental waveforms at 2.5 kW under dual-loop control.

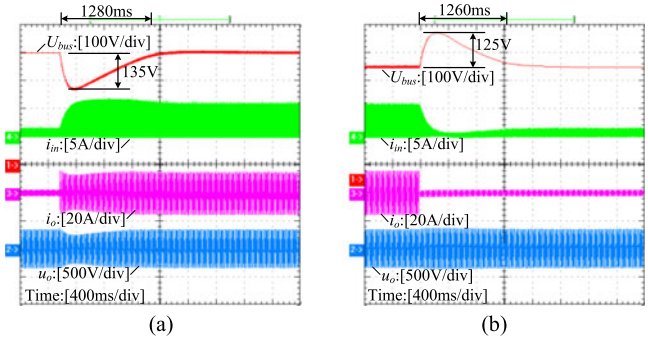


Fig. 21. Load transient responses between 0.4 and 2.5 kW under dual-loop control: (a) Load increases. (b) Load decreases.

that the input ripple difference is small after ripple reduction when the output power varies, and LCFF has good ripple attenuating performances at different power levels. The steady-state waveforms can effectively prove the ripple reduction ability of LCFF as well as the operation performance analysis above.

B. Dynamic Performance Verification

Fig. 19 shows transient responses of the systems without and with the LCFF control in which the ac output load changes from 2.5 to 0.4 kW and then back to 2.5 kW at last.

By comparing the waveforms in (a) and (b) of Fig. 19, it can be seen that the dynamic regulation processes for the systems without and with LCFF are almost same. When the load steps down from 2.5 to 0.4 kW, the input currents fall down rapidly, and the overshoots of the dc bus voltage are both close to 9 V. The settling times of dc bus voltage are almost 750 ms. Similarly, when the load steps up from 0.4 to 2.5 kW, the input currents rise up quickly where the maximums are less than 8 A, and the intermediate dc bus voltages have a certain drop which is less than 10 V. The settling times of the dc bus voltage for two systems are both nearly 950 ms. Both the overshoots/undershoots and settling times of the dc bus voltage are basically same for the systems without and with LCFF control.

The dynamic characteristic of the original system under traditional VMC is determined by the voltage regulator and circuit parameters, while it is almost unchanged after introducing LCFF control. This phenomenon agrees well with the aforementioned dynamic performance discussion.

C. Some Comparisons With Dual-Loop Control

The dual-loop control for the front-end dc–dc converter is formed by the outer intermediate dc bus voltage loop and the inner inductor current loop. This part offers some experimental comparisons between LCFF and dual-loop control. Here, the common PI regulators are used for the inner and outer controllers, and it has been pointed out by some literatures to be an effective and simple method for reducing the input current ripple. According to [20], the crossover frequencies of outer and inner loops should be well separated in order to obtain a good ripple reduction effect, and one decade separation around 100 Hz is recommended. The crossover frequency of the current loop should be pushed high, while the one of the outer loop must be designed as low as possible. For this prototype shown in Table V, the crossover frequencies of outer and inner loops are designed as 1 and 990 Hz, respectively. The outer-loop parameters are $K_{\rm pu} = 0.01$ and $K_{\rm iu} = 0.1$, while the inner-loop parameters are $K_{\rm pi}U_{\rm in} = 25$ and $K_{\rm ii}U_{\rm in} = 100$.

Fig. 20 shows the steady-state experimental waveforms at 2.5 kW for the system under dual-loop control, and the operating condition is same with the one in Fig. 17(b). In Fig. 20, the dc component of dc bus voltage $U_{\rm bus}$ is 400.6 V, and the second harmonic component is 0.77%. For the input current $i_{\rm in}$, the dc component is 3.59 A, while the second harmonic ripple proportion is nearly 1.12%. The low-frequency input current ripple can also be reduced to below 2% when traditional VMC with LCFF is adopted as shown in Table VI, and the second harmonic component proportions in $i_{\rm in}$ are similar under two different reduction methods. It indicates that LCFF control can achieve the same input ripple suppression effect as the dual-loop control does.

Fig. 21 shows the transient response waveforms of the system under the dual-loop control where the ac output load changes between 2.5 and 0.4 kW. The operating condition is almost same with the one in Fig. 19(b). When the load increases suddenly in Fig. 21(a), the dc bus voltage $U_{\rm bus}$ falls down 135 V, and the settling time reaches 1280 ms. Since $U_{\rm bus}$ drops too much in the dynamic state, the tops and bottoms of the ac output voltage and current waveforms are cut off in some first line periods. As the load decreases suddenly in Fig. 21(b), the dc bus voltage has a overshoot about 125 V, and the settling time is nearly 1260 ms. Comparing with the transient response waveforms in Fig. 19(b), it can be discovered that the dynamic performance of VMC with LCFF is much better than the one of simple dual-loop control, for it has smaller voltage overshoot/undershoot and shorter settling time.

There is a tradeoff between the dc bus voltage transient response speed and ripple reduction effect for the simple dual-loop control; therefore, the dynamic performance must be sacrificed if the effective input ripple suppression is required. Comparing the experimental results under two different reduction methods, it can be found that when the low-frequency input ripple suppression ability is almost same, the traditional VMC with LCFF will have a better dynamic performance than the simple dual-loop control.

V. Conclusion

To solve the input current low-frequency ripple problem caused by the pulsating power in a two-stage single-phase inverter, a control method is developed in this paper based on the front-end dc–dc converter LCFF. It intends to control the intermediate dc bus voltage to swing properly at the twice the output frequency and make the dc bus capacitor supply nearly all the ripple current. The implementation method of LCFF is illustrated, and performance analysis as well as parameter design principle is presented. The experiments are performed on a two-stage single-phase inverter prototype to confirm the effectiveness. Key features of the proposed LCFF control can be concluded as follows.

1) The input current ripple can be significantly reduced meanwhile with less affecting other original system performances. In the steady state, the low-frequency input ripple is well suppressed from 27.35% to 1.83% for the prototype at 2.5 kW; in the intermediate dc bus voltage, the dc component can still track the reference without error, and the second harmonic component will not be increased after ripple reduction. When the load step changes, the settling time and overshoot on dc bus voltage remain basically unchanged which means the dynamic characteristic is not influenced after applying LCFF.
2) This ripple reduction method can be realized without the need for auxiliary circuits. The voltage controller can be designed by the conventional approach, thus the design complexity will not be increased. It is because that the loop gain and system stability are not altered after introducing LCFF path.

Last of all, the idea of utilizing LCFF to reduce the input current ripple can be further expanded to other types of buck-derived (also called voltage-source type) dc–dc converters, such as the push–pull-forward, phase-shifted full-bridge, etc., since this method is not based on any feature which is particular to a buck converter.

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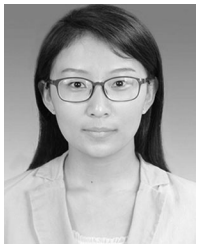

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