Improved Testing Capability of the Model-Assisted Testing Scheme for a Modular Multilevel Converter

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***Abstract*—Modular multilevel converters (MMCs) for high-power applications may contain over a thousand submodules. In work such as submodule design or innovation to build a full system with as many levels to test the submodule is time consuming and costly. To solve the problem, testing schemes are being developed to allow an individual submodule to be tested without a complete MMC. This paper presents a new submodule testing scheme that builds on a recent development to improve the testing capability. The improved structure is introduced along with design and control techniques. A design example of a test platform to test SMs with 2000-V rated voltage is introduced, which only requires a 545-V dc supply. The voltage testing capability is increased by more than five times when compared with the original scheme. In addition, simulation results show that the proposed method can offer better current tracking accuracy than the original with the same parameter settings. A prototype test platform, designed to test submodules with 400-V rated voltage and 14-A current, has been built and tested experimentally in order to verify the design.**

***Index Terms*—Design validation, electromagnetic and electrothermal characteristics, modular multilevel converter (MMC), submodule (SM), testing.**

I. Introduction

THE modular multilevel converter (MMC) is a promising technology for the next generation of high-power voltage-source converters targeting grid and other applications. The efficiency is usually improved because of the reduced switching frequency of the semiconductor devices [1]. The large number of steps in the synthesized ac-side voltage waveform produces a low distortion level and good EMC performance, which significantly reduces the need of passive filtering. The modular structure obviates direct series connection of the semiconductor devices [2]–[4].

Fig. 1 shows a typical dc to three-phase ac MMC that consists of six arms, each containing a string of submodules (SMs). In the work for SM design or topology innovation, it would be important to verify the design performance before the final assembly, in terms of electromagnetic, electrothermal, and electromechanical characteristics under practical operational conditions including SM faults. Building a complete MMC for SM testing would be both time consuming and costly. Various alternative methods were proposed to test the SM individually without a complete MMC [5]–[10]. Such single SM testing applies to any well-balanced system with identical SMs. The test of one SM can well predict the performance of the rest. There are two major challenges in single SM testing. First, the arm current that passes through the SM usually contains not only a sinusoidal component at the fundamental frequency, but also a dc offset and low-order harmonic circulating current components. Second, the switching frequency of the SM can be as low as the line frequency that is independent of the current passing through it. Hence, to accomplish the test, a current source is required to generate the reference "arm current" without the cooperation (switching) of the SM under test. Most of the test methods presented in the past [5]–[9] failed to address the two requirements simultaneously.

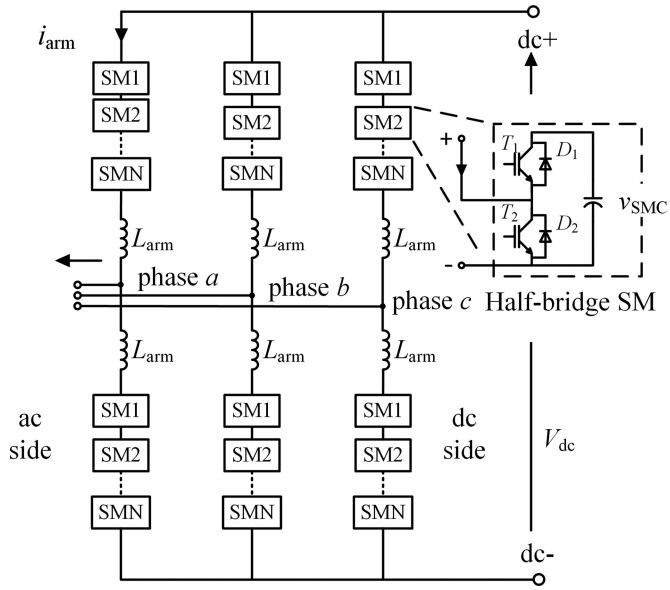

Fig. 1. Typical diagram of a MMC (half-bridge SM).

Tang *et al.* [10] proposed to use a full-bridge converter with a coupling inductor to emulate the required "arm current" through hysteresis control, as shown in Fig. 2. Both the generated "arm current" and the SM switching sequence are very close to the situation as if the SM were installed in a complete MMC. However, in order to generate the current in hysteresis control, the dc supply voltage of the full-bridge must be higher than the peak SM capacitor voltage. In some cases, the required dc supply voltage

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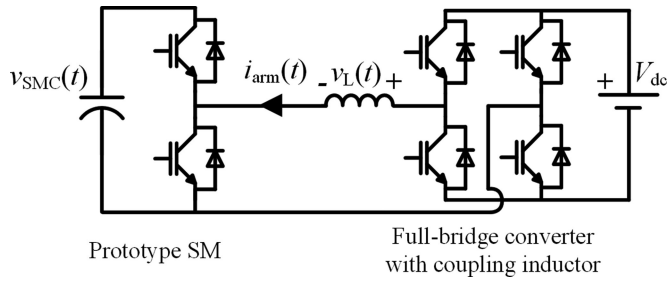

Fig. 2. Circuit diagram of the reported SM testing circuit extracted from [10].

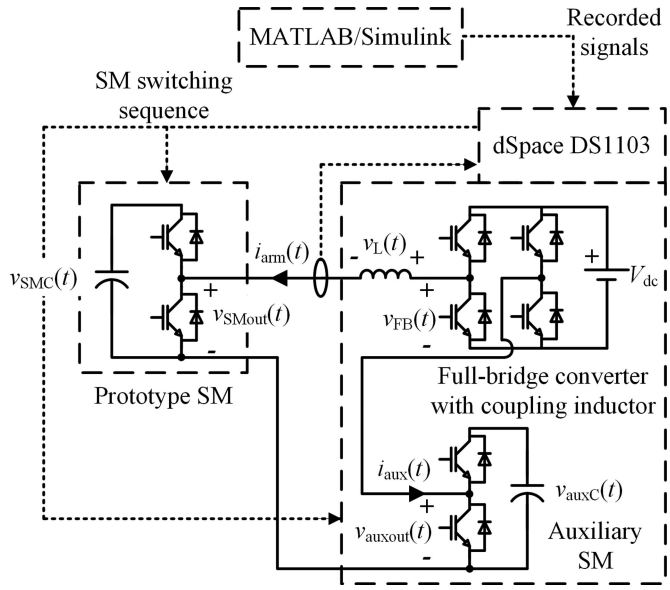

Fig. 3. Compensated SM testing scheme with half-bridge prototype SM.

would be more than double the rated voltage of the tested SM, which calls for much higher voltage withstanding capability of the power switches in the full-bridge converter. For tested SMs with rated voltage lower than 2 kV, the required dc supply voltage may be as high as 4 kV. In such a case, IGBT/diode power modules with higher voltage level (such as 6.5 kV) are still commercially available for the full-bridge, but if the SM rated voltage is higher than 2 kV, leading to more than 4-kV dc supply voltage, no existing IGBT/diode power modules can be directly used. Series connection of power switches in the full-bridge may have to be adopted to withstand the much higher dc supply voltage, leading to complex circuitry and voltage balancing scheme.

In order to improve the testing capability of the existing test platform as in Fig. 2, this paper proposes the use of an auxiliary SM to compensate the large dc voltage across the capacitor of the SM under test. By doing that the dc supply only needs to be higher than the SM capacitor voltage ripple (ac variation) that is much lower than the SM rated voltage, leading to largely reduced dc supply voltage demand, power switches' voltage withstanding capability, as well as the coupling inductance. The rest of this paper is organized as follows. Section II introduces the basic structure of the compensated SM testing scheme and its control strategy. As the original capacitor voltage regulator in [10] has opposite effects on the added auxiliary SM, a new voltage control is proposed for the auxiliary SM capacitor. Components selection to implement the current source is provided in Section III. After that the dc supply and coupling inductance demands of the proposed method are compared with the original. In Section IV, a design example of a test platform to test SMs up to 2000-V rated voltage is given. The testing capability of the same platform while using the original method is also presented. It shows that the proposed method can help us to increase the voltage testing capability by more than five times with even better current tracking accuracy. Computer simulation verifies the design. In Section V, a scaled-down prototype test platform, designed to test SMs with 400-V rated voltage and 14-A current, is built and tested experimentally. Section VI concludes this paper.

II. Compensated Model-Assisted SM Testing Scheme: Method and Control Strategy

A. Basic Concept and Circuit Diagram

Fig. 3 shows the compensated SM test platform with offline simulation as proposed in this paper. The MATLAB/Simulink is used as the reference signal generator and a dSpace DS1103 as the interface between the computer and the platform. The switching sequence and "arm current" signals are pregenerated and recorded through computer-aided simulation of a complete MMC. The recorded signals are then used to drive the current source and the SMs directly. If a powerful simulator is available to run the complete MMC simulation model in real time, the SM can be tested in an online environment. In such a case, the test platform acts as an output power amplifier that acquires the SM capacitor voltage signal in the physics domain and sends back to the simulator to close the control loop.

Similar to the uncompensated test platform shown in Fig. 2, the current source in the proposed compensated test platform also consists of a full-bridge converter and a coupling inductor. As the difference, an auxiliary SM is connected in series with the prototype SM in a reversed direction. Both SMs have the same current and voltage ratings. Note the ratings of the auxiliary SM can be higher than the prototype. With the same switching sequence, the two SM capacitors will be switched into the circuit simultaneously and the dc component in both capacitor voltages will be cancelled out leaving only small ac voltage variations. The voltage ripple of the two SMs would have the same shape but opposite polarities when identical capacitors are used. They are added together and the dc supply voltage $V_{\rm dc}$ only needs to be higher than the total peak voltage ripple of the two SMs to achieve the hysteresis current control. As the SM capacitor voltage ripple is usually very small in MMCs, the required dc supply voltage can be much less than the SM rated voltage.

B. Control Strategy—Hysteresis Control

Fig. 4 shows the control diagram of the proposed test platform. As discussed in [10], since the PI and the proportional-resonant (PR) controllers for single-phase inverters can only operate for a single frequency, in order to generate the desired "arm current" with not only the fundamental but also dc offset and other

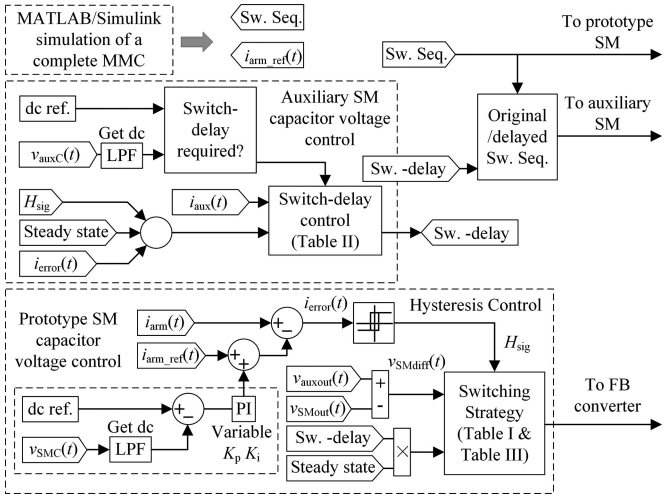

Fig. 4. Control diagram of the compensated SM test bench.

low order harmonics, multiple PI or PR controllers have to operate concurrently [11]–[13], complicating the controller design. In contrast, the hysteresis current control offers a simple and robust way to track the current reference with multiple components [14], [15]; it is therefore adopted. Simulation results showed that the hysteresis current controller is adequate, and the high-frequency current tracking errors introduced by the hysteresis switching have negligible impacts on the SM under test.

As shown in Fig. 3, the hysteresis current control can be realized by varying the voltage on the coupling inductor through switching the full-bridge converter. In order to limit the *di/dt* of the generated "arm current," the switching of the full-bridge shall not only consider the current tracking error $i_{\rm error}(t)$, but also outputs of the two SMs. In order to include such effect, as shown in Fig. 4 (the bottom dashed box), $v_{\rm SMdiff}(t)$ is defined as the output difference of the two SMs due to the reversed-series-connection configuration. The other control variable that affects the switching of the full-bridge is related to capacitor-voltage control of the auxiliary SM. In such as case, the two SMs will not be switched simultaneously for the reason to become clear later. Simultaneous switching is first assumed in analysis.

$i_{\rm error}(t)$ is the difference between the actual "arm current" $i_{\rm arm}(t)$ achieved by the hysteresis switching and its reference $i_{\rm arm\_ref}(t)$. The hysteresis band is defined as $\pm H_{\rm band}$. The selection of $H_{\rm band}$ will be discussed later. When $i_{\rm error}(t)$ is above the hysteresis band $+H_{\rm band}$, the output signal of the hysteresis block will be $H_{\rm sig}=1$, indicating that the actual "arm current" needs to be reduced. When $i_{\rm error}(t)$ is below $-H_{\rm band}$, $H_{\rm sig}$ will be 0, indicating that the actual "arm current" needs to be increased.

According to Fig. 3, the voltage on the coupling inductor $v_L(t)$ is

$$v_L(t)=v_{\rm FB}(t)+v_{\rm SMdiff}(t) \tag{1}$$

where $v_{\rm FB}(t)$ is the output voltage of the full-bridge. $v_{\rm SMdiff}(t)$ can be derived by

$$v_{\rm SMdiff}(t)=v_{\rm auxout}(t)-v_{\rm SMout}(t) \tag{2}$$

TABLE I
OUTPUT STRATEGIES FOR THE FULL-BRIDGE CONVERTER

Prototype and auxiliary SMs are simultaneously switched in/out			
$i_{\rm arm}$ is too small ($H_{\rm sig}=0$)	$v_{\rm FB}(t)$	$v_{\rm SMdiff}(t)<V_{\rm thres}$	$v_{\rm SMdiff}(t)\geq V_{\rm thres}$
		$+V_{\rm dc}$	0
	$v_L(t)$	$V_{\rm dc}+v_{\rm SMdiff}(t)$	$v_{\rm SMdiff}(t)$
$i_{\rm arm}$ is too large ($H_{\rm sig}=1$)	$v_{\rm FB}(t)$	$v_{\rm SMdiff}(t)\leq -V_{\rm thres}$	$v_{\rm SMdiff}(t)>-V_{\rm thres}$
		0	$-V_{\rm dc}$
	$v_L(t)$	$v_{\rm SMdiff}(t)$	$-V_{\rm dc}+v_{\rm SMdiff}(t)$

where $v_{\rm auxout}(t)$ is the output voltage of the auxiliary SM and $v_{\rm SMout}(t)$ is the output voltage of the prototype (see Fig. 3 for reference directions). When the capacitor of the auxiliary or the prototype SM is switched into the circuit, the output voltage $v_{\rm auxout}(t)$ or $v_{\rm SMout}(t)$ is about the capacitor voltage $v_{\rm auxC}(t)$ or $v_{\rm SMC}(t)$. When the SM is bypassed, the output voltage is approximately zero.

The switching strategy of the full-bridge converter is simple when both SMs are bypassed. In such a case, the full-bridge will output either $+V_{\rm dc}$ or $-V_{\rm dc}$ when the "arm current" is too small or too large. When the two SMs are switched into the circuit, as (1) shows, the inductor voltage is a combined effect of both the full-bridge output and the outputs of the SMs. When the actual "arm current" is too small and needs to be increased ($H_{\rm sig}=0$), $v_L(t)$ must be positive. One way to generate the positive $v_L(t)$ is through switching the full-bridge to have $v_{\rm FB}(t)=V_{\rm dc}$. This applies when $v_{\rm SMdiff}(t)$ is negative or positive but with small amplitude. As $v_{\rm SMdiff}(t)$ further increases, the total voltage ripple of the two SM capacitors is enough to increase the "arm current" at a comparable rate [compared with the case when $v_{\rm FB}(t)=V_{\rm dc}$]. In such a case, the full-bridge converter will only output zero voltage to limit the value of $v_L(t)$, which helps to limit the *di/dt* of the current and also the switching frequency. As a result, the coupling inductance can be very small and the switching frequency of the full-bridge would only vary in a small range. The threshold voltage to decide whether the full-bridge converter shall output $V_{\rm dc}$ or 0 is defined as $V_{\rm thres}$. The situation is similar when the actual "arm current" is too large and needs to be reduced ($H_{\rm sig}=1$). Due to symmetry, the threshold voltage in this case is $-V_{\rm thres}$. Detailed output strategies for the full-bridge are concluded in Table I.

One way to select the threshold voltage $V_{\rm thres}$ for the full-bridge to output zero voltage is to ensure that the changing rate of the current is faster than in the case when the full-bridge outputs $\pm V_{\rm dc}$. For instance, when $i_{\rm arm}(t)$ is too small and needs to be increased ($H_{\rm sig}=0$), the slowest rising rate of $i_{\rm arm}(t)$ in the case when $v_{\rm FB}(t)=V_{\rm dc}$ corresponds to the minimum coupling inductor voltage as

$$V_{L\min}=V_{\rm dc}+V_{\rm SMdiffmin} \tag{3a}$$

$$V_{\rm SMdiffmin}=-\left(\widehat{V}_{\rm SMCac}+\widehat{V}_{\rm auxCac}\right) \tag{3b}$$

where $\widehat{V}_{\rm SMCac}$ and $\widehat{V}_{\rm auxCac}$ are the amplitudes of the prototype and the auxiliary SM capacitor voltage ripples, respectively. For simplicity, the capacitor voltage ripple is assumed symmetrical

around its time average (dc component). The small difference between the positive and negative peaks is neglected. Two parameters k_{SMCac} and k_{auxCac} are defined as the ratio between the peak-to-peak voltage ripple and the rated dc voltage. That is

$$k_{\mathrm{SMCac}} = \frac{2\widehat{V}_{\mathrm{SMCac}}}{V_{\mathrm{SMCdc}}} \tag{4a}$$

$$k_{\mathrm{auxCac}} = \frac{2\widehat{V}_{\mathrm{auxCac}}}{V_{\mathrm{auxCdc}}} \tag{4b}$$

where V_{SMCdc} and V_{auxCdc} are the rated dc voltage of the prototype and the auxiliary SM capacitors, respectively. In order to achieve better voltage cancellation effect, the rated dc voltage of the auxiliary SM is set to be equal to that of the prototype, i.e.,

$$V_{\mathrm{auxCdc}} = V_{\mathrm{SMCdc}}. \tag{5}$$

As stated above, when the full-bridge converter outputs zero voltage, the minimum coupling inductor voltage would be equal to V_{thres}. The selection of V_{thres} must be large enough so that the rising rate of $i_{\mathrm{arm}}(t)$ is faster than the slowest case given by (3a). On the other hand, since the maximum inductor voltage will be $(V_{\mathrm{thres}} + V_{\mathrm{dc}})$ when $v_{\mathrm{FB}}(t) = V_{\mathrm{dc}}$, V_{thres} needs to be chosen as small as possible to limit the maximum current step. Hence, a suitable value for V_{thres} can be derived by substituting (3b), (4a), and (4b) into (3a), that is

$$V_{\mathrm{thres}} = V_{\mathrm{dc}} - \frac{1}{2}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right) V_{\mathrm{SMCdc}} \tag{6}$$

where V_{auxCdc} equals V_{SMCdc} when needed.

Due to symmetry, the negative threshold voltage is set at $-V_{\mathrm{thres}}$. In some cases, when both capacitor voltage ripples are so small that the threshold voltage is never met, the full-bridge converter will always output $\pm V_{\mathrm{dc}}$.

C. Control Strategy—Capacitor Voltage Control

In steady state, the time average (dc component) of a SM capacitor voltage will be constant for any given "arm current" and switching sequence from computer simulation. In practice, due to the switch-ON dead band, nonideal characteristics of power switches, and current tracking error of the current control, the capacitor dc voltage may not be balanced anymore [10]. As shown in Fig. 4, the prototype SM adopts the voltage regulator proposed in [10] through injecting small compensation current into the "arm current." The value of the injected current is derived by a PI controller with variable gains. The input of the PI controller is the error between the SM capacitor dc voltage reference and the actual measurement. During energizing and discharging of the SM capacitor, the proportional gain (K_{p}) is large and the integral gain $(K_{\mathrm{i}})$is very small for fast transient response. When the system reaches steady state, K_{p} is largely reduced and K_{i} is increased so that the PI controller will then be dominated by the integral part with very small bandwidth to limit noise effect. The advantage of this voltage regulator is that no time delay will be introduced between the "arm current" and the switching sequence of the SM to ensure high accuracy of the test. In steady state, the injected current is usually less than 1% of the peak "arm current" and it has been shown to have negligible impacts on the test results [10].

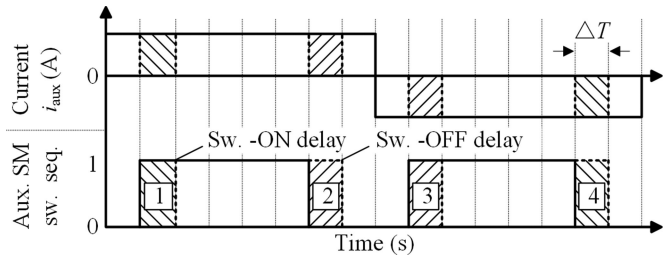

Fig. 5. Auxiliary SM (aux. SM) capacitor voltage regulator through switch-delay control.

For the auxiliary SM, however, the aforementioned voltage regulator will have opposite effects on its capacitor dc voltage $v_{\mathrm{auxCdc}}(t)$ due to the reversed-series-connection configuration. Positive injected current will actually reduce $v_{\mathrm{auxCdc}}(t)$. To solve this problem, Fig. 5 shows a switch-delay control for the auxiliary SM, which is independent from the prototype SM voltage regulator. The top graph is the current flowing into the auxiliary SM $i_{\mathrm{aux}}(t)$ (see Fig. 3) and the bottom shows its switching sequence, where "1" stands for SM switched-in and "0" means SM bypassed. ΔT is the sampling period of the test platform. When $i_{\mathrm{aux}}(t)$ is positive, if a switch-ON delay is applied, the capacitor will not get charged during the delay period, and if a switch-OFF delay is applied, the capacitor will get further charged. In the other case, when $i_{\mathrm{aux}}(t)$ is negative, the capacitor will be discharged less or get further discharged if switch-ON or switch-OFF delay is applied.

Note when the switching of the auxiliary SM is delayed, the two SMs will be no longer switched simultaneously. $v_{\mathrm{SMdiff}}(t)$ will equal to one full SM capacitor voltage, either $v_{\mathrm{SMC}}(t)$ or $v_{\mathrm{auxC}}(t)$, which is usually much higher than V_{dc}. In such a case, the full-bridge converter will not be able to control the "arm current" $i_{\mathrm{arm}}(t)$ and the dynamics of $i_{\mathrm{arm}}(t)$ will be dominated by $v_{\mathrm{SMdiff}}(t)$. For instance, when $v_{\mathrm{auxCdc}}(t)$ is too high, switch-OFF delay can be applied when $i_{\mathrm{aux}}(t)$ is negative to get further discharged. At this moment, only the auxiliary SM capacitor is connected in the circuit and $v_{\mathrm{SMdiff}}(t)$ equals $v_{\mathrm{auxC}}(t)$ according to (2). As V_{dc} is always smaller than $v_{\mathrm{auxC}}(t)$, $i_{\mathrm{arm}}(t)$ tends to increase in any event. In order to ensure that the current error is always within the allowable band in steady state, the switch-OFF delay can be only applied when $i_{\mathrm{arm}}(t)$ actually needs to be increased $(H_{\mathrm{sig}} = 0)$, and the current tracking error $i_{\mathrm{error}}(t)$ is less than a threshold current $I_{\mathrm{thres-}}$. $I_{\mathrm{thres-}}$ is usually negative and is set to leave enough margin for $i_{\mathrm{error}}(t)$ to increase. If the permitted maximum current tracking error is defined as ΔI_{max} and the maximum current change of $i_{\mathrm{error}}(t)$ during a switch-delay period is $dI_{\mathrm{error\_delay}}$. The current threshold can be derived as

$$I_{\mathrm{thres-}} = \Delta I_{\mathrm{max}} - dI_{\mathrm{error\_delay}}. \tag{7a}$$

In the same case [$v_{\mathrm{auxCdc}}(t)$ is too high], when $i_{\mathrm{aux}}(t)$ is positive, the switch-ON delay can be applied and the auxiliary SM capacitor will not be charged during the delay period. At this

TABLE II
SWITCH-DELAY STRATEGIES FOR THE AUXILIARY SM

$v_{\mathrm{auxCdc}}(t)$	$i_{aux}(t) \le 0$ (flow out)	$i_{\mathrm{aux}}(t) > 0$ (flow in)
Too high	Switch-OFF delay ($H_{\mathrm{sig}} = 0$ and $i_{\mathrm{error}}(t) < I_{\mathrm{thres}-}$)[a]	Switch-ON delay ($H_{\mathrm{sig}} = 1$ and $i_{\mathrm{error}}(t) > I_{\mathrm{thres}+}$)[a]
Too low	Switch-ON delay ($H_{\mathrm{sig}} = 1$ and $i_{\mathrm{error}}(t) > I_{\mathrm{thres}+}$)[a]	Switch-OFF delay ($H_{\mathrm{sig}} = 0$ and $i_{\mathrm{error}}(t) < I_{\mathrm{thres}-}$)[a]

[a]Only applied in steady state.

TABLE III
OUTPUT STRATEGIES FOR THE FULL-BRIDGE CONVERTER

Auxiliary SM switch-delay control active (steady state)		
Switch-OFF delay	$v_{\mathrm{FB}}(t)$	$-V_{\mathrm{dc}}$
	$v_L(t)$	$-V_{\mathrm{dc}} + v_{\mathrm{auxC}}(t)$
Switch-ON delay	$v_{\mathrm{FB}}(t)$	$+V_{\mathrm{dc}}$
	$v_L(t)$	$V_{\mathrm{dc}} - v_{\mathrm{SMC}}(t)$

moment, $v_{\mathrm{SMdiff}}(t)$ would equal to $-v_{\mathrm{SMC}}(t)$ and $i_{\mathrm{arm}}(t)$ tends to decrease in any event. Hence, the switch-ON delay can only be applied when $i_{\mathrm{arm}}(t)$ actually needs to be reduced ($H_{\mathrm{sig}} = 1$) and $i_{\mathrm{error}}(t)$ is higher than a positive threshold current $I_{\mathrm{thres}+}$. Similar to (7a), the value of $I_{\mathrm{thres}+}$ can be derived by

$$I_{\mathrm{thres}+} = -\Delta I_{\max} + dI_{\mathrm{error\_delay}}. \tag{7b}$$

Detailed switch-delay strategies for the auxiliary SM are concluded in Table II. As the conditions in the brackets would slow down the dynamics of the voltage control, they are only applied in steady state. In transient, the switch delay is used whenever $v_{\mathrm{auxCdc}}(t)$ is outside the permitted range. The period of the switch delay is usually chosen as short as possible to limit the resulting large current error. In the prototype, it equals the sampling period ΔT (50 μs) of the test platform dSpace DS 1103.

Table III offers another measure to limit the current error during the switch-delay period by compensating the large $v_{\mathrm{SMdiff}}(t)$. The full-bridge converter will output $-V_{\mathrm{dc}}$ when the switch-OFF delay is used and will output $+V_{\mathrm{dc}}$ when the switch-ON delay is used.

III. COMPONENTS SELECTION TO IMPLEMENT THE CURRENT SOURCE

The primary objective of the test platform is to provide the desired "arm current" and inject it into the prototype SM. Due to the constant switching of the SM capacitor, the load conditions of the full-bridge converter vary frequently. Hence, in order to keep the current tracking error within an allowable range at all times, parameters of the test platform must be carefully chosen. In this section, dynamic characteristics of the "arm current" generated by the proposed testing method are first analyzed and compared with the original method [10]. Based on the understanding of the current tracking error, a method is provided to select the coupling inductance L and the full-bridge converter dc supply voltage V_{dc}, which can be applied to both testing methods. After that the component demands and testing capabilities of the two methods are compared in detail.

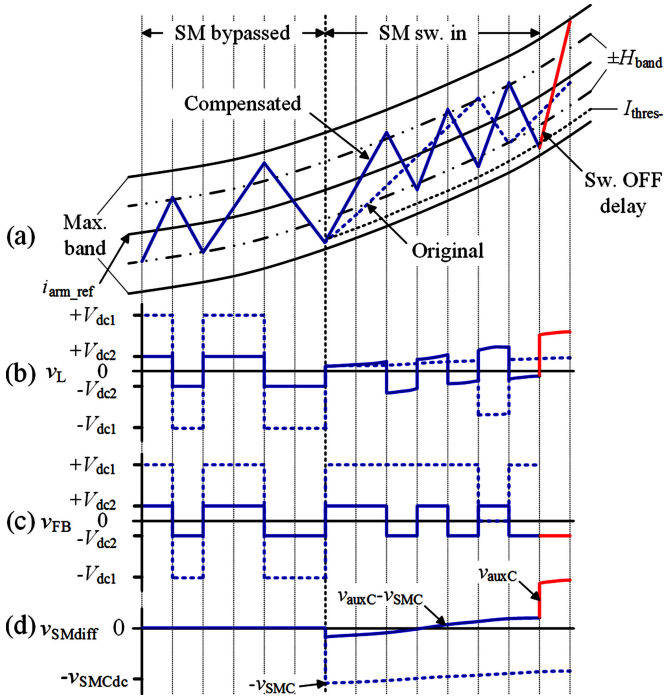

Fig. 6. (a) Typical "arm current" waveforms; (b) inductor voltages (V_{dc1} is the dc supply voltage for the original method and V_{dc2} is for the proposed method); (c) full-bridge converter output voltages and (d) SM output voltage difference (for the original method, v_{auxC} always equals 0).

A. Current Dynamics and Tracking Error

Fig. 6 shows the measured characteristics of current and voltage waveforms of the two testing methods. The solid saw-tooth line represents waveforms for the proposed method, while the dashed saw-tooth line is for the original method. When the prototype SM capacitor is bypassed (as well as the auxiliary SM capacitor in the proposed method), the coupling inductor voltage $v_L(t)$ will equal the full-bridge output $v_{\mathrm{FB}}(t)$ for both methods as in Fig. 6(b) and (c). When the SM capacitor is switched in, for the original method, the inductor voltage would be equal to either the entire SM capacitor voltage $v_{\mathrm{SMC}}(t)$ or the difference between $v_{\mathrm{FB}}(t)$ and $v_{\mathrm{SMC}}(t)$ depending on the current tracking error thereby leading to unsymmetrical increasing and decreasing rate of i_{arm}. For the proposed method, the inductor voltage in such a case would be the difference between $v_{\mathrm{FB}}(t)$ and the total voltage ripple $v_{\mathrm{SMdiff}}(t)$ or $v_{\mathrm{SMdiff}}(t)$ alone. Both the increasing and decreasing rate of i_{arm} would depend on $v_{\mathrm{SMdiff}}(t)$. In all cases, although the proposed method uses a much lower supply voltage, due to the smaller coupling inductor, the current dynamics in the two methods are similar. The last segment (waveform) for the proposed method shows the current and voltage responses during the switch-delay control. At this moment, one entire SM capacitor voltage, either the prototype or the auxiliary will be applied on the inductor. Components selection for the proposed method shall also consider the switch-delay control in order to keep the current error within the allowable bands at all times.

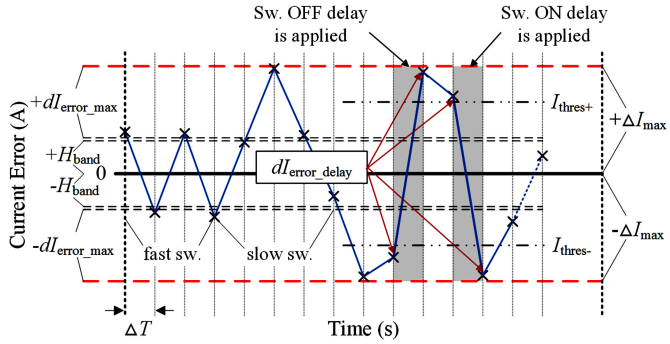

Fig. 7. Typical waveform of the current error $i_{\mathrm{error}}(t)$.

Fig. 7 shows a typical waveform of the current tracking error $i_{\mathrm{error}}(t)$ when using the proposed testing method. The outermost dashed lines define the permitted current error range $[-\Delta I_{\max}, +\Delta I_{\max}]$ that $i_{\mathrm{error}}(t)$ must never exceed. The innermost double dashed lines are the thresholds for the hysteresis control. When $i_{\mathrm{error}}(t) > +H_{\mathrm{band}}$, $H_{\mathrm{sig}} = 1$ and when $i_{\mathrm{error}}(t) < -H_{\mathrm{band}}$, $H_{\mathrm{sig}} = 0$. Due to the limited sampling frequency f_s of the test platform, the actual current error may be much larger than the hysteresis band. That is the reason a margin is left between the outer $\pm\Delta I_{\max}$ and inner $\pm H_{\mathrm{band}}$. The minimum width of this band equals the maximum current error step in a sampling period ΔT, i.e., $dI_{\mathrm{error\_max}}$. The remaining two double-dots dashed lines are the current thresholds $I_{\mathrm{thres}+}$ and $I_{\mathrm{thres}-}$ for the auxiliary SM switch-delay control.

B. Selection of Control Parameters

The maximum permitted current error $\pm\Delta I_{\max}$ defines the current tracking performance of the test platform. One way to determine $\pm\Delta I_{\max}$ is according to the resulting error in the experiment outputs, such as losses in the prototype SM power switches. A detailed selection process can be found in [10]. In order to quantify and compare the current tracking performance of different test platforms, $\Delta I_{\max}$ can be written as

$$\Delta I_{\max} = k_{\Delta I_{\max}} A \tag{8}$$

where A is the peak amplitude of the fundamental component in the reference "arm current" and $k_{\Delta I_{\max}}$ is defined as the error constant. Usually, $k_{\Delta I_{\max}}$ is around 0.1–0.15 depending on the required current tracking accuracy of certain tests. The impacts of different $k_{\Delta I_{\max}}$ settings on the component selection will be detailed later.

Once the permitted current error $\pm\Delta I_{\max}$ is decided, the hysteresis band $\pm H_{\mathrm{band}}$ can be selected. As the hysteresis band directly decides the switching of the full-bridge converter, one design criterion of $\pm H_{\mathrm{band}}$ is to ensure that the upper switching frequency limit of the full-bridge ($f_{\mathrm{sw\_max}}$) will never be exceeded for heat dissipation and EMC reasons. As shown by the "fast switching" in Fig. 7, in such a case, the full-bridge would change its output at the very sampling instant as the current error is always larger than the hysteresis band $[-H_{\mathrm{band}}, +H_{\mathrm{band}}]$. In such a case, the actual switching frequency will be half of the sampling frequency f_s. If the permitted switching frequency is lower than that value, the width of the hysteresis band must be larger than the maximum current error step $dI_{\mathrm{error\_max}}$ in a sampling period. This can be derived as

$$dI_{\mathrm{error\_max}} = \frac{1}{L} V_{L\max} \Delta T + \omega A \Delta T \tag{9}$$

where $V_{L\max}$ is the maximum inductor voltage, and ω is the MMC ac-side line frequency. Here, in estimation, the harmonic circulating current components are neglected because of their much lower amplitudes. In cases where the harmonic currents are not small, their effects shall be included. A fixed relation can be found between H_{band} and $dI_{\mathrm{error\_max}}$ to ensure that $f_{\mathrm{sw\_max}}$ is never exceeded as [10]

$$H_{\mathrm{band}} = \frac{1}{2} \left\lfloor \frac{f_s}{2 f_{\mathrm{sw\_max}}} \right\rfloor dI_{\mathrm{error\_max}}. \tag{10}$$

C. Selection of Component Parameters

This section will focus on the selection of the components for the coupling inductance L and the dc supply voltage V_{dc}. First, in order to ensure the current error is always within the permitted range $[-\Delta I_{\max}, +\Delta I_{\max}]$, the minimum gap between $\pm\Delta I_{\max}$ and $\pm H_{\mathrm{band}}$ must equal the maximum current error step $dI_{\mathrm{error\_max}}$, given by

$$\Delta I_{\max} - H_{\mathrm{band}} \geq dI_{\mathrm{error\_max}}. \tag{11}$$

Substituting (9) and (10) into (11) gives

$$\frac{V_{L\max}}{L} \leq \frac{2\Delta I_{\max} f_s}{2 + \left\lfloor \frac{f_s}{2 f_{\mathrm{sw\_max}}} \right\rfloor} - \omega A. \tag{12}$$

Note that $\Delta T = 1/f_s$. Equation (12) gives the upper limit of the ratio between $V_{L\max}$ and L. Another design criterion is that the rising speed of the "arm current" must be faster than its reference at any time. With the harmonic components neglected, the fastest rising speed of the reference occurs when the current crosses its dc offset from underneath. At that instant, the slope equals to ωA and (13) must be satisfied

$$\frac{V_{L\min}}{L} > \omega A \tag{13}$$

where $V_{L\min}$ is the minimum inductor voltage.

Due to symmetry, only the case when $i_{\mathrm{arm}}(t)$ is rising is considered. $V_{L\max}$ and $V_{L\min}$ are the maximum and minimum inductor voltage when it is positive (or absolute value). The above equations also apply when $i_{\mathrm{arm}}(t)$ is decreasing.

According to (3)–(6) and Table I, $V_{L\max}$ and $V_{L\min}$ can be derived as

$$V_{L\max} = 2V_{\mathrm{dc}} - \frac{1}{2}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right) V_{\mathrm{SMCdc}} \tag{14a}$$

$$V_{L\min} = V_{\mathrm{dc}} - \frac{1}{2}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right) V_{\mathrm{SMCdc}}. \tag{14b}$$

Note that the auxiliary SM switch-delay control is assumed inactive here.

Substituting (14a) and (14b) into (12) and (13) leads to

$$\omega LA + \frac{1}{2}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right) V_{\mathrm{SMCdc}} < V_{\mathrm{dc}} \leq \frac{k_{\Delta I_{\max}} f_s LA}{2 + \left\lfloor \frac{f_s}{2 f_{\mathrm{sw\_max}}} \right\rfloor} - \frac{\omega LA}{2} + \frac{1}{4}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right) \times V_{\mathrm{SMCdc}}. \quad (15)$$

As the maximum value of (15) must be larger than the minimum, leading to the lower limit of the inductance L as

$$L > \frac{\frac{1}{2}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right)}{\frac{2k_{\Delta I_{\max}} f_s}{2 + \left\lfloor \frac{f_s}{2 f_{\mathrm{sw\_max}}} \right\rfloor} - 3\omega} \frac{V_{\mathrm{SMCdc}}}{A} \quad (16)$$

where $\Delta I_{\max}$ equals $k_{\Delta I_{\max}} A$ when needed as in (8).

Equations (15) and (16) give the criteria to choose V_{dc} and L for the current source. If the platform is required to test different SMs with various specifications, the inductance can be chosen as the highest value for all cases. Then, V_{dc} can be decided by (15).

Note that (14a) does not include the auxiliary SM switch-delay control. When all parameters are decided, the current thresholds $I_{\mathrm{thres+}}$ and $I_{\mathrm{thres-}}$ can be derived by (7a) and (7b). If the two thresholds are outside the permitted region $[-\Delta I_{\max}, +\Delta I_{\max}]$, the switch-delay period shall be reduced or the supply voltage V_{dc} shall be increased to further compensate the large inductor voltage due to the switch-delay control.

D. Component Demands Comparison

This section compares the component demands of the two testing methods. In this section, design parameters with subscript "1" are for the original uncompensated testing method, while those with subscript "2" are for the proposed compensated method. For the original method, both (12) and (13) can be also applied. The maximum inductor voltage $V_{L\max 1}$ can be found in Fig. 6(b) which equals the dc supply voltage V_{dc1}. The minimum inductor voltage $V_{L\min 1}$ (absolute value) would be the dc supply voltage minus the peak SM capacitor voltage. Based on the above analysis, $V_{L\max 1}$ and $V_{L\min 1}$ can be written as

$$V_{L\max 1} = V_{\mathrm{dc1}} \quad (17a)$$

$$V_{L\min 1} = V_{\mathrm{dc1}} - V_{\mathrm{SMCmax}} = V_{\mathrm{dc1}} - \left(1 + \frac{1}{2}k_{\mathrm{SMCac}}\right) \times V_{\mathrm{SMCdc}}. \quad (17b)$$

Substituting (17a) and (17b) into (12) and (13) gives

$$\omega L_1 A + \left(1 + \frac{1}{2}k_{\mathrm{SMCac}}\right) V_{\mathrm{SMCdc}} < V_{\mathrm{dc1}} \leq \frac{2k_{\Delta I_{\max}} A f_{s1} L_1}{2 + \left\lfloor \frac{f_{s1}}{2 f_{\mathrm{sw\_max}}} \right\rfloor} - \omega L_1 A. \quad (18)$$

Also, the minimum required inductance can be derived as

$$L_1 > \frac{\left(1 + \frac{1}{2}k_{\mathrm{SMCac}}\right)}{\frac{2k_{\Delta I_{\max}} f_{s1}}{2 + \left\lfloor \frac{f_{s1}}{2 f_{\mathrm{sw\_max}}} \right\rfloor} - 2\omega} \frac{V_{\mathrm{SMCdc}}}{A}. \quad (19)$$

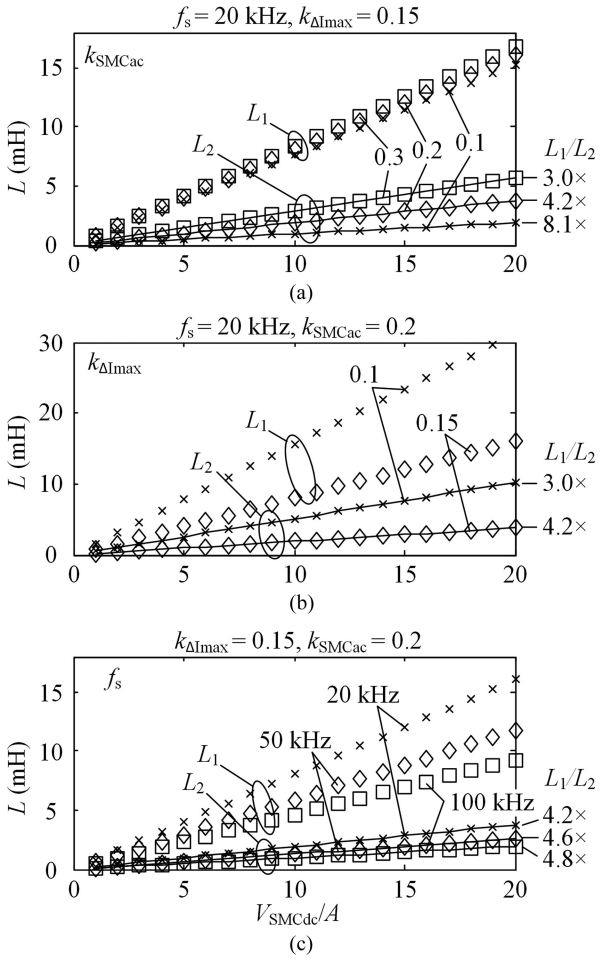

Fig. 8. Comparison of the coupling inductance demand between the two testing methods with different (a) SM capacitor voltage ripple k_{SMCac}, (b) current tracking accuracy $k_{\Delta I_{\max}}$, and (c) sampling frequency f_s.

The dc supply voltage and coupling inductor demand functions of the original method as in (18) and (19) have the same structure as the demand functions for the proposed method as in (15) and (16). In the following, the component demands of the two testing methods to test the same SM will be compared using the above equations. As the entire "arm current" would pass through the coupling inductor and the full-bridge in both testing methods, the current testing capability of two methods are assumed equal. Hence, only the required coupling inductance and the dc supply voltage of the full-bridge are compared.

Fig. 8 shows a group of comparisons of the required inductance between the two testing methods. The marked curves without a central line stand for the original method while the ones with a central line are for the proposed method. In all cases, the original method requires much larger inductance than the proposed one and both would increase with increasing (V_{SMCdc}/A), which is the ratio between the SM rated voltage and the peak amplitude of the fundamental component in the "arm current." Note that this applies only when the harmonic circulating currents are small and can be neglected. Otherwise, the parameter A shall include not only the fundamental component but also other major harmonic components.

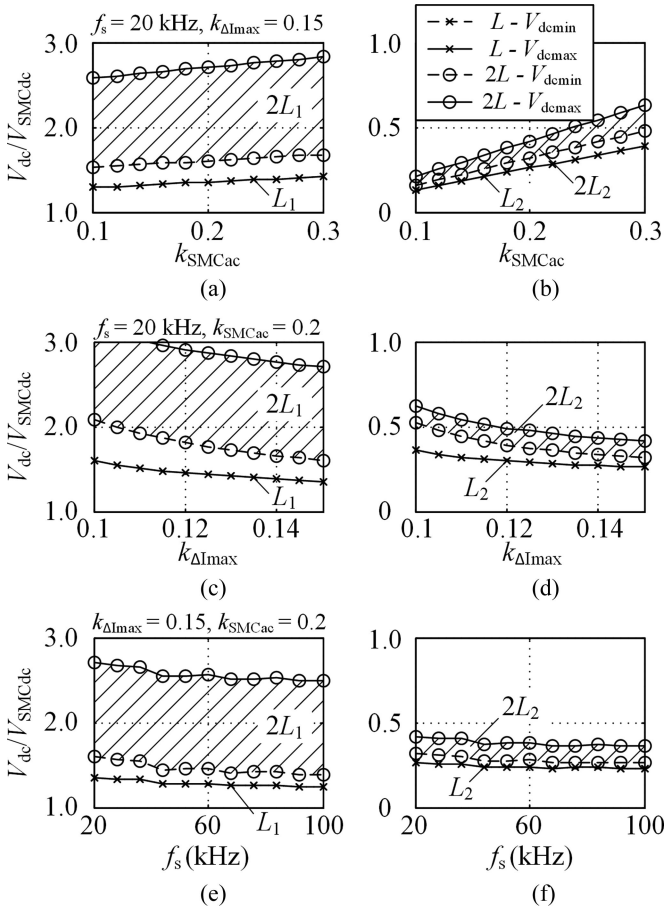

Fig. 9. Comparison of the dc supply voltage demand between the two testing methods with different (a) and (b) SM capacitor voltage ripple k_{SMCac}, (c) and (d) current tracking error $k_{\Delta I_{\mathrm{max}}}$, and (e) and (f) sampling frequency f_s.

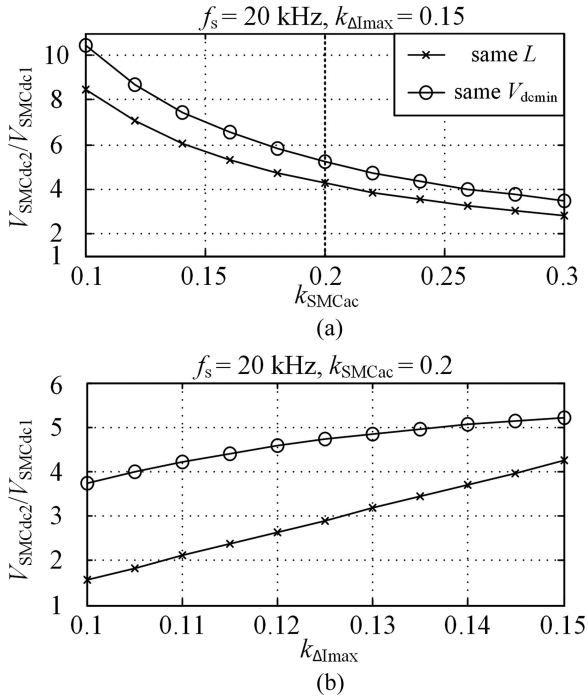

Fig. 10. Testing capability comparison between the two testing methods with different (a) SM capacitor voltage ripple k_{SMCac} and (b) current tracking error $k_{\Delta I_{\mathrm{max}}}$.

More specifically, Fig. 8(a) illustrates how the inductance demand would vary with different SM capacitor voltage ripple k_{SMCac}. In the proposed method, the capacitor voltage ripple of the auxiliary SM is set equal to that of the prototype. As the voltage ripple contributes to a major part of the inductor voltage, the inductance demand is more sensitive to k_{SMCac} in the proposed method. Larger k_{SMCac} calls for larger *L*. As a comparison, for the original method, as the entire SM capacitor voltage will be added to the coupling inductor when being switched in, the impacts of k_{SMCac} on its inductance demand is not as significant. Hence, as calculated on the right side of Fig. 8(a), the proposed method could offer larger inductance reduction when the voltage ripple is small. As shown in Fig. 8(b), for both methods, larger *L* is needed if higher current tracking accuracy (or smaller $k_{\Delta I_{\mathrm{max}}}$) is required in order to reduce the current step in each sampling period. Another way to reduce the current step is by increasing the sampling frequency f_s as in Fig. 8(c). For both methods, when f_s is increased, smaller *L* is required to test SMs with the same conditions (k_{SMCac} and $k_{\Delta I_{\mathrm{max}}} A$). Note the maximum switching frequency of the full-bridge is always limited at 6 kHz.

Fig. 9 compares the dc supply voltage demand between the two methods. The vertical axis is the ratio between the required V_{dc} and the rated voltage of the SM to be tested. The horizontal axis stands for different testing configurations, including k_{SMCac}, $k_{\Delta I_{\mathrm{max}}}$, and f_s. The figures on the left [Fig. 9(a), (c), and (e)] show the supply voltage demand of the original method and the figures on the right [Fig. 9(b), (d), and (f)] show the supply voltage demand for the proposed method with identical configurations. In all figures, the curves with "x" symbols represent the required V_{dc} derived when *L* equals the minimum value given by (16) or (19). The curves with "o" symbols represent the case when *L* equals twice the minimum value. In addition, the dashed curves are for the minimum V_{dc} and the solid curves are for the maximum V_{dc}, as in (15) or (18).

As shown in Fig. 9, in all considered cases, the required supply voltage of the proposed method is always lower than the SM rated voltage V_{SMCdc}, while the required V_{dc} of the original method is always higher than V_{SMCdc}. More specifically, as shown in Fig. 9(a) and (b), the required V_{dc} of the proposed method is more sensitive to the voltage ripple, k_{SMCac}, as larger voltage ripple calls for higher full-bridge output voltage for the hysteresis control. In addition, as in Fig. 9(c) and (d), higher current tracking accuracy calls for slightly higher supply voltage for both testing methods as larger coupling inductance is used to achieve the goal. As shown in Fig. 9(e) and (f), faster sampling would help to reduce the demand of V_{dc} for both methods. Again, the maximum switching frequency of the full-bridge is always limited to 6 kHz.

E. Testing Capability Comparison

Figs. 8 and 9 compare the component demands between the two testing methods when the same SM is to be tested, showing that the proposed method requires much less coupling inductance and dc supply voltage for the same test conditions. Fig. 10

TABLE IV
COMPLETE MMC SYSTEM MODEL PARAMETERS FOR SIMULATION

Item	Value
dc-link voltage	40 kV (pole-to-pole)
Grid voltage	23 kV line-to-line (rms), 50 Hz
Rated modulation index	$m = 0.9$
Rated output line current	500-A rms
Rated capacity	19.1 MW (PF = 1)
Transformer inductance	0.1 p.u.
Number of SMs	20 per arm
Arm inductance	0.2 p.u.
IGBT/diode module	Infineon FZ1000R33HE3
V_{SMCdc}	2000 V
Prototype SM C	2.7 mF
Auxiliary SM C	2.7 mF
k_{SMCac}	0.15
A	353.5 A

further compares the testing capability of the two methods when the same test equipment is used, i.e., the same dc supply and coupling inductor. The current carrying capability, the sampling frequency, and the maximum switching frequency are also assumed the same. As shown in the figure, the vertical axis $V_{\mathrm{SMCdc2}}/V_{\mathrm{SMCdc1}}$ is the ratio between the maximum SM rated voltage that can be tested using the proposed method and the original. V_{SMCdc1} is derived when $k_{\mathrm{SMCac}} = 0.2$ and $k_{\Delta I_{\max}} = 0.15$. There are two ways to calculate V_{SMCdc2}. One is by assuming the same coupling inductance as in the original. The results are shown by curves with "x" symbols. The other is by assuming the same supply voltage (lower voltage boundary) as in the original. The results are shown by the curves with "o" symbols. The lower value derived by the two methods is the actual maximum V_{SMCdc2}. Both Fig. 10(a) and (b) shows that the proposed method has a much higher voltage testing capability. Besides the higher voltage capability, as shown in Fig. 10(b), the proposed method is able to offer higher current tracking accuracy with the same test platform. In both cases, the coupling inductor is the major factor that limits the testing capability improvement of the proposed method. By slightly increasing the coupling inductance, the testing capability of the same platform can be further improved.

IV. DESIGN EXAMPLE AND SIMULATION VERIFICATION

A. Design Example

This section shows a design example of a test platform using the proposed method to test SMs for a hypothetic grid-connected MMC. As a comparison, the testing capability of the example platform is evaluated when using the original method.

A hypothetic 21-level 19.1-MW grid-connected MMC with half-bridge SMs is modeled in MATLAB/Simulink. System parameters are summarized in Table IV. The converter is connected to a $\pm$20-kV dc-link and a 23-kV (line-to-line rms) 50-Hz ac-grid bus-bar through a three-phase transformer. The arm inductor is 0.2 p.u. All p.u. values are based on ac-side voltage and current. There are 20 SMs in each arm with 2000-V SM rated dc voltage, V_{SMCdc}. The SM capacitance is designed to be 2.7 mF [4] to give a 15% peak-to-peak (of V_{SMCdc}) voltage ripple at the rated power. The modulation and voltage balanceing control adopt the one proposed in [1]. No third-order harmonic voltage injection is used. The harmonic circulating current is assumed eliminated. The arm current can be estimated by [16]

$$i_{\mathrm{arm}}(t) = \frac{\sqrt{2}I_s}{4} m\cos\varphi + \frac{\sqrt{2}I_s}{2}\sin(\omega t - \varphi) \qquad (20)$$

where I_s is the rms value of the rated line current, m is the modulation index, and the φ is the ac-side power factor angle. In this design example, $I_s = 500\mathrm{A}$, $m = 0.9$, and $\varphi = p$. Hence, the design parameter A, which is the peak amplitude of the fundamental component in the arm current, can be derived to be 353.5 A.

Equations (15) and (16) are used to find the required supply voltage and coupling inductance for the test platform to run the SM testing with the proposed method. Sampling frequency f_s of the test platform is assumed to be 20 kHz and the maximum switching frequency $f_{\mathrm{sw\_max}}$ of the power module in the full-bridge converter is set at 6 kHz. The current error constant $k_{\Delta I_{\max}}$ is set at 0.1 and the permitted current tracking error $\pm\Delta I_{\max}$ can be derived to be $\pm$35.4 A according to (8). The peak arm current would be 513 A according to (20). The permitted current tracking error is less than 7% of that.

The auxiliary SM is assumed to be the same as the prototype (with the same capacitance) that k_{auxCac} equals k_{SMCac}. The minimum required coupling inductance can be derived by (16) to be 2.2 mH. With this minimum inductance, both the maximum and minimum supply voltage equals 545 V according to (15). When the auxiliary SM switch-delay control is active, the maximum inductor voltage in such a case equals the difference between one peak SM voltage and V_{dc}, which is 1605 V (= 2150–545 V). $dI_{\mathrm{error\_delay}}$ can be derived using (9) to be 42 A. Then, the current threshold $I_{\mathrm{thres}-}$ equals $-6.6\mathrm{A}$ using (7a) and $I_{\mathrm{thres}+}$ equals $+6.6$ A using (7b). As both current thresholds are within the permitted band $\pm$35.4 A, even when the switch-delay control is applied, the current tracking accuracy is guaranteed. In normal cases when the switch-delay is not active, $dI_{\mathrm{error\_max}}$ can be derived to be 23.5 A using (9) and the hysteresis band is set to $\pm$11.8 A using (10). All design parameters for the test platform using the proposed method are concluded in the second column in Table V.

For comparison, the testing capability of the test platform using the original method is derived as follows. First, as the current testing capability is limited by the current carrying capability of the power module in the full-bridge and the coupling inductor, the output current of the hypothetic system is assumed unchanged. Other design variables, f_s, $f_{\mathrm{sw\_max}}$, k_{SMCac}, and $k_{\Delta I_{\max}}$ are kept the same as well. One way to derive the maximum SM rated voltage V_{SMCdc1} that can be tested using the original method is to ensure that the supply voltage $V_{\mathrm{dc}} = 545\mathrm{V}$ is not exceeded. According to (18), the following expression must be satisfied:

$$\frac{2k_{\Delta I_{\max}} A f_{s1} L_1}{2 + \left\lfloor \frac{f_{s1}}{2f_{\mathrm{sw\_max}}} \right\rfloor} - \omega L_1 A \le V_{\mathrm{dc2}} = 545. \qquad (21)$$

Equation (21) gives the maximum coupling inductance ($L_1 = 1.51\mathrm{mH}$) for the original method, which is less than the required

TABLE V
TEST BENCH MODEL PARAMETERS FOR SIMULATION

Item	Value	
	Proposed method	Original method
$V_{\mathrm{SMCdc}}(V_{\mathrm{auxCdc}})$	2000 V (2000 V)	350 V (–)
$k_{\mathrm{SMCac}}(k_{\mathrm{auxCac}})$	0.15 (0.15)	0.15 (–)
A	353.5 A	353.5 A
$k_{\Delta I\,\mathrm{max}}$	0.1	0.1
f_s	20 kHz	20 kHz
$f_{\mathrm{sw\_max}}$	6 kHz	6 kHz
V_{dc}	545 V	545 V
L	2.2 mH	1.51 mH
$V_{L\,\mathrm{max}}$	790 V	545 V
$V_{L\,\mathrm{min}}$	245 V	169 V
ΔI_{max}	±35.4 A	±35.4 A
H_{band}	±11.8 A	±11.8 A
$dI_{\mathrm{error\_max}}$	23.5 A	23.5 A
$dI_{\mathrm{error\_delay}}$	42 A	–

inductance for the proposed method. In practice, the different inductance settings can be achieved by certain configurations, such as tap-changing mechanisms. Substituting $L_1 = 1.51\mathrm{mH}$ into (18) gives V_{SMCdc1} to be 350 V, which is only 17.5% of the voltage that can be tested with the proposed method. The rest design parameters of the platform using the original method are derived and listed in the third column in Table V. The hypothetic MMC model is scaled down to ±7 kV dc, 3.34 MW with the rated line current kept at 500 A in order to derive the reference signals for the 350-V rated SM. In steady state, when the two converters operate at their rated power, signals with a duration of one second for both the arm current and switching sequence of one SM in each system are recorded and used to run the two test benches, respectively.

B. Simulation Results

Fig. 11 shows the simulation results of the test platform testing a 2000-V rated SM using the proposed method. Fig. 11(a) shows the system startup with both the prototype SM (red solid line in the middle) and auxiliary SM (green-dashed line) capacitor voltages ramping up according to a reference from 0 to 2000 V using the voltage controllers proposed in Section II-C. During the charging process, positive injection current will be added to the "arm current" reference to increase the prototype SM capacitor voltage. As this current would have opposite effects on the auxiliary SM capacitor, the ramping speed of v_{auxC} is slower than v_{SMC}. Hence, during system startup, longer switch-delay period is set for the auxiliary SM capacitor voltage control, which equals 100 μs. After the time averages of both v_{SMC} and v_{auxC} reach the set reference (2000 V), the test platform switches to the steady-state control according to Table I to III. In steady state, detailed SM capacitor voltages can be found in Fig. 11(b). The figure shows that the prototype SM capacitor voltage achieved in the test platform (solid red) agrees well with its reference from the complete model simulation (solid blue). The dashed green line is the auxiliary SM capacitor voltage that has an identical shape as the prototype but opposite polarity. Its average voltage is well controlled at the 2000-V reference using

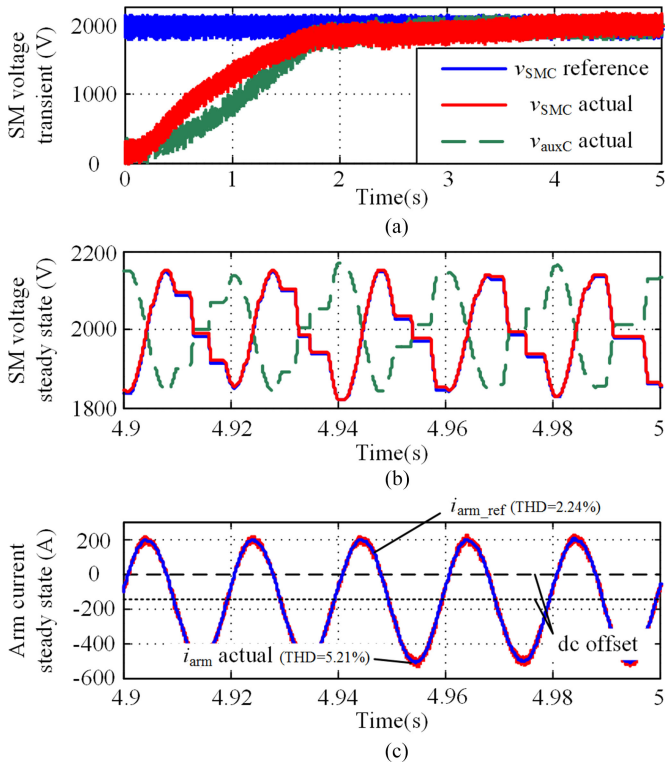

Fig. 11. Simulation results of the test platform using the proposed method: (a) SM capacitor voltages, (b) SM capacitor voltages in steady state, and (c) arm current in steady state.

the switch-delay control. Fig. 11(c) shows that the actual "arm current" generated by the hysteresis switching (red in the back) tightly tracks its reference (blue in the front). Total harmonic distortion (THD) of the reference is 2.24% while that of the actual "arm current" is 5.21%. The additional harmonics are introduced by the hysteresis switching.

Fig. 12(a) shows the injected current to control the prototype SM capacitor voltage. During the system startup, large current is added to the "arm current" reference to increase v_{SMC}. When the system reaches steady state, the injected current drops down to less than 0.2 A to compensate the small voltage difference caused by current errors. Fig. 12(b) shows the current tracking error during both system startup and steady state. During the system startup, the switch-delay period is set to 100 μs and the delay control is applied whenever v_{auxCdc} is outside the permitted range for fast response, leading to very large current tracking error. When the system turns to the steady-state control at 2.3 s, the current error immediately drops into the permitted range [−35.4, +35.4 A]. Fig. 12(c) shows a zoomed view of the current error. Even when the switch delay is applied, the current error is always within the permitted region.

As shown in Table V, with the same test platform, the original method is only able to test SMs with rated voltage up to 350 V. Fig. 13 compares the current tracking error between simulations using the proposed and the original methods. The SM rated voltage in the simulation of the original method is set to 350 V. Both the "arm current" and current tracking accuracy are set the same as in the simulation of the proposed method. As

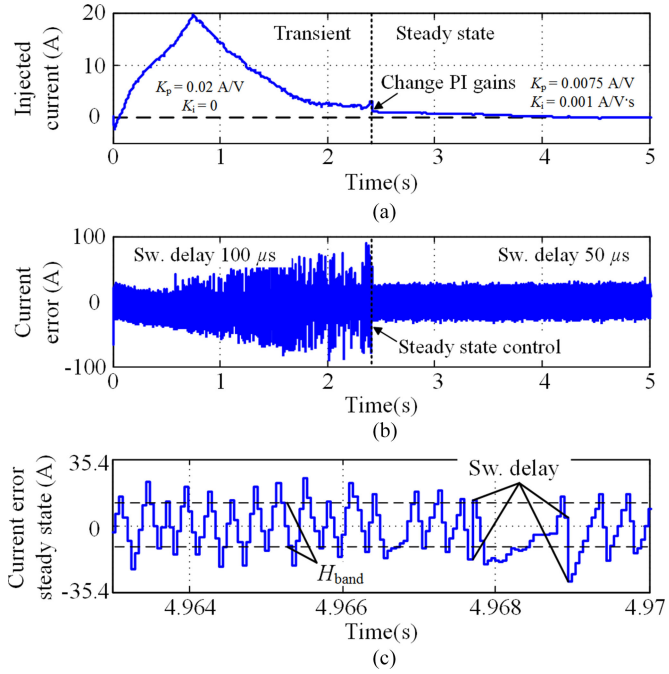

Fig. 12. Simulation results of the test platform using the proposed method: (a) injected current, (b) current error, and (c) current error in steady state.

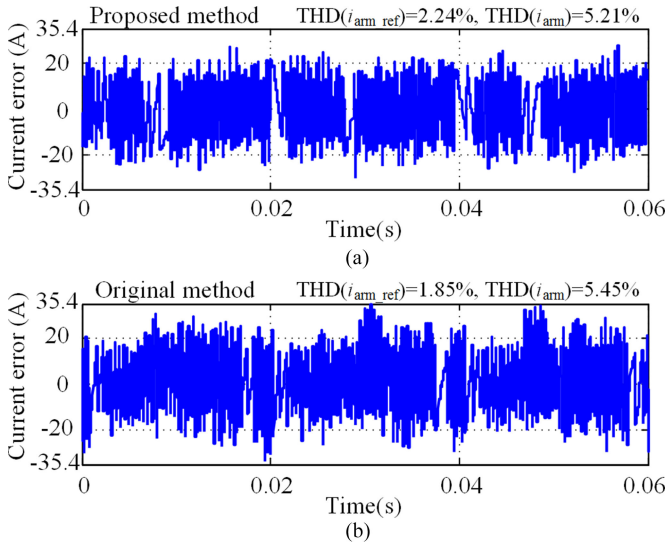

Fig. 13. Current error comparison between the proposed and the original testing method.

shown by the figure, the current errors in Fig. 13(a) are smaller than those in Fig. 13(b). Similar results can be found in the harmonic analysis of the current. THD of $i_{\rm arm}$ generated by the proposed method is 5.21% while the THD of its reference $i_{\rm arm\_ref}$ is 2.24%. As a comparison, THD of $i_{\rm arm}$ generated by the original method is 5.45%, while the THD of its reference $i_{\rm arm\_ref}$ is only 1.85%. In other words, even with the same current tracking accuracy setting, the proposed method gives better current tracking performance.

The reason can be explained by Fig. 14. The vertical axis is the actual inductor voltage divided by the maximum inductor voltage $V_{L\max1}$ or $V_{L\max2}$ for normalization. As shown in

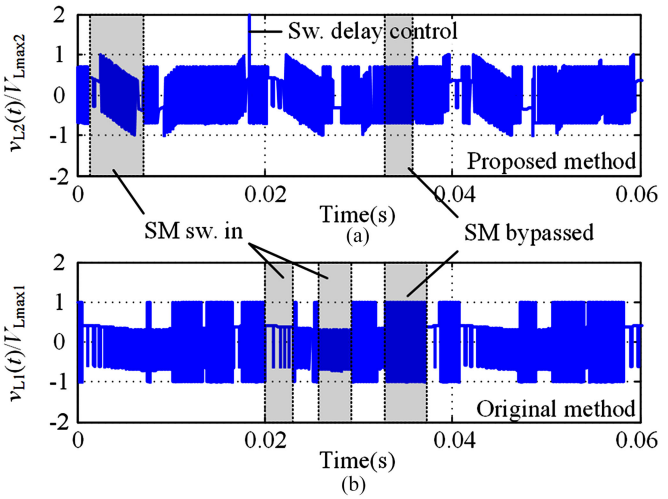

Fig. 14. Inductor voltage comparison between the proposed and the original testing method.

TABLE VI
DESIGN PARAMETERS FOR EXPERIMENT

Item	Value	
	Proposed	Original [10]
$V_{\rm SMCdc}$ ($V_{\rm auxCdc}$)	400 V (400 V)	200 V (–)
$k_{\rm SMCac}$ ($k_{\rm auxCac}$)	0.15 (0.075)	0.25 (–)
A	9.8 A	8 A
$k_{\Delta I\max}$	0.15	0.14
f_s	20 kHz	20 kHz
$f_{\rm sw\_max}$	6 kHz	6 kHz
$V_{\rm dc}$	100 V	240 V
L	10 mH	20 mH
$V_{L\max}$	155 V	240 V
$V_{L\min}$	55 V	15 V
$\Delta I_{\max}$	±1.4 A	±1.1 A
$H_{\rm band}$	±0.47 A	±0.37 A
$dI_{\rm error\_max}$	0.93 A	0.73 A
$dI_{\rm error\_delay}$	1.81 A	–

Fig. 14(a), when the proposed method is used, the maximum inductor voltage is only met when both SMs are switched into the circuit and their voltage ripples are at the maximum. During the rest of the time, $v_{L2}(t)$ is always less than $V_{L\max2}$, leading to smaller current step, and, hence, smaller current error. Although the switch-delay control will lead to very large inductor voltage and large current step, the control only applies in limited situations as in Table II in steady state, leading to negligible impacts. As a comparison, as shown in Fig. 14(b), when the original method is used, the maximum inductor voltage is met each time when the SM is bypassed. Hence, for around half of the time (SM bypass period, depending on the converter system control), $v_{L1}(t)$ equals $V_{L\max1}$ and the current step would be equal to the maximum, leading to larger current errors.

V. EXPERIMENT VERIFICATION

Computer simulations have been used to compare the difference between the two testing methods, showing that the proposed method is able to provide much higher voltage testing capability and better current tracking accuracy than the original

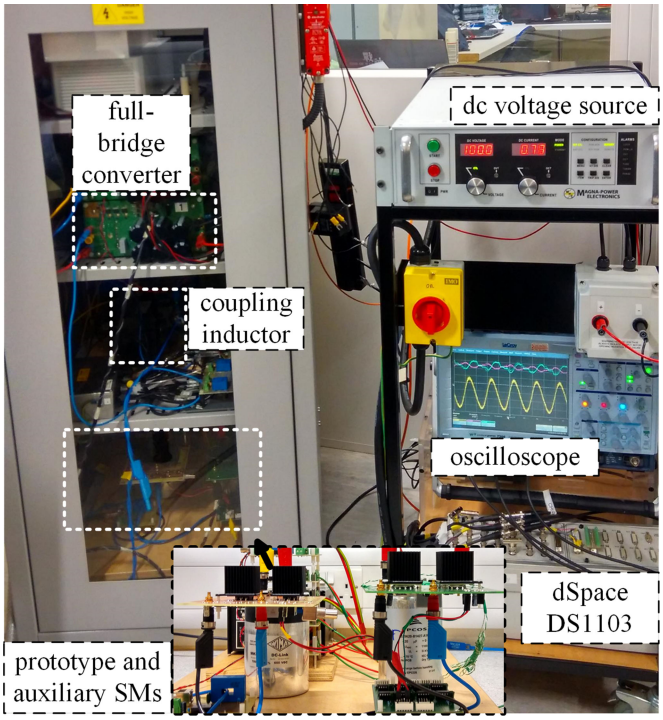

Fig. 15. Compensated SM test bench installed in a protected enclosure.

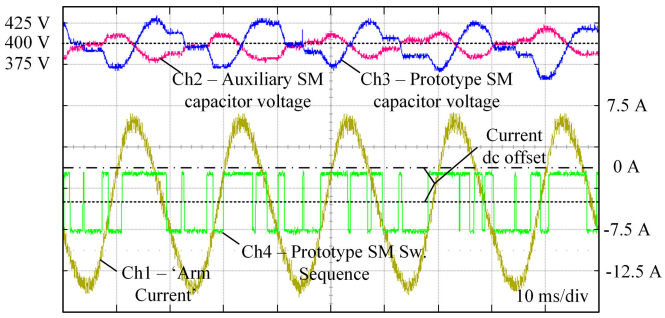

Fig. 16. Experiment results recorded by the oscilloscope. Horizontal axis: 10 ms/div. Ch1—"arm current": 5 A/div, −0.5 div offset (yellow). Ch2—auxiliary SM capacitor voltage: 50 V/div, −5.5 div offset (red). Ch3—prototype SM capacitor voltage: 50 V/div, −5.5 div offset (blue). Ch4—prototype SM switching sequence (green).

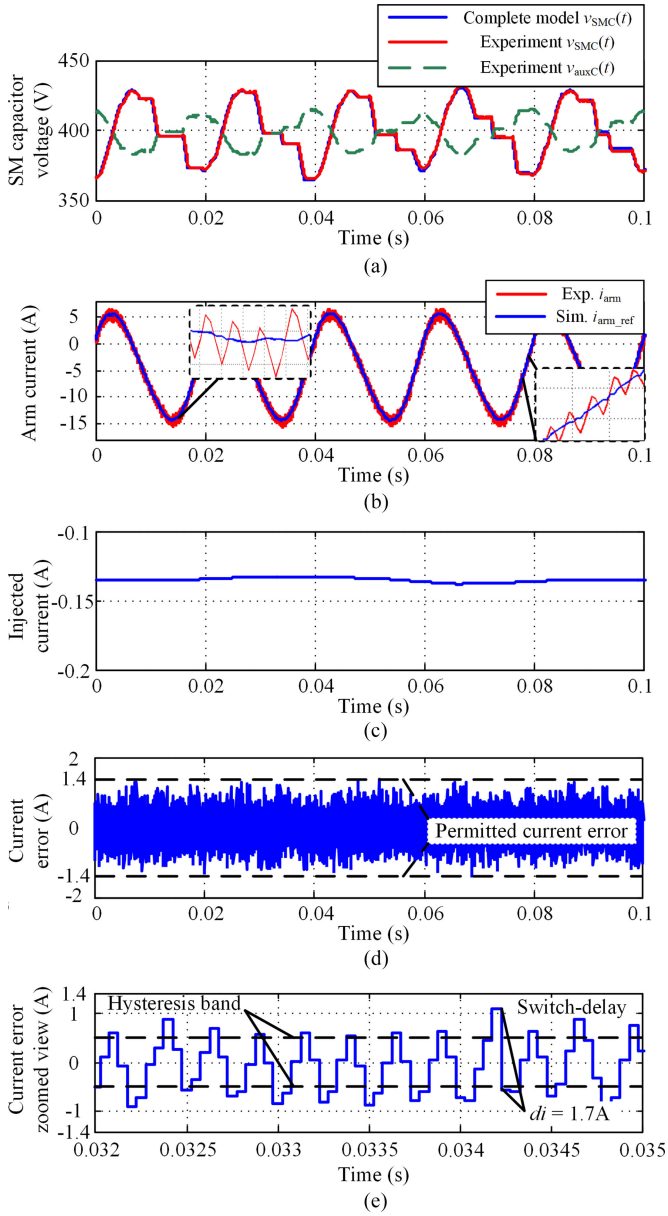

Fig. 17. Comparison between the experiment results and the complete model simulation: (a) SM capacitor voltages; (b) "arm current"; (c) injected current; (d) current error; and (e) zoomed view of the current error.

method using the same test platform. This section focuses on the experimental verification of the proposed method. The hypothetic MMC system in the simulation is scaled down to ±4 kV dc 106 kVA for experiment. The rated ac line current reduces to 14-A rms and the SM rated voltage V_{SMCdc} drops down to 400 V. With 373-μF SM capacitance, the voltage ripple is around 15% peak-to-peak of V_{SMCdc}. In order to run the experiment, computer simulations of the scaled-down system helped to record the reference "arm current" and the switching sequence of the SM to be tested. All design parameters for the test platform are concluded in the second column in Table VI. Note that the actual inductance is chosen to be twice of the minimum value given by (16) ($L_{\min} = 5$ mH) in order to limit the large current error introduced by the auxiliary SM switch-delay control. As shown in Table VI, parameters of the prototype system are compared with the experimental test bench given in [10] using the original method. It also shows that the proposed method is able to test SMs with double the rated voltage using less than half the supply voltage, while the rest conditions such as current tracking accuracy are kept similar.

Fig. 15 shows the prototype platform assembled and installed in a protection enclosure for the validation of the proposed testing scheme. Fig. 16 shows an oscilloscope snapshot of the experimental results. From top to bottom are the waveforms for the SM capacitor voltages (larger ripple—prototype and smaller ripple—auxiliary), the actual "arm current" and the prototype SM switching sequence. Time average voltages of the two SM capacitors are controlled to be around the reference 400 V owing to the two independent voltage controllers described in Section II-C. With the same switching frequency and due to the reversed

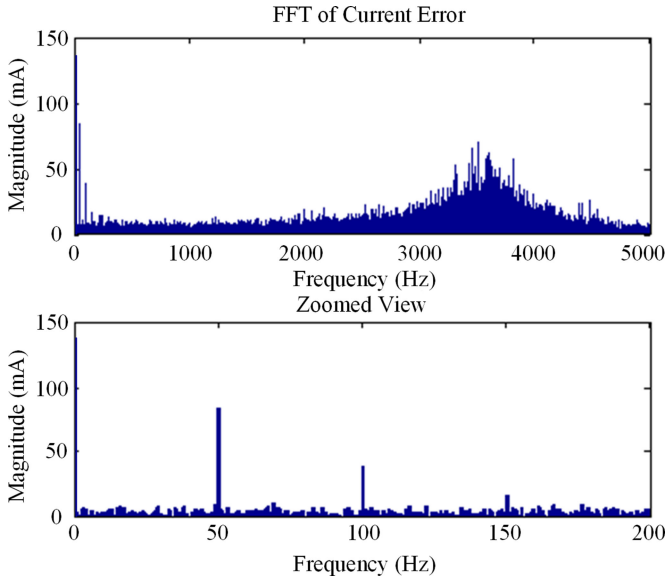

Fig. 18. Top: FFT of the current error; bottom: zoomed view.

series-connection configuration, the two capacitor voltage ripples have a similar shape but opposite polarities. The voltage ripple of the auxiliary SM is smaller than that of the prototype due to the larger capacitance used. The "arm current" with a dc offset is faithfully achieved using the hysteresis switching, which is not affected by the switching of the two SMs.

In order to show the performance of the test platform, Fig. 17 compares the experimental results to the complete model simulation. Fig. 17(b) shows that the current flowing into the prototype SM tightly tracks the given reference from the computer simulation. The two zoomed views give the details of the actual "arm current" achieved by the hysteresis switching. Owing to the excellent current tracking performance as well as accurate switching of the prototype SM, its capacitor voltage in the experiment also tightly tracks the reference given by the complete model simulation as in Fig. 17(a). As both the voltage and current of the prototype SM perfectly agree with the simulation results of a complete system, the other output characteristics of the SM, including electrothermal, electromechanical, and electromagnetic characteristics would be representative of the SM installed in a complete MMC. Fig. 17(c) shows the actual injected current by the prototype SM capacitor voltage regulator. As in the steady state, K_{i} ($= 0.01$ A/V$\dot{\mathrm{c}}$s) is set large with very small K_{p} ($= 0.002$ A/V) to filter out high-frequency noises, the injected current is nearly dc with a magnitude around -130 mA, which is less than 1% of the peak "arm current." Current tracking errors are shown in Fig. 17(d) and (e). In all cases, the current errors are controlled to be within the allowable ± 1.4 A region. As shown in the zoomed view in Fig. 17(e), when the switch delay is not active, the current error steps are always less than the designed 0.93 A. When the switch-delay is being used, the current error step is measured to be 1.7 A. Owing to the control method described in Table II, the current error in such a case is still kept in the allowable region.

Fig. 18 gives the fast Fourier transform (FFT) analysis of the current error. The high-order harmonics mainly distribute around 3.7 kHz due to the hysteresis switching. As shown in the zoomed view, the error at dc can be explained by the injected current that is around -130 mA in the experiment. The error at the fundamental frequency 50 Hz is around 80 mA. The current error at 100 Hz is for the harmonic circulating current component in the "arm current." The amplitudes of the above errors are small when compared with the peak "arm current." If those errors are not acceptable in certain applications, methods, such as narrower permitted current error band, faster sampling frequency, and/or variable hysteresis band could be adopted.

VI. Conclusion

A compensated model-assisted SM testing scheme for the MMC is proposed in this paper. This testing scheme uses an auxiliary SM to compensate the dc component in the prototype SM output voltage aiming at increasing the testing capability of the original testing method. As a result, the required coupling inductance and dc supply voltage can be largely reduced when compared with the original method to test the same SM. In addition, with the same test platform, the proposed method is able to offer more than five times of voltage testing capability with even better current tracking accuracy. The proposed testing method can be easily applied to the test platform designed for the original method with only one additional SM, which can be the same as the prototype. A new switch-delay controller is proposed to independently control the auxiliary SM capacitor voltage. The energizing and discharging of both prototype and auxiliary SM capacitors can be achieved without additional auxiliary circuits. Both simulations and experiments have shown the validity and performance of the proposed testing method.

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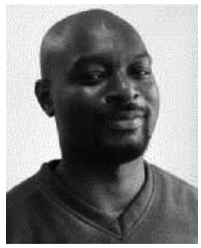

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