A Variable Duty Cycle Soft Startup Strategy for *LLC* Series Resonant Converter Based on Optimal Current-Limiting Curve

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***Abstract*—For the *LLC* series resonant converter (*LLC*-SRC), the resonant current inrush during the startup is a threat to the safe operation of the main switches, and frequency-decreasing startup method is usually adopted. The very high initial start-up frequency can suppress this inrush effectively, but increases the output current demand of drive ICs. In this paper, a variable duty cycle soft startup strategy based on optimal current-limiting curve is presented, which can realize the suppression of the resonant current inrush under low startup frequency. Due to the nonlinearity of the *LLC*-SRC, the mode transition conditions are illustrated and a generalized numerical model of the *LLC*-SRC is established, providing a highly accurate prediction on resonant variables and output during the startup process. Based on the numerical model, the relationship between the startup current, initial startup frequency, and the duty cycle is revealed to quantify the startup process and achieve optimal initial startup parameters. A numerical algorithm is presented to obtain the optimal current-limiting curve during the startup. Two variable duty cycle startup methods are applied to verify the effectiveness of the proposed strategy, namely the PWM startup method and the phase-shift startup method. The experimental results are presented to verify the proposed soft startup strategy.**

***Index Terms*—Current-limiting curve, *LLC* resonant converter, numerical model, soft startup, variable duty cycle.**

NOMENCLATURE

C_1–C_4	Parallel capacitors of the main switches.
C_e	Equivalent capacitor.
C_o	Output capacitor.
C_r	Resonant capacitor.
C_s	Equivalent series capacitor.
D	Duty cycle.
D_0	Initial startup duty cycle.
$D_{\rm begin}$	Start duty cycle of calculation.
$D_{\rm end}$	End duty cycle of calculation.
ΔD	Duty cycle increment.
f_0	Initial startup frequency.
$f_{\rm begin}$	Start frequency of calculation.
$f_{\rm end}$	End frequency of calculation.
f_n	Normalized switching frequency.
$f_{\rm min}$	Minimal switching frequency.
f_s	Switching frequency.
f_r	Natural resonant frequency.
Δf	Frequency increment.
i_d	Output current of the uncontrolled rectifiers.
$i_{\rm lim}$	Limiting value of the resonant current.
i_r	Resonant inductor current.
i_{r0}	Initial value of i_r.
i_{rn}	Normalized form of i_r.
$i_{rn\max}$	Maximum value of i_{rn}.
i_{rp}	Peak value of i_r.
i_m	Magnetic inductor current.
i_{mn}	Normalized form of i_m.
$i_{rp\rm nom}$	Peak value of i_r under nominal load.
$i_{rp\rm shorted}$	Peak value of i_r under shorted load.
I_N	Current reference value.
j	Step counter.
L_e	Equivalent inductor.
L_m	Magnetic inductor.
L_r	Resonant inductor.
L_s	Equivalent series inductor.
M_n	Mode n.
M_{n+1}	Mode $n+1$.
n_T	Transformer ratio.
N_c	Total calculation steps in one switching period.
$N_{\rm sim}$	Total number of switching period.
p	Period counter.
R_o	Output resistor.
$R_{\rm nom}$	Rated output resistor.
$S_{\rm in}$	Input port state of resonant tank.
$S_{\rm out}$	Output port state of resonant tank.
v_{ce}	Voltage of equivalent capacitor C_e.
v_{ce0}	Initial value of v_{ce}.
v_r	Resonant capacitor voltage.
v_{rn}	Normalized form of v_r.
v_m	Voltage of L_m.
v_{mn}	Normalized form of v_m.
v_{sn}	Normalized form of V_s.
$v_{\rm on}$	Normalized form of V_o.
$\Delta v_{\rm sum}$	Summation of $\Delta v_{\rm on}$.
V_N	Voltage reference value.
V_e	Equivalent voltage.
$V_{\rm in}$	Input voltage.
V_o	Output voltage.

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V_{o0}	Initial value of V_o.
V_{onom}	Rated output voltage.
V_s	Voltage between midpoint of two bridge legs.
ΔV_o	Output voltage increment.
ω_0	Natural resonant angular frequency (L_rC_r).
ω_1	First resonant angular frequency (L_sC_r).
ω_2	Second resonant angular frequency (L_rC_s).
ω_3	Third resonant angular frequency (L_sC_s).
ω_e	Equivalent resonant angular frequency (L_eC_e).
$\boldsymbol{X}$	State vector.
$\boldsymbol{X}_{\rm n}$	State vector n.
$\boldsymbol{X}_{\rm n+1}$	State vector $n+1$.
Z_0	Natural resonant impendence.
Z_1	First resonant impendence.
Z_2	Second resonant impendence.
Z_3	Third resonant impendence.
Z_e	Equivalent resonant impendence.
ε	Convergent boundary.

I. Introduction

THE *LLC* series resonant converter shown in Fig. 1 attracts more and more attention due to the advantages of high efficiency, high operation frequency, and low electromagnetic interference [1]–[6]. As shown in Fig. 2, the *LLC* series resonant converter (*LLC*-SRC) normally operates at the resonant point to ensure zero-voltage switching (ZVS) for the primary switches and obtain the best efficiency. Above the resonant point (AR), the normalized voltage gain is less than 1 and the *LLC*-SRC can still realize ZVS [7]. In some cases, the *LLC*-SRC also operates below the resonant point (BR) to boost the voltage gain [8], [9]. In the BR region, however, only under some restricted conditions can the ZVS be realized.

Usually, the *LLC*-SRC starts up from the AR region and decreases the frequency to the resonant point gradually [10]–[15], which is called the frequency-decreasing startup method. If the startup frequency is not high enough, a very large startup inrush will happen in the resonant tank, as shown in Fig. 3. Therefore, the startup frequency has to be much higher than the resonant point to suppress this startup inrush sufficiently. However, the output current demand of drive ICs will increase obviously as well.

So far, a few literatures have focused on the startup problems of the *LLC*-SRC. A kind of startup method proposed in [16] needs two steps. At the starting stage, the full-bridge *LLC* converter works at half-bridge mode, i.e., T3 in Fig. 1 is forced OFF and T4 is forced ON. Once the output voltage is charged up, the *LLC* turns to full-bridge mode. However, the experimental results show that there is still a large current inrush at the startup instant, and the startup frequency is very high as well. Optimal trajectory control in [17] can guarantee that there will be no current and voltage stress in the resonant tank during the startup process. However, it is difficult to implement for the low-performance DSPs. A soft starting strategy based on the phase-shift control is proposed in [18]. During the startup process, the *LLC*-SRC operates in the phase-shift control mode. The phase-shift angle changes from 0 to π. Another analogous

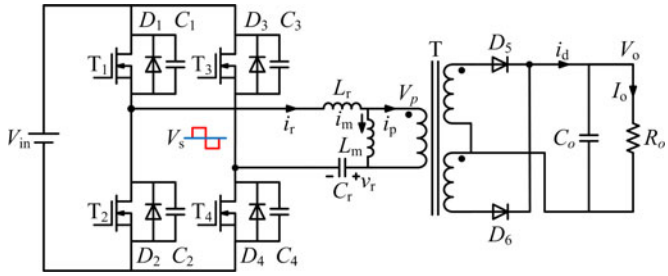

Fig. 1. Topology of the *LLC*-SRC.

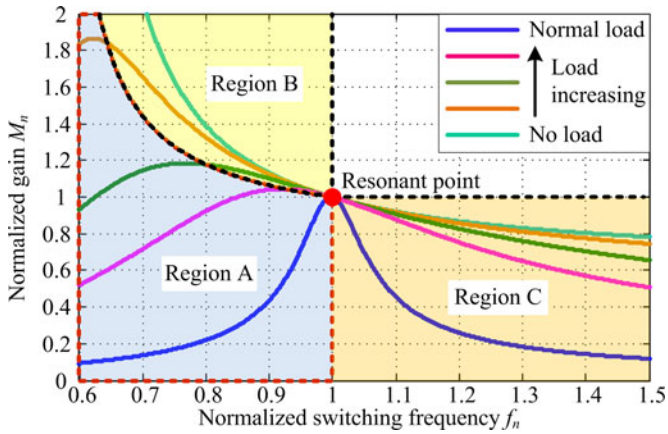

Fig. 2. Voltage gain of the *LLC*-SRC.

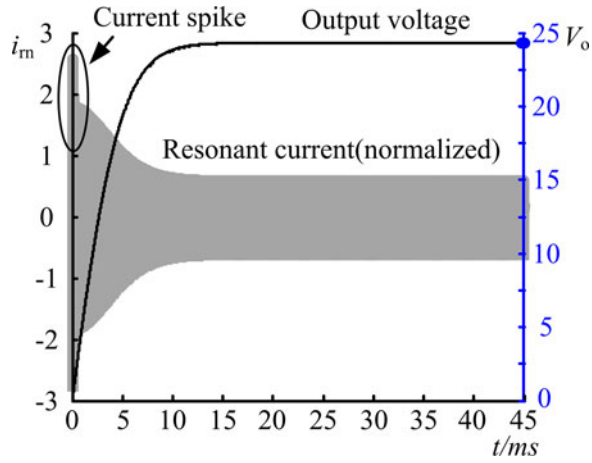

Fig. 3. Resonant current and output voltage waveform with the frequency-decreasing start-up method.

strategy proposed in [19] applies PWM control to the *LLC*-SRC to realize current limiting in overload or short-circuit condition. However, Chen *et al.* [18] and Yang *et al.* [19] only provide qualitative analysis.

It is hard to analyze the startup process due to the nonlinearity of the *LLC*-SRC. In this paper, a generalized numerical model of the *LLC*-SRC is established, providing highly accurate prediction on the resonant variables and output during the startup process. Base on this model, a variable duty cycle soft startup strategy based on optimal current-limiting curve is presented, which can realize suppression of the startup current inrush with low startup frequency.

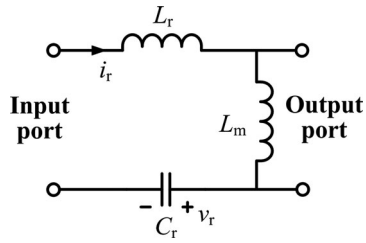

Fig. 4. Resonant tank of the *LLC*-SRC.

This paper is organized as follows: Mode decomposition of the *LLC*-SRC is introduced in Section II. The numerical model of the *LLC*-SRC during startup process is established in Section III. In Section IV, the relationship between startup current, initial startup frequency, and the duty cycle is analyzed. The optimization of startup process is described in Section V. The experimental results are presented in Section VI.

II. Mode Decomposition of the *LLC*-SRC

Some variables that will be used hereafter are defined as follows:

$$\begin{cases} V_N = V_{\text{in}}, & I_N = V_{\text{in}}/Z_0 \\ L_s = L_r + L_m, & C_s = C_1 C_r/(C_1 + C_r) \\ Z_0 = \sqrt{L_r/C_r}, & \omega_0 = 1/\sqrt{L_r C_r} \\ Z_1 = \sqrt{L_s/C_r}, & \omega_1 = 1/\sqrt{L_s C_r} \\ Z_2 = \sqrt{L_r/C_s}, & \omega_2 = 1/\sqrt{L_r C_s} \\ Z_3 = \sqrt{L_s/C_s}, & \omega_3 = 1/\sqrt{L_s C_s}. \end{cases} \tag{1}$$

To generalize the analysis, some variables may be used in normalized form, marking with subscript *n*, which are defined as

$$\begin{cases} v_n = v/V_N \\ i_n = i \cdot I_N. \end{cases} \tag{2}$$

The resonant tank of the *LLC*-SRC consists of an input port, three resonant components, and an output port, as shown in Fig. 4. The input and output states vary with the status of the main switches and the output rectifier diodes, respectively, leading to the multiple modes in the resonant tank.

Considering the dead time, there are four states of the input port, which are defined as follows:

1) State *P*: This state will appear when T_1 and T_4 are ON or D_1 and D_4 are conductive. In state *P*, V_s is equal to the supply voltage $+V_{\text{in}}$, as shown in Fig. 5(a).
2) State O_1: This state exists during the dead time, as all the switches and parallel diodes are OFF. In state O_1, the parallel capacitors C_1–C_4 are participating in the resonant tank, as shown in Fig. 5(b).
3) State O_2: This state will appear when T_1 and T_3 or T_2 and T_4 are ON. The input port is shorted in state O_2, as shown in Fig. 5(c).
4) State *N*: This state will appear when T_2 and T_3 are ON or D_2 and D_4 are conductive. The voltage V_s is equal to the reversed supply voltage $-V_{\text{in}}$, as shown in Fig. 5(d).

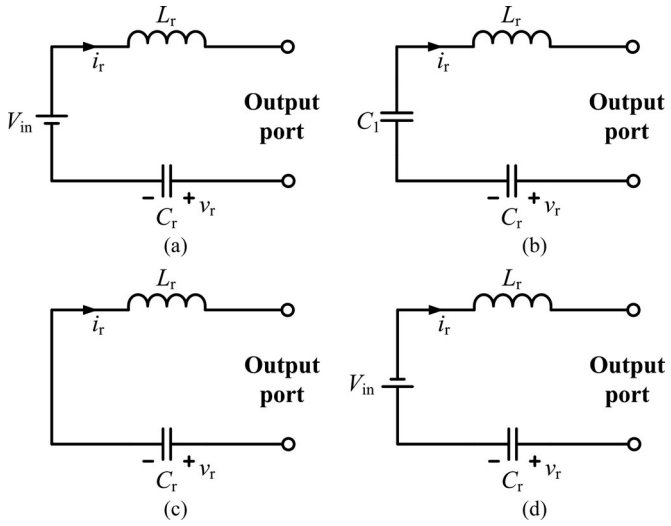

Fig. 5. States of input port. (a) State *P*, (b) state O_1; (c) state O_2; (d) state *N*.

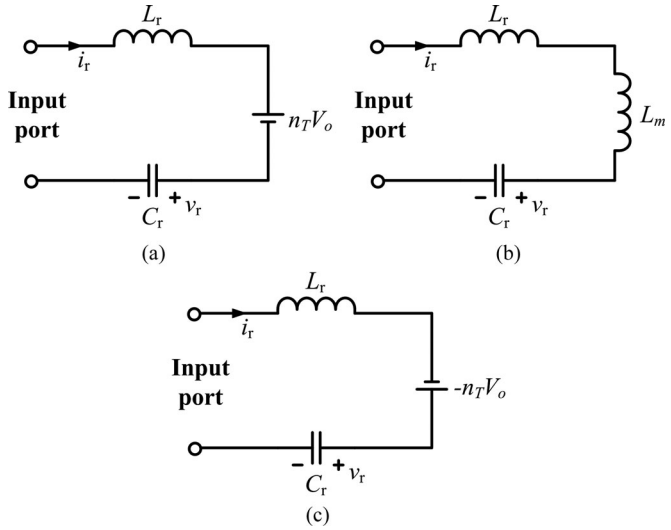

Fig. 6. States of output port. (a) State *P*; (b) state *O*; (c) state *N*.

For the output port, the states are defined as follows:

1) State *P*: the output rectifier diode D_5 is ON and the magnetic inductor L_m is clamped by the output voltage $+n_T V_o$, as shown in Fig. 6(a);
2) State *O*: the output rectifier diodes D_5 and D_6 are all OFF. The magnetic inductor L_m is participating in the resonant tank, as shown in Fig. 6(b);
3) State *N*: the output rectifier diode D_6 is ON and the magnetic inductor L_m is clamped by the reversed output voltage $-n_T V_o$, as shown in Fig. 6(c).

As a combination of the input states and the output states, the resonant tank can be decomposed into 12 modes, namely *PP*, *PO*, *PN*, O_1P, O_1O, O_1N, O_2P, O_2O, O_2N, *NP*, *NO,* and *NN* mode.

For each mode, the resonant tank can be simplified to a linear circuit shown in Fig. 7, consisting of an equivalent voltage source V_e, an equivalent inductor L_e, and a capacitor C_e.

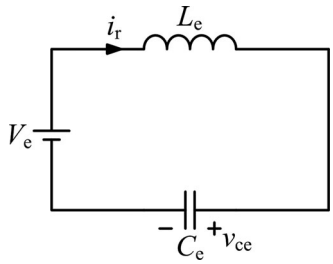

Fig. 7. Equivalent circuit of the resonant tank in each mode.

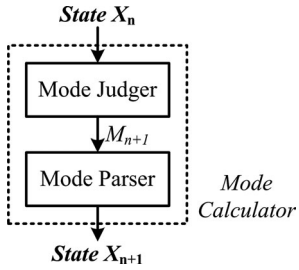

Fig. 8. Numerical model of the resonant tank.

The resonant variables can be solved analytically

$$\begin{cases} v_{ce} = i_{r0} Z_e \sin(\omega_e t) + (v_{ce0} - V_e)\cos(\omega_e t) + V_e \\ i_r = i_{r0}\cos(\omega_e t) + (v_{ce0} - V_e)\sin(\omega_e t)/Z_e \end{cases} \tag{3}$$

where v_{ce} is the voltage of equivalent capacitor C_e, v_{ce0} is the initial voltage of equivalent capacitor C_e, i_{r0} is the initial current of equivalent inductor L_e, and Z_e is the equivalent impedance, which is defined as $\sqrt{L_e/C_e}$.

According to the input port states, the modes of resonant tank can be classified into four groups.

A. PP, PO, and PN Modes

In these cases, the resonant current flows through the switch T_1 and T_4 or D_1 and D_4. The equivalent voltage source V_e, equivalent inductor L_e, and capacitor C_e are

$$\begin{cases} PP: V_e = V_{\text{in}} - n_T V_o,\ L_e = L_r,\ C_e = C_r,\ Z_e = Z_0, \\ \qquad \omega_e = \omega_0 \\ PO: V_e = V_{\text{in}},\ L_e = L_s,\ C_e = C_r,\ Z_e = Z_1,\ \omega_e = \omega_1 \\ PN: V_e = V_{\text{in}} + n_T V_o,\ L_e = L_r,\ C_e = C_r,\ Z_e = Z_0, \\ \qquad \omega_e = \omega_0. \end{cases} \tag{4}$$

B. O_1P, O_1O, and O_1N Modes

When all the switches and corresponding parallel diodes are OFF, the resonant current flows through the parallel capacitors C_1–C_4, leading to O_1P, O_1O, and O_1N modes. As C_1–C_4 are considered equal, the input port can be regarded as C_1. Then, the equivalent voltage source V_e, equivalent inductor L_e, and capacitor C_e are

$$\begin{cases} O_1P: V_e = -n_T V_o,\ L_e = L_r,\ C_e = C_s,\ Z_e = Z_2,\ \omega_e = \omega_2 \\ O_1O: V_e = 0,\ L_e = L_s,\ C_e = C_s,\ Z_e = Z_3,\ \omega_e = \omega_3 \\ O_1N: V_e = n_T V_o,\ L_e = L_r,\ C_e = C_s,\ Z_e = Z_2,\ \omega_e = \omega_2. \end{cases} \tag{5}$$

C. NP, NO, and NN Modes

In *NP*, *NO*, and *NN* modes, the resonant current flows through the switch T_2 and T_3 or D_2 and D_3. The equivalent voltage source V_e, equivalent inductor L_e, and capacitor C_e are

$$\begin{cases} NP: V_e = -V_{\text{in}} - n_T V_o,\ L_e = L_r,\ C_e = C_r,\ Z_e = Z_0,\ \omega_e = \omega_0 \\ NO: V_e = -V_{\text{in}},\ L_e = L_s,\ C_e = C_r,\ Z_e = Z_1,\ \omega_e = \omega_1 \\ NN: V_e = -V_{\text{in}} + n_T V_o,\ L_e = L_r,\ C_e = C_r,\ Z_e = Z_0,\ \omega_e = \omega_0. \end{cases} \tag{6}$$

D. O_2P, O_2O, and O_2N Modes

In O_2P, O_2O, and O_2N modes, the resonant current flows through T_1 and T_3 or T_2 and T_4. The input port is shorted. These modes appear in the phase-shift control mode. The equivalent voltage source V_e, equivalent inductor L_e, and capacitor C_e in these modes are

$$\begin{cases} O_2P: V_e = -n_T V_o,\ L_e = L_r,\ C_e = C_r,\ Z_e = Z_0,\ \omega_e = \omega_0 \\ O_2O: V_e = 0,\ L_e = L_s,\ C_e = C_r,\ Z_e = Z_1,\ \omega_e = \omega_1 \\ O_2N: V_e = n_T V_o,\ L_e = L_r,\ C_e = C_r,\ Z_e = Z_0,\ \omega_e = \omega_0. \end{cases} \tag{7}$$

III. Numerical Model of the *LLC*-SRC During Startup Process

In Section II, the resonant tank is decomposed into 12 linear modes and the corresponding analytical solutions are derived. In fact, more than two modes will appear in one switching period. As mentioned in [20], the mode combination in a switching period varies with switching frequency and load. Therefore, the closed form of the resonant variables is unable to derive. However, if the transition conditions from one mode to another are known, the resonant variables can be described by the numerical method, namely the numerical model of the startup process.

As the dynamic of output stage is far slower than the resonant tank, the numerical model can be divided into two parts: the resonant tank and the output stage.

A. Numerical Model of the Resonant Tank

The numerical model of resonant tank is shown in Fig. 8, which is called mode calculator, containing two parts inside. $\boldsymbol{X}$ is state vector, which is defined as follows:

$$X = [v_{rn}\ i_{rn}\ v_{mn}\ i_{mn}\ v_{sn}\ v_{\text{on}}] \tag{8}$$

where v_{mn} is the normalized voltage of L_m.

Mode judger consists of the transition conditions that decide the next mode M_{n+1} based on $\boldsymbol{X}_{\text{n}}$. Actually, the mode of resonant tank is decided by the input port state S_{in} and the output port state S_{out}.

During the duty cycle in one switching period, S_{in} is decided by the status of switches, which can be described as below:

$$\begin{cases} S_{\text{in}} = 1, & T_1, T_4 \text{ ON} \\ S_{\text{in}} = 0, & T_1, T_3 \text{ or } T_2, T_4 \text{ ON} \\ S_{\text{in}} = -1, & T_2, T_3 \text{ ON}. \end{cases} \tag{9}$$

During the dead time, T_1–T_4 are all OFF and $S_{\rm in}$ is decided by the status of parallel diodes D_1–D_4. Compared with the input voltage $V_{\rm in}$, the forward voltage of diode can be ignored. Therefore, $S_{\rm in}$ during the dead time is described as follows:

$$\begin{cases} S_{\rm in} = 1, & V_s \geq V_{\rm in} \text{ and } i_{rn} < 0 \\ S_{\rm in} = -2, & -V_{\rm in} < V_s < V_{\rm in} \\ S_{\rm in} = -1, & V_s \leq -V_{\rm in} \text{ and } i_r > 0. \end{cases} \tag{10}$$

As for $S_{\rm out}$, it can be judged by the status of output diodes D_5 and D_6. When $i_r > i_m$, D_5 turns ON and v_m is clamped by $n_T V_o$. When $i_r < i_m$, D_6 turns ON and v_m is clamped by $-n_T V_o$. When $i_r = i_m$, D_5 and D_6 are all OFF if $|v_m| < n_T V_o$. Then, the transition of $S_{\rm out}$ can be expressed as

$$\begin{cases} S_{\rm out} = 1, & i_r > i_m \\ S_{\rm out} = 0, & i_r = i_m \text{ and } |v_m| < n_T V_o \\ S_{\rm out} = -1, & i_r < i_m. \end{cases} \tag{11}$$

With (9)–(11), the transition conditions of $S_{\rm in}$ and $S_{\rm out}$ during one switching period are illustrated. Then, mode M_{n+1} is expressed as

$$M_{n+1} = -3S_{\rm in} - S_{\rm out} + 5. \tag{12}$$

For example, assuming $S_{\rm in} = 1$ and $S_{\rm out} = 1$ at the present calculation step, so $M_n = 1$ according to (12), namely *PP* mode. Then, all the state variables in the state vector $\boldsymbol{X}_{\rm n}$ can be solved by the mode parser in Fig. 8 with (3) and (4). In the next calculation step, the status of switches and the state vector $\boldsymbol{X}_{\rm n}$ will be the inputs of the mode judger. The mode judger consists of all rules in (9)–(11), which can figure out the next $S_{\rm in}$ and $S_{\rm out}$ and the next mode M_{n+1}. According to M_{n+1}, $\boldsymbol{X}_{\rm n\ +1}$ is derived by the corresponding solutions analyzed in Section II.

B. Numerical Model of the Output Stage

The expression of output stage can be written as

$$C_o \frac{dV_o}{dt} + \frac{V_o}{R_o} = i_d \tag{13}$$

where i_d is output current of the uncontrolled rectifier, $i_d = n_T|i_r - i_m|$. R_o is the output resistance, and C_o is the output capacitance.

$S_{\rm out}$ can be used as the sign of i_d. Regarding V_o as a constant during one switching cycle, the integration of (13) can be written as

$$C_o \Delta V_o + \frac{V_o}{R_o}\Delta t = n_T S_{\rm out} \int_{t_0}^{t_1} (i_r - i_m)dt = n_T S_{\rm out} \cdot K. \tag{14}$$

During the time when $S_{\rm out}$ is 1 or -1, the positive part of exciting current i_m is symmetric with the negative part. As a result, the integration of i_m is zero. When $S_{\rm out}$ is zero, the right side of (14) is always zero. Therefore, (14) can be regarded as the uniform expression of output voltage. Combined with the relationship between v_r and i_r, K can be written as

$$K = C_r \Delta v_r. \tag{15}$$

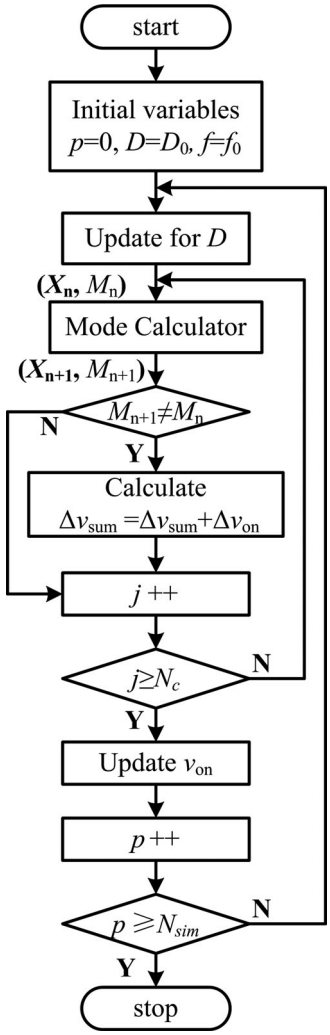

Fig. 9. Numerical model of the *LLC*-SRC during the startup process.

By substituting (15) into (14), the normalized form of output increment $\Delta v_{\rm on}$ is

$$\Delta v_{\rm on} = \frac{nS_{\rm out}C_r\Delta v_{rn}}{C_o} - \frac{v_{\rm on}}{R_o C_o}\Delta t_{M_n} \tag{16}$$

where Δt_{Mn} is the duration of mode M_n.

C. Numerical Model of the LLC-SRC During Startup Process

Based on the results of Sections A and B, the numerical model of the *LLC*-SRC can be established. Before startup, all the variables are initialized. For the frequency-decreasing method, switching frequency is initialized to f_0, as shown in Fig. 9.

In Fig. 9, the switching period is quantized to N_c, which is the total calculation step in one switching period. *j* is a step counter. During one period, the mode calculator figures out ($\boldsymbol{X}_{\rm n\ +1}$, M_{n+1}) according to ($\boldsymbol{X}_{\rm n}$, M_n). The output increment $\Delta v_{\rm on}$ is calculated and accumulated into $\Delta v_{\rm sum}$ when mode M_n ends. If the calculation in one switching period is over, the output voltage $v_{\rm on}$ is updated and period counter *p* is added by 1. When *p* reaches to $N_{\rm sim}$, the calculation is over.

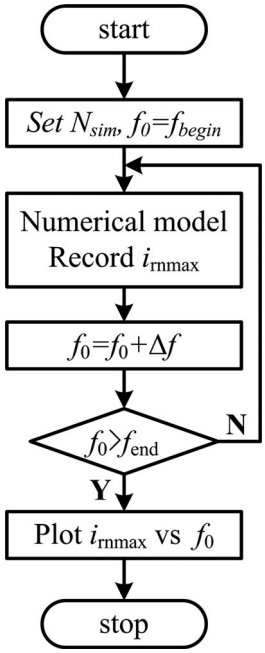

Fig. 10. Iterative algorithm of the relationship between the startup current and startup frequency.

IV. Relationship Between Startup Current, Initial Startup Frequency, and Duty Cycle

The startup current inrush is related to the startup frequency and duty cycle. For now, the literatures have only carried the qualitative description of this relationship. For the frequency-decreasing method, the startup frequency is designed with a large margin to ensure the limitation of the startup current. However, the very high startup frequency increases the output current demand for drive ICs.

To pick up an appropriate initial frequency and duty cycle, the relationship between the startup current, initial frequency, and duty cycle should be revealed.

A. Relationship Between Startup Current and Startup Frequency With 50% Duty Cycle

For the frequency-decreasing method, the duty cycle is maintained at 50%. To figure out the relationship between startup current and startup frequency, an iterative algorithm is adopted based on the numerical model, as shown in Fig. 10.

As the current inrush usually happens within the dozens of switching periods, $N_{\rm sim}$ in Fig. 10 can be set to a small value. The maximum resonant current with startup frequency f_0 can be easily obtained by implanting bubble sort in the numerical model. Setting $f_{\rm begin} = f_r$ and $f_{\rm end} = 8f_r$, the curves with three different output parameters are presented in Fig. 11, which are duplicated with each other, indicating that the maximum resonant current is not affected by the output parameters. This is reasonable because the output voltage is almost zero at the beginning.

As shown in Fig. 11, with the startup frequency increasing, the current inrush decreases, but the effect is increasingly weak.

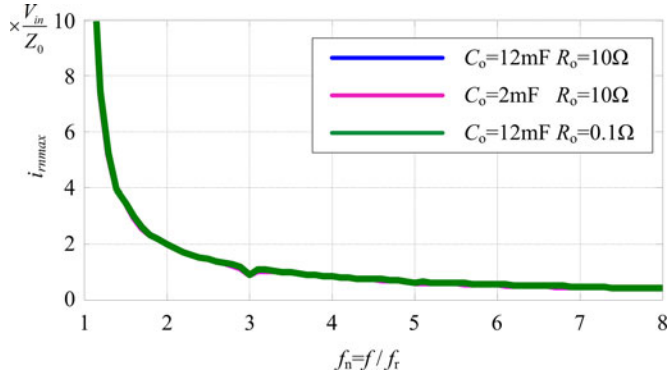

Fig. 11. Relationship between startup current and initial frequency with different output filter parameters.

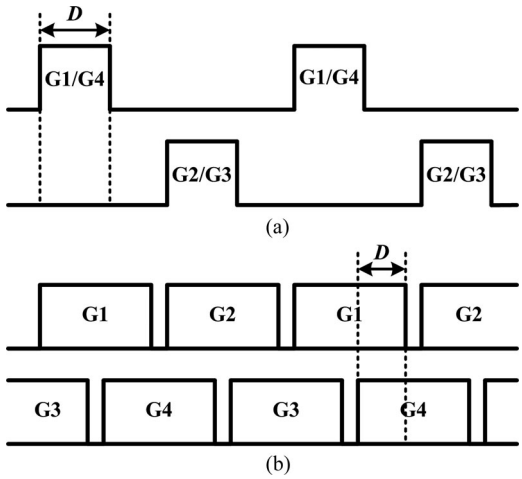

Fig. 12. Two schemes to realize the duty cycle increasing startup strategy. (a) PWM startup method; (b) phase-shift startup method.

In the area where $f_n > 3$, the maximum resonant current hardly varies with startup frequency.

If the maximum resonant current is set, the lowest startup frequency can be determined by the iterative algorithm.

B. Relationship Between Startup Current and Duty Cycle at Resonant Frequency

The frequency-decreasing method requires a very high initial frequency to suppress the current inrush, which increases the output current demand for drive ICs. Another startup method is applied to reduce the startup frequency by increasing the duty cycle gradually from an appropriate initial value. During the startup process, the frequency is maintained at resonant frequency. To realize this strategy, two schemes can be used, which are shown in Fig. 12.

The G1–G4 are the drive signals of T_1–T_4, respectively. In Fig. 12(a), G1 is the same with G4 and G2 is the same with G3. During the startup process, the duty cycle of G1 and G2 increases symmetrically, and is called PWM startup method. In Fig. 12(b), the duty cycle of G1–G4 is almost 50%, ignoring the dead time. G1 is complementary to G2 and G3 is complementary

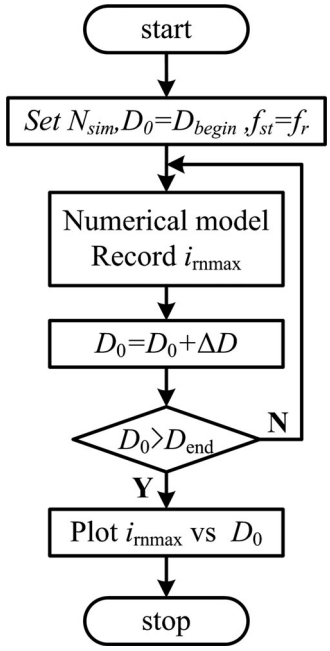

Fig. 13. Iterative algorithm of the relationship between startup current and initial duty cycle.

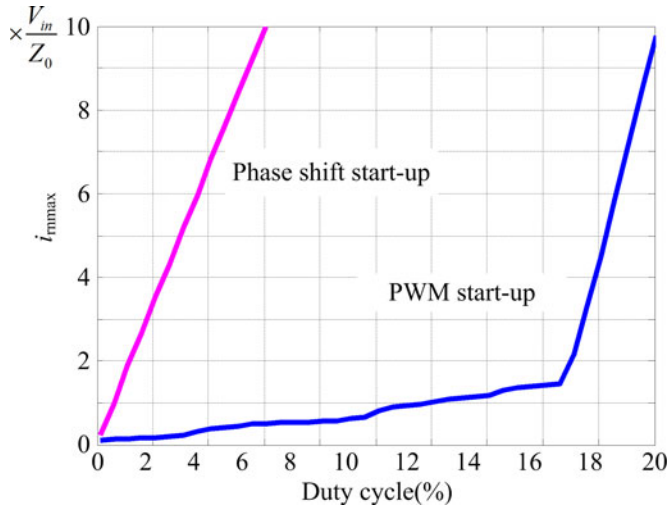

Fig. 14. Relationship between startup current and initial duty cycle with PWM startup method and phase-shift startup method.

to G4. During the startup process, the overlapping part of G1 and G4 increases gradually, which is called phase-shift startup method.

To determine the initial duty cycle, the iteration algorithm is also adopted, as shown in Fig. 13. Setting $D_{\rm begin} = 0$ and $D_{\rm end} = 25\%$, the curve of the maximum resonant current with different initial duty cycle is plotted in Fig. 14.

As shown in Fig. 14, both the PWM startup method and the phase-shift startup method can suppress the startup inrush with apposite initial duty cycle. The current inrush can be suppressed effectively when D_0<17% with the PWM startup method. However, as for the phase-shift startup method, the initial duty cycle should be very small to suppress the startup inrush. This discrepancy is due to the different modes in the two startup methods. For the PWM startup method, the input port state can be *P* state, *N,* and O_2 except O_1 state, but for the phase-shift startup method, the input port states are *P* state, *N,* and O_1 except O_2 state.

V. Optimization of Startup Process

The PWM startup method and phase-shift startup method can eliminate current inrush effectively at the beginning of startup process, and the startup frequency is the resonant frequency. Meanwhile, the curve of duty cycle during the startup process will also impact the current inrush. If the duty cycle increases very fast, current inrush will appear. If the duty cycle increases very slowly, the response speed of output voltage cannot be guaranteed. Therefore, the startup process with PWM startup method and phase-shift startup method should be optimized to achieve the soft startup with low current stress and fast response of the output voltage.

As analyzed in Section II, the resonant tank can be regarded as a two-port network. With the switching frequency f_s, duty cycle *D,* and output voltage V_o known, the steady state of the resonant tank can be determined uniquely. Therefore, the peak value of the resonant current can be described as

$$i_{rp} = f(f_s, D, V_o). \tag{17}$$

As for the PWM startup method and phase-shift startup method, f_s is equal to the resonant frequency. During the startup process, the peak value of the resonant current is limited to a certain value $i_{\rm lim}$. As a result, (17) can be written as

$$D = f(V_o)|_{f_s = f_r, i_{rp} = i_{\rm lim}}. \tag{18}$$

Equation (18) shows that the relationship between the duty cycle *D* and the output voltage V_o under the limited value $i_{\rm lim}$ can be expressed as a 2-D curve, which is called the current-limiting curve.

For the *LLC*-SRC, the dynamic of resonant tank is very fast, while the dynamic of output voltage is quite slow. During one control period, the output voltage can be considered as a constant voltage source V_o. Before the next control period, the resonant tank already reaches the steady state. During the startup process, the resonant current can be limited to the value $i_{\rm lim}$ by controlling the duty cycle according to the limiting curve.

To obtain the current-limiting curve, a numerical algorithm is applied, as shown in Fig. 15. Set the current limit value $i_{\rm lim}$ and the initial value (V_{o0}, D_0). After the numerical model calculation, the peak value i_{rp} of the resonant current is obtained. If the absolute value of error $(i_{rp} - i_{\rm lim})$ is larger than value ε, keep searching duty cycle *D* according to the polarity of error $(i_{rp} - i_{\rm lim})$. Once the convergence condition is satisfied, save the point (V_o, *D*). Increase the output value from V_{o0} to rated value $V_{o\rm nom}$, and find out the corresponding duty cycle *D*. Finally, the current-limiting curve under the limiting value $i_{\rm lim}$ is obtained.

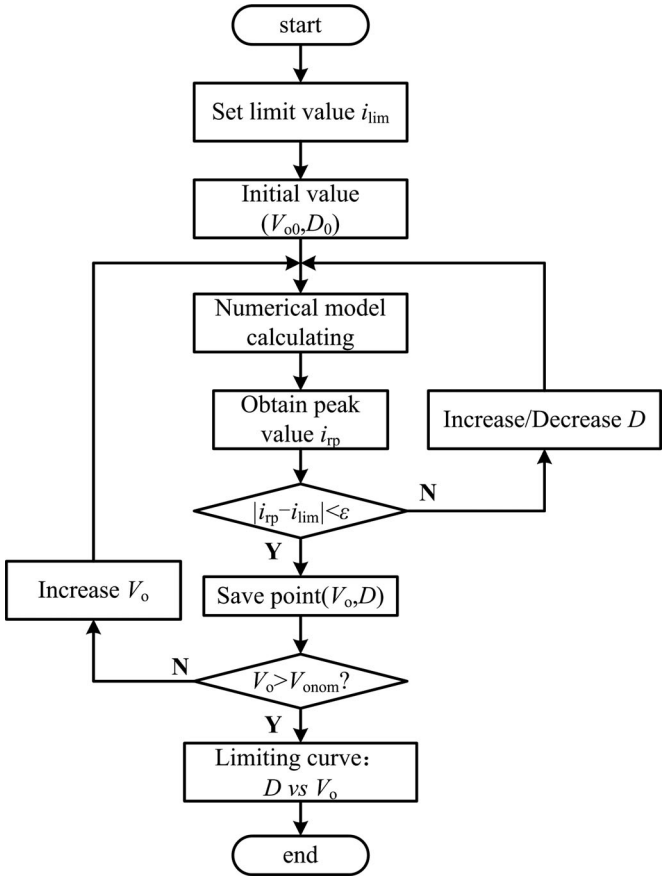

Fig. 15. Numerical algorithm of current-limiting curve.

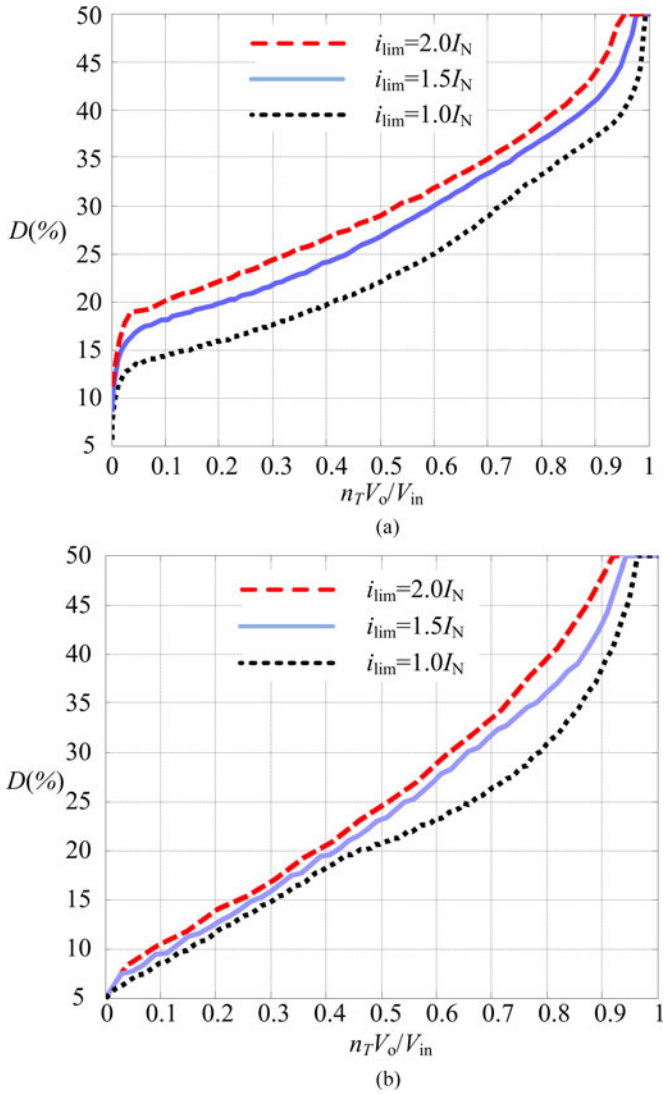

Fig. 16. Current-limiting curves under different limiting value. (a) PWM startup method; (b) phase-shift startup method.

For the PWM startup method and the phase-shift startup method, Fig. 16 shows three current-limiting curves under the limiting value $1.0I_N$, $1.5I_N$, and $2.0I_N$. In practice, we can set a reasonable limiting value according to circuit parameters and find out the corresponding current-limiting curve. Disperse the curve into 1024 points and make a table. Then, solidify the table into the MCU. During the startup process, the duty cycle D is chosen according to the output voltage V_o by lookup table method.

VI. Experimental Results

To verify the analysis, a 250-W prototype is developed. The parameters are shown in Table I.

The resonant frequency of the prototype is 112.5 kHz and the based current I_N is 3.96 A. Fig. 17 shows the calculated and experimental results of startup process with the frequency-decreasing method. Fig. 17(a) shows the comparison result of the resonant current during the startup process. The startup frequency is 250 kHz. The calculated outline of the resonant current fits the experimental result very well. Fig. 17(b) shows the comparison result of output voltage. Similarly, the calculated result is very consistent with the experimental one. In conclusion, the numerical model can provide accurate prediction of the resonant current and output voltage during the startup process.

TABLE I
Parameters of the Prototype

Parameters	Values
Input Voltage (V_{in})	240 V
Output Voltage (V_o)	24 V
Resonant Inductor (L_r)	86 μH
Resonant Capacitor (C_r)	23.5 nF
Magnetic Inductor (L_m)	266.5 μH
Transformer Turns Ratio (n_T)	10:1:1
Output Capacitor (C_o)	3.96 mF

Fig. 18 shows the experimental results of the relationship between startup current and startup frequency with 50% duty cycle, and the relationship between startup current and duty cycle at resonant frequency. The experimental results are almost in line with the calculated results, verifying the correctness of the analysis.

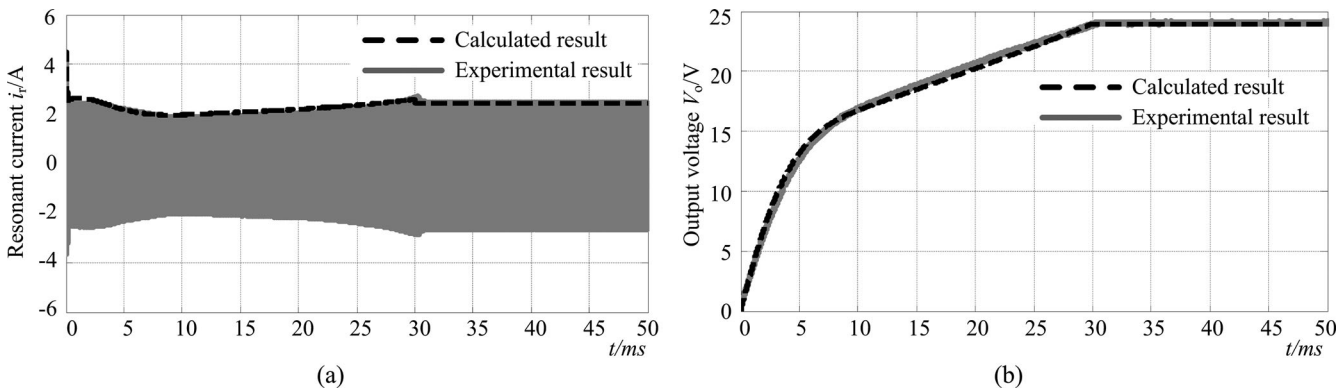

Fig. 17. Calculated and experimental results of the startup process with frequency-decreasing method. (a) Resonant current; (b) output voltage.

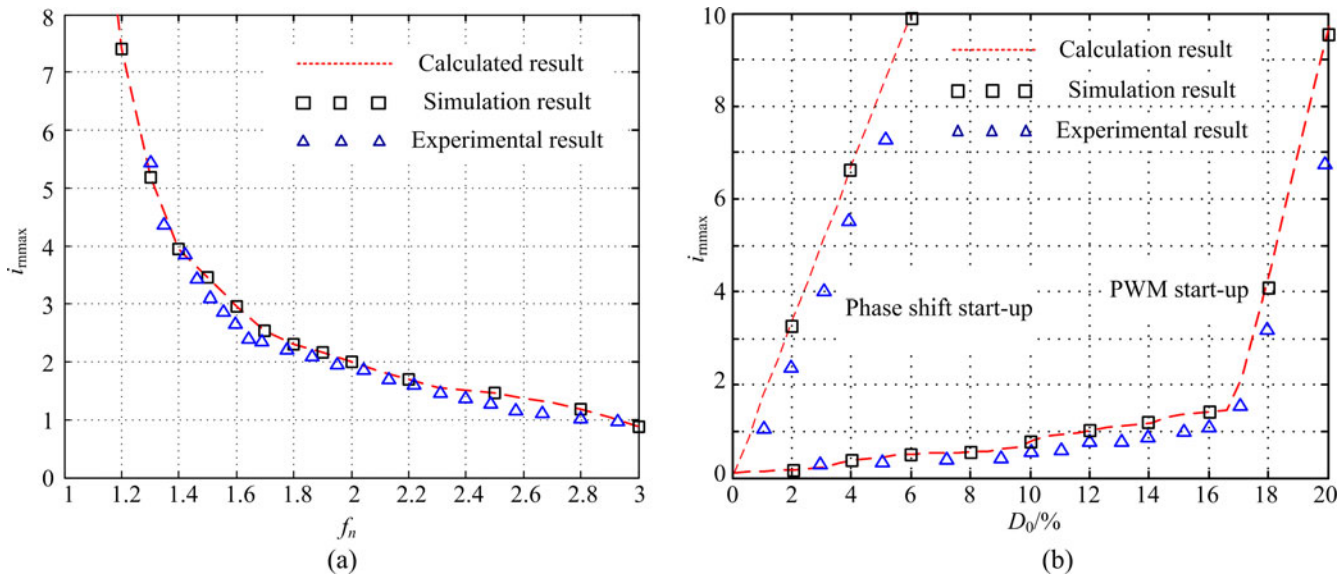

Fig. 18. Experimental results of startup current inrush. (a) The startup current inrush under different initial frequencies with 50% duty cycle; (b) The startup current inrush under different initial duty cycle at resonant frequency.

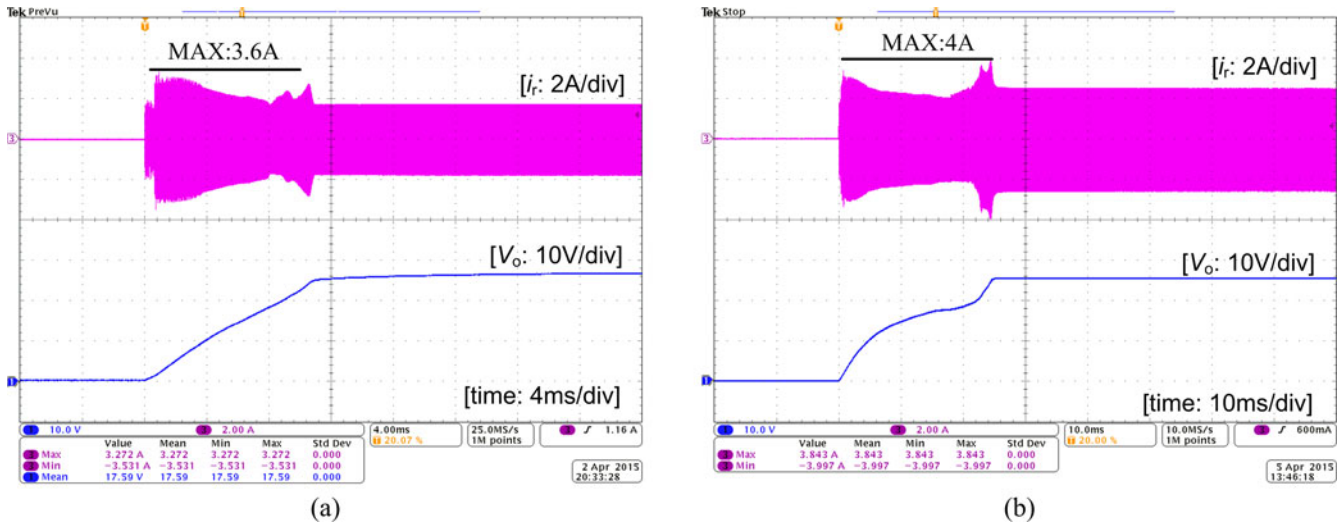

Fig. 19. Experimental waveforms of the resonant current and output voltage during startup with the optimized PWM startup method. (a) No-load condition; (b) full-load condition.

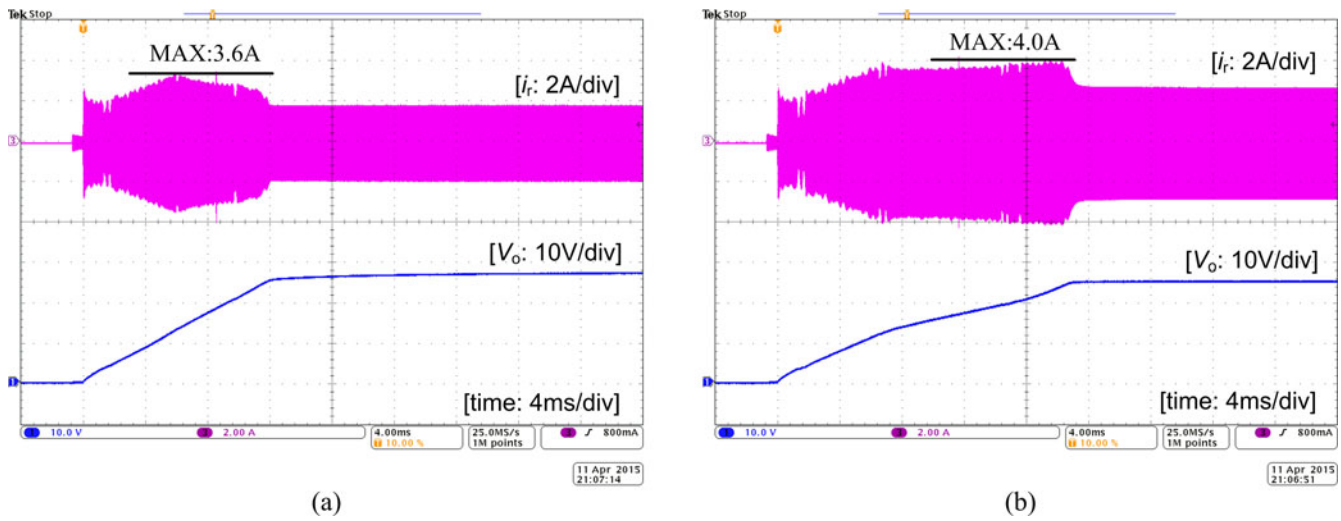

Fig. 20. Experimental waveforms of the resonant current and output voltage during startup with the optimized phase-shift startup method. (a) No-load condition; (b) full-load condition.

The peak value of the resonant current under a nominal load can be calculated as

$$i_{rp\mathrm{nom}} = \sqrt{\left(\frac{\pi V_{\mathrm{in}}}{2n_T^2 R_{\mathrm{nom}}}\right)^2 + \left(\frac{V_{\mathrm{in}}}{L_m}\cdot\frac{T_r}{4}\right)^2} = 2.52\ \mathrm{A}. \quad (19)$$

If the output is shorted, the output voltage regulator will decrease the frequency to the lowest and cause the overcurrent protection. The minimum frequency is designed to 75 kHz to avoid large short current. The peak value of the resonant current under shorted condition is

$$i_{rp\mathrm{shorted}} = \frac{1}{\cos\left[(1-\frac{f_r}{2f_{\mathrm{min}}})\cdot\pi\right]}\cdot\frac{V_{\mathrm{in}}}{Z_0} = 5.6\ \mathrm{A}. \quad (20)$$

To avoid the overcurrent protection during the startup, the limiting value i_{lim} can be set to 4 A. Applying the optimization algorithm to the PWM startup method, the experimental waveforms of the resonant current and the output voltage during the startup are shown in Fig. 19. Under no-load condition, the maximum current during the startup is 3.6 A. Under full-load condition, the maximum current during startup is 4.0 A. The experimental results verify that the resonant current can be limited to value i_{lim} by the optimized PWM startup method.

Similarly, applying the optimization algorithm to the phase-shift startup method, the experimental waveforms of the resonant current and the output voltage during the startup are shown in Fig. 20. Under no-load condition, the maximum current during the startup is 3.6 A. Under full-load condition, the maximum current during the startup is 4.0 A. The experimental results verify that the resonant current can be limited to value i_{lim} by the optimized phase-shift startup method.

VII. Conclusion

The *LLC* resonant converter usually adopts a very high startup frequency to suppress the startup current inrush effectively, which increases the output current demand of drive ICs at the same time. In this paper, a variable duty cycle soft startup strategy based on optimal current-limiting curve is presented, which can realize the suppression of the resonant current inrush under a low startup frequency. Due to the nonlinear characteristics of the *LLC*-SRC, the resonant tank is decomposed to several linear modes and a generalized numerical model of the *LLC*-SRC is established, providing highly accurate prediction on the resonant variables and output during the startup process. Based on the numerical model, the relationship between the startup current, initial startup frequency, and duty cycle is revealed to quantify the startup process and achieve optimal initial startup parameters. A numerical algorithm is presented to obtain the optimal current-limiting curve during the startup process. In order to verify the effectiveness of the proposed strategy, the startup process with the PWM control and the phase-shift control is optimized, respectively. The proposed soft startup strategy is verified by the experimental results.

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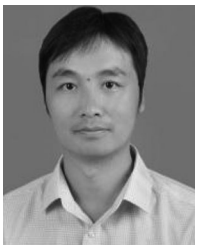

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