A Novel Phase-Shift Dual Full-Bridge Converter With Full Soft-Switching Range and Wide Conversion Range

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***Abstract*—This paper proposes a novel phase-shift dual full-bridge converter with shared leading leg and dual outputs in series. Full soft-switching range of the active switches can be achieved based on the parallel full-bridge configuration of the converter, and the dual outputs of the proposed converter are connected in series. The output voltage can be regulated by primary-side phase-shift and secondary-side phase–shift dual-mode control scheme, and a wide conversion range can be achieved. Furthermore, the circulating current in the primary-side full-bridge circuits can be extinguished. Therefore, the proposed converter would be useful for constant peak power and wide output voltage range applications. Steady-state operation and relevant analysis results of the proposed converter are presented and verified on a 1.5-kW hardware prototype. The experimental results show that the proposed converter can achieve a peak efficiency of 95.3%.**

***Index Terms*—Circulating current, constant peak power, dual full bridge, full soft-switching range, phase-shift control, shared leading leg.**

I. Introduction

HIGH-VOLTAGE power supplies generally require the characteristic of constant peak power for plasma sputtering, space electric propulsion, lasers, and bench power supplies for telecommunications testing [1]. Power supplies like this require a wide full-power conversion range that allows them to provide low current at high output voltages and high current at low output voltages [2], [3]. With a constant peak power characteristic, the full rated power of the power supplies can be used over the entire output voltage range [4]. The constant peak power and wide conversion range requirements have always been a challenging issue.

In recent years, conventional phase-shift full-bridge (PSFB) converters have received considerable attention for high-power applications [5]–[9] because of the advantages of high conversion efficiency, high power density, and low electromagnetic interference (EMI). All primary switches can be turned on under zero-voltage switching (ZVS) using the transformer leakage inductance and switch intrinsic capacitance without any external passive components [10]–[13]. It is well known that the energy stored in the leakage inductance of the transformer may be insufficient to realize ZVS for the lagging-leg switches especially under high input voltage and/or light-load conditions. The ZVS range can be extended by increasing the leakage inductance and/or adding a suitable series inductance. However, having a large series inductance can reduce the effective duty ratio of the converter and result in high-voltage spikes on the secondary-side rectifiers [14]–[19]. Moreover, excessive energy can be stored to produce large circulation currents, especially under high power and small duty cycle conditions, resulting in increasing the primary-side conduction loss.

In order to solve these problems, attention has recently been drawn to zero-voltage zero-current-switching (ZVZCS) PSFB converters [20]–[31]. The common characteristic is that the primary circulating current during freewheeling time can be reset by different ways. Using the reverse avalanche voltage of the leading-leg IGBTs to reset the primary current has been discussed in [20], but this scheme requires a very small leakage inductance. The primary current can be reset by using the dc blocking capacitor in [21] and [22]. In order to prevent the primary current from reversing, two diodes are added in series with the lagging leg in [21], while a saturable inductor is used in [22]. However, the conduction loss or saturable reactor loss is too high for these two schemes especially in high-power applications. It is popular to use a secondary-side-assisted circuit consisted of a tapped inductor and a diode to extinguish primary circulating current [23], [24], whereas the current ripple increases. By adding a secondary active clamp and controlling the clamp switch moderately, the primary current is reset without adding any lossy components or saturable reactors [25], [26]. Nevertheless, the control is complex since the clamp switch should be driven according to the driving logic of the primary switches. The methods proposed in [27] and [28] use the auxiliary winding of transformer to reset the primary current, but at the cost of increased complexity of the transformer. Several energy recovery clamp circuits (ERCCs) have been proposed in [29]–[31], and they have been applied in the secondary side to extinguish the primary current as well as clamp secondary rectifier voltage. However, in most of the ERCCs techniques,

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the amount of the clamped voltage depends on the duty ratio and input voltage of the converter. Moreover, all the above methods require additional power devices and passive components. Recently, the current-driven PSFB topologies have been proposed in [32] and [33] as a counterpart of the voltage-driven full-bridge converters. It clamps the voltage of the output rectifier and also satisfies ZVZCS operation conditions, so that it can achieve superior efficiency in all power range. Hence, it is very suitable for high-voltage and wide load range applications.

In order to solve the problems with the conventional primary-side phase-shift (PPS) control scheme, the phase-shift scheme based on an active rectifier [secondary-side phase shift (SPS)] has been proposed in [34]–[38]. In this control strategy, the duty cycle of all the active switches maintains at 0.5, and the output voltage is regulated by controlling the phase-shift angle between the primary and secondary switches. The SPS PWM converter proposed in [38] utilizes reverse blocking active switches for the controlled leg of the secondary rectifier to reduce the circulating current of the primary-side inverter as well as that of the secondary-side rectifier. Furthermore, the primary-side and secondary-side active switches can operate in ZVS and ZCS for all power range, respectively. Thus, it is preferable for electric vehicle battery charger applications.

Recently, several hybrid half-bridge full-bridge (HB-FB) converters based on "shared leg" technique have been proposed in [39]–[42]. Their common characteristic is that the input energy can be transferred to the output even in the freewheeling interval of the output inductor. In this way, the requirements for filter are less because of the three-level voltage waveforms of the secondary-side rectifier, and the efficiency can be greatly increased because of the parallel power processing technique [43]. The hybrid HB-FB converter in [39] utilizes the magnetizing current of the additional transformer to achieve full ZVS range of the lagging-leg switches. However, when the primary side of the main transformer is shorted in the freewheeling interval, a circulating current will be created due to the series connection of secondary sides of the two transformers, resulting in excessive conduction loss. A ZVZCS hybrid converter combining the PSFB and half-bridge *LLC* resonant converter configuration with shared leading leg has been proposed in [41]. In this method, full ZVS range of the leading-leg switches can be realized based on the parallel *LLC* resonant half-bridge configuration. The primary circulating current is quickly extinguished by the parallel secondary-side constant dc voltage source during the freewheeling period. However, this way also results in high-voltage spikes on the secondary-side rectifiers because of the lack of clamping feature. In consequence, this will increase the voltage stress across the rectifiers and may result in EMI problems.

This paper proposes a novel dual full-bridge converter with full soft-switching range and shared leading leg based on PPS and SPS dual control modes. In this converter scheme, ZVS of MOSFETs in the leading leg can be achieved from true zero load to full load by using the magnetizing current of transformer. Full ZCS range of the lagging-leg IGBTs can be realized with the current-driven rectifier configuration. It is also shown that the voltage stresses on the output terminal power devices can be reduced because of the dual outputs in series configuration. Furthermore, very wide conversion range can be achieved because both the series-connected outputs can be regulated through the PPS and SPS dual control modes. Hence, there is a lot of potential for this converter to be used for constant peak power and wide output range applications. Another advantage of this converter is that the primary-side circulating current of the two transformers is extinguished, and, therefore, the relevant conduction losses can be effectively reduced. Also, the ZCS of secondary-side active switches can be achieved for the entire load range.

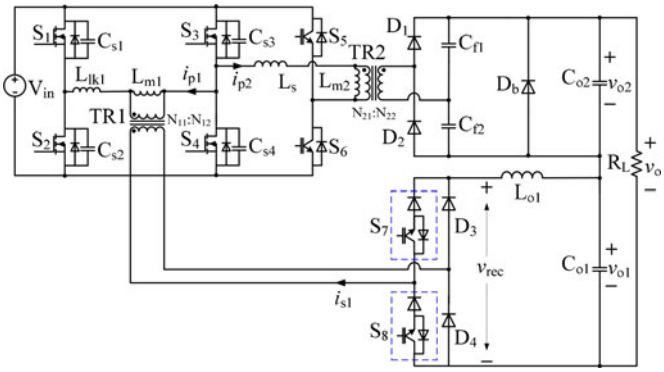

Fig. 1. Circuit configuration for the proposed converter.

This paper is organized as follows. Section II describes the circuit configuration and detailed operation principle of the power stage. In Section III, some detailed features and characteristics are analyzed. In Section IV, a 1.5-kW hardware converter prototype has been designed, made, and tested to verify the validity and performance of the proposed circuit. Finally, conclusion is drawn in Section V.

II. Circuit Description and Operation Principle

Fig. 1 shows the circuit diagram of the proposed converter which is composed of two parts. The first part is a SPS full-bridge PWM circuit (SPS-FBC), including four MOSFETs S_1–S_4, a tightly coupled transformer TR1 with an air gap, a secondary-side rectifier (reverse blocking active switches S_7 and S_8 and diodes D_3 and D_4), an *LC* output filter (L_{o1} and C_{o1}), and a bypass diode D_b. The second part is a PPS current-fed full-bridge circuit (PPS-FBC), including two MOSFETs S_3 and S_4 as leading-leg, two IGBTs (S_5 and S_6) as the lagging leg, a tightly coupled transformer TR2, a series ac inductor L_s, a secondary voltage-doubler-type rectifier (rectifier capacitors C_{f1} and C_{f2} and diodes D_1 and D_2), and an output capacitor C_{o2}. The reason why IGBTs are introduced to S_5 and S_6 when MOSFETs are used in S_1–S_4 is because MOSFETs are majority-carrier semiconductors; hence, the best soft-switching choice would be ZVS, where the turn-on capacitive losses can be eliminated. On the other hand, IGBTs are minority-carrier semiconductors, the ZCS technique can effectively avoid the turn-off losses caused by the current tail. Furthermore, ZVS of S_1–S_4 and ZCS of S_5 and S_6 can be realized for all power range in the proposed converter.

The topology is operating in two modes: the PPS control mode and the SPS control mode. In PPS control mode, the SPS-FBC is uncontrolled and the active switches S_1, S_4, and S_7 or S_2, S_3, and S_8 conduct together. During this interval, the output voltage (v_{o1}) of the SPS-FBC is at its maximum value ($V_{o1,\mathrm{PPS}}$) and the whole output voltage is regulated by PPS-FBC. When the total output voltage is required to be lower than $V_{o1,\mathrm{PPS}}$, the gate signals of switches S_3 and S_6 or S_4 and S_5 are completely out of phase and the output voltage of PPS-FBC reaches zero. In this way, the converter turns into the SPS control mode. In this mode, the whole output voltage is adjusted by the SPS-FBC, and, therefore, very wide conversion range can be achieved by using the dual modes control scheme with PPS and SPS.

The behavior of the converter in each mode is analyzed in detail in this section and the analysis is based on the following assumptions:

1) all components and devices are ideal;
2) the converter works in steady state so that the average current through a capacitor and the average voltage across an inductor are all zero;
3) the output capacitors of switches S_1–S_4 are expressed as $C_{\mathrm{so}} = C_{\mathrm{s1}} = C_{\mathrm{s2}} = C_{\mathrm{s3}} = C_{\mathrm{s4}}$.

A. PPS Control Mode

The proposed converter goes through eight stages during a half-switching cycle in this mode. The equivalent operation circuits and key waveforms for different stages are shown in Figs. 2 and 3, respectively.

In the PPS mode, the bypass diode D_b is reverse biased. Switches S_2, S_3, and S_5 conduct prior to stage 1 and the primary current i_{p2} in the transformer TR2 is reset due to discontinuous-conduction mode (DCM) operation of the series inductor L_s. Meanwhile, the magnetizing current of TR2 is negligible since the magnetizing inductance L_{m2} is designed to be large.

Stage 1 [$t_0 \le t < t_1$]: At t_0, S_5 has been turned OFF with ZCS since the transformer TR2 primary current i_{p2} maintains zero. During this interval, S_2 and S_3 are conducting and the input power is delivered to the output through the SPS-FBC. Meanwhile, the secondary-side diodes D_1 and D_2 are reversed biased and are off.

Stage 2 [$t_1 \le t < t_2$]: At t_1, IGBT S_6 is turned ON. During this stage, the output diode D_1 conducts and clamps the secondary voltage of TR2 to the voltage across capacitor C_{f1}. It is supposed that the capacitors C_{f1} and C_{f2} equal to each other and are large enough so that the output voltage v_{o2} can be shared by them. Thus, there is a constant voltage across the inductance L_s, which is the combination of the series inductance and the leakage inductance of TR2. Therefore, the primary current i_{p2} ramps up to its peak value. According to Fig. 2(b), the primary current i_{p2} is given by

$$i_{p2}(t) = \frac{V_{\mathrm{in}} - k_2 \frac{v_{o2}}{2}}{L_s}(t - t_1) \tag{1}$$

where V_{in} is an input voltage of the converter and k_2 denotes the turns ratio $N_{21} : N_{22}$ of the transformer TR2. It is assumed that $T_{2,\mathrm{on}}$ is the active interval when S_3, S_6 or S_4, S_5 are turned ON together by phase-shift control, and T_s is the switching period, then we can derive $D_2 = 2\,T_{2,\mathrm{on}}/T_s$ as the duty cycle which determines the peak value I_{p2} of the primary current i_{p2}

$$I_{p2} = i_{p2}(t_2) = \frac{V_{\mathrm{in}} - k_2 \frac{v_{o2}}{2}}{L_s} D_2 \frac{T_s}{2}. \tag{2}$$

During this stage, the magnetizing current i_{Lm1} of transformer TR1 increases with a constant slope

$$i_{\mathrm{Lm1}}(t) = i_{\mathrm{Lm1}}(t_1) + \frac{V_{\mathrm{in}}}{L_{m1} + L_{\mathrm{lk1}}}(t - t_1) \tag{3}$$

where L_{m1} and L_{lk1} are the magnetizing inductance and leakage inductance of transformer TR1, respectively. This stage will end once the MOSFETs S_2 and S_3 are turned OFF. At t_2, i_{Lm1} reaches its peak value I_{Lm1} and I_{Lm1} is given by

$$I_{\mathrm{Lm1}} = i_{\mathrm{Lm1}}(t_2) = \frac{V_{\mathrm{in}}}{2\,(L_{m1} + L_{\mathrm{lk1}})} \frac{T_s}{2}. \tag{4}$$

Stage 3 [$t_2 \le t < t_3$]: During this stage, the output capacitors of S_2 and S_3 are charged and that of S_1 and S_4 are discharged. Also, i_{Lm1}, i_{p2} and the output inductor current i_{Lo1} are considered to be constant during this stage. According to Fig. 2(c), the output voltage of the inverter v_{AB} is given by

$$v_{AB}(t) = v_{\mathrm{s4}}(t) - v_{\mathrm{s2}}(t) \tag{5}$$

where $v_{\mathrm{s2}}(t)/v_{\mathrm{s4}}(t)$ is the voltage across the active switch S_2/S_4 and $v_{\mathrm{s2}}(t)/v_{\mathrm{s4}}(t)$ is calculated as

$$v_{\mathrm{s4}}(t) = V_{\mathrm{in}} - \frac{i_{\mathrm{Lm1}}(t_2) + i_{Lo1}(t_2)/k_1 + i_{p2}(t_2)}{2C_{\mathrm{so}}}(t - t_2) \tag{6}$$

$$v_{s2}(t) = \frac{i_{\mathrm{Lm1}}(t_2) + i_{Lo1}(t_2)/k_1}{2C_{\mathrm{so}}}(t - t_2) \tag{7}$$

where k_1 denotes the turns ratio $N_{11} : N_{12}$ of transformer TR1. By using (2) and (4)–(7), v_{AB} is given by

$$v_{AB}(t) = V_{\mathrm{in}} - \frac{2\,[I_{\mathrm{Lm1}} + i_{Lo1}(t_2)/k_1] + I_{p2}}{2C_{\mathrm{so}}}(t - t_2). \tag{8}$$

This stage will end once v_{AB} reaches zero, and the end of this interval, t_3 can be obtained by solving (8) and t_3 will be

$$t_3 = t_2 + \Delta t_{2,3} = t_2 + \frac{2C_{\mathrm{so}} V_{\mathrm{in}}}{2\,[I_{\mathrm{Lm1}} + i_{Lo1}(t_2)/k_1] + I_{p2}} \tag{9}$$

where $\Delta t_{2,3}$ is the time interval of stage 3.

Stage 4 [$t_3 \le t < t_4$]: At t_3, the secondary-side diode D_4 begins to conduct. During this interval, L_{lk1} resonates with the switch output capacitors and the secondary current i_{s1} decreases from $i_{Lo1}(t_2)$ to zero. The voltages across S_2 and S_4 are expressed, respectively, as

$$-C_{\mathrm{so}} \frac{dv_{\mathrm{s4}}(t)}{dt} = \frac{I_{p2} + I_{\mathrm{Lm1}} + i_{\mathrm{s1}}(t)/k_1}{2} \tag{10}$$

$$C_{\mathrm{so}} \frac{dv_{\mathrm{s2}}(t)}{dt} = \frac{I_{\mathrm{Lm1}} + i_{\mathrm{s1}}(t)/k_1}{2} \tag{11}$$

where i_{s1} is the secondary-side current of TR1 and i_{s1} can be expressed as

$$\frac{L_{\mathrm{lk1}}}{k_1} \frac{di_{\mathrm{s1}}(t)}{dt} = v_{\mathrm{s4}}(t) - v_{\mathrm{s2}}(t). \tag{12}$$

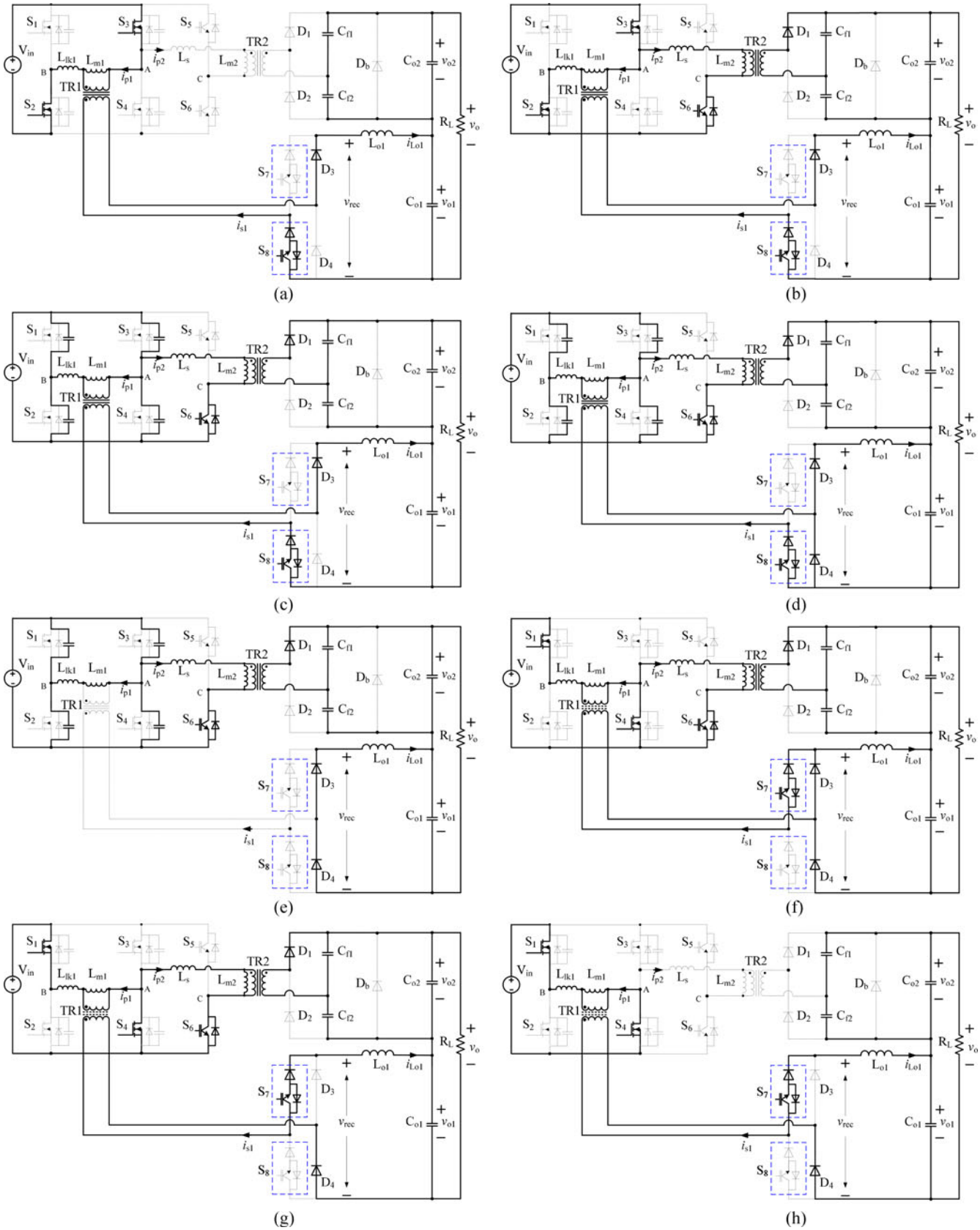

Fig. 2. Topological stages of the proposed converter in PPS mode. (a) Stage 1, (b) stage 2, (c) stage 3, (d) stage 4, (e) stage 5, (f) stage 6, (g) stage 7, and (h) stage 8.

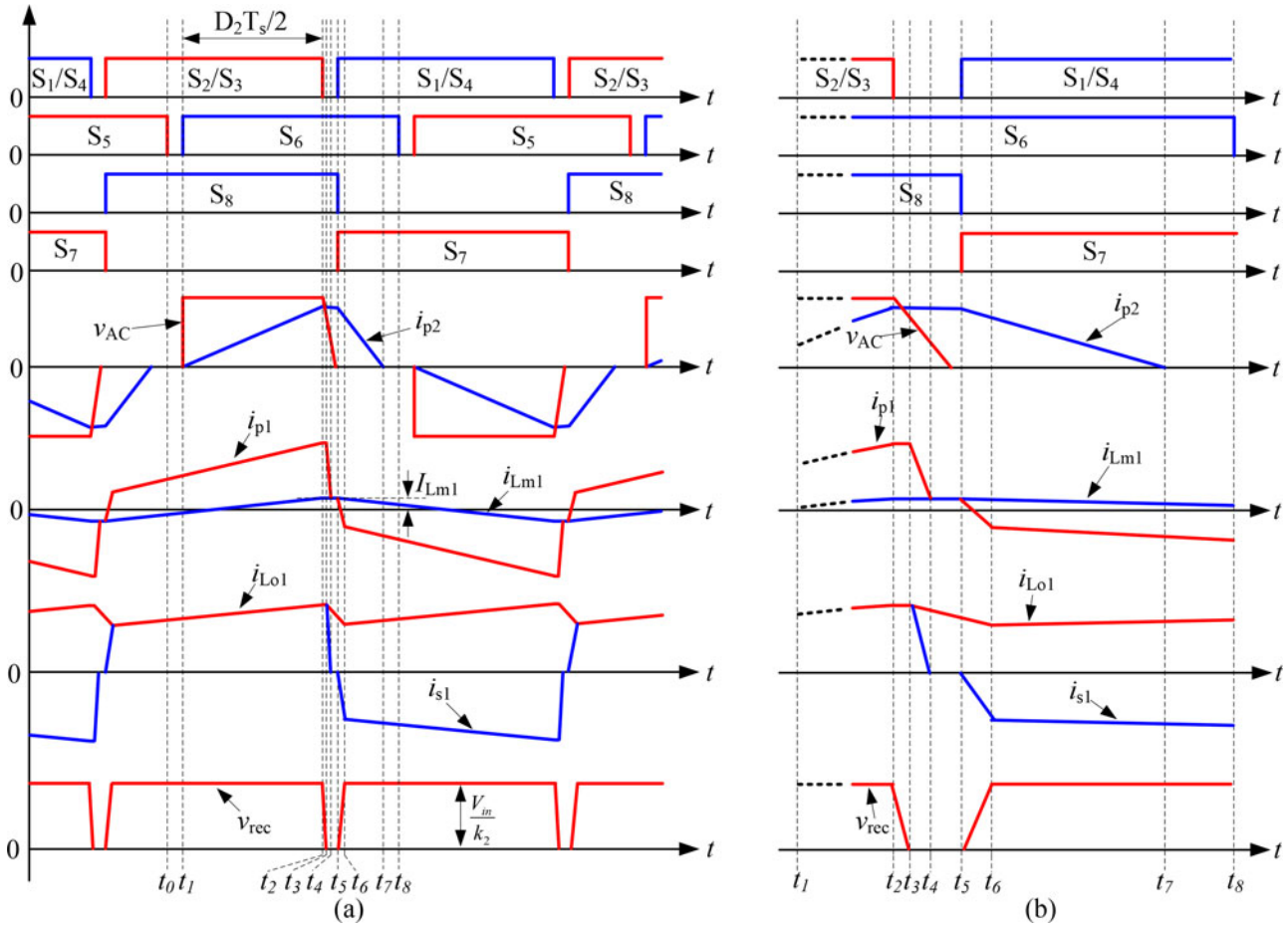

Fig. 3. (a) Key waveforms of the proposed converter in the PPS mode operation. (b) Enlarged waveforms from t_2 to t_8.

By using (10)–(12), the expressions for i_{s1} is calculated as

$$i_{s1}(t) = i_{Lo1}(t_2)\cos[\omega(t-t_3)] + \frac{[v_{s4}(t_3)-v_{s2}(t_3)]}{Z}\sin[\omega(t-t_3)] - \frac{k_1(I_{p2}+2I_{Lm1})}{2}\{1-\cos[\omega(t-t_3)]\} \quad (13)$$

where $\omega = 1/\sqrt{k_1 C_{so} L_{lk1}}$ and $Z = \sqrt{L_{lk1}/k_1 C_{so}}$; $v_{s2}(t_3)$ and $v_{s4}(t_3)$ are the switch voltages of S_2 and S_4 at t_3, respectively. Stage 4 will end once the current i_{s1} reaches zero, and the whole output inductor current i_{Lo1} flows through D_3 and D_4 so that the secondary active switch S_8 can be turned OFF with ZCS.

Stage 5 [$t_4 \le t < t_5$]: During this stage, the output capacitors of S_2 and S_3 continues to be charged up to V_{in} and that of S_1 and S_4 are discharged down to zero by the magnetizing current I_{Lm1}. Then, the body diodes of S_1 and S_4 begin to conduct, and stage 5 will end once S_1 and S_4 are turned ON with ZVS.

Stage 6 [$t_5 \le t < t_6$]: At t_5, switches S_1, S_4, and S_7 have been turned ON. During this stage, the voltage v_{AC} is zero; hence, the primary current i_{p2} decreases with a constant slope as depicted as follows:

$$-\frac{di_{p2}(t)}{dt} = \frac{k_2 v_{o2}}{2L_s}. \quad (14)$$

During this interval, the secondary voltage of TR1 is constantly zero, and the input voltage is applied to the leakage inductance L_{lk1}. Thus, the currents i_{p1} and i_{s1} increase gradually. Then, the secondary current i_{s1} is given by

$$i_{s1}(t) = \frac{k_1 V_{in}}{L_{lk1}}(t-t_5). \quad (15)$$

The secondary current i_{s1} gradually commutates to S_7. Stage 6 will end once i_{s1} reaches the output inductor current i_{Lo1}.

Stage 7 [$t_6 \le t < t_7$]: At t_6, the diode D_3 turns off. During this stage, S_1 and S_4 are ON and the entire input voltage V_{in} is placed across the primary winding of TR1. Thus, the output inductor current i_{Lo1} increases with a constant slope as

$$\frac{di_{Lo1}(t)}{dt} = \frac{V_{in}/k_1 - v_{o1}}{L_{o1}}. \quad (16)$$

During this interval, i_{p2} continues to ramp down to reach zero at the end of this stage and then S_6 can be turned OFF with ZCS. Stage 7 will end once i_{p2} reaches zero.

Stage 8 [$t_7 \le t < t_8$]: At t_7, the output diode D_1 naturally turns off with zero current. During this stage, switches S_1, S_4, and S_6 are ON and i_{p2} keeps zero. The input energy continues to be transferred to the output by the SPS-FBC, while the load current is fed by the output capacitors C_{f1}, C_{f2}, and C_{o2} for

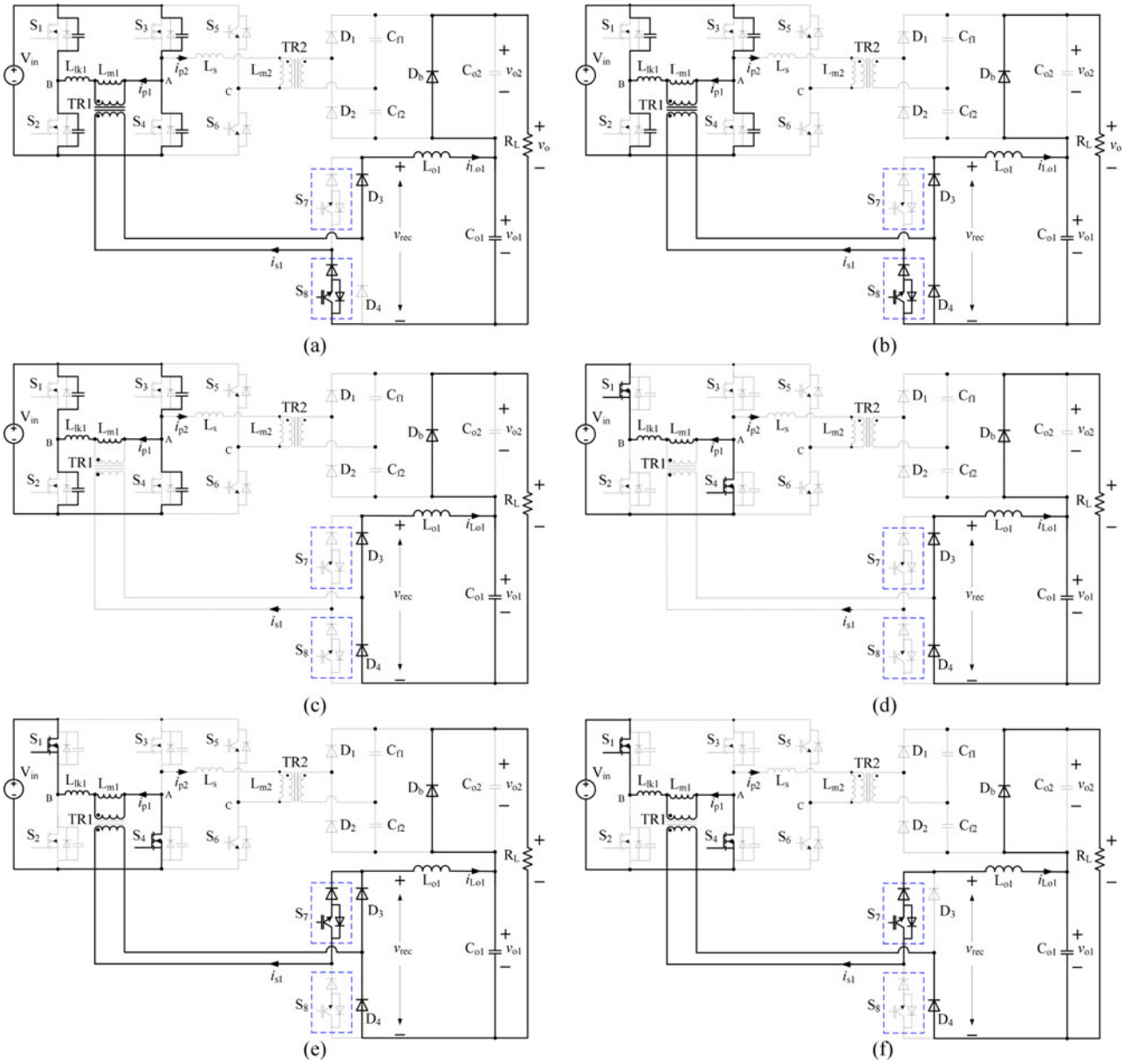

Fig. 4. Topological stages of the proposed converter in SPS Mode. (a) Stage 1, (b) stage 2, (c) stage 3, (d) stage 4, (e) stage 5, and (f) stage 6.

PPS-FBC. Stage 8 will end once IGBT S_6 is turned OFF with ZCS and the next half switching cycle starts.

B. SPS Control Mode

When the converter is in the SPS control mode, the gate signal of switch S_3/S_4 is the same as that of S_5/S_6 and the output voltage v_{o2} of PPS-FBC is zero. The bypass diode D_b is conducting, and, therefore, the SPS-FBC passes the input energy to the output with only one diode voltage drop in the current path. Thus, the conduction loss is effectively reduced by this arrangement.

The proposed converter goes through six stages during a half-switching cycle in this mode. The equivalent operation circuits and key waveforms for different stages are shown in Figs. 4 and 5, respectively. The whole output voltage v_o is regulated by the SPS-FBC and the SPS-FBC operation in this mode is almost the same as in PPS control mode except for stage 4, and, therefore, only stage 4 is discussed in detail in this section.

Stage 4 [$t_3 \le t < t_4$]: The body diodes of S_1 and S_4 conduct before stage 4 and at t_3, MOSFETs S_1 and S_4 are turned ON with ZVS. During this stage, switches S_1, S_4, and S_8 are ON, and the secondary current i_{s1} stays at zero so that the primary-side and secondary-side power circuits are separated. The entire input voltage V_{in} is placed across the primary winding of TR1. Meanwhile, the entire load current flows through D_3, D_4, and L_{o1} for freewheeling. The stage ends once S_8 is turned OFF with ZCS and then S_7 is turned ON.

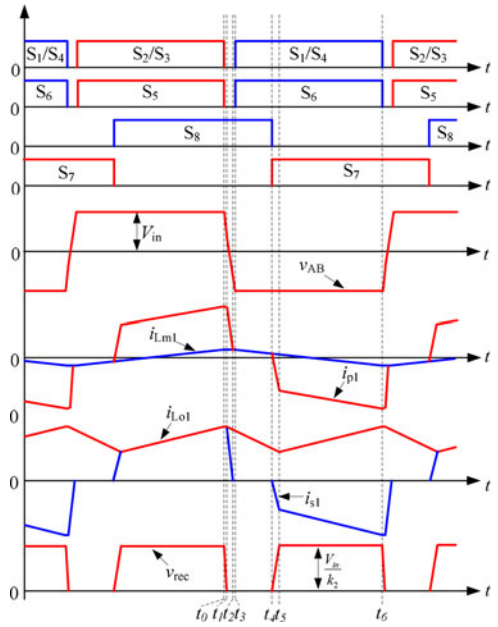

Fig. 5. Key waveforms of the proposed converter in SPS mode operation.

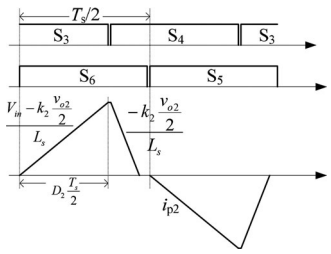

Fig. 6. Gate pulses sequences for the primary-side switches of PPS-FBC and the series inductance current waveform.

III. Analysis of the Proposed Converter

A. Analysis of the Steady-State Operation

1) PPS Control Mode: In the PPS control mode, the dual outputs of the proposed converter are connected in series, and the whole output voltage is regulated by the PPS-FBC. The voltage conversion ratios of PPS-FBC and SPS-FBC in this mode will be calculated successively.

Fig. 6 illustrates gate pulses sequences for the primary-side switches of the PPS-FBC and the series inductance current waveform. In order to calculate the conversion ratio of the PPS-FBC, the average current through the series inductance L_s should be determined. The average value of the series inductance current is given by

$$\bar{I}_{p2} = \frac{1}{T_s}\left(\frac{V_{\rm in} - k_2 v_{o2}/2}{L_s}\right)\left(D_2\frac{T_s}{2}\right)^2\left(\frac{2V_{\rm in}}{k_2 v_{o2}}\right). \quad (17)$$

Based on the basic principle of energy conservation, the following equations can be derived:

$$k_2\frac{v_{o2}}{2}\bar{I}_{p2} = v_{o2} i_{L,\rm PPS} \quad (18)$$

$$i_{L,\rm PPS} = \frac{(v_{o2} + V_{o1,\rm PPS})}{R_e} \quad (19)$$

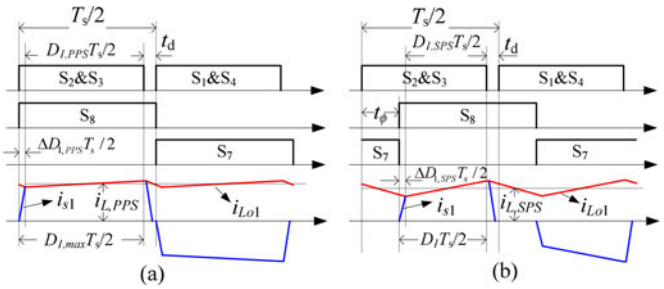

Fig. 7. Waveforms of current $i_{\rm s1}$, i_{Lo1} and gate pulses sequences for the active switches of SPS-FBC (a) in PPS control mode and (b) in SPS control mode.

where $i_{L,\rm PPS}$ is the load current, R_e is the effective load of the converter, and $V_{o1,\rm PPS}$ is the output voltage of SPS-FBC in this mode. By using (17)–(19), the dc gain characteristic of the PPS-FBC is given by

$$G_{vo2,\rm PPS} = \frac{v_{o2}}{V_{\rm in}} = \frac{2}{\frac{V_{o1,\rm PPS}}{V_{\rm in}}\frac{4L_s}{D_2^2 T_s R_e} + \frac{k_2}{2} + \sqrt{\left(\frac{V_{o1,\rm PPS}}{V_{\rm in}}\frac{4L_s}{D_2^2 T_s R_e} + \frac{k_2}{2}\right)^2 + \frac{16L_s}{R_e D_2^2 T_s}}}. \quad (20)$$

In this scheme, fully ZVS for the primary switches of SPS-FBC can be achieved by using the magnetizing current of TR1. Thus, the leakage inductance $L_{\rm lk1}$ of TR1 can be designed as small as possible, however it is still not zero, and, therefore, the slope in the rising edge of the secondary current $i_{\rm s1}$ is finite. This slope reduces the duty cycle available in the secondary. Fig. 7(a) shows the waveforms of current $i_{\rm s1}, i_{Lo1}$, and gate pulses sequences for the active switches of SPS-FBC in PPS mode. The voltage gain of SPS-FBC in this mode is given by

$$G_{vo1,\rm PPS} = \frac{V_{o1,\rm PPS}}{V_{\rm in}} = \frac{D_{1,\rm PPS}}{k_1}. \quad (21)$$

According to Fig. 7(a), the effective duty cycle of the SPS-FBC in PPS mode is given by

$$D_{1,\rm PPS} = D_{1,\max} - \Delta D_{1,\rm PPS} \quad (22)$$

where $\Delta D_{1,\rm PPS}$ is the duty cycle loss due to the finite slope of the rising edge of the secondary current; $D_{1,\max}$ is the peak value of the primary duty cycle and is given by

$$D_{1,\max} = 1 - \frac{2t_d}{T_s} \quad (23)$$

where $t_{\rm d}$ is the dead time. Looking at Fig. 7(a) and using (15), $\Delta D_{1,\rm PPS}$ is given by

$$\Delta D_{1,\rm PPS} = \frac{2L_{\rm lk1}}{k_1 V_{\rm in} T_s}\left[i_{L,\rm PPS} - \frac{V_{o1,\rm PPS}}{2L_{o1}}(1 - D_{1,\rm PPS})\frac{T_s}{2}\right]. \quad (24)$$

In the PPS mode, the term containing $(1 - D_{1,\rm PPS})$ is relatively small comparing with $i_{L,\rm PPS}$. Thus, by using (19) and (21)–(24), the voltage gain of SPS-FBC in the PPS mode is

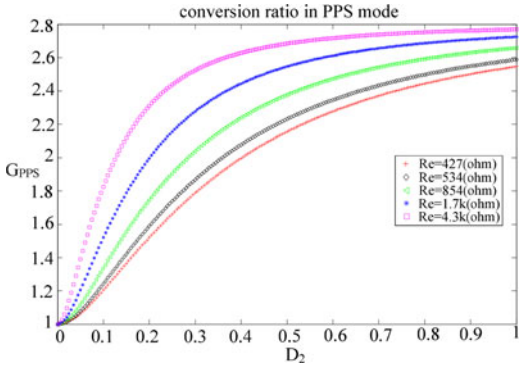

Fig. 8. Converter gain in PPS control mode for different loads.

given by

$$G_{vo1,\mathrm{PPS}} = \frac{V_{o1,\mathrm{PPS}}}{V_{\mathrm{in}}} = \frac{D_{1,\max} - \frac{2L_{\mathrm{lk1}}G_{vo2,\mathrm{PPS}}}{k_1 T_s R_e}}{k_1 + \frac{2L_{\mathrm{lk1}}}{k_1 T_s R_e}}. \tag{25}$$

The total gain of the proposed converter in PPS mode can be derived based on (20) and (25) and is given by

$$\begin{aligned} G_{\mathrm{PPS}} &= G_{vo1,\mathrm{PPS}} + G_{vo2,\mathrm{PPS}} \\ &= \frac{D_{1,\max}}{k_1 + \frac{2L_{\mathrm{lk1}}}{k_1 T_s R_e}} + \frac{k_1}{k_1 + \frac{2L_{\mathrm{lk1}}}{k_1 T_s R_e}} \\ &\quad \frac{2}{\frac{4L_s G_{vo1,\mathrm{PPS}}}{D_2^2 T_s R_e} + \frac{k_2}{2} + \sqrt{\left(\frac{4L_s G_{vo1,\mathrm{PPS}}}{D_2^2 T_s R_e} + \frac{k_2}{2}\right)^2 + \frac{16L_s}{R_e D_2^2 T_s}}}. \end{aligned} \tag{26}$$

It can be seen from above that when L_{lk1} is small enough, the term containing L_{lk1} can be ignored and (26) can be written as

$$\begin{aligned} G_{\mathrm{PPS}} &= G_{vo1,\mathrm{PPS}} + G_{vo2,\mathrm{PPS}} = \frac{D_{1,\max}}{k_1} \\ &+ \frac{2}{\frac{4L_s}{D_2^2 T_s R_e}\frac{D_{1,\max}}{k_1} + \frac{k_2}{2} + \sqrt{\left(\frac{4L_s}{D_2^2 T_s R_e}\frac{D_{1,\max}}{k_1} + \frac{k_2}{2}\right)^2 + \frac{16L_s}{R_e D_2^2 T_s}}}. \end{aligned} \tag{27}$$

Fig. 8 shows the converter gain in (27) varying with D_2 under different load conditions. It can be seen that the variation of the gain is more obvious for light loads in smaller values of duty cycle, and less prominent for heavier loads.

2) SPS Control Mode: In the SPS control mode, the output voltage of PPS-FBC maintains zero, and the whole output voltage is adjusted by the SPS-FBC. The voltage gain of the proposed converter in this mode is given by

$$G_{\mathrm{SPS}} = \frac{V_{o1,\mathrm{SPS}}}{V_{\mathrm{in}}} = \frac{D_{1,\mathrm{SPS}}}{k_1}. \tag{28}$$

According to Fig. 7(b), the following equations can be obtained:

$$D_{1,\mathrm{SPS}} = D_1 - \Delta D_{1,\mathrm{SPS}} \tag{29}$$

$$D_1 = 1 - \frac{2\left(t_d + t_\phi\right)}{T_s} \tag{30}$$

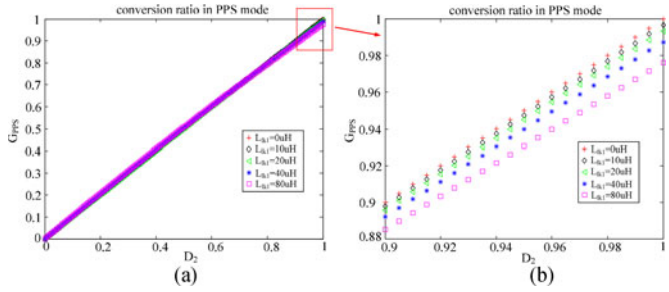

Fig. 9. Converter gain in SPS mode for different leakage inductance: (a) Full duty cycle range; (b) duty cycle range from 0.9 to 1.

where t_ϕ is the phase-shift interval; $\Delta D_{1,\mathrm{SPS}}$ is the duty cycle loss and is given by

$$\Delta D_{1,\mathrm{SPS}} = \frac{2L_{\mathrm{lk1}}}{k_1 V_{\mathrm{in}} T_s}\left[i_{L,\mathrm{SPS}} - \frac{V_{o1,\mathrm{SPS}}}{2L_{o1}}\left(1 - D_{1,\mathrm{SPS}}\right)\frac{T_s}{2}\right] \tag{31}$$

where $i_{L,\mathrm{SPS}}$ is the load current in this mode and is given by

$$i_{L,\mathrm{SPS}} = \frac{V_{o1,\mathrm{SPS}}}{R_e} \tag{32}$$

The gain of the proposed converter in SPS mode can be derived based on (28)–(32) and is given by

$$\begin{aligned} G_{\mathrm{SPS}} &= \frac{V_{o1,\mathrm{SPS}}}{V_{\mathrm{in}}} = \frac{D_{1,\mathrm{SPS}}}{k_1} = \frac{D_1}{k_1} \\ &\frac{2}{1 + \frac{2L_{\mathrm{lk1}}}{T_s R'_e} - \frac{L_{\mathrm{lk1}}}{2L'_{o1}} + \sqrt{\left(1 + \frac{2L_{\mathrm{lk1}}}{T_s R'_e} - \frac{L_{\mathrm{lk1}}}{2L'_{o1}}\right)^2 + \frac{2D_1 L_{\mathrm{lk1}}}{L'_{o1}}}} \end{aligned} \tag{33}$$

where $R'_e = k_1^2 R_e$ and $L'_{o1} = k_1^2 L_{o1}$ are the load resistance and filter inductor reflected to the primary.

Fig. 9 shows the variation of gain as a function of the duty cycle D_1 for different leakage inductance L_{lk1}. The curve with $L_{\mathrm{lk1}} = 0$ corresponds to the SPS-FBC without leakage inductance. As L_{lk1} increases, the maximum attainable voltage gain of the converter decreases for a given value of duty cycle. Thus, considering the effect of the leakage inductance, the turn's ratio k_1 should be adjusted to achieve the required voltage gain of SPS-FBC.

Based on the above analysis, it can be seen that the proposed converter has a very wide conversion range, and it is very suitable for constant peak power and wide output voltage range applications.

B. DCM Conduction of the Series AC Inductor L_s

The operation in DCM of the series inductor L_s plays an important role in realizing ZCS for the lagging-leg switches S_5 and S_6 (IGBTs), as well as eliminating the voltage spikes across the diode rectifiers (D_1 and D_2). It can be seen from Fig. 6 that when IGBT S_5 (or S_6) is turned OFF, the current in the series inductor is zero and the ZCS turn-off of IGBTs S_5 and S_6 is guaranteed. Also, the voltage spikes across the secondary rectifiers of the PPS-FBC are eliminated due to the current-driven configuration

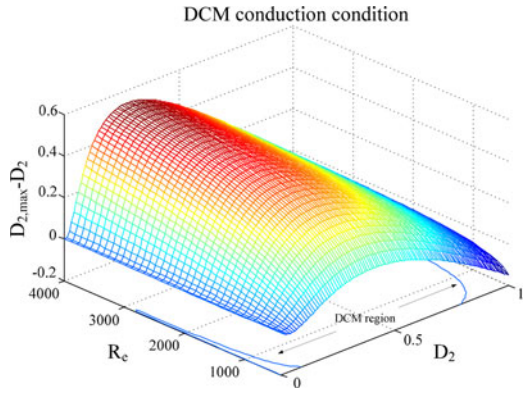

Fig. 10. DCM conduction condition of series inductor L_s varying with D_2 and R_e when $k_2 = 1.1$, $L_s = 80\ \mu$H, and $G_{vo1,\mathrm{PPS}} = 1$.

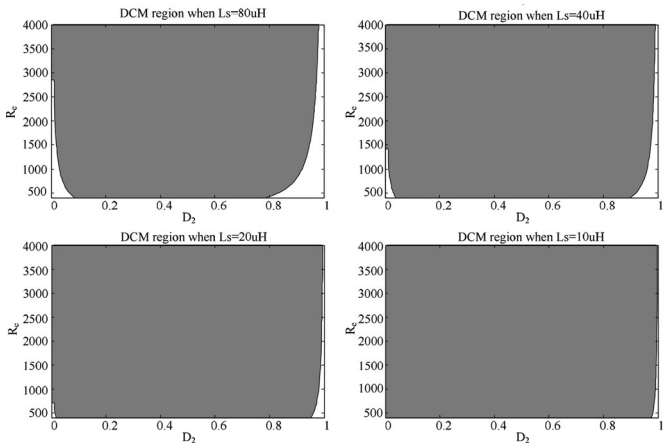

Fig. 11. DCM region as the function of D_2 and R_e for different series inductor L_s.

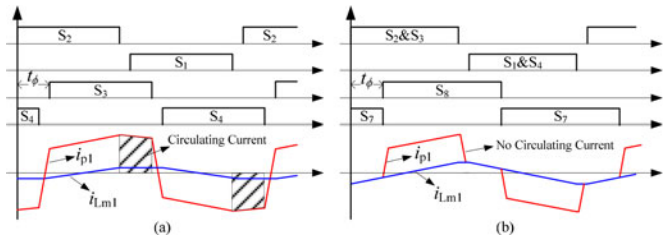

Fig. 12. Gate pulses and current waveforms of the primary-side full-bridge circuits: (a) Conventional PSFB converter and (b) SPS-FBC.

at the primary side and capacitive filter at the secondary side. The output diodes (D_1 and D_2) turn off naturally because of the relatively slow downslope of the triangular current in the series inductor L_s, so reverse recovery and switching losses in D_1 and D_2 can be reduced. The energy stored in the leakage inductance of transformer TR2 is accommodated by the series inductor L_s, and, therefore, no more duty cycle loss and circulation loss will be resulted. However, the DCM operation increases the RMS and peak values of the series inductor current, resulting in more primary-side conduction loss.

In order to guarantee DCM conduction of L_s, the maximum duty cycle $D_{2,\max}$ should be determined. $D_{2,\max}$ appears under the situation that the lagging-leg switches (S_5 and S_6) are turned OFF exactly at the time when the series inductor current reaches zero. According to Fig. 6, DCM conduction condition of L_s can be expressed as

$$D_{2,\max} - D_2 = \frac{k_2 v_{o2}}{2V_{\mathrm{in}}} - D_2 \geq 0. \tag{34}$$

By using (20), (34) can be written as

$$D_{2,\max} - D_2 = \frac{k_2}{\frac{4L_s G_{vo1,\mathrm{PPS}}}{D_2^2 T_s R_e} + \frac{k_2}{2} + \sqrt{\left(\frac{4L_s G_{vo1,\mathrm{PPS}}}{D_2^2 T_s R_e} + \frac{k_2}{2}\right)^2 + \frac{16L_s}{R_e D_2^2 T_s}}} - D_2 \geq 0. \tag{35}$$

Fig. 10 shows the DCM conduction condition of L_s varying with D_2 and R_e when $k_2 = 1.1$, $L_s = 80\ \mu$H, and $G_{vo1,\mathrm{PPS}} = 1$. Fig. 11 shows the DCM region (the shadow area) as a function of D_2 and R_e with different series inductor L_s. It can be seen from Figs. 10 and 11 that the series inductor also operates in continuous-conduction mode when the duty cycle D_2 is very small for a given value L_s (for example, $L_s = 80\ \mu$H). This is due to the fact that the primary-side current i_{p2} in L_s cannot be extinguished to zero by the small output voltage of the PPS-SPC during the freewheeling interval. As seen in Fig. 11, the value of L_s should be reduced in order to extend the DCM region. However, the RMS and peak values of the series inductor current increases as L_s decreases, and, therefore, the value of L_s should be carefully selected based on the above analysis. In addition, a dc blocking capacitor is utilized in series with L_s to ensure DCM operation of the series inductor under small duty cycle condition [22]. It is should be noted that the saturable inductor in [22] is not needed since the reverse current is blocked by the large magnetizing inductance of TR2 due to the capacitive output filter at the secondary side.

According to Fig. 8, enlarging $D_{2,\max}$ is a feasible choice to increase the maximum attainable dc gain of the proposed converter. However, a larger $D_{2,\max}$ results in faster downslope of the triangular current in the series inductor L_s, and this will increase the reverse recovery and switching losses in the output diodes of the PPS-FBC. Thus, the optimum design for $D_{2,\max}$ is a tradeoff between the maximum dc gain of the converter and the reverse recovery and switching losses for the output diodes. It can be seen from Fig. 8 that when $D_{2,\max}$ is larger than 0.8 approximately under full-load condition ($R_e = 427\ \Omega$), the curve slope becomes relatively slow and the dc gain does not increase significantly when larger $D_{2,\max}$ is selected. Therefore, the optimal duty cycle range of $D_{2,\max}$ is around 0.8.

C. Soft-Switching Conditions for the Active Switches of SPS-FBC

Fig. 12 illustrates the primary-side current and magnetizing current waveforms for the conventional PSFB converter and SPS-FBC, respectively. In the SPS-FBC, there is no circulating

TABLE I
CIRCUIT PARAMETERS

Components	Parameters
Transformer TR1	Ferroxcube E42/21/20-3C95 ferrite core; two winding side-by-side arrangement; primary turns $N_{11} = 38$, 6∗AWG#25; secondary turns $N_{12} = 42$, 5∗AWG#25; magnetizing inductance $L_{m1} = 800\ \mu$H; leakage Inductance $L_{lk1} = 20\ \mu$H
DC Blocking Capacitor C_{b1} and C_{b2}	15-μF 250-V high-frequency film capacitor
Output Inductance L_{o1}	Arnold MS-130125-2 Sendust core turns $N = 64$, $L_{o1} = 520\ \mu$H, AWG#18
Output Capacitor C_{o1}	14-μF 630-V high-frequency film capacitor
Series Inductance L_s	Ferroxcube E42/21/15-3C95 ferrite core turns $N = 8$, $L_s = 80\ \mu$H, 5∗AWG#25
Transformer TR2	Ferroxcube E42/21/15-3C95 ferrite core; two winding side-by-side arrangement; Primary turns $N_{21} = 33$, 5∗AWG#25; Secondary turns $N_{22} = 30$, 5∗AWG#25
Rectifier Capacitors C_{f1} and C_{f2}	14-μF 630-V high-frequency film capacitor
Output Capacitor C_{o2}	4.7-μF 630-V high-frequency film capacitor
Primary Switches	ST Microelectronic STW45NM60
S_1–S_4	650 V, 45 A. $R_{ds,on} = 0.09\ \Omega$
Primary Switches	Fairchild IGBT FGH75T65UPD
S_5 and S_6	650 V, 75 A
Secondary-Side Active Switches S_7 and S_8	Fairchild IGBT FGH75T65UPD 650 V, 75 A and Infineon SiC Schottky diode IDW30G65C5 650 V, 30 A
Output Diodes D_1 and D_2, D_b	Fairchild ultrafast diode MUR1560 600 V, 15 A
Output Diodes D_3 and D_4	Infineon SiC Schottky diode IDW30G65C5 650 V, 30 A

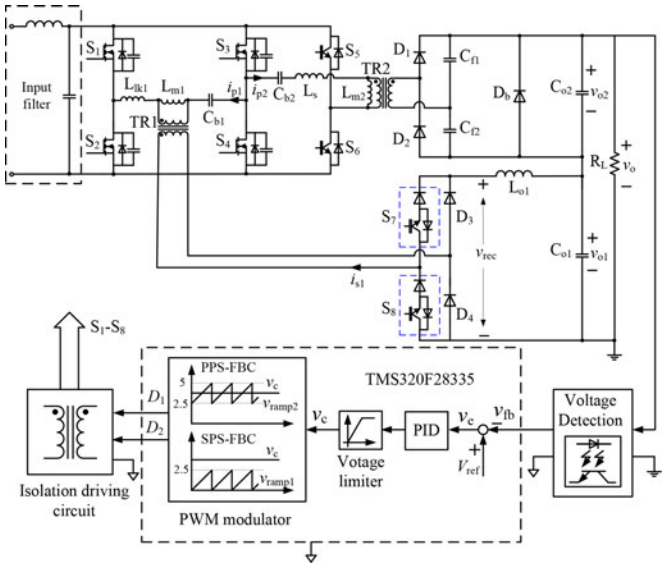

Fig. 13. Schematic diagram of the laboratory prototype.

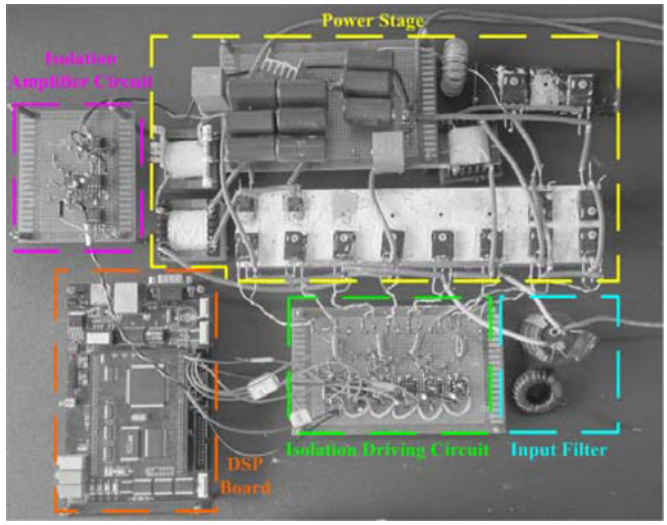

Fig. 14. Experimental prototype.

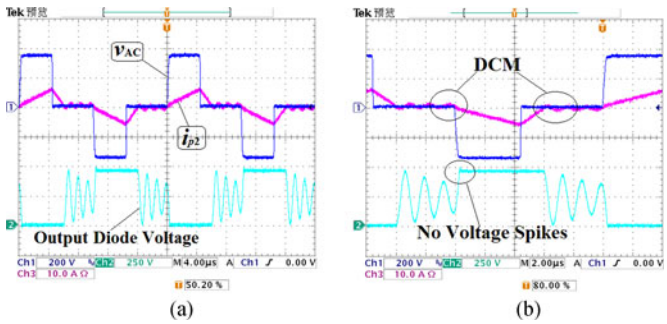

Fig. 15. (a) PPS-FBC waveforms in PPS mode at $v_o = 800$ V and $P_o = 800$ W. (b) PPS-FBC enlarged waveforms in PPS mode at $v_o = 800$ V and $P_o = 800$ W.

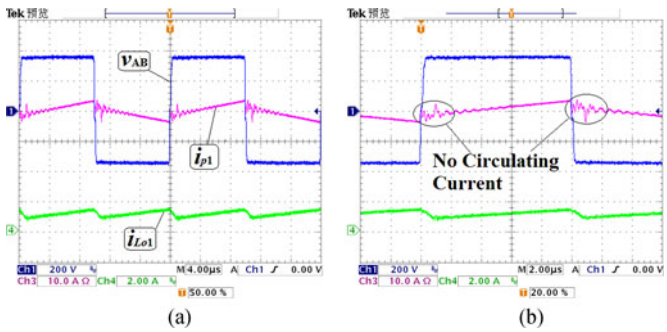

Fig. 16. (a) SPS-FBC waveforms in PPS mode at $v_o = 800$ V and $P_o = 800$ W. (b) SPS-FBC enlarged waveforms in PPS mode at $v_o = 800$ V and $P_o = 800$ W.

current in the primary-side full-bridge circuits compared to the conventional PSFB converter. As shown in Fig. 12(b), the peak value of magnetizing current i_{Lm1} is independent of load condition. The ZVS conditions for the primary-side switches of SPS-FBC can be expressed as

$$\frac{1}{2}\left(L_{m1} + L_{\mathrm{lk1}}\right) I_{\mathrm{Lm1}}^2 \geq 2C_{\mathrm{so}} V_{\mathrm{in}}^2. \tag{36}$$

As indicated in (4) and (36), the energy needed to realize ZVS depends only on the magnitude of the input voltage, and is independent of the output voltage. By using (4), the magnetizing inductance L_{m1} is defined as

$$L_{m1} \leq \frac{T_s^2}{64C_{\mathrm{so}}} - L_{\mathrm{lk1}}. \tag{37}$$

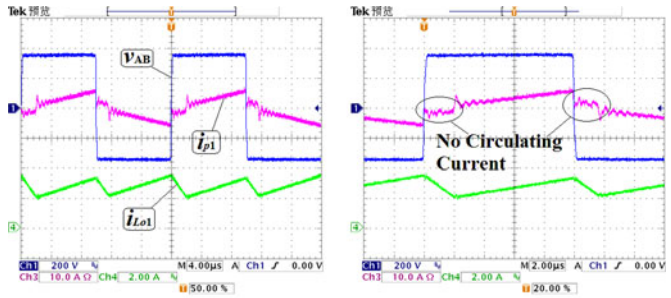

Fig. 17. (a) SPS-FBC waveforms in SPS mode at $v_o = 300$ V and $P_o = 800$ W. (b) SPS-FBC enlarged waveforms in SPS mode at $v_o = 300$ V and $P_o = 800$ W.

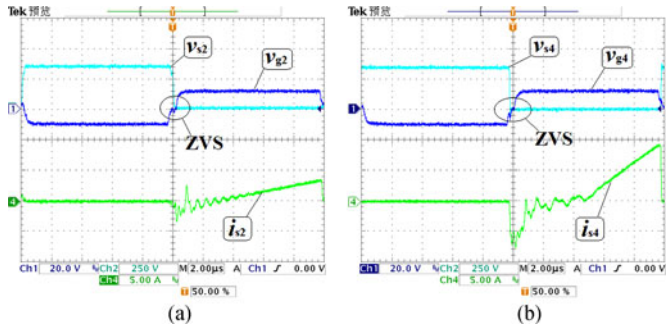

Fig. 18. Measured switching waveforms in PPS mode at $v_o = 800$ V and $P_o = 800$ W. (a) Primary-side switch S_2. (b) Primary-side switch S_4.

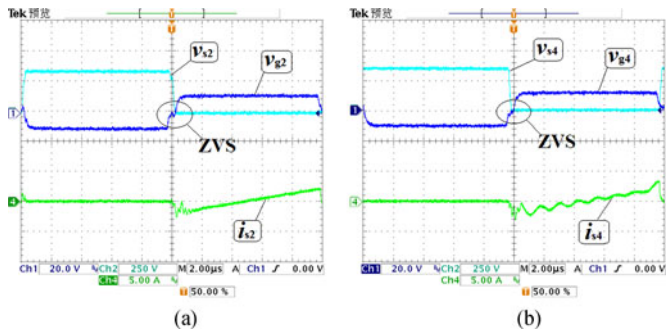

Fig. 19. Measured switching waveforms in PPS mode at $v_o = 800$ V and $P_o = 30$ W. (a) Primary-side switch S_2. (b) Primary-side switch S_4.

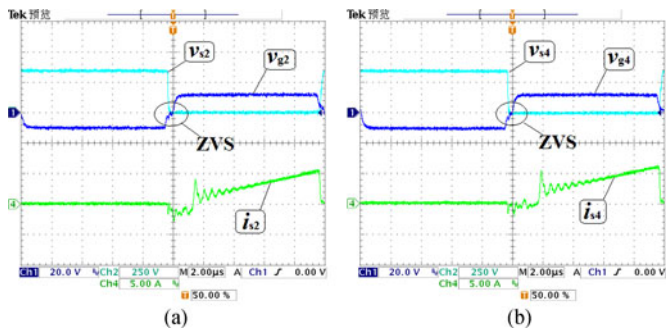

Fig. 20. Measured switching waveforms in SPS mode at $v_o = 300$ V and $P_o = 800$ W. (a) Primary-side switch S_2. (b) Primary-side switch S_4.

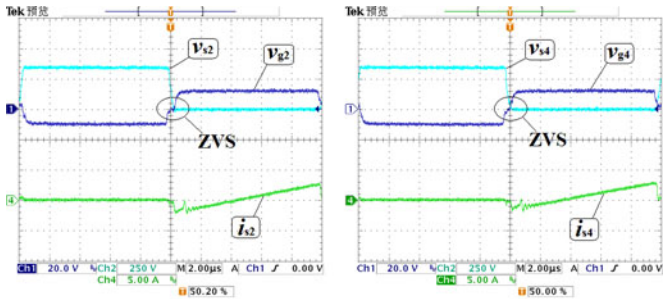

Fig. 21. Measured switching waveforms in SPS mode at $v_o = 300$ V and $P_o = 30$ W. (a) Primary-side switch S_2. (b) Primary-side switch S_4.

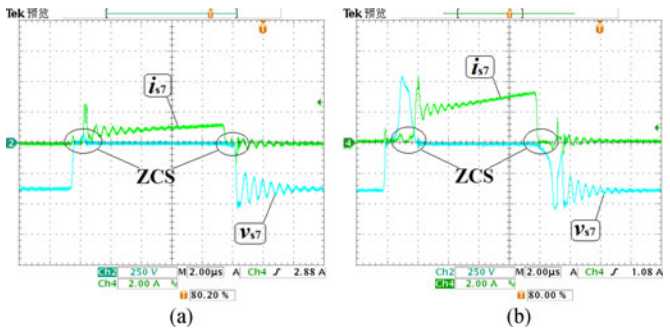

Fig. 22. Secondary-side active switch S_7 waveforms: (a) In PPS mode at $v_o = 800$ V and $P_o = 800$ W. (b) In SPS mode at $v_o = 300$ V and $P_o = 800$ W.

In order to ensure ZVS, the dead time t_d, should be adjusted to allow the output capacitors of MOSFETs S_1–S_4 to fully charge and discharge under no-load condition, and it is given by

$$t_d \geq \frac{2C_{\rm so}V_{\rm in}}{I_{\rm Lm1}} = \frac{8C_{\rm so}(L_{m1}+L_{\rm lk1})}{T_s}. \tag{38}$$

ZVS of S_1–S_4 can be achieved from true zero load to full load by selecting of the proper L_{m1} and t_d. The selections of L_{m1} and t_d are independent of the input voltage and load condition, as shown in (37) and (38). Thus, ZVS of S_1–S_4 is independent of input voltage variations, the output voltage, and output current.

According to Fig. 7(a), the on-intervals for the secondary-side active switches S_7 and S_8 of the SPS-FBC should be extended to 50% to ensure ZCS turn-off. It means that there is no dead time between the gate pulse timings of S_7 and S_8. Meanwhile, the secondary current i_{s1} should be reset during the dead time t_d to guarantee the ZCS operations of S_7 and S_8. Thus, t_d is required to satisfy (39) and $\Delta t_{3,4}$ can be found using (40) based on (13)

$$t_d \geq \Delta t_{2,3} + \Delta t_{3,4} \tag{39}$$

$$\begin{aligned} i_{s1}(t) &= i_{Lo1}(t_2)\cos(\omega\Delta t_{3,4}) \\ &\quad + \frac{[v_{s4}(t_3) - v_{s2}(t_3)]}{Z}\sin(\omega\Delta t_{3,4}) \\ &\quad - \frac{k_1(I_{p2}+2I_{\rm Lm1})}{2}[1-\cos(\omega\Delta t_{3,4})] = 0 \end{aligned} \tag{40}$$

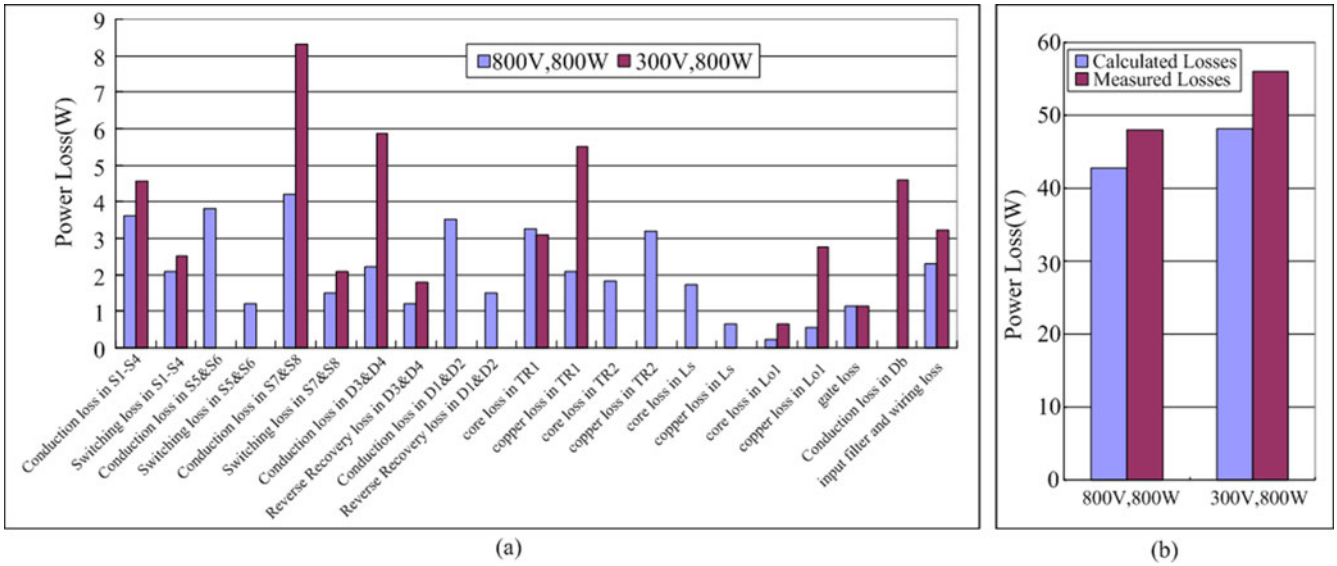

Fig. 23. Loss evaluation in the two control modes with 800-W output power: (a) Loss breakdown and (b) a comparison between the calculated losses with measured values.

where $\Delta t_{3,4}$ is the time interval of stage 4 in PPS mode. The primary current i_{p1} is larger than or equivalent with the magnetizing current I_{Lm1} during the dead time, and, therefore, the following expression is obtained:

$$\frac{8C_{\mathrm{so}}(L_{m1}+L_{\mathrm{lk1}})}{T_s} > \Delta t_{2,3}+\Delta t_{3,4}. \tag{41}$$

Based on (38), (39), and (41), (42) can be obtained to ensure ZCS turn-off of S_7 and S_8

$$t_d \geq \frac{8C_{\mathrm{so}}\,(L_{m1}+L_{k1})}{T_s}. \tag{42}$$

As indicated in (42), ZCS turn-off of S_7 and S_8 can be realized for all power range, and is also independent of input voltage variations.

IV. Experiment Results and Discussions

A 1.5-kW hardware prototype of the proposed converter has been designed, made, and tested to verify the circuit operation principles. The prototype converter has the following specifications: input voltage $V_{\mathrm{in}} = 350$ V; output voltage $V_o = 300 - 800$ V; and switching frequency $f_s = 50$ kHz. The circuit parameters are illustrated in Table I. Fig. 13 shows the schematic diagram of experimental circuit. In this scheme, a DSP controller (TMS320F28335) is used as the digital controller for the closed-loop control and gate signals generation. The control voltage v_c in Fig. 13 is based on the error between the actual and desired output voltage, and is designed to vary from 2.5 to 5 V in PPS mode. The ramp voltage for SPS-FBC varies from 0 to 2.5 V. Thus, SPS-FBC operates with full pulse width in the PPS mode. The ramp voltage for PPS-FBC is shifted, and varies from 2.5 to 5 V. Therefore, the pulse width of PPS-FBC is adjusted to control the whole output voltage. In SPS mode, the control voltage falls below 2.5 V; hence, the pulse width of SPS-FBC is controlled now, and PPS-FBC operates with zero pulse width. Therefore, very wide output voltage and power range can be achieved by this arrangement. A photograph of the experimental prototype is shown in Fig. 14.

Fig. 15 shows the waveforms of PPS-FBC in PPS mode under the condition of $v_o = 800$ V and $P_o = 800$ W. According to this figure, the series inductor L_s operates in DCM; hence, the current in the series inductor is zero when IGBT S_5 (or S_6) is turned ON/OFF. It can be concluded that the IGBTs of PPS-FBC undergo ZCS turn-on and turn-off. Meanwhile, there are no voltage spikes across the secondary-side diodes of PPS-FBC. Figs. 16 and 17 show the waveforms of SPS-FBC for the two control modes. It can be confirmed from the measured waveforms that the primary circulating current of SPS-FBC has been greatly reduced in both control modes.

Figs. 18–21 show the switching waveforms of S_2 and S_4 in the two control modes for different load conditions. It can be clearly demonstrated that ZVS of MOSFETs in the proposed converter can be actually realized from true zero load to full load over wide output voltage range. The switching waveforms of the secondary-side active switch are shown in Fig. 22 for different operating modes. It can be seen from this figure that ZCS turn-on/off in the secondary-side active switch is actually attained. Fig. 23(a) shows the loss evaluation for several main parts of the proposed converter in both control modes with the same output power according to the parameters shown in Table I. A comparison between the calculated losses with measured values is given in Fig. 23(b). As shown in Fig. 23(a), the conduction losses of power devices and the copper losses of transformers dominate the main parts of the power loss breakdown, especially in the SPS control mode. Thus, the effect of utilizing the soft-switching technologies is confirmed herein. Meanwhile, the switching loss in S_5 and S_6 and the reverse recovery loss in D_1 and D_2 are relatively small compared to the conduction loss, and, therefore, the optimum design for the maximum duty cycle $D_{2,\max}$ is also verified. The measured efficiency with different loads and different output voltages is given in Fig. 24. It can be seen that high efficiency over wide output voltage and load

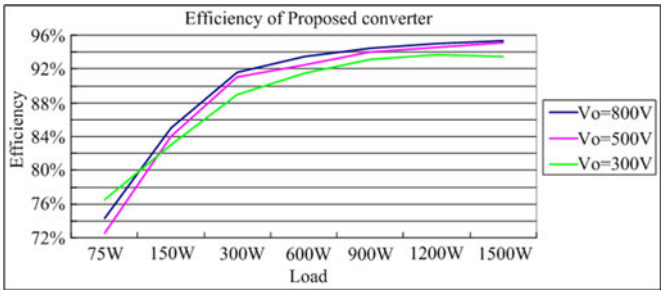

Fig. 24. Experimental results of efficiency at different loads and different output voltages.

range is achieved, and the peak efficiency achieves 95.3% under 1.5-kW output power and 800-V output voltage conditions. The conduction losses of the active switches and output diodes are reduced with lower current stresses leading to better efficiency with a higher output voltage.

V. Conclusion

This paper presents a novel PPS and SPS dual mode controlled dual full-bridge converter with shared leading leg and dual outputs in series. ZVS of MOSFETs and ZCS of IGBTs in the proposed converter is realized from true zero load to full load over wide output voltage range. The primary-side current of the two transformers during the freewheeling period is effectively reset. The voltage stresses across the output terminal power devices are significantly reduced because of the dual outputs in series configuration. In addition, very wide conversion range is achieved due to the fact that the dual outputs can be adjusted successively. Hence, there is a great potential for this converter to be used for constant peak power and wide output range applications. Experimental results obtained from a laboratory-made prototype have been presented to demonstrate the performance of this converter.

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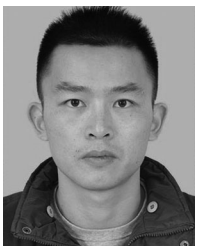

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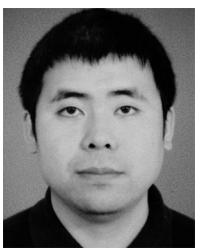

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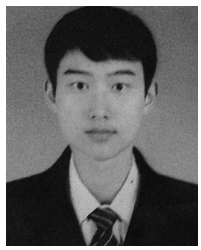

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