A Fault-Tolerant Strategy Based on Fundamental Phase-Shift Compensation for Three-Phase Multilevel Converters With Quasi-Z-Source Networks With Discontinuous Input Current

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***Abstract*—This paper proposes a new fault-tolerant strategy for a multilevel converter with an integrated impedance-source network. The proposed fault-tolerant strategy leverages the flexibility provided by the impedance-source network to implement the fundamental phase-shift compensation (FPSC) method in order to restore operation of a multilevel converter with one or more faulty switches to the prefault conditions. In case of a fault occurrence, the proposed fault-tolerant strategy makes the most use of the remaining converter capacity and generates balanced line-to-line voltages, while evenly distributing an inevitable voltage stress increase, over all converter switches. In this paper, first, a brief background about an impedance-source based cascaded H-bridge converter and a suitable modulation method for it is provided. Then, the FPSC method is explained and the proposed fault-tolerant strategy based on this method is introduced. Finally, several experimental results from a prototype converter are provided to validate the operation of the proposed strategy.**

***Index Terms*—Fault-tolerant strategy, fundamental phase-shift compensation, impedance-source multilevel converter, multilevel converter, Z-source CHB.**

I. Introduction

THE medium-to-high-voltage industrial settings involving electric energy conversion demand for safe, reliable, and efficient power electronic stages [1]. This has fostered a myriad of research and development activities in the areas of high-power/high-voltage energy conversion and high-power electronics through the past decade [2], [3]. Two of the prominent technologies developed recently to facilitate high-power conversion are multilevel converters and impedance-source networks for power electronic converters [4], [5]. Multilevel converters are becoming increasingly popular in industrial apparatus aimed at medium-to-high-power conversion applications. Compared to conventional inverters, they feature superior characteristics such as lower total harmonic distortion (THD), higher efficiency, and lower switching voltage stress [6]–[8]. The impedance-source networks overcome several limitations of the conventional voltage/current source inverters and provide an efficient and flexible means of power conversion between the source and load in a very wide range of power conversion applications [9], [10].

Numerous power conversion topologies incorporating different types of impedance-source networks have been proposed in the literature recently [11]–[14]. Among them, the multilevel converters incorporating Z-source networks (ZSI) [9], [15], quasi-Z-Source networks (qZSI) [16], [17], or qZSI with discontinuous input current networks (qZSId) [18], [19] are of utmost importance for scholars in the area of high-power conversion. These topologies provide an excellent opportunity to marry the benefits of the multilevel converters with the flexibility provided by the impedance-source networks to achieve the best of both worlds: lower THD, higher efficiency, and lower switching stress [20] combined with a wide range of ac output that can be lower or higher than the input voltage [21]. In particular, the Z-source networks can be easily fused with cascaded H-bridge (CHB) converters to relieve the voltage gain requirements for H-bridge modules in a CHB [4], [19], [22], [23]. This combination provides single-stage energy conversion with higher equivalent output pulse width modulation (PWM) frequency [15], [24], [25] while featuring an excellent boost function [26]. Therefore, higher inversion efficiency can be achieved while reducing the size of the output filter and the number of H-bridge modules required to match the output voltage generated by a conventional CHB [22]. The reduced number of H-bridge cells makes the system less expensive, less complex, and more reliable [27].

Despite the improvements provided by multilevel converters, since the number of power electronic switches in a multilevel converter topology is higher than that of a conventional inverter, the chances of fault occurrence on the switches is higher, and thus, the converter's reliability is relatively lower compared to conventional inverters [28], [29]. High reliability for power converters in commercial and industrial applications is critical due to extreme monetary ramifications of interruption of operation. As a result, developing fault-tolerant operation schemes for multilevel converters has always been a topic of great interest for researchers in the related areas [30]–[33]. Several fault-tolerant operation schemes for multilevel converters have been recently proposed in the literature; however, almost all of these techniques can be classified into two main categories: techniques that modify the converter hardware topology after fault diagnosis [34], [35] and techniques that modify the converter control algorithm, particularly the modulation method, after fault diagnosis [36].

Manuscript received October 04, 2015; revised December 08, 2015; accepted January 07, 2016. Date of publication January 21, 2016; date of current version June 24, 2016. Recommended for publication by Associate Editor G. Baoming.

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Digital Object Identifier 10.1109/TPEL.2016.2520884

Although several valuable fault-tolerant strategies for multilevel converters have been developed by researchers, the development of fault-tolerant strategies that are applicable to multilevel inverters with impedance-source networks is not a very well explored area [37], [38]. Few works concerned with fault-tolerant operation of impedance-source-based inverters are only concerned with conventional two-level ZSIs [39], [40]. The authors of this paper believe that the inherent boosting characteristic of a Z-source network, if leveraged properly, provides a viable countermeasure to compensate for the adverse effects of a faulty switch in a multilevel converter.

The purpose of this paper is to propose a new fault-tolerant strategy for postfault operation of an impedance-source multilevel converter with one or more faulty switches. The proposed fault-tolerant strategy generates balanced line-to-line voltages without bypassing any healthy converter elements, makes better use of the converter capacity, and generates ac output voltages with no amplitude reduction in the event of a fault. The proposed strategy exploits the advantages of the boosting capability of the Z-source network in conjunction with a slightly modified fundamental phase-shift compensation (FPSC) technique [41] to generate balanced voltages with the same amplitude as the voltages during the normal operation. In case of a fault occurrence on a switch, the proposed strategy increases the voltage gain of the remaining healthy H-bridge cells to compensate for the negative effects of bypassing a faulty cell while revising the phase shifts between the phase voltages to achieve balanced line-to-line voltages, all while keeping the voltage stress of the healthy switches at the minimum possible value. The proposed strategy is applicable to any impedance-source CHB converter with three or more voltage levels.

II. Groundwork

A. Converter Topology

CHB multilevel converters feature modular structure, simple physical layout, and numerous redundant switching states [20]. Therefore, CHB converters are excellent topologies for designing fault-tolerant inversion stages. Various voltage-fed ZSI configurations such as the traditional ZSI, qZSI, and qZSId [42] can be readily combined with the CHB topology to enhance its fault-tolerant properties. In this work, a qZSId network is integrated into the traditional CHB converter topology to assemble a fault-tolerant CHB converter with a very high degree of flexibility. The qZSId network is especially selected due to the lower voltage rating requirement for its capacitors compared to the traditional ZSI network [19]. Nevertheless, the proposed fault-tolerant strategy can be applied to a CHB converter with any of the mentioned Z-source networks.

Fig. 1 illustrates the circuit diagram of the *n*-level qZSId-based CHB converter, referred to as the qZSId-CHB converter hereinafter. As pictured, the proposed qZSId-CHB converter places a qZSId network on the input side of each standard H-bridge cell. These modified H-bridge cells are referred to as qZSId cells hereinafter. Each phase of the qZSId-CHB converter is made up of m qZSId cells ($n = 2m + 1$). The qZSId cells exhibit two distinct categories of operating modes:

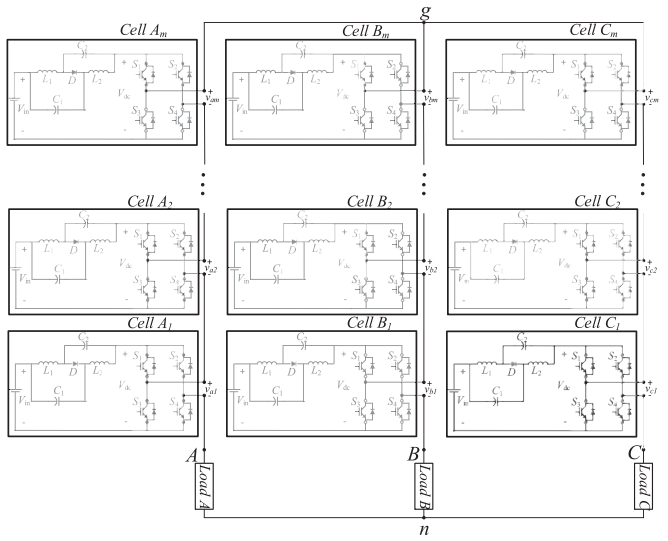

Fig. 1. Three-phase *n*-level qZSId-CHB converter with *m* series connected H-bridge cells in each phase.

Nonshoot-through operating modes and shoot-through operating modes. When a qZSd cell is in a nonshoot-through mode, it operates similar to a conventional H-bridge cell while also boosting the input voltage to its H-bridge stage to [18]

$$V_{\rm dc} = B \times V_{\rm in} = \frac{1}{1-2D} \times V_{\rm in} \tag{1}$$

where D is the shoot-through duty ratio, B is the boost factor of the qZSId network, $V_{\rm in}$ is the input voltage to the qZSId cell, and $V_{\rm dc}$ is the input voltage to the H-bridge stage of the qZSId cell (see Fig. 1). When a qZSId cell is in a shoot-through mode, the input terminal to the H-bridge stage is short circuited, rendering the value of $V_{\rm dc}$ to zero.

In a shoot-through mode, the output terminal voltage of the qZSId cell is always equal to zero. However, in a nonshoot-through mode, the output terminal voltage can be equal to $V_{\rm dc}$, 0, or $-V_{\rm dc}$ based on the status of conduction of the switches in the H-bridge stage. Therefore, due to the series connection of m qZSId cells in each phase of the qZSId-CHB converter, the following n voltage levels can be generated by each phase of the converter: $-mV_{\rm dc}, \ldots, -V_{\rm dc}, 0, V_{\rm dc}, \ldots, mV_{\rm dc}$ [20].

B. Modulation Method

A large variety of modulation methods for multilevel converters have been discussed in the literature throughout the last decade [43], [44]. Several of these methods can be employed to control the proposed qZSId-CHB converter [21], [45]. However, a certain carrier-based PWM method, called phase-shifted PWM [43], is very well suited to implement the proposed fault-tolerant strategy in this paper [34]. For the purpose of this work, the PS-PWM method is modified slightly to generate shoot-through switching states in addition to traditional nonshoot-through states. Fig. 2 illustrates the switching logic of the modified PS-PWM technique for one of the qZSId cells in the qZSId-CHB converter.

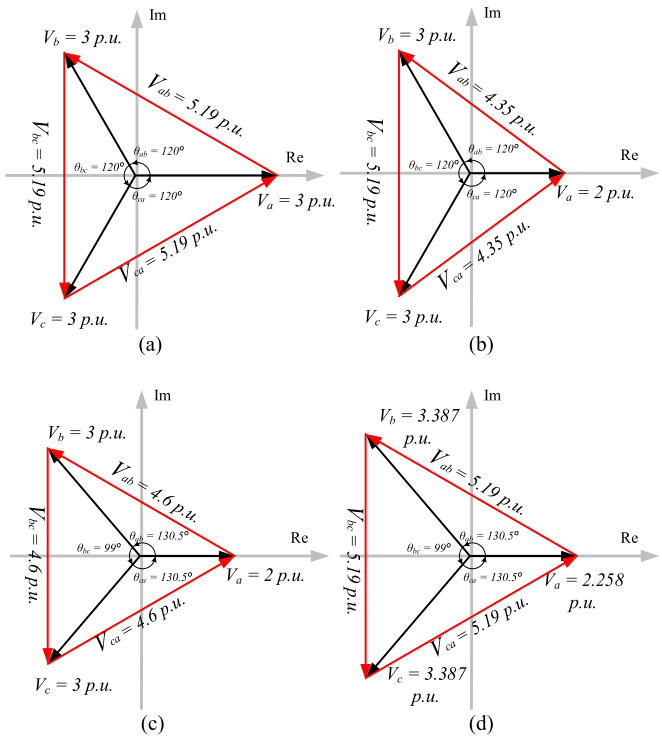

Fig. 2. Phasor diagram of phase voltages in a qZSId-CHB converter. (a) Healthy operation. (b) Faulty condition in which the faulty cell is bypassed and the line-to-line voltages are unbalanced. (c) Phase angles are modified according to the FPSC strategy to generate balanced line-to-line voltages with less voltage reduction. (d) Voltage gain is modified by changing the shoot-through ratio to compensate for the line-to-line voltage reduction in the postfault condition.

The traditional PS-PWM uses two carrier signals with 180° phase shift for each H-bridge cell in a CHB converter (c_i and c_i' in [14, Fig. 6]) [19]. The relative phase angle of carrier signals for each phase of the converter depends on the number of H-bridge cells in each phase [14]

$$\begin{cases} \theta_{\mathrm{ci}} = (i-1) \times \dfrac{360}{2m} \\ \theta_{c'i} = \theta_{\mathrm{ci}} + 180 \end{cases}, \qquad i = 1, 2, 3, \ldots, m. \tag{2}$$

A sinusoidal reference signal (m_j) is compared with the two carrier signals associated with each H-bridge cell in a converter phase and the switching signals for the H-bridge switches are generated accordingly. To generate the shoot-through states using the modified PS-PWM technique, a new shoot-trough signal with amplitude of $1-D$ is introduced to the switching logic. This new signal is represented as a cyan line in [14, Fig. 6]. Also, the switching logic is modified so that whenever the carrier signal is smaller than the shoot-through signal, the H-bridge stage in the corresponding qZSId cell is short circuited by its switches. The generated shoot-through states are depicted as shaded areas in [14, Fig. 6].

C. Minimizing Voltage Stress on Switches

In a typical ZSC inverter, the amplitude of the generated voltages can be increased by increasing the duration of the shoot-through states. However, increasing the shoot-through leads to an increase in the output voltage of the ZSI circuitry (the V_{dc} in Fig. 1) [10]. This dc-link voltage is the voltage stress that the inverter switches need to tolerate. Therefore, when increasing the amplitude of the generated voltages using shoot-through states, it is essential to ensure that the amplitude of the dc-link voltage does not exceed the stress rating of the switches [38]. Additionally, increasing the dc-link voltage results in a significant increase in the current of the inductors in a ZSI network [18]. As such, for any operating point, it is desirable to minimize the dc-link voltage and achieve the required output voltage level by increasing the modulation index rather than the shoot-through.

In the qZSId cell of Fig. 1, the dc-link voltage is equal to BV_{in}, and the upper limit of the dc-link voltage is the voltage stress rating of the H-bridge switches (V_{BN})

$$BV_{\mathrm{in}} \le V_{\mathrm{BN}}. \tag{3}$$

Therefore, the maximum boost factor allowed is equal to $V_{\mathrm{BN}}/V_{\mathrm{in}}$. As a result, the maximum allowed shoot-through is equal to

$$D_{\max} = \left(\left(\frac{V_{\mathrm{BN}}}{V_{\mathrm{in}}}\right) - 1\right) \Big/ \left(\frac{2V_{\mathrm{BN}}}{V_{\mathrm{in}}}\right). \tag{4}$$

This gives a hard upper limit on the amount of shoot-through that the proposed method can generate.

To minimize the dc-link voltage for any inverter voltage gain (G), the amount of shoot-through needs to be minimized, while the modulation index is maximized. The modulation index (M) is always greater than zero and less than ($1-D$). To maximize the modulation index and to minimize the shoot-through ratio, the shoot-through ratio must be equal to $1-M$. According to the formulations for a qZSId circuit [18]

$$G = B_{\min} \times M_{\max} = \frac{1}{1-2D_{\min}} \times (1 - D_{\min}). \tag{5}$$

By careful inspection of (5), one can realize the minimized shoot-through is

$$D_{\min} = \frac{G-1}{2G-1} \tag{6}$$

while the maximized modulation index will be equal to

$$M_{\max} = 1 - D_{\min}. \tag{7}$$

The results in (6) and (7) will be used as the basis for balancing the shoot-thorough versus modulation index by the proposed method whenever necessary.

III. Fault-Tolerant Strategy

The problem of detecting a fault, finding the location, and then taking appropriate action is the basis of fault-tolerant control. Fortunately, many fault detection methods have been proposed over the last few years [46]. However, the main challenge in this paper is limited to take appropriate action after fault diagnosis. In this paper, it is assumed that the type and location of the fault has been detected by the proposed method in [46]. In this section, a fault-tolerant strategy for a qZSId-CHB converter based

on FPSC technique is proposed. The proposed fault-tolerant strategy combines the voltage gain flexibility provided by the qZSId-cells with the phase-shifting property of the FPSC technique to fully recover the converter operation upon occurrence of single or multiple faults on inverter switches. The proposed fault-tolerant strategy works in two stages to compensate for the faulty switches in the inverter. The first stage involves bypassing the faulty cells, while the second stage involves applying the FPSC technique to recover the amplitude and balance the phase angles of the inverter voltages.

In case there are one or more faulty switches in a qZSId-CHB converter, based on the fault type and the location of the faulty switches, the faulty qZSId-cells fail to generate all of the previously mentioned feasible output terminal voltage levels in a nonshoot-through mode ($V_{\rm dc}$, 0, $-V_{\rm dc}$). As a result, the inverter phases with faulty cells can no longer generate phase voltages that are symmetric around the zero-volt level. Therefore, the faulty phases of the inverter start generating unbalanced phase voltages that contain dc offset components. In its first stage of operation, the proposed method bypasses all of the faulty qZSId-cells to prevent generation of the dc offset by making the phase voltages symmetric around zero-volt level. However, in this condition, the amplitude of the voltages generated by all three phases of the converter is no longer equal. The phases with bypassed cells can no longer generate all of the voltage levels, and thus, the amplitude of the voltages generated by these phases will be less than that of the healthy phases. For instance, in a seven-level qZSId-CHB converter with one faulty cell, the healthy phases can generate voltages with a maximum amplitude of $3V_{\rm dc}$ (3 p.u.), while the faulty phase can only generate a voltage with a maximum amplitude of $2V_{\rm dc}$ (2 p.u.). This leads to generation of unbalanced inverter line-to-line voltages. The phasor diagram of Fig. 2(a) and (b) elaborates on the operation of a seven-level converter before and after occurrence of a fault. According to Fig. 2(b), after bypassing the faulty phase, the amplitude of $V_{\rm bc}$ is equal to 5.19 p.u., while the amplitude of $V_{\rm ab}$ and $V_{\rm ca}$ is equal to 4.35 p.u. To fully recover the converter operation, the line-to-line voltages need to be both balanced and have the same amplitude as the voltages in a healthy inverter.

To balance and increase the voltage amplitudes to the prefault condition, it is easy to come up with the simple idea of increasing the voltage gain of the faulty phases by increasing their associated shoot-through levels. However, this simple idea comes with two major drawbacks: by increasing the shoot-through in the faulty phases, the voltage stress on all of remaining healthy switches in the faulty phases increases significantly, leading to a higher possibility of a subsequent fault in the already faulty phases; additionally, the current of the inductors on all remaining healthy cells in the faulty phase increases considerably as well. In the previously mentioned seven-level qZSId-CHB converter with one faulty cell, to fully recover the converter operation by increasing the shoot-through of the faulty phase, the voltage gain of the faulty phase will be increased for a 1.5 factor resulting to a considerable increase in voltage stress over the healthy switches in this phase. As a result, rather than only increasing the shoot-through of the faulty cells, the proposed fault-tolerant strategy employs the FPSC technique to evenly distribute the rise of voltage stress between all of the inverter switches.

The conventional FPSC technique is discussed in [41]. The FPSC technique modifies the phase angles of the inverter phase voltages ($\theta_{\rm ab}$, $\theta_{\rm bc}$, $\theta_{\rm ca}$ in Fig. 2) to generate balanced line-to-line voltages. Fig. 2(c) demonstrates how modifying the phase angles of inverter voltages can lead to balanced line-to-line voltages for a seven-level qZSId-CHB converter with one bypassed faulty cell. According to this figure, although the amplitudes of the phase voltages ($V_{\rm b}$, $V_{\rm c}$) are not equal, by properly adjusting the phase angles ($\theta_{\rm ab}$, $\theta_{\rm bc}$, $\theta_{\rm ca}$), the amplitudes of the line-to-line voltages ($V_{\rm ab}$, $V_{\rm bc}$, $V_{\rm ca}$) are made all equal (4.6 p.u.). The phase angles that result in balanced line-to-line voltages can be found by solving the following set of equations for $\theta_{\rm ab}$, $\theta_{\rm bc}$, and $\theta_{\rm ca}$ [41]

$$\begin{cases} V_{\rm a}^2 + V_{\rm b}^2 - 2V_{\rm a}V_{\rm b}\cos(\theta_{\rm ab}) \\ \qquad = V_{\rm b}^2 + V_{\rm c}^2 - 2V_{\rm b}V_{\rm c}\cos(\theta_{\rm bc}) \\ V_{\rm b}^2 + V_{\rm c}^2 - 2V_{\rm b}V_{\rm c}\cos(\theta_{\rm bc}) \\ \qquad = V_{\rm c}^2 + V_{\rm a}^2 - 2V_{\rm c}V_{\rm a}\cos(\theta_{\rm ca}) \\ \theta_{\rm ab} + \theta_{\rm bc} + \theta_{\rm ca} = 360^\circ \end{cases} \tag{8}$$

where $\theta_{\rm ab}$, $\theta_{\rm bc}$, and $\theta_{\rm ca}$ are the modified phase shifts between phase voltages and V_a, V_b, and V_c are the amplitude of the phase voltages after bypassing the faulty cells. For instance, in case of the previously mentioned seven-level qZSId-CHB converter with one bypassed cell (assuming the bypassed phases is phase "a"), substituting $V_a = 2$ p.u. and $V_b = V_c = 3$ p.u. in (8) yields $\theta_{\rm ab}, = \theta_{\rm ca} = 130.5^\circ$ and $\theta_{ba} = 99^\circ$. Therefore, for generating balanced line-to-line voltages, the phase shifts between phase voltages should be adjusted according to the obtained values. The phase angles of the inverter phase voltages can be easily adjusted in PS-PWM through adjusting the phase angles of the sinusoidal reference signals (m_j in [14, Fig. 6]).

Although by applying the FPSC technique to a qZSId-CHB converter with faulty cells, balanced line-to-line voltages can be generated, however, the converter operation is not fully recovered because the amplitudes of the generated line-to-line voltages are less than those of a healthy converter. In the seven-level qZSId-CHB converter of above, for instance, according to Fig. 2(a), the amplitude of the line-to-line voltages before fault occurrence is equal to 5.19 p.u.; however, after application of the FPSC, the amplitude of the line-to-line voltages is reduced to 4.6 p.u. The proposed method in this work leverages the flexibility provided by the shoot-through states in a qZSId circuit to fully recover the amplitude of the line-to-line voltages to their prefault condition. To recover the line-to-line voltages, the proposed method increases the postfault inverter voltage gain ($G_{\rm fault}$) to

$$G_{\rm fault} = \frac{G_{\text{pre-fault}}}{K_G} \tag{9}$$

where $G_{\text{pre-fault}}$ is the inverter voltage gain before fault occurrence and K_G is a performance reduction factor found from

$$K_G = \frac{|V_{\rm LL}|_{\rm fault}}{|V_{\rm LL}|_{\text{pre-fault}}}. \tag{10}$$

In (10), $|V_{\rm LL}|_{\rm fault}$ and $|V_{\rm LL}|_{\rm pre\text{-}fault}$ are the amplitudes of the line-to-line voltages of the inverter post- and prefault conditions, respectively. For the seven-level qZSId-CHB converter of above, $|V_{\rm LL}|_{\rm pre\text{-}fault} = 5.19\,{\rm p.u.}$ and $|V_{\rm LL}|_{\rm fault} = 4.6\,{\rm p.u.}$ which results in a performance reduction factor of $K_G = 0.885$. According to (9), this means that the inverter voltage gain should be increased by a factor of $K_G^{-1} = 1.129$ after applying the FPSC in order to fully recover the inverter operation. The resulting phasor diagram for this postfault condition is shown in Fig. 2(d). Comparing Fig. 2(a) with Fig. 2(d) clearly demonstrates that in the postfault condition, by applying the proposed method, despite having unbalanced phase voltages, the inverter line-to-line voltages are fully recovered to their prefault condition. It is worth mentioning that typically the correct line-to-line voltages fully satisfy the requirements of the load and result in uninterrupted operation of the inverter system.

As mentioned in Section II, for any operating point of the inverter, the shoot-through (and thus the voltage stress of the switches) should be minimized while modulation index is maximized. The minimum shoot-through that will result in the required postfault gain ($G_{\rm fault}$) can be found from (6)

$$D_{\rm fault,min} = \frac{G_{\rm fault} - 1}{2G_{\rm fault} - 1} \tag{11}$$

while the modulation index in this condition can be calculated from (7)

$$M_{\rm fault,max} = 1 - D_{\rm fault,min}. \tag{12}$$

Finally, the value of $D_{\rm fault,min}$ from (11) is compared to the upper limit $D_{\rm max}$ in (4) to make sure the switches will not get damaged in the postfault condition. As long as the $D_{\rm fault,min}$ is found to be less than $D_{\rm max}$, the proposed method can fully recover the converter operation regardless of the type and place of the faults.

As mentioned earlier, one advantage of the proposed method is that rather than only increasing the shoot-through of the faulty cells and thus increasing the voltage stress of the switches considerably in the faulty phases, it evenly increases the voltage stress on all inverter switches for a small amount. In the previously mentioned seven-level qZSId-CHB converter with one faulty cell, to fully recover the converter operation by only increasing the shoot-through of the faulty phase, the voltage gain of two remaining cells must be increased by a 1.5 factor. Assuming the converter is operating with $M = 0.85$ and $D = 0.15$, using (1) and (5), the boost factor and the voltage gain in normal operation are found as $B = 1.42$ and $G = 1.21$. As mentioned, after fault occurrence, the voltage gain on remaining cells needs to be increased to $G_{\rm fault} = 1.5 \times 1.21 = 1.82$, which results in $D_{\rm fault} = 0.31$ and $B_{\rm fault} = 2.64$. Therefore, the voltage stress on the switches in the faulty phase is increased for a factor of $B_{\rm fault}/B = 1.85$. In the other words, the voltage stress on the switches in the faulty phase increases for 85%, but it remains the same for the switches in the healthy phases. In contrast, using the proposed fault-tolerant strategy, the voltage gain of all of the healthy cells of the inverter increases by a factor $K_G^{-1} = 1.129$. Following the same calculations as before using 1.129 for voltage gain, it can be concluded that the voltage stress on the inverter switches increases for only 20% in this condition. This greatly reduces the possibility of a subsequent fault in the already faulty inverter.

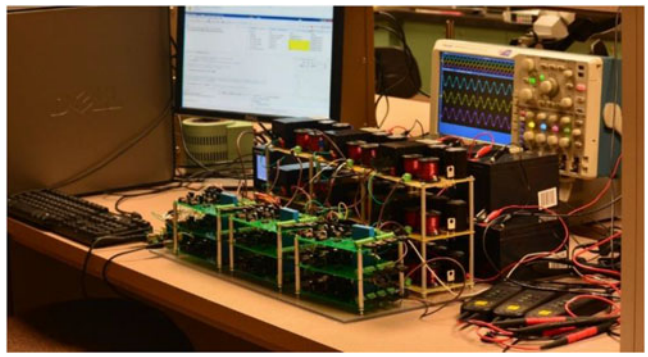

Fig. 3. Prototype three-phase seven-level qZSId-CHB converter and 12-V batteries.

IV. Experimental Results

This section provides experimental results generated through utilizing the proposed fault-tolerant strategy to restore the operation of a prototype seven-level qZSId-CHB converter to the prefault conditions, in case of three different fault scenarios. The experimental setup is shown in Fig. 3.

In this setup, the input side of each Z-Source network is connected to a 12-V battery and the output side is connected to the dc-link terminal of each H-bridge cell. The power semiconductor devices used in this prototype are power MOSFETs with drain-to-source voltage rating of 100 V ($V_{\rm BN} = 100$). The Z-source components are $C_1 = C_2 = 2200\ \mu$F, and $L_1 = L_2 = 500\ \mu$H. The output terminals of the qZSId-CHB converter are connected to a three-phase inductive load with a 0.9 power factor assembled using a 7-Ω resistor in series with a 1.2-mH inductor in each phase. The proposed method was implemented using the TMS320F28335 digital signal processor. In the operating point used for generating the results ($V_{\rm load} = 44$ V, $I_{\rm load} = 6$ A), in order to minimize the voltage stress on the switches, the modulation index and the shoot-through ratio are set to 0.85 and 0.15, respectively. By substituting these values in (5), the voltage gain in normal operation ($G_{\rm Pre\text{-}fault}$) is found as 1.21. The fundamental and switching frequencies of the PS-PWM method are 50 Hz, and 2 kHz, respectively. The phase voltages, line-to-line voltages, load voltages, and the dc-link voltage of one H-bridge cell of the inverter for the prefault condition are shown in Fig. 4. According to Fig. 4, in this operating point, the amplitudes of phase voltages, line-to-line voltages, load voltages, and the dc-link voltage of each H-bridge cell are equal to 44, 76, 44, and 17 V, respectively. The THD of the load voltages in this condition is calculated as 9.5%.

The first experiment analyzes the occurrence of a single fault in phase "*b*." In this case, the faulty cell is bypassed at the first step. Therefore, the number of operative cells in phase "*b*" is reduced to two cells ($V_b = 2$ p.u., $V_a = V_c = 3$ p.u.). In this condition, to generate balanced line-to-line voltages, based on (8), the phase shifts between the inverter phase voltages need to

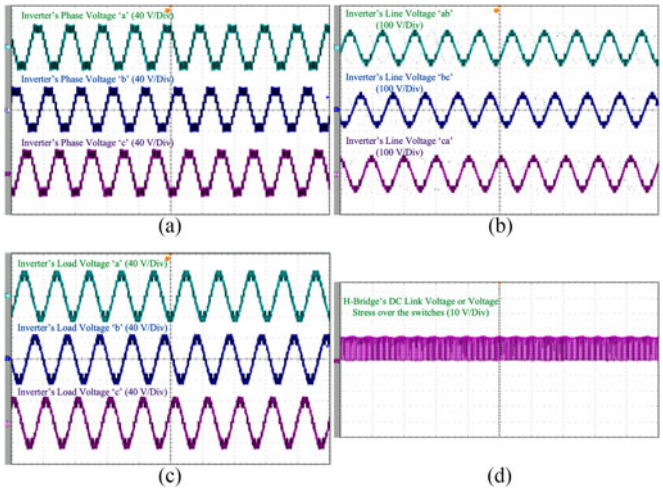

Fig. 4. qZSId-CHB's voltages in normal operating condition. (a) Inverter's phase voltages. (b) Line-to-line voltages. (c) Load voltages. (d) DC-link voltage of one H-Bridge cell (the voltage across H-Bridge's switches).

be adjusted to $\theta_{\rm bc} = \theta_{\rm ab} = 130.5^\circ$. The performance reduction factor (K_G) and the voltage gain in the faulty condition ($G_{\rm fault}$) in this experiment are calculated from (9) and (10) as 0.885 and 1.37, respectively. Subsequently, the new modulation index and shoot-through ratio that compensate the loss of one operative cell in phase "b," while keeping the voltage stress across the switches at minimum can be calculated from (6). These parameters (M and D) are found to be equal to 0.78 and 0.22, respectively. The calculated shoot-through ratio is checked against the maximum applicable shoot-through ratio found from (4) as $D_{\max} = 0.44$ to make sure the voltage stress will not exceed the limitations of the switches as a result of implementing the proposed fault-tolerant strategy. The new values of M and D along with the adjusted phase shifts are used by the PS-PWM algorithm to generate modified switching commands to restore the operation of the converter to the prefault conditions.

The generated phase voltages of the converter during the normal operation ($t \le t_0$), the fault recovery period ($t_0 \le t \le t_1$), and the postfault operation ($t \ge t_1$) are shown in Fig. 5(a). Due to the inferior quality of the waveforms in this scope shot, the actual raw data from the oscilloscope were exported to MATLAB to generate Fig. 5(a). As pictured in Fig. 5(a), during the normal operation ($t \le t_0$), the phase voltages reach all seven levels; however, during the fault recovery period ($t_0 \le t \le t_1$) and upon bypassing the faulty cell in phase "b," this phase only generates five voltage levels. In this condition, the amplitude of the phase "b" voltage is equal to 35.1 V, while the amplitude of the voltages in the healthy phases "a" and "c" are equal to 52.55 and 52.6 V, respectively.

According to the readings provided in Fig. 5(a) for the waveforms in the postfault condition, the phase shifts between the waveforms are accurately adjusted to the intended values of $\theta_{\rm bc} = \theta_{\rm ab} = \alpha = 130.5^\circ$ by the proposed strategy. To verify generation of balanced line-to-line voltages, the raw data from Fig. 5(b) were imported to MATLAB to plot Fig. 5(b). According to this figure, the amplitudes of the line-to-line

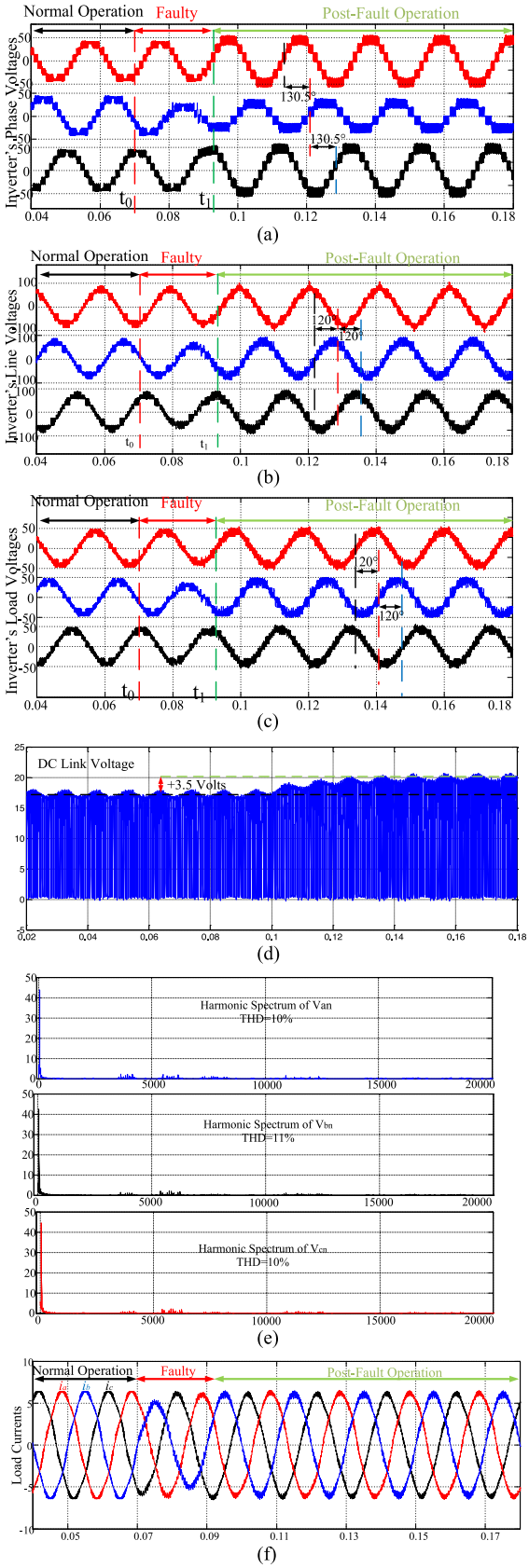

Fig. 5. qZSId-CHB voltages in the event of a faulty switch in phase "b" (first experiment). (a) Inverter's phase voltages. (b) Line-to-line voltages. (c) Load voltages. (d) DC-link voltage of one H-bridge cell. (e) Harmonic spectrum of the load voltages. (f) Load currents.

voltages are all equal to 76.5 V, and the phase shifts between these voltages are also all equal to 120°. This confirms the validity of the proposed fault-tolerant strategy for generating balanced line-to-line voltages in the event of a bypassed faulty H-bridge. The waveforms plotted in Fig. 5(c) confirm generation of balanced load voltages in the postfault condition as well. Fig. 5(d) shows the dc-link voltage of one of the H-bridge power cells during this experiment. According to this figure, the value of the dc-link voltages is increased for only 3.5 V in the postfault condition. The harmonic spectrums of the load voltage for the postfault condition is shown in Fig. 5(e). The THDs of the load voltages are calculated using the data imported from the oscilloscope as 10%, 11%, and 10% for the $V_{\rm an}$, $V_{\rm bn}$, and $V_{\rm cn}$, respectively. This shows a negligible increase of THD in the postfault condition. Finally, the load currents in the event of a single faulty phase are given in Fig. 5(f). As it can be seen, the amplitude of the current in the postfault operation of the inverter is equal to the amplitude of this current in normal operation of the inverter. However, the THD of the current is slightly increased in the postfault operation. The current THD is increased from 2.9% to 3.3% due to fault occurrence.

The second experiment analyzes the case of two faulty switches: one in phase "b" and another one in phase "c." In this condition, the phase shifts of the inverter phase voltages need to be adjusted to $\theta_{\rm ab} = \theta_{\rm ca} = \alpha = 101.5°$. To emulate the fault condition, one switch in phase "b" and another one in phase "c" were manually short circuited at $t = t_0$. The faulty H-bridge cells were bypassed, and the fault-tolerant strategy was triggered at $t = t_1$. The generated voltage waveforms for this experiment are shown in Fig. 6. According to Fig. 6(a), in the fault recovery period, the amplitude of the phase "a" voltage is equal to 60.58 V, while the amplitudes of the voltages in the other two phases are reduced to 41.1 and 41.2 V. Similar to before, upon triggering the proposed fault-tolerant strategy, the phase shifts between the waveforms are accurately adjusted to $\theta_{\rm ab} = \theta_{\rm ca} = \alpha = 101.5°$. Consequently, balanced line-to-line voltages with equal amplitudes of 76 V and phase shift of 120° were generated. The THDs of load voltage are calculated in this experiment as 11%, 12%, and 12% for the $V_{\rm an}$, $V_{\rm bn}$, and $V_{\rm cn}$, respectively. The third experiment analyzes the occurrence of multiple faults in one phase of the converter. In this experiment, two switches in phase "b" are manually short circuited to emulate the fault condition. In this case, the phase shifts of the inverter phase voltages need to be adjusted to $\theta_{\rm ab} = \theta_{\rm bc} = \alpha = 140°$. Similar to the previous experiments, the fault-tolerant strategy bypasses the faulty cells and modifies the phase angles and shoot-through ratio to generate balanced line-to-line voltages. The generated voltage waveforms for this experiment are shown in Fig. 7.

V. Conclusion

In this paper, a new fault-tolerant strategy for improving the performance of a qZSId-CHB converter under faulty condition was proposed. Using the proposed method, only the faulty qZSId cell was bypassed and the remaining healthy cells were remained operative to use the maximum capacity of the converter. By adopting the FPSC method, instead of just increasing

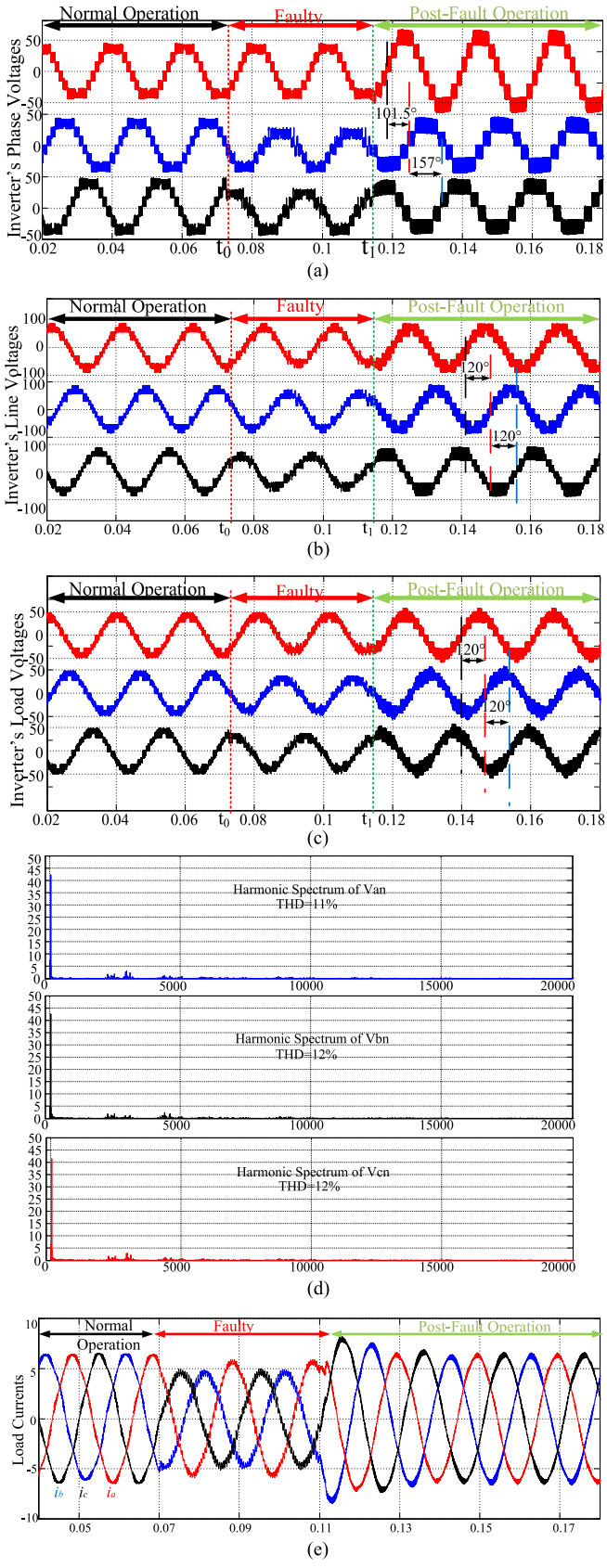

Fig. 6. qZSId-CHB voltages in the event of a faulty switch in phase "b" and another faulty switch in phase "c" (second experiment). (a) Inverter's phase voltages. (b) Line-to-line voltages. (c) Load voltages. (d) Harmonic spectrum of the load voltages. (f) Load currents.

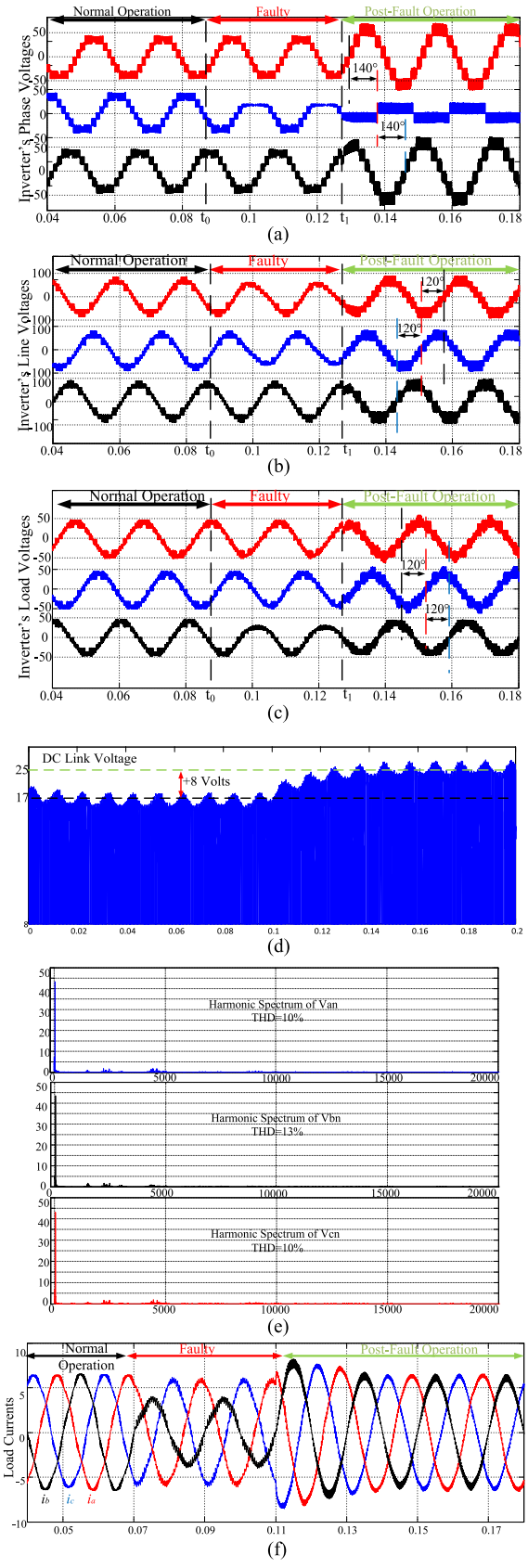

Fig. 7. qZSId-CHB voltages in the event of two faulty switches in phase "b" (third experiment). (a) Inverter's phase voltages. (b) Line-to-line voltages. (c) Load voltages. (d) DC-link voltage of one H-bridge cell. (e) Harmonic spectrum of the load voltages. (f) Load currents.

the voltage gain in the faulty phase, the voltage gain of all the operative cells were increased evenly to minimize the voltage stress over the healthy switches. The proposed strategy can be easily implemented on any multilevel inverter with an incorporated Z-source network without limitation on the topology or the number of inverter voltage levels.

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