A Class-E Power Amplifier Design Considering MOSFET Nonlinear Drain-to-Source and Nonlinear Gate-to-Drain Capacitances at Any Grading Coefficient

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***Abstract*—This paper presents theory and analysis for class-E power amplifier considering MOSFET nonlinear gate-to-drain and nonlinear drain-to-source capacitances at any grading coefficient of the MOSFET body junction diode. The nonlinearity degree of a MOSFET parasitic capacitance is determined by the grading coefficient. When the grading coefficient is not considered in design procedure, the switch voltage waveform of the class-E power amplifier does not satisfy the switching conditions, which results in a decrease of the power conversion efficiency. Therefore, the grading coefficient is an important parameter to satisfy the class-E zero-voltage switching (ZVS) and zero-derivative switching (ZDS) conditions. The MOSFET gate-to-drain capacitance is highly nonlinear, and it is more nonlinear than drain-to-source capacitance for most MOSFETs. In some cases, the change in the gate-to-drain capacitance can be as large as 100 times. The results show that this nonlinearity affects the class-E power amplifier properties, such as switch voltage, power output capability, and maximum switch voltage. Therefore, it is necessary to consider the nonlinearity of the gate-to-drain capacitance, along with the drain-to-source capacitance. A design example at 4 MHz operating frequency is also given to describe the design procedure. The ZVS and ZDS conditions are achieved in the obtained switch voltage. The circuit simulation was performed using PSpice software. For verification of the presented theory, a class-E power amplifier is fabricated. The measured results are verified with simulation and theory results.**

***Index Terms*—Class-E power amplifier, MOSFET parasitic capacitances, nonlinear gate-to-drain capacitance, nonlinear drain-to-source capacitance, zero-voltage switching (ZVS) and zero-derivative switching (ZDS) conditions.**

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I. Introduction

ONE of the most important switching mode power amplifiers is the class-E amplifier, which is being used in power electronics and radio-frequency applications [1], [2]. In principle, the class-E amplifier efficiency can approach 100%. The ZVS and ZDS conditions are essential for the class-E power amplifier to achieve zero switching loss, low noise, and high efficiency at high frequencies [3]–[7]. ZVS and ZDS conditions are also essential for several applications, such as class DE amplifiers [8], [9], dc–dc power converters [10], [11], class-E rectifiers [12], and many power electronics amplifiers.

Recently, several analyses have been performed on the class-E power amplifier, considering the MOSFET parasitic capacitances [13]–[24]. As the operating frequency increases, the analysis of the class-E amplifier with a nonlinear shunt capacitance becomes more interesting [17]. The shunt capacitance is necessary to satisfy the class-E ZVS and ZDS conditions [13]. However, the shunt capacitance includes the MOSFET nonlinear drain-to-source capacitance ($C_{\rm ds}$) and an external output parallel linear capacitance [18]. Several approaches have mentioned the necessity of considering MOSFET nonlinear drain-to-source capacitance and also have tried to apply this capacitance to their analyses [7], [13]–[24]. However, the drain-to-source capacitance is not the only parasitic capacitance. Also some approaches have suggested that it is important to consider the gate-to-drain parasitic capacitance ($C_{\rm gd}$) [7], [13], [19]–[22]. In [20], the effect of linear $C_{\rm gd}$ is investigated on the output current and the output power, while the other parameters of class-E power amplifier are not considered. The effect of linear $C_{\rm gd}$ is also considered in [21], but the switch voltage is approximated for the sake of simplicity. In [19]–[21], the MOSFET drain-to-source parasitic capacitance is assumed linear, which leads to a deficient analysis of the class-E power amplifier. Both linear gate-to-drain and nonlinear drain-to-source capacitances have been assumed in some studies [13], [22]. However, in fact, the gate-to-drain capacitance is a nonlinear function of voltage, while its nonlinearity has not been considered in aforementioned investigations.

The gate-to-drain capacitance is the most important parasitic element because it provides a feedback between output and input of the circuit. It is also called the Miller's capacitance because it makes the total dynamic input capacitance to become greater than the sum of the static capacitances [25], [26]. The

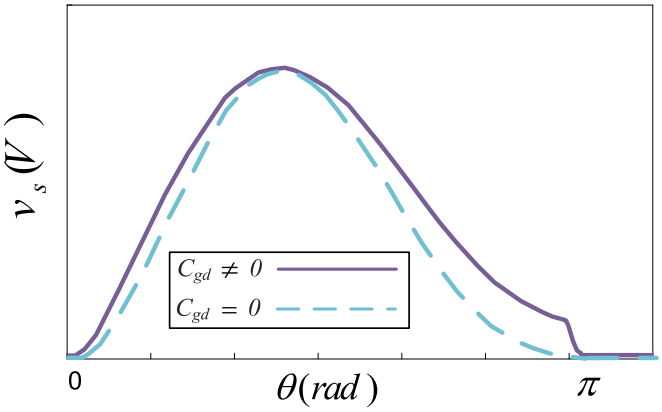

Fig. 1. Simulated switch voltage waveform of class-E power amplifier with the obtained values from the design equations in [24].

nonlinearity degree of a MOSFET parasitic capacitance is determined by grading coefficient. The range of the grading coefficient of real MOSFETs is wide. Therefore, it is important to obtain the design equations for the class-E power amplifier at any grading coefficient [23]. Inspection of over than 150 SPICE MOSFET models, shows $C_{\rm gd}$ and $C_{\rm ds}$ grading coefficients typically range from 0.3 to 0.9. The grading coefficient of nonlinear $C_{\rm gd}$ (m_2) is larger than that of nonlinear $C_{\rm ds}$ (m_1) in most of the investigated models. This fact confirms that the nonlinearity of $C_{\rm gd}$ is higher than that of $C_{\rm ds}$ for most MOSFETs.

Ignoring the MOSFET gate-to-drain capacitance in the class-E power amplifier design results in occurrence of errors on the switch voltage waveform because the actual MOSFET has nonlinear gate-to-drain capacitance. For instance, a simulated switch voltage waveform, obtained by using the same component values in [24] is shown in Fig. 1. According to this figure, when the MOSFET gate-to-drain capacitance is not considered, the class-E ZVS/ZDS conditions will be achieved, while if the MOSFET gate-to-drain capacitance is assumed in the PSpice model, the ZVS/ZDS conditions will no longer be satisfied. The experimental results in [24] confirm the fact that neglecting the gate-to-drain capacitance may result in design failure of class-E power amplifier.

To the best knowledge of the authors, the nonlinear effect of MOSFET gate-to-drain capacitance has not been considered in any analysis of the class-E power amplifier, while the actual MOSFET includes a high nonlinear gate-to-drain parasitic capacitance. However, these parameters should be considered in the design of a practical class-E power amplifier to achieve a more accurate result. In this paper, the MOSFET nonlinear gate-to-drain and drain-to-source capacitances at any grading coefficients of m_1 and m_2 are considered in the analysis of the class-E power amplifier. PSpice simulation and experimental results are also given to verify theory analysis.

II. MOSFET Parasitic Capacitances

According to the IRF530 MOSFET data sheet, the typical values of input ($C_{\rm iss}$), output ($C_{\rm oss}$) and reverse transfer ($C_{\rm rss}$) capacitances [28] are shown in Fig. 2(a). These values are obtained at $v_{\rm gs} = 0$ V and $f = 1$ MHz which are relative to the

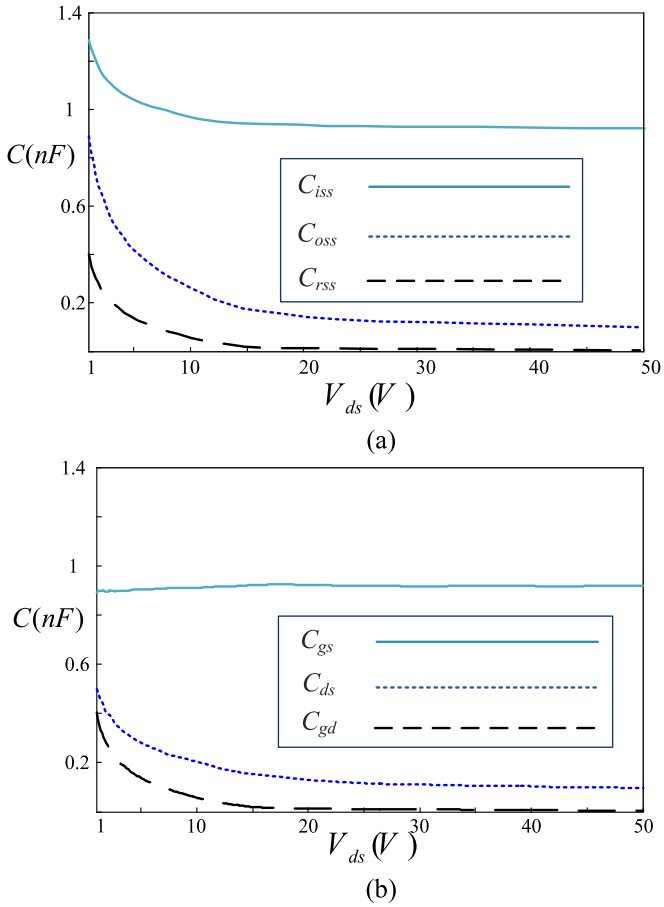

Fig. 2. Typical values of IRF530 MOSFET capacitances according to the data sheet. (a) Values of input ($C_{\rm iss}$), output ($C_{\rm oss}$), and reverse transfer ($C_{\rm rss}$) capacitances. (b) MOSFET parasitic drain-to-source ($C_{\rm ds}$), gate-to-drain ($C_{\rm gd}$), and gate-to-source ($C_{\rm gs}$) capacitances.

MOSFET parasitic capacitances as follows:

$$C_{\rm iss} = C_{\rm gs} + C_{\rm gd} \tag{1}$$

$$C_{\rm rss} = C_{\rm gd} \tag{2}$$

$$C_{\rm oss} = C_{\rm ds} + C_{\rm gd}. \tag{3}$$

The MOSFET parasitic capacitances are calculated according to (1)–(3), which are shown in Fig. 2(b). According to this figure, both the drain-to-source and the gate-to-drain capacitances are voltage dependent because they are affected by depletion layers within the device [29]. Therefore, the capacitance value changes depending on the voltage that appears across them. Also, it can be seen from the figure that the gate-to-drain capacitance is more nonlinear than the drain-to-source capacitance. In some cases, the change in $C_{\rm gd}$ can be as large as by a factor of 100 [26]. However, $C_{\rm gs}$ has only a small voltage change across it and consequently has a small capacitance change. Hence, it is considered as a linear capacitance in this paper.

The nonlinear drain-to-source capacitance can be expressed as [17]

$$C_{\rm ds} = \frac{C_{j01}}{(1 + v_s/V_{\rm bi1})^{m1}} \tag{4}$$

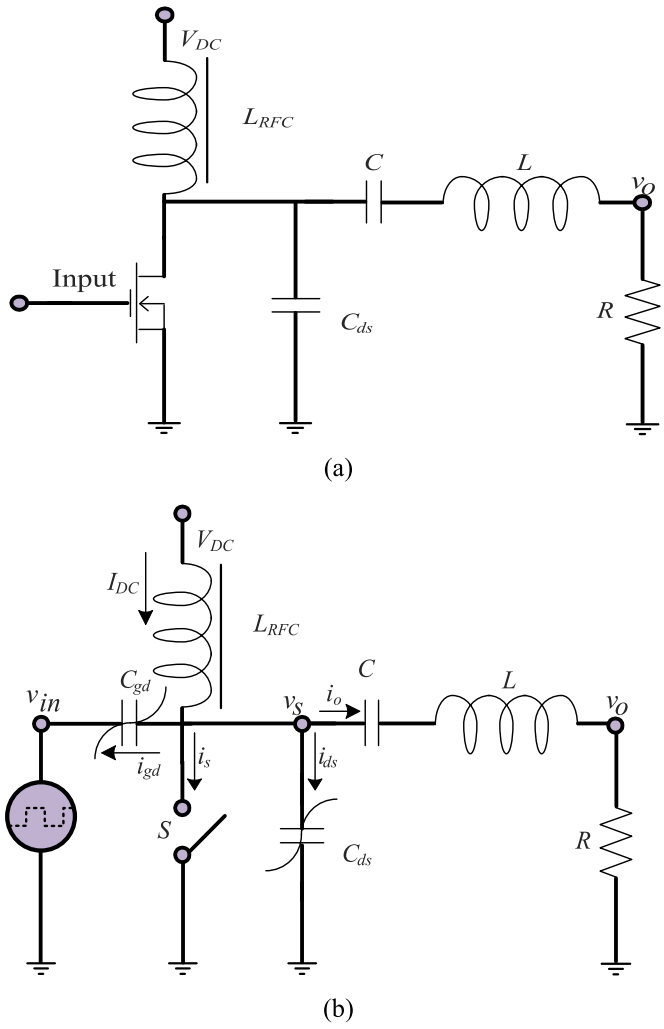

Fig. 3. Class-E power amplifier. (a) Typical circuit. (b) Equivalent circuit, used in the proposed paper to analyze.

where v_s is the switch voltage, C_{j01} is the drain-to-source capacitance at $v_s = 0$, and $V_{\rm bi1}$ is the built-in potential between drain and source. The gate-to-drain capacitance is also assumed nonlinear and can be expressed as follows [30]:

$$C_{\rm gd} = \frac{C_{j02}}{(1 + v_{\rm gd}/V_{\rm bi2})^{m2}} \tag{5}$$

where $v_{\rm gd}$ is the voltage across the gate-to-drain capacitance, C_{j02} is the initial gate-to-drain capacitance at $v_{\rm gd} = 0$, and $V_{\rm bi2}$ is built-in potential corresponding to $C_{\rm gd}$. The parameters m_1 and m_2 in (4) and (5) are the nonlinear $C_{\rm ds}$ and $C_{\rm gd}$ grading coefficients, respectively.

III. Analysis

A conventional class-E power amplifier structure is illustrated in Fig. 3(a), consisting of a MOSFET as a switch device, dc supply voltage ($V_{\rm dc}$), series inductor (L), series capacitor (C), shunt MOSFET parasitic capacitance ($C_{\rm ds}$) and a dc-feed inductance ($L_{\rm RFC}$). The resonant inductor can be divided into L_r and L_X, while L_r with C form an ideal filter to resonant at the operating frequency and the inductance L_X shifts the phase of the output current [13]. The class-E power amplifier equivalent circuit, used in the proposed paper is shown in Fig. 3(b). As seen in the figure, the MOSFET is modeled with a switch and two parasitic capacitances $C_{\rm gd}$ and $C_{\rm ds}$. The following assumptions are considered to derive design equations:

1) the duty cycle is constant and equal to 0.5;
2) $C_{\rm ds}$ and $C_{\rm gd}$ are considered as nonlinear capacitances;
3) the grading coefficients of MOSFET nonlinear drain-to-source and nonlinear gate-to-drain capacitances are not constant and considered as m_1 for $C_{\rm ds}$ and m_2 for $C_{\rm gd}$;
4) the only shunt capacitance is the MOSFET $C_{\rm ds}$ parasitic capacitance;
5) the gate-to-source voltage is considered to be square wave, which is zero during $0 \le \theta < \pi$ and equal to $V_{\rm in}$ at $\pi \le \theta < 2\pi$;
6) the on resistance of the MOSFET is zero while the off resistance is infinite, so the MOSFET works as an ideal switch;
7) the dc-feed inductance ($L_{\rm RFC}$) is large enough to ignore current ripples;
8) the output current is a pure sine wave at the operating frequency, due to large assumption of loaded quality factor (Q) of the output resonant circuit;
9) ZVS and ZDS conditions are satisfied, i.e., $v_s(\pi) = 0$ and $dv_s(\theta)/d\theta = 0$ at $\theta = \pi$.

A. Design Equations

The relation between the currents of feedback capacitance ($i_{\rm gd}$), dc feed inductance ($I_{\rm dc}$), load (i_o), and nonlinear shunt capacitance ($i_{\rm ds}$) can be obtained using a KCL node equation for the v_s node as follows:

$$I_{\rm dc} - i_o = i_{\rm ds} + i_{\rm gd} + i_s. \tag{6}$$

As mentioned in assumption 5), during the first half of the period, the gate-to-source voltage is zero. Hence, the switch is off and i_s is equal to zero. Due to the high value of Q (assumption 8), the output current is sinusoidal wave and assumed to be

$$i_o(\theta) = I_m \sin(\theta + \varphi) \tag{7}$$

where I_m is the output current amplitude, $\theta = \omega t$ represents the angular time, and φ is the phase shift between source voltage and the output current. The currents of the nonlinear capacitances can be obtained according to (4) and (5)

$$i_{\rm ds} = \omega C_{j01}(1 + v_s/V_{\rm bi1})^{-m1}\frac{dv_s}{d\theta} \tag{8}$$

$$i_{\rm gd} = \omega C_{j02}(1 + v_{\rm gd}/V_{\rm bi2})^{-m2}\frac{dv_s}{d\theta}. \tag{9}$$

According to equations (6)–(9), (6) can be rewritten as

$$I_{\rm DC} - I_m \sin(\theta + \varphi) = \omega(C_{j01}(1 + v_s/V_{\rm bi1})^{-m1} + C_{j02}(1 + v_{\rm gd}/V_{\rm bi2})^{-m2})\frac{dv_s}{d\theta}. \tag{10}$$

As mentioned in assumption 5), in the first half of the period, the gate-to-source voltage is zero. Therefore in this time interval the voltage across the drain to gate capacitance is the same as

the voltage across the drain-to-source capacitance. Integration from (10) leads to

$$\frac{\omega R C_{j01}}{(V_{\rm dc}/V_{\rm bi1})(1-m_1)}\left(1+\frac{v_s}{V_{\rm dc}}\times\frac{V_{\rm dc}}{V_{\rm bi1}}\right)^{1-m_1} + \frac{\omega R C_{j02}}{(V_{\rm dc}/V_{\rm bi2})(1-m_2)}\left(1+\frac{v_s}{V_{\rm dc}}\times\frac{V_{\rm dc}}{V_{\rm bi2}}\right)^{1-m_2} - \frac{R I_{\rm dc}\theta}{V_{\rm dc}} - \frac{R I_m}{V_{\rm dc}}(\cos(\theta+\varphi)-\cos(\varphi)) - \frac{\omega R C_{j01}}{(V_{\rm dc}/V_{\rm bi1})(1-m_1)} - \frac{\omega R C_{j02}}{(V_{\rm dc}/V_{\rm bi2})(1-m_2)} = 0. \quad (11)$$

According to assumption 9), the ZVS and ZDS conditions should be satisfied in (11). Applying the ZVS leads to

$$I_{\rm dc} = \frac{2 I_m \cos(\varphi)}{\pi} \quad (12)$$

while using the ZDS conditions in (10) gives another equation for dc current

$$I_{\rm dc} = -I_m \sin(\varphi). \quad (13)$$

Using (12) and (13), the value of φ can be obtained

$$\tan(\varphi) = -\frac{2}{\pi}. \quad (14)$$

As seen, the value of φ is constant and equal to -0.576 rad. This value will be changed, if the input voltage is assumed sinusoidal or if the gate resistance is considered in the analysis. However, in this paper, these conditions are not taken into account for the sake of simplicity, but the obtained equation can be recalculated for the mentioned conditions. The power relations can be calculated as follows, considering high efficiency for the amplifier:

$$P_o = P_{\rm dc} \quad (15)$$

where output power (P_o) and dc power ($P_{\rm dc}$) are defined as

$$P_o = \frac{R I_m^2}{2}. \quad (16)$$

and

$$P_{\rm dc} = V_{\rm dc} \times I_{\rm dc}. \quad (17)$$

According to (12) and (15)–(17), the output current amplitude can be written as

$$I_m = \frac{4 V_{\rm dc}\cos(\varphi)}{\pi R}. \quad (18)$$

Using (16) and (18), the output power can be obtained as follows:

$$P_o = \frac{8 V_{\rm dc}^2 \cos(\varphi)^2}{\pi^2 R}. \quad (19)$$

The output power can be achieved independent of the φ, using (14)

$$\frac{R P_o}{V_{\rm dc}^2} = \frac{8}{4+\pi^2}. \quad (20)$$

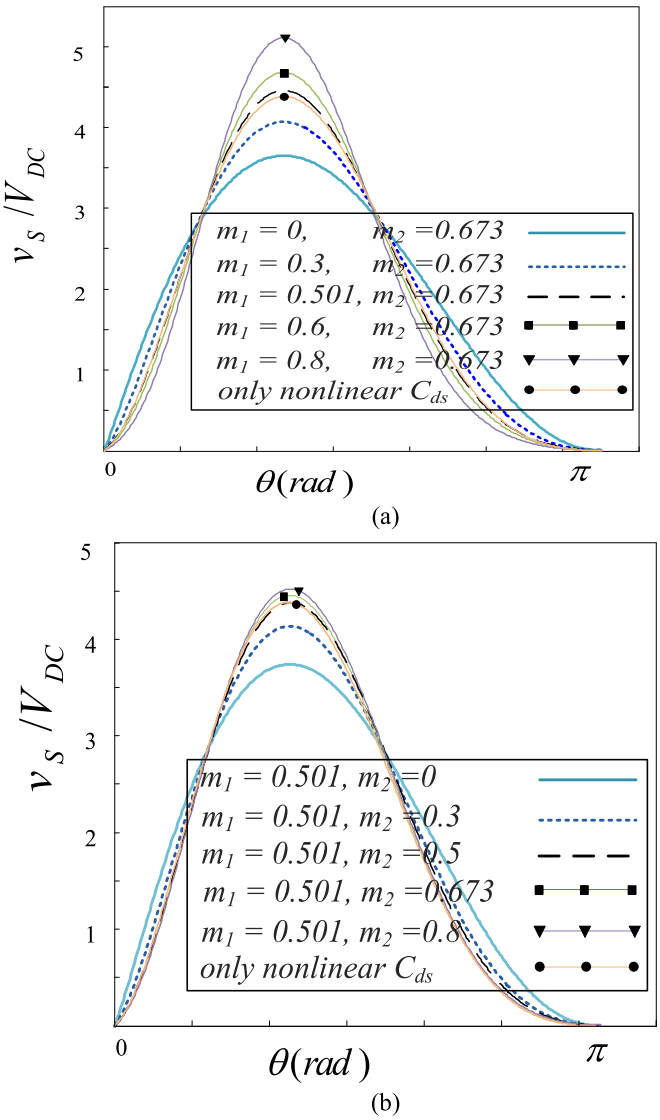

Fig. 4. Theoretical waveforms of the normalized switch voltage. For different values of (a) m_1 and (b) m_2.

Since the dc supply voltage drop across the dc feed ($I_{\rm RFC}$) is zero, the average value of the switch voltage, within a period is equal to $V_{\rm dc}$

$$2\pi = \int_0^{2\pi} \frac{v_s(\theta)}{V_{\rm dc}} d\theta. \quad (21)$$

The switch voltage equation is described in (11), while does not have analytical solution. It can be solved easily using Newton–Raphson method. Considering the obtained switch voltage and satisfying (21), the design specifications of class-E amplifier can be achieved. The normalized switch voltage ($v_s/V_{\rm dc}$) for the IRF530 MOSFET is obtained from (11), which is shown in Fig. 4. Corresponding parameters, which are needed to solve this equation, are shown in Table I. These parameters are obtained from MOSFET PSpice models at International Rectifier. According to Fig. 4(a), the maximum switch voltage raises, as m_1 increases. This effect may change the class-E power

TABLE I
MODEL PARAMETERS OF MOSFETS

	C_{j01} (pF)	$V_{\rm bi1}$ (V)	m_1	C_{j02} (pF)	$V_{\rm bi2}$ (V)	m_2
IRF530	1031	1.466	0.501	750	0.801	0.673
IRF510	298	0.774	0.423	185	0.500	0.651
IRF540	1818	1.128	0.449	2497	0.500	0.900

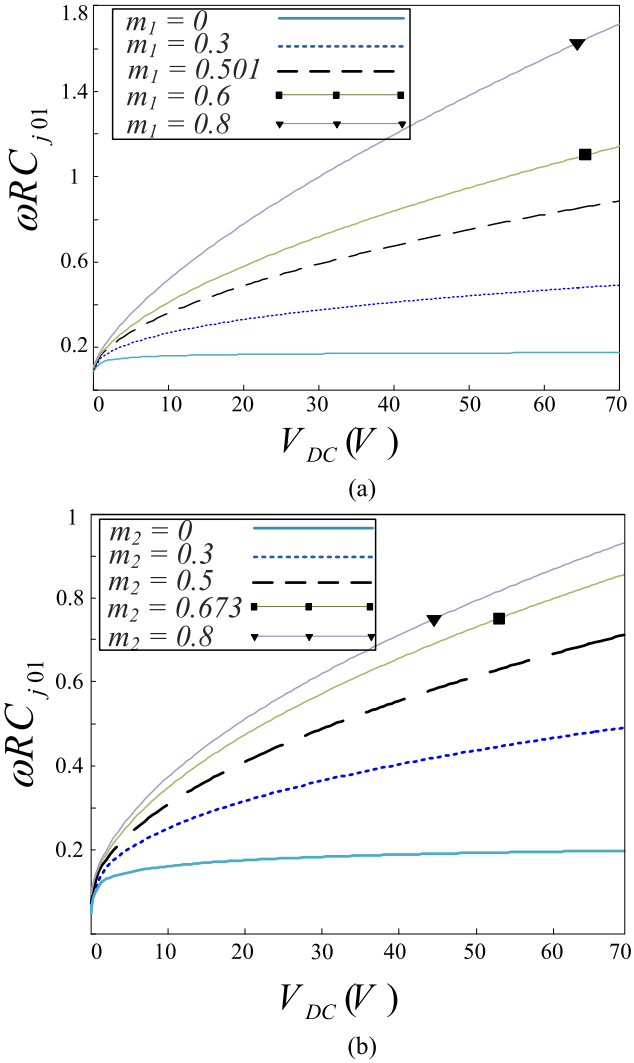

Fig. 5. ωRC_{j01} as a function of $V_{\rm dc}$. For different values of (a) m_1 and (b) m_2.

amplifier specifications, for instance it can decrease the power output capability, which will be discussed in next sections. In Fig. 4(b), the effect of the m_2 has been also shown in the switch voltage, which has approximately the same effect, compared with m_1. The normalized switch voltage waveform of the proposed class-E Power amplifier, without considering the nonlinear $C_{\rm gd}$, is also illustrated in Fig. 4. As can be seen, the nonlinearity of $C_{\rm gd}$ affects the switch voltage and the other design parameters of the class-E power amplifier, so it is important to consider its nonlinearity.

In Fig. 5(a) and (b), the appropriate values of ωRC_{j01} as a function of $V_{\rm dc}$ are obtained using IRF530 MOSFET parameters. The effects of different grading coefficients for $C_{\rm ds}$ and $C_{\rm gd}$ are shown in this figure. It is seen that large values of ωRC_{j01} is needed as the value of m_1 *or* m_2 are increased. It is also seen from this figure that, if the value of m_1 *or* m_2 is considered zero, the value of ωRC_{j01} will be approximately constant. The appropriate value of ωRC_{j01} as a function of m_1 and m_2 for fixed value of $V_{\rm dc}$, using IRF530 MOSFET parameters, is shown in Fig. 6. In this figure, the value of $V_{\rm dc}$ is 20 V, while m_1 and m_2 change from zero up to 1. The larger values of m_1 and m_2 need greater ωRC_{j01} and therefore larger load resistance. Additionally, for the grading coefficients greater than 0.3, changing of m_1 leads to larger variation in the value of appropriate load resistance, compared with m_2.

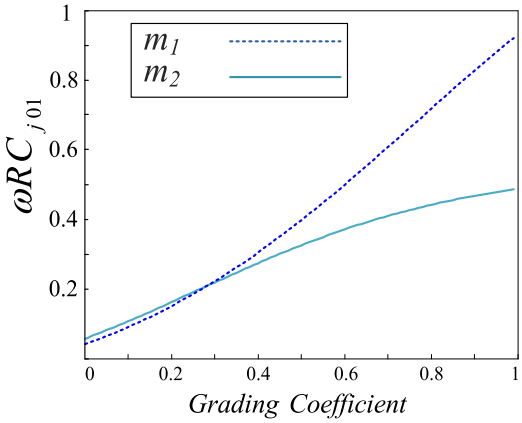

Fig. 6. ωRC_{j01} as a function of m_1 and m_2 for fixed value of $V_{\rm dc}$.

B. Voltage Across the Series Reactance

The value of series inductor (L) can be obtained using the following equation:

$$L = \frac{RQ}{\omega} \tag{22}$$

where Q is the loaded quality factor according to assumption 8). At the fundamental frequency, the resonant circuit $L_r - C$ acts like a short circuit. Therefore, the fundamental component of the switch voltage is the sum of the voltage across L_X and the output voltage

$$v_{s1}(\theta) = V_o \sin(\theta + \varphi) + v_{L_x 1}(\theta) = V_1 \sin(\theta + \varphi_1) \tag{23}$$

which V_o is the amplitude of the output voltage, V_1 is the fundamental component of the switch voltage amplitude, φ_1 is the phase shift of the fundamental component of the switch voltage with respect to the input voltage, and $v_{Lx}1$ is the fundamental component of the voltage across L_x. The $v_{Lx}1$ can be defined as follows:

$$v_{L_x 1}(\theta) = X \frac{di_o}{dt} = \frac{X}{R} V_o \cos(\theta + \varphi) \tag{24}$$

where X is the inductive reactance of L_x. V_1 and φ_1 can be written as [31]

$$V_1 = V_o \sqrt{1 + \left(\frac{X}{R}\right)^2} \tag{25}$$

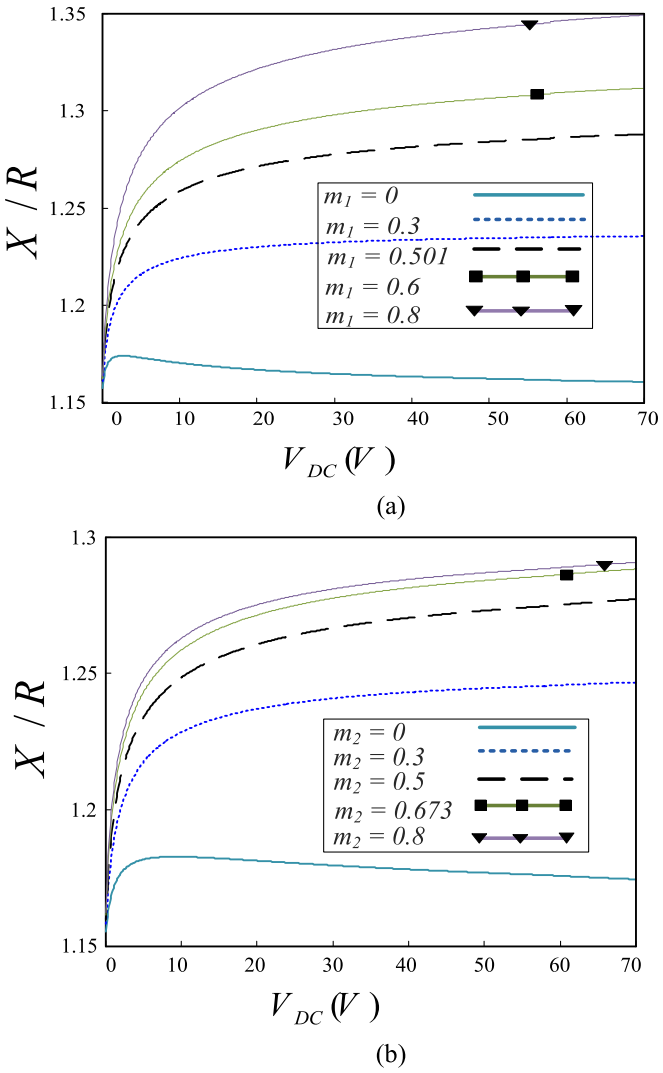

Fig. 7. *X*/*R* as a function of $V_{\rm dc}$. For different values of (a) m_1 and (b) m_2.

and

$$\varphi_1 = \varphi + \tan^{-1}\left(\frac{X}{R}\right). \tag{26}$$

As mentioned, the resonant circuit acts like a short circuit at the fundamental frequency, so the reactance of the resonant circuit is zero. Therefore

$$\frac{\int_0^{2\pi} v_s(\theta)\cos(\theta+\varphi_1)\,d\theta}{\pi} = 0. \tag{27}$$

The value of φ_1 can be obtained using (27) as follows:

$$\varphi_1 = \tan^{-1}\left(\frac{\int_0^{\pi} v_s(\theta)\cos(\theta)\,d\theta}{\int_0^{\pi} v_s(\theta)\sin(\theta)\,d\theta}\right). \tag{28}$$

Using (26), the inductive reactance to load resistance ratio can be defined as

$$\frac{X}{R} = \tan(\varphi_1 - \varphi). \tag{29}$$

Fig. 7 shows *X*/*R* as a function of $V_{\rm dc}$ for different values of m_1 and m_2, using IRF530 MOSFET parameters. As the value of m_1 or m_2 increases the values of *X*/*R* and also inductive reactance becomes larger, which leads to a larger L_x and therefore a smaller L_r.

IV. Output Power Capability

The output power of a class-E power amplifier can be studied using a parameter, called the output power capability (C_P). The C_P equation can be written as [17], [29]

$$c_P = \frac{P_{o,\max}}{v_{s,\max} i_{s,\max}} = \frac{1}{(v_{s,\max}/V_{\rm dc})(i_{s,\max}/v)} \tag{30}$$

where $P_{o,}\max$ is the maximum output power, which is equal to the dc power ($V_{\rm dc}\times I_{\rm dc}$), and $v_{s,\max}$ is the maximum value of switch voltage, which occurs during the first half of the period ($0 \le \theta < \pi$). $i_{s,\max}$ is the maximum value of switch current, which is equal to $I_m + I_{\rm dc}$ and appears in the second half of the period ($\pi \le \theta < 2\pi$). Using (12), the maximum switch-current-to-dc-current ratio can be rewritten as

$$\frac{i_{s,\max}}{I_{\rm dc}} = 1 + \frac{I_m}{I_{\rm dc}} = 1 + \frac{\pi}{2\cos\varphi}. \tag{31}$$

When maximum value of switch voltage occurs ($\theta = \theta_{\max}$), the derivative of switch voltage (v_s) becomes zero. The $\theta_{\max}$ can be obtained easily from (10) and (13) when $dv_s/d\theta$ considered zero as follows:

$$\theta_{\max} = -2\varphi. \tag{32}$$

The relation between the maximum switch voltage and $\theta_{\max}$ can be achieved using equation (11). Solving this equation and satisfying (21), the value of $v_{s,\max}$ can be obtained.

The values of $v_{s,\max}/V_{\rm dc}$ as a function of $V_{\rm dc}$ for different values of m_1 and m_2, using IRF530 MOSFET parameters, are shown in Fig. 8(a) and (b), respectively. For m_1 or m_2 equal to zero, the value of $v_{s,\max}/V_{\rm dc}$ decreases as $V_{\rm dc}$ increases. For the other values of m_1 and m_2, $v_{s,\max}/V_{\rm dc}$ raises as the dc voltage increases. From (31), the value of $i_{s,\max}/I_{\rm dc}$ is constant and equal to 2.86. According to obtained value of $v_{s,\max}/V_{\rm dc}$ and $i_{s,\max}/I_{\rm dc}$, the output power capability can be calculated, as shown in Fig. 9. The output power capability, as a function of $V_{\rm dc}$ for different values of m_1 is shown in Fig. 9(a). The effect of m_2 in C_P is also depicted in Fig. 9(b). According to Figs. 8 and 9, the C_P is proportional to inverse of $v_{s,\max}/V_{\rm dc}$. However, it is obvious that the nonlinearity of either $C_{\rm ds}$ or $C_{\rm gd}$ causes decrement in the output power capability of the class-E power amplifier. From Fig. 9, it can be also concluded that the increasing of the dc supply voltage leads to decrement in C_P, except for condition in which m_1 or m_2 was assumed to be zero.

V. Power Conversion Efficiency

The equivalent series resistance (ESR) in each component leads to power loss in the class-E power amplifier. The drain efficiency can be calculated by considering the total power loss in the presented circuit. The ESRs of dc-feed inductance (r_{LRFC}), series resonant circuit (r_{LC}), and the MOSFET on-resistance ($r_{\rm DS}$) are considered. The drain efficiency of the presented

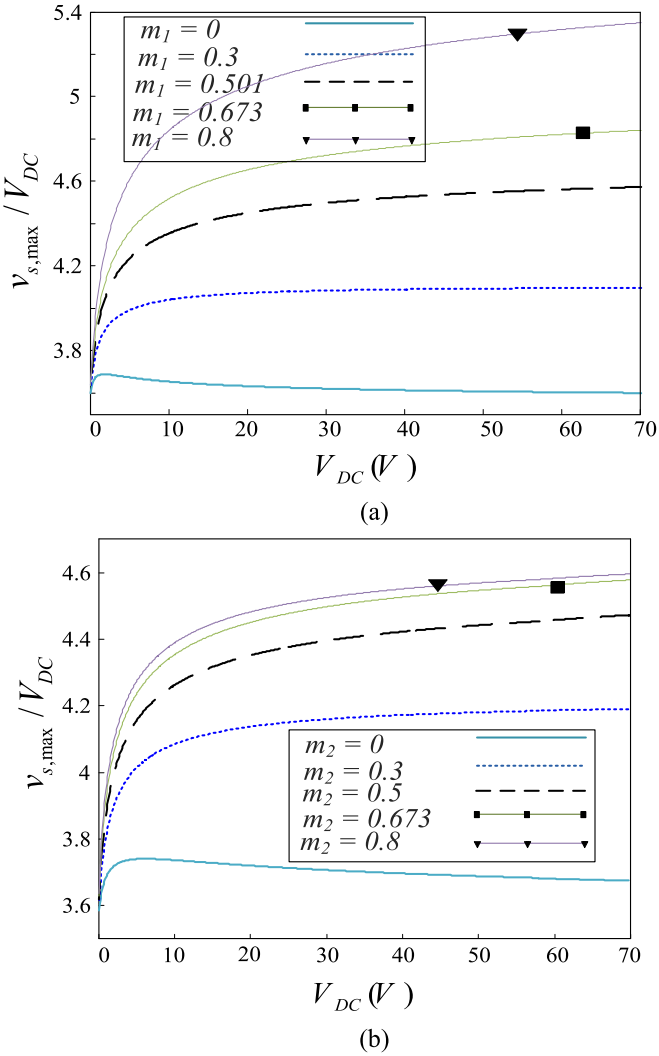

Fig. 8. Maximum switch voltage to DC voltage ratio ($v_{s,\max}/V_{\rm DC}$) as a function of $V_{\rm dc}$. For different values of (a) m_1 and (b) m_2.

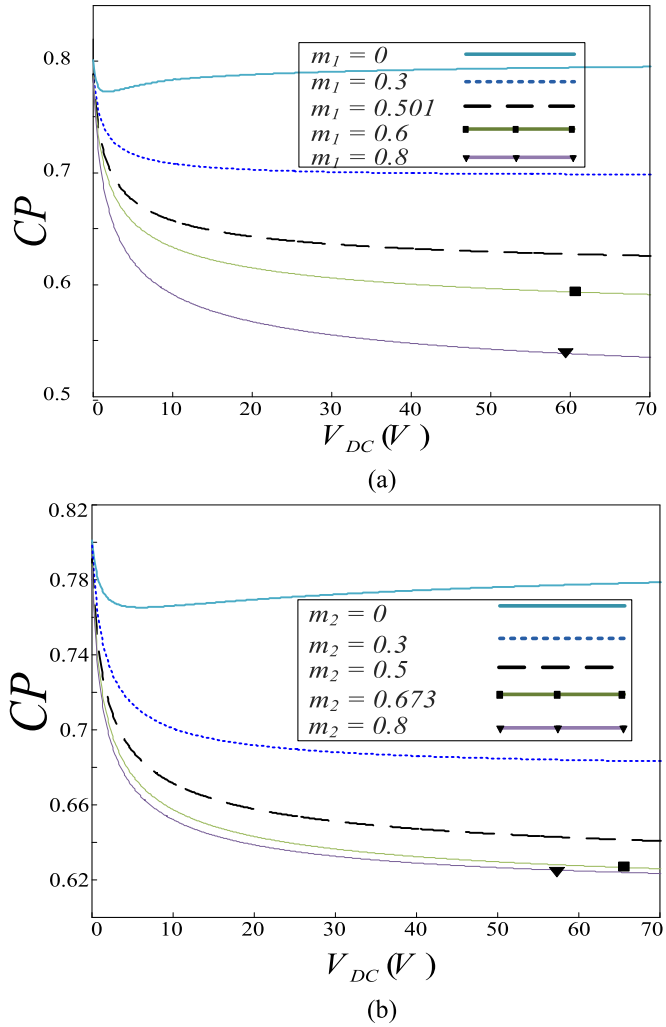

Fig. 9. Output power capability, (C_P) as a function of $V_{\rm dc}$. For different values of (a) m_1 and (b) m_2.

amplifier can be written as

$$\eta = \frac{P_o}{P_o + P_{\rm Loss}} \tag{33}$$

where the output power (P_o) was defined in (16). Additionally, $P_{\rm Loss}$, which is the total power loss, is given as

$$P_{\rm Loss} = P_{r_{L_{\rm RFC}}} + P_{r_{\rm LC}} + P_{r_{\rm DS}} \tag{34}$$

where $P_{r_{L\rm RFC}}$, $P_{r_{LC}}$, and $P_{r_{\rm DS}}$ are power losses in ESRs of dc-feed inductance, series resonant circuit, and MOSFET on-resistance, respectively. The power losses in $r_{L\rm RFC}$ and r_{LC} can be obtained as

$$\begin{aligned} P_{r_{L_{\rm RFC}}} &= \frac{1}{2\pi}\int_0^{2\pi} r_{L_{\rm RFC}} I_{\rm dc}^2 d\theta = r_{L_{\rm RFC}} I_{\rm dc}^2 \\ &= r_{L_{\rm RFC}} I_m^2 \sin^2(\varphi) \end{aligned} \tag{35}$$

$$P_{r_{LC}} = \frac{1}{2\pi}\int_0^{2\pi} r_{LC} i_o^2 d\theta = \frac{1}{2} r_{LC} I_m^2. \tag{36}$$

The power loss in the MOSFET on-resistance can be expressed as

$$\begin{aligned} P_{r_{\rm DS}} &= \frac{1}{2\pi}\int_0^{2\pi} r_{\rm DS} i_s^2 d\theta \\ &= \frac{1}{2\pi}\int_0^{2\pi} r_{\rm DS} (I_{\rm dc} - i_o)^2 d\theta. \end{aligned} \tag{37}$$

By substituting i_o and $I_{\rm dc}$ in (37), the power loss in the MOSFET on-resistance can be obtained as

$$P_{r_{\rm DS}} = r_{\rm DS} I_m^2 \left(\frac{\sin^2(\varphi)}{2} + \frac{1}{4} - \frac{\sin(2\varphi)}{\pi}\right). \tag{38}$$

From (33)–(38), the drain efficiency can be calculated as

$$\eta = \frac{1}{1 + (r_{LC}/R) + (2r_{L\rm RFC}/R)\sin^2(\varphi) + (r_{\rm DS}/R)\left(\sin^2(\varphi) + (1/2) - (2\sin(2\varphi)/\pi)\right)} \tag{39}$$

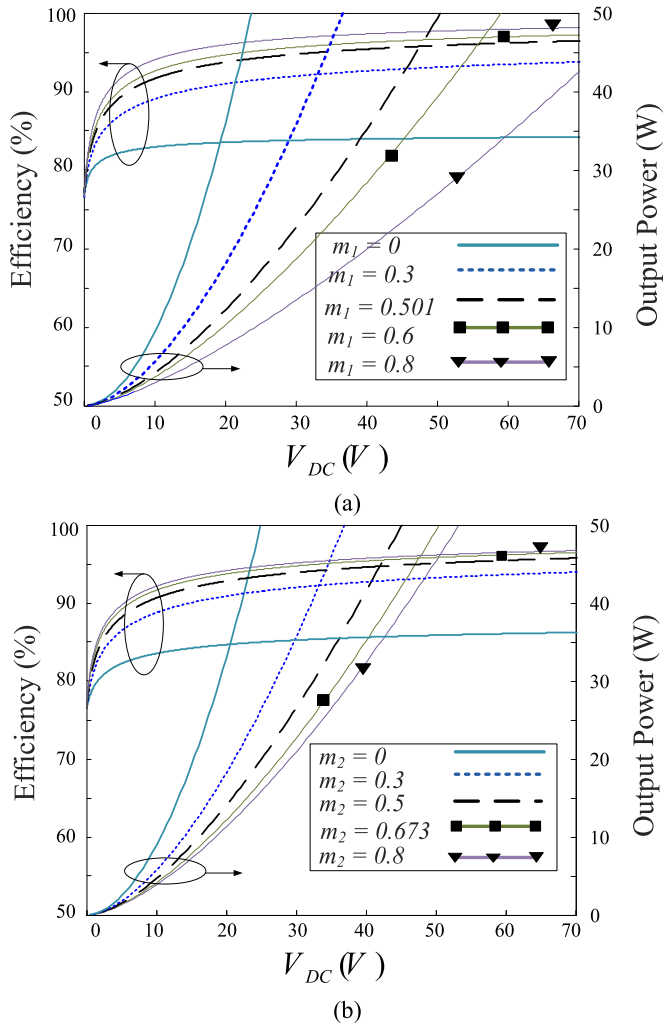

Fig. 10. Drain efficiency and output power as a function of $V_{\rm dc}$. For different values of (a) m_1 and (b) m_2.

According to (39) as shown at the bottom of the previous page, the drain efficiency is a function of φ, ESRs, and load resistance. It is obviously seen from (39) that higher drain efficiency can be obtained with the high value of load resistance. Fig. 10 shows the drain efficiency and the output power as functions of $V_{\rm dc}$ for different values of m_1 and m_2. The obtained efficiency and output power are calculated using IRF530 MOSFET parameters. The values of ESRs, which are used in (39), are given in Table II. The larger values of m_1 and m_2 lead to the greater load resistance and, therefore, result in higher drain efficiency. However, it is seen from Fig. 10 that the output power decreases as the values of m_1 and m_2 increase.

VI. Design Examples and Design Procedure

Two design examples for class-E power amplifier are presented in this section using IRF530 and IRF540 MOSFETs. The nonlinear drain-to-source and nonlinear gate-to-drain capacitances are considered in the design procedure.

TABLE II
Theoretical, PSpice Simulation, and Experimental Measurement Results of Designed Class-E Power Amplifiers

MOSFETs		Theoretical	Simulation	Measured
IRF530	$V_{\rm in}$	5 V	5 V	5 V
	$V_{\rm dc}$	20 V	20 V	20 V
	f	4 MHz	4 MHz	4 MHz
	R	19 Ω	19 Ω	19 Ω
	L	7.7 μH	7.7 μH	7.6 μH
	C	234.9 pF	234.9 pF	235pF
	$L_{\rm RFC}$	100 μH	100 μH	100 μH
	$r_{L\rm RFC}$	0.6 Ω	0.6 Ω	0.6 Ω
	r_{LC}	0.7 Ω	0.7 Ω	0.7 Ω
	$r_{\rm DS}$	0.16 Ω	0.16 Ω	–
	$V_{s,\max}$	89 V	93 V	92.8 V
	V_o	21.48 V	21.16 V	21.08 V
	$P_{\rm out}$	12.14 W	11.78 W	11.69 W
	η	93.77	93.24	91.33
IRF540	$V_{\rm in}$	5 V	5 V	5 V
	$V_{\rm dc}$	15 V	15 V	15 V
	f	4 MHz	4 MHz	4 MHz
	R	9.8 Ω	9.8 Ω	9.8 Ω
	L	3.87 μH	3.87 μH	3.81 μH
	C	469.8 pF	469.8 pF	470 pF
	$L_{\rm RFC}$	100 μH	100 μH	100 μH
	$r_{L\rm RFC}$	0.5 Ω	0.5 Ω	0.5 Ω
	r_{LC}	0.45 Ω	0.45 Ω	0.45 Ω
	$r_{\rm DS}$	0.077 Ω	0.077 Ω	–
	$V_{s,\max}$	67 V	66.7 V	68 V
	V_o	16.11 V	15.8 V	15.3 V
	$P_{\rm out}$	13.24 W	12.74 W	11.94 W
	η	92.09	91.24	90.82

A. First Design Example

The IRF530 MOSFET is selected as the switching device for the first design example. The used model is a sub circuit PSpice model, provided by the manufacturer, in which the nonlinearity of drain-to-source and gate-to-drain capacitances is considered. The initial capacitances (C_{j01} and C_{j02}), built-in potentials ($V_{\rm bi1}$ and $V_{\rm bi2}$), and grading coefficients (m_1 and m_2) are selected according to Table I. The other assumed design specifications for the first design example are $V_{\rm dc} = 20$ V and operating frequency $f = 4$ MHz. From (21), the value of R can be obtained according to the dc supply voltage, which is determined as $R = 19\ \Omega$. If another value of load resistance (R) was desired, the appropriate design specifications could be chosen to satisfy the design equations. The values of φ and P_o can be determined using (14) and (20), respectively. Using (22) and the appropriate value of Q, the value of series inductance (L) can be calculated, which is obtained as 7.7 μH. From (29), the inductive reactance, X is determined as 24.15 Ω. According to achieved values of X and L, the value of series capacitance can be calculated, which is 234.9 pF.

B. Second Design Example

Another design example using IRF540 MOSFET is given to verify the analysis with different parameters. The design procedure is similar to the first design example and the design specifications are given in Table II. The design parameters for the second example are $V_{\rm dc} = 15$ V and operating frequency f

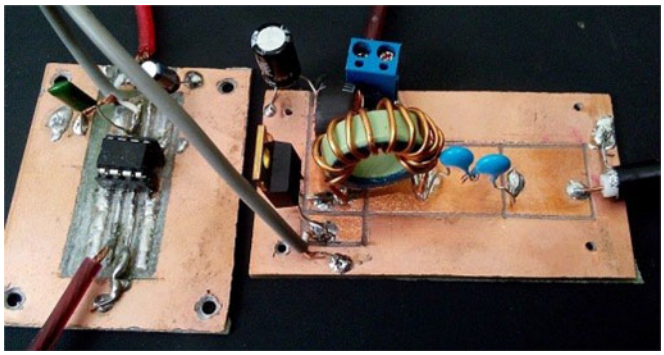

Fig. 11. Implemented class-E amplifier using IRF530 MOSFET.

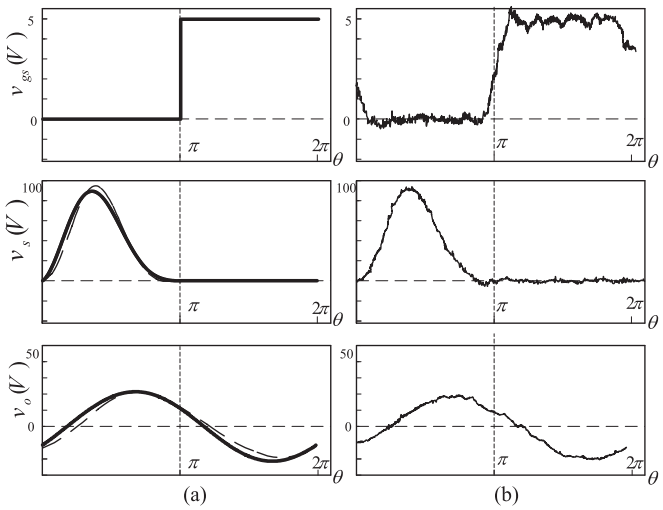

Fig. 12. Waveforms of the first design example, considering nonlinear drain-to-source and nonlinear gate-to-drain capacitances. (a) Theoretical expressions (solid line), PSpice simulations (dashed line) and (b) experimental results of gate-to-source voltage ($v_{\rm gs}$), switch voltage (v_s), and the output voltage (v_o).

$= 4$ MHz, while the value of load resistance is obtained as $R = 9.8\ \Omega$ using (21). According to (14) and (20), the values of φ and P_o can be determined. From (22) and (29) values of the series inductance (L) and the inductive reactance (X) are calculated as 3.87 μH and 12.51 Ω, respectively. Therefore, the value of series capacitance can be calculated, which is 469.8 pF.

VII. Simulation and Experimental Results

In this section, the results of the designed circuits are shown for experimental verification of the design procedure. The photograph of the implemented class-E amplifier using IRF530 MOSFET is shown in Fig. 11. The theoretical, PSpice simulation and experimental results of the given examples are shown in Figs. 12 and 13. The values of r_{LRFC} and r_{LC} were measured for two examples, which are given in Table II. Additionally, the values of $r_{\rm DS}$ were obtained as 0.16 Ω and 0.077 Ω for IRF530 and IRF540 MOSFETs, respectively, according to the PSpice models and the MOSFETs datasheets. The measured efficiency of the designed class-E amplifiers were 91.33% and 90.82%, for the first and second design examples, respectively. The applied gate-to-source voltage is assumed as square wave with the amplitude of 5 V. The theoretical, simulation and

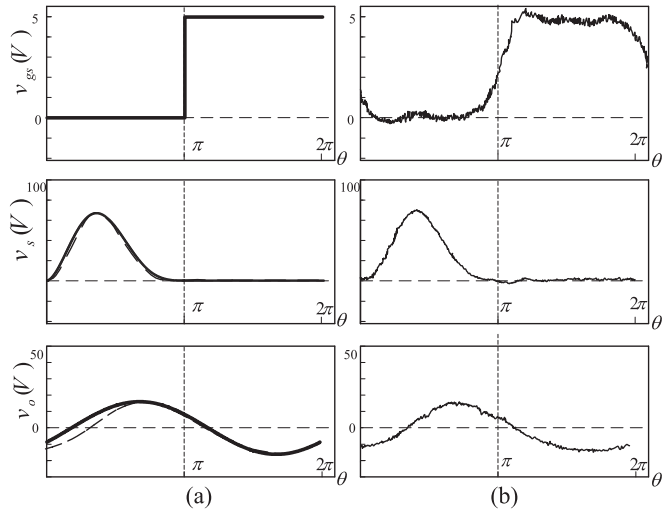

Fig. 13. Waveforms of the second design example, considering nonlinear drain-to-source and nonlinear gate-to-drain capacitances. (a) Theoretical expressions (solid line), PSpice simulations (dashed line) and (b) experimental results of gate-to-source voltage ($v_{\rm gs}$), switch voltage (v_s), and the output voltage (v_o).

experimental results of designed class-E power amplifiers are listed in Table II.

VIII. Conclusion

This paper confirmed that the gate-to-drain capacitance is highly nonlinear and this nonlinearity can severely impact the design specifications of class-E power amplifier. Therefore, to have a more accurate design, the grading coefficient of $C_{\rm gd}$ should be considered as a design parameter. The considered MOSFET parasitic capacitances in this paper are very similar to those of the real MOSFET according to datasheet measurement data. A theoretical analysis and design procedure were also given using the mentioned assumptions. According to the analysis, the ZVS and ZDS conditions could be satisfied using nonlinear $C_{\rm ds}$ and $C_{\rm gd}$. The effects of the grading coefficients of these two parasitic capacitances on the class-E power amplifier specification were also studied. Eventually, two design examples were given to describe the design procedure and verify the agreement between theoretical, simulation and experimental results.

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