Research on A Novel Modulation Strategy for Double Auxiliary Resonant Commutated Pole Soft-switching Inverter With the Shunt Dead Time

Enhui Chu, Xing Zhang, and Liang Huang

***Abstract*—Aimed at the problem that the auxiliary commutation circuit (ACC) of auxiliary resonant commutated pole (ARCP) inverters has a high loss in commutation processes, this paper presents a novel modulation strategy with shunt dead time based on a double ARCP (DARCP) inverter. In comparison with the original modulation strategy, this modulation strategy cannot only achieve soft switching for all switches, but also avoid the superposition of resonance current and load current at commutation moments in double ACCs (DACCs) and make the maximum current through DACCs approximately equal to load current in commutation processes. So, the circulating current loss in DACCs and the current stress of auxiliary switches can be effectively reduced. According to the equivalent circuits in different operation modes under the novel modulation strategy, this paper analyzes the operation principle, soft-switching implementation condition, and optimal parameter design procedure of the DARCP inverter. Finally, a 10-kW–16-kHz DARCP inverter prototype with insulated gate bipolar transistor-based switches is built. Experimental results are given to demonstrate the validity and features of the DARCP inverter under the novel modulation strategy.**

***Index Terms*—Double auxiliary resonant commutated pole (DARCP), modulation strategy, shunt dead time, soft-switching inverter.**

NOMENCLATURE

E	Input dc voltage.
$V_{\rm rms}$	Effective value of output line voltage.
v	Instantaneous voltage.
i	Instantaneous current.
P_o	Output power.
t	Time.
f_o	Output frequency.
f_s	Switching frequency.
ω	Angular frequency.
T_S	Switching cycle.
$Q_1(S_1/D_1), Q_2(S_2/D_2)$	Main switches.
S_3, S_4	The first auxiliary switches.
S_5, S_6	The second auxiliary switches.
C_1, C_2	Main resonant capacitors.
C_3, C_4	The first auxiliary resonant capacitors.
C_5, C_6	The second auxiliary resonant capacitors.
L_1, L_2	The first auxiliary resonant inductors.
L_3, L_4	The second auxiliary resonant inductors.
$D_3 \sim D_{10}$	Auxiliary diodes.
D_{11}, D_{12}	Energy regeneration feedback diodes.
i_a	Current of phase-a.
$i_{a\max}$	Maximum current of phase-a.
$i_{L1\max}$	Maximum value of the current through L_1.
C_a	Values of main resonant capacitors.
C_b	Values of the first auxiliary resonant capacitors.
C_c	Values of the second auxiliary resonant capacitors.
L_a	Values of the first auxiliary resonant inductors.
L_b	Values of the second auxiliary resonant inductors.
δ_{t11}	Shunt dead time (the turn-on delay time of the first auxiliary switch after turning OFF main switch).
δ_{t12}	Turn-on delay time of main switch after turning ON the first auxiliary switch.
δ_{t2}	Turn-off delay time of the first auxiliary switch after turning ON main switch.
δ_{t3}	Turn-off delay time of the second auxiliary switch after turning OFF the first auxiliary switch.
t_{dead}	Dead time in conventional hard-switching PWM inverter.
T_{ZVS}	Time for S_1 to achieve ZVS turn-on.
$D_{eff-\max}$	Maximum effective duty cycle.
$D_{\min}$	Minimum duty cycle.
D_{S1-D2}	Duty cycle of the load current is commutated from S_1 to D_2.
D_{D2-L1}	Duty cycle of the load current is commutated from D_2 to L_1.

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D_{ZVS}	Duty cycle for S_1 to achieve ZVS turn-on.
D_{L1-S1}	Duty cycle of the load current is commutated from L_1 to S_1.
η	Efficiency.

I. Introduction

NOWADAYS, with the development of soft-switching inverter techniques, high-power soft-switching inverters have become a research focus, which are applied to uninterrupted power supply (UPS), static var generator (SVG), active power filter (APF), the distributed grid-connected generation and so on [1]–[8]. The application of soft-switching techniques to inverters cannot only realize high frequency, miniaturization, and lightweight, but also reduce the electromagnetic interference (EMI) and switching noise. Moreover, the quality of output power can be improved [9]–[19]. Among many inverter topologies, the auxiliary resonant inverter is an important type. It can be divided into resonant dc-link inverters [20], [21] and auxiliary resonant commutated pole (ARCP) inverters [22], [23], according to the location of the auxiliary commutation circuit (ACC) in inverters. Because the current and voltage stresses of main power switches are not increased, ARCP inverters are more suitable for high-power applications.

The work in [22] and [23] are two famous ARCP inverter topologies that were, respectively, proposed by W. Mcmurray and R. W. De Doncker originally, who initiate the research on ARCP inverters. Subsequently, many improved ARCP inverters were proposed [24]–[33]. However, these topologies need either two bulk capacitors or complex coupled inductors, or transformers with corresponding magnetic flux reset circuits. Furthermore, the three single-phase resonant circuits of some inverters are coupled with each other. In addition, in order to achieve soft switching, some topologies also need additional detection circuits and peripheral logic circuits. Hence, the main circuit and control circuit will become complicated.

Then, an improved ARCP inverter topology with the function of pulse current regeneration was proposed in [34]. It overcame all the aforementioned problems. The inverter not only avoids using two bulk capacitors, but also eliminates the neutral point potential variation. Moreover, the three single-phase ACCs of the inverter are independent of each other, thus various modulation strategies can be used easily. In addition, because two groups of auxiliary components are used for two main switches separately in each phase, the voltage stresses of auxiliary switches are no more than input dc voltage. Thus, the inverter topology is more suitable for high-power applications.

In the ARCP inverter in [34], the main power switches can always achieve zero voltage switching (ZVS) turn-off reliably because each of them is in parallel with a capacitor. However, for auxiliary switches, there is a precondition to achieve ZVS turn-off. The condition is parasitic inductance and capacitance in circuits equal to zero. In practical application, this condition is destroyed by parasitic circuit elements, so the auxiliary switches cannot achieve ZVS turn-off reliably. Moreover, the longer the distances from auxiliary switch to auxiliary capacitor and input dc power supply are, the greater the influence of parasitic circuit elements will be. And this influence is particularly obvious in high-power applications, due to the complex wiring process. Therefore, this is a key problem of applying ARCP inverters in high-power applications and must be solved in the future.

In order to overcome the aforementioned problem, Chu *et al.* [35] puts forward a double ARCP (DARCP) inverter topology and modulation strategy. In comparison with [34], each auxiliary switch is in parallel with a new increased auxiliary capacitor in the DARCP inverter. Moreover, to recycle the energy in the new increased auxiliary capacitors, a new auxiliary resonant circuit is increased, and the energy in the new increased auxiliary resonant circuit can be recycled and reused. Thus, the DARCP inverter can avoid that the ZVS turn-off of auxiliary switches is influenced by parasitic circuit elements from the wiring process. And it is assured that the auxiliary switches achieve ZVS turn-off reliably.

However, most research objectives on ARCP inverters are focused on achieving soft switching of switches, improving switching frequency and enhancing inverters' efficiency. But the efficiency of most soft-switching inverters is better than hard-switching inverters' efficiency only when the output power is larger than 50% of rated power. When the output power is lower than 50% of rated power, the soft-switching inverter's efficiency is unsatisfactory, even lower than the hard-switching inverter's efficiency. The main reason is that in order to achieve soft switching, there will be an additional resonance current through ACCs, and the current through ACCs is the sum of resonance current and load current at the moment of commutation. The resonance current will cause high current stresses and lead to additional conduction and switching losses in ACCs. The high loss of ACCs limits the improvement of inverters' efficiency. It is the main problem of applying ARCP inverters to reality and must be resolved in the future.

In order to overcome the aforementioned problem, this paper puts forward a novel modulation strategy with the shunt dead time based on the DARCP inverter [35]. This modulation strategy cannot only achieve soft switching for all switches, but also avoid the superposition of resonance current and load current at commutation moments in double ACCs (DACCs) and make the maximum current in DACCs approximately equal to load current in commutation processes. The current stress of auxiliary switches and loss in DACCs can be reduced effectively. So, the soft-switching inverter can maintain a high efficiency within the whole load range.

II. Circuit Topology and Operation Principle

A. Topology and Characteristics of Circuit

Fig. 1 shows the three-phase DARCP inverter topology. Because the three single-phase DACCs are identical and can be modulated by themselves, this paper analyzes one phase leg of the inverter, representatively. The one phase leg equivalent circuit of the inverter is shown in Fig. 2 and its DACC consists of the first auxiliary switches (S_3, S_4), the second auxiliary switches (S_5, S_6), main resonant capacitors (C_1, C_2), the first auxiliary resonant capacitors (C_3, C_4), the second auxiliary resonant capacitors (C_5, C_6), the first auxiliary resonant inductors

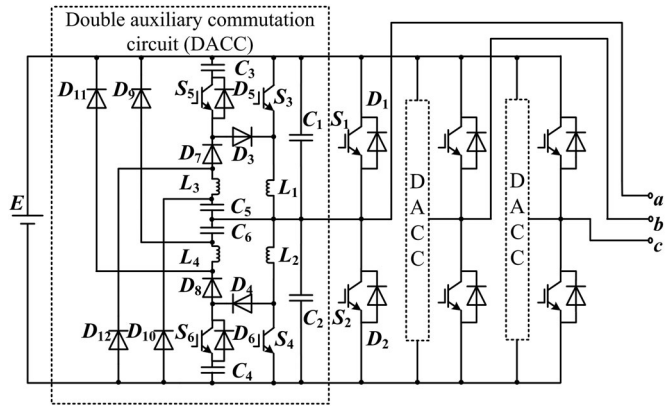

Fig. 1. Three-phase DARCP inverter.

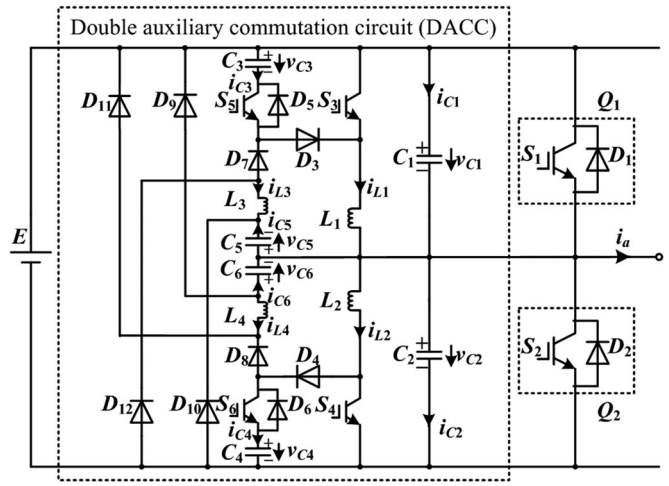

Fig. 2. One phase leg equivalent circuit.

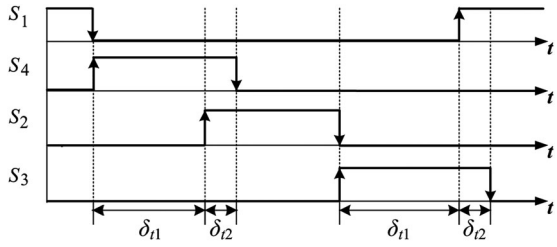

Fig. 3. Original modulation strategy.

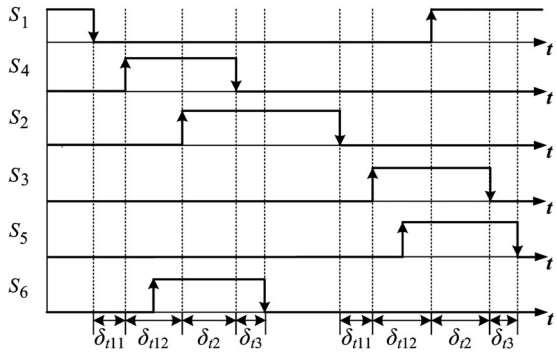

Fig. 4. Novel modulation strategy.

(L_1, L_2), the second auxiliary resonant inductors (L_3, L_4), auxiliary diodes (D_3, D_4), (D_5, D_6), (D_7, D_8), (D_9, D_{10}), and energy regeneration feedback diodes (D_{11}, D_{12}). The main characteristics of the circuit are explained as follow.

During the turn-on period of main switch S_1 (S_2), the load current $i_a > 0 (i_a < 0)$ flows through main switch S_1 (S_2), and the voltage across main resonant capacitor $C_1 (C_2)$ is zero. When main switch $S_1 (S_2)$ is turned OFF, main resonant capacitors C_1, C_2 and the second auxiliary resonant capacitor C_5 (C_6) will limit the voltage change rate of main switch S_1 (S_2) and provide ZVS turn-off condition to main switch S_1 (S_2). After the first auxiliary switch S_3 (S_4) is turned ON, the current through the first auxiliary resonant inductor L_1 (L_2) increases from zero, which provides zero current switching (ZCS) turn-on condition to the first auxiliary switch S_3 (S_4). During the turn-on period of the first auxiliary switch S_3 (S_4), the energy in the first auxiliary resonant capacitor C_3 (C_4) transfers to the second auxiliary resonant capacitor C_5 (C_6) totally, and the voltage across the first auxiliary resonant capacitor C_3 (C_4) falls to zero. After the first auxiliary switch S_3 (S_4) is turned OFF, the energy in the first auxiliary resonant inductor L_1 (L_2) begins to transfer to the first auxiliary resonant capacitor $C_3 (C_4)$, and the charging voltage across the first auxiliary resonant capacitor C_3 (C_4) increases from zero, which provides ZVS turn-off condition to the first auxiliary switch S_3 (S_4). When the charging voltage across the first auxiliary resonant capacitor C_3 (C_4) reaches to input dc voltage E, the residual energy in the first auxiliary resonant inductor L_1 (L_2) feeds back to input dc power supply through the energy regeneration feedback diode D_{12} (D_{11}).

B. Operation Principle

Fig. 3 shows the original modulation strategy of the DARCP inverter. The operating sequences of switches are explained as follow. To avoid main switch S_1 and S_2 conducting simultaneously, a period of δ_{t1} is set between the switching process of S_1 and S_2, which is determined by the dead time t_{dead} in conventional hard-switching PWM inverters. At the moment of turning OFF main switch S_1 (S_2), auxiliary switch S_4 (S_3) is turned ON immediately. From the moment of turning ON main switch $S_2 (S_1)$, it is delayed for a period of δ_{t2}, and then, auxiliary switch $S_4 (S_3)$ is turned OFF. Fig. 4 shows the novel modulation strategy proposed in this paper. In comparison with the original modulation strategy, the main difference of the novel modulation strategy is that it sets a fixed delay time δ_{t11} in switching dead time called shunt dead time. The operation sequence of each switch under the novel modulation strategy is that the moment of turning ON the first auxiliary switch $S_4 (S_3)$ is prolonged for δ_{t11} compared with that of turning OFF main switch S_1 (S_2). The moment of turning ON the second auxiliary switch S_6 (S_5) is prolonged for t_{2-3} compared with that of turning ON the first auxiliary switch S_4 (S_3). The moment of turning ON main switch S_2 (S_1) is prolonged for δ_{t12} compared with that of turning ON the first auxiliary switch S_4 (S_3). The moment of turning OFF the first auxiliary switch S_4 (S_3) is prolonged for δ_{t2} compared with that of turning ON main

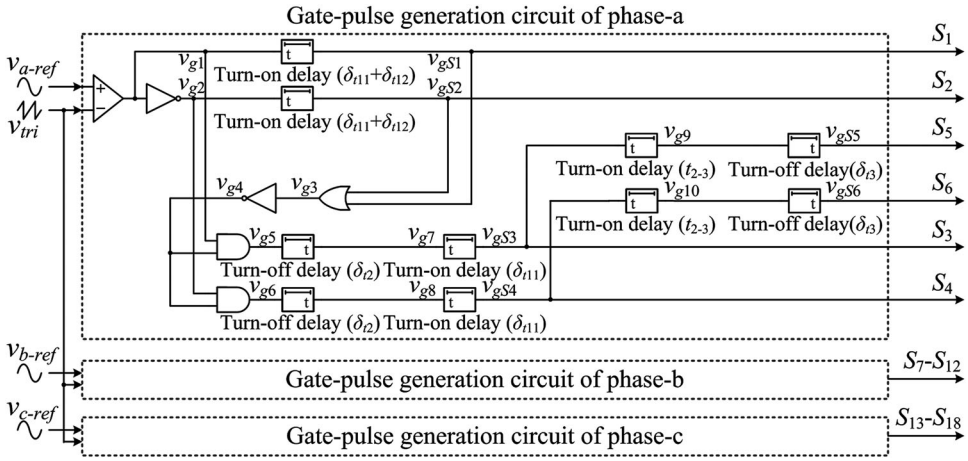

Fig. 5. Gate-pulse generation circuit.

switch S_2 (S_1). And the moment of turning OFF the second auxiliary switch $S_6(S_5)$ is prolonged for δ_{t3} compared with that of turning OFF the first auxiliary switch $S_4(S_3)$. In sine-wave triangular-comparison pulsewidth modulation (PWM), the operation sequence is designed as the ON and OFF periods of main switches alternate at intervals of π.

For the three single-phase circuits of the proposed inverter are identical and can be modulated independently, the gate-pulse generation circuit of phase-a is shown specifically in Fig. 5. The gate-pulse generation method of main switches is the same as conventional hard-switching PWM inverters. The complementary SPWM pulses (v_{g1}, v_{g2}) can be extracted by comparing a triangular wave v_{tri} with a reference sine wave v_{a-ref}. The pulses (v_{g1}, v_{g2}) go through a rising-edge-delay (named as Turn-on delay, delay time is $\delta_{t11} + \delta_{t12}$), which result in the pulses of main switches (v_{gS1}, v_{gS2}). The gate-pulse generation of the first auxiliary switches just depends on the pulses of main switches. First, the pulse v_{gS1} and v_{gS2} go through a logical OR, which results in the pulse v_{g3}. Next, the pulse v_{g3} goes through a logical NOT, which results in the pulse v_{g4}. Then, the pulse v_{g4} and v_{g1} go through a logical AND, which results in the pulse v_{g5}. The pulse v_{g4} and v_{g2} go through a logical AND, which results in the pulse v_{g6}. Then, the pulses (v_{g5}, v_{g6}) go through a falling-edge-delay (named as Turn-off delay, delay time is δ_{t2}), which result in the pulses (v_{g7}, v_{g8}). Finally, the pulses (v_{g7}, v_{g8}) go through a rising-edge-delay (delay time is δ_{t11}), which result in the pulses of the first auxiliary switches (v_{gS3}, v_{gS4}). The gate-pulse generation of the second auxiliary switches just depends on the pulses of the first auxiliary switches. First, the pulses (v_{gS3}, v_{gS4}) go through a rising-edge-delay (delay time is t_{2-3}), which result in the pulses (v_{g9}, v_{g10}). Then, the pulses (v_{g9}, v_{g10}) go through a falling-edge-delay (delay time is δ_{t3}), which result in the pulses of the second auxiliary switches (v_{gS5}, v_{gS6}). The pulses $(v_{gS1}, v_{gS2}, v_{gS3}, v_{gS4}, v_{gS5}, v_{gS6})$ through the drive circuits are used to trigger the switches $(S_1, S_2, S_3, S_4, S_5, S_6)$, respectively.

In order to facilitate the analysis, several assumptions are employed as follows:

1) all switches, diodes, capacitors, and inductors are ideal devices;
2) the values of main resonant capacitors (C_1, C_2) are $C_1 = C_2 = C_a$. The values of the first auxiliary resonant capacitors (C_3, C_4) are $C_3 = C_4 = C_b$. The values of the second auxiliary resonant capacitors (C_5, C_6) are $C_5 = C_6 = C_c$, the values of the first auxiliary resonant inductors (L_1, L_2) are $L_1 = L_2 = L_a$, the values of the second auxiliary resonant inductors (L_3, L_4) are $L_3 = L_4 = L_b (L_b \gg L_a)$;
3) the load current i_a approximates a constant during one switching cycle, because the switching frequency f_s is much larger than the output current/voltage frequency f_o;
4) the referential positive directions of physical quantities in the DACC are consistent with the directions of arrowheads in Fig. 2.

Under the novel modulation strategy, the key theoretical waveforms are shown in Fig. 6 and the equivalent circuits of different operation modes are shown in Fig. 7. In the following, the operation modes of the circuit during $i_a > 0$ are analyzed in detail.

Mode 0 $[\sim t_0]$: Before t_0, S_1 is in the turn-on state, S_2, S_3, S_4, S_5, S_6 are in the turn-off state, and all diodes are in the turn-off state. This mode is a stable state that S_1 carries load current, where $v_{C1} = v_{C4} = v_{C6} = 0, v_{C2} = v_{C3} = v_{C5} = E$, $i_{L1} = i_{L2} = i_{L3} = i_{L4} = 0$, and $i_{S1} = i_a$.

Mode 1 $[t_0, t_1]$: At instant t_0, S_1 is turned OFF. And the load current i_a is commutated to C_1, C_2 and C_5 immediately. The voltages across C_2 and C_5 fall linearly from E. At the same time, the voltage across C_1 rises linearly from zero as shown in the waveforms of Fig. 6. S_1 is ZVS turn-off. The voltages and currents of C_1, C_2 and C_5 are, respectively

$$i_{C1}(t) = -i_{C2}(t) = \frac{C_a}{2C_a + C_c} \cdot i_a \tag{1}$$

$$i_{C5}(t) = -\frac{C_c}{2C_a + C_c} \cdot i_a \tag{2}$$

$$v_{C1}(t) = \frac{i_a}{2C_a + C_c} t \tag{3}$$

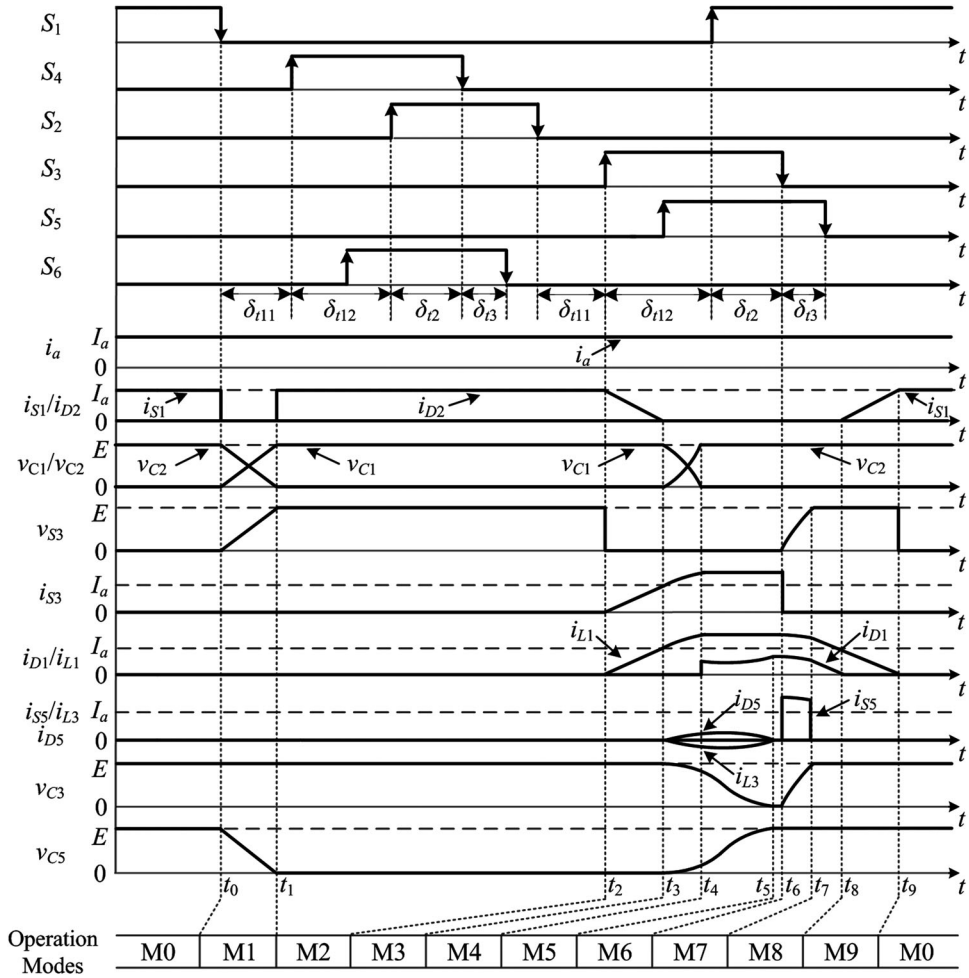

Fig. 6. Key theoretical waveforms of the circuit.

$$v_{C2}(t) = v_{C5}(t) = E - \frac{i_a}{2C_a + C_c}t. \tag{4}$$

When the voltages across C_2 and C_5 decrease to zero, mode 1 ends. According to (3), the duration of this mode is

$$t_{0-1} = \frac{E\,(2C_a + C_c)}{i_a}. \tag{5}$$

In the parameter design, the delay time δ_{t11} should not be less than the time t_{0-1}, which is determined by (5), under the condition of the maximum load current $i_{a\max}$.

Mode 2 $[t_1, t_2]$: At instant t_1, the voltage across C_1 is charged to *E* and the voltages across C_2 and C_5 are discharged to zero. Diode D_2 starts conducting and the load current i_a is commutated to D_2 immediately. S_2 achieves ZVS turn-on in D_2 conduction duration. During this mode, the current through D_2 equals to the load current i_a. When S_3 is turned ON, mode 2 ends.

Mode 3 $[t_2, t_3]$: At instant t_2, S_3 is turned ON. Since D_2 is conducting, the voltage across L_1 is *E*. So, the current through L_1 rises linearly from zero. At the same time, the current through D_2 falls linearly from i_a. The load current is commutated from D_2 to L_1. S_3 achieves ZCS turn-on. In S_3 conduction duration, S_5 achieves zero voltage zero current switching (ZVZCS) turn-on. The currents of L_1 and D_2 are, respectively

$$i_{L1}(t) = \frac{E}{L_a} \cdot t \tag{6}$$

$$i_{D2}(t) = i_a - \frac{E}{L_a} \cdot t. \tag{7}$$

When the current through L_1 reaches to i_a, the current through D_2 falls to zero, D_2 turns OFF naturally, and mode 3 ends. According to (7), the duration of mode 3 is

$$t_{2-3} = \frac{L_a}{E} \cdot i_a. \tag{8}$$

Mode 4 $[t_3, t_4]$: At instant t_3, D_2 turns OFF, and the load current i_a is commutated to L_1 totally. At the moment, C_1 and C_2 begin to resonate with L_1. And C_3, C_5, and L_3 begin to resonate with L_1, too. C_3 is discharged from *E*, and C_5 is charged from zero. The energy in C_3 begins to transfer to C_5. The voltage across C_1 falls from *E*, and the voltage across C_2 rises from zero. The current through L_1 is the sum of resonance current and load current. It is notable that the voltage across C_6 is zero and C_6 is not participating in the resonance. With the condition of $L_b \gg L_a$, $C_c \geq C_b$, the voltages and currents of

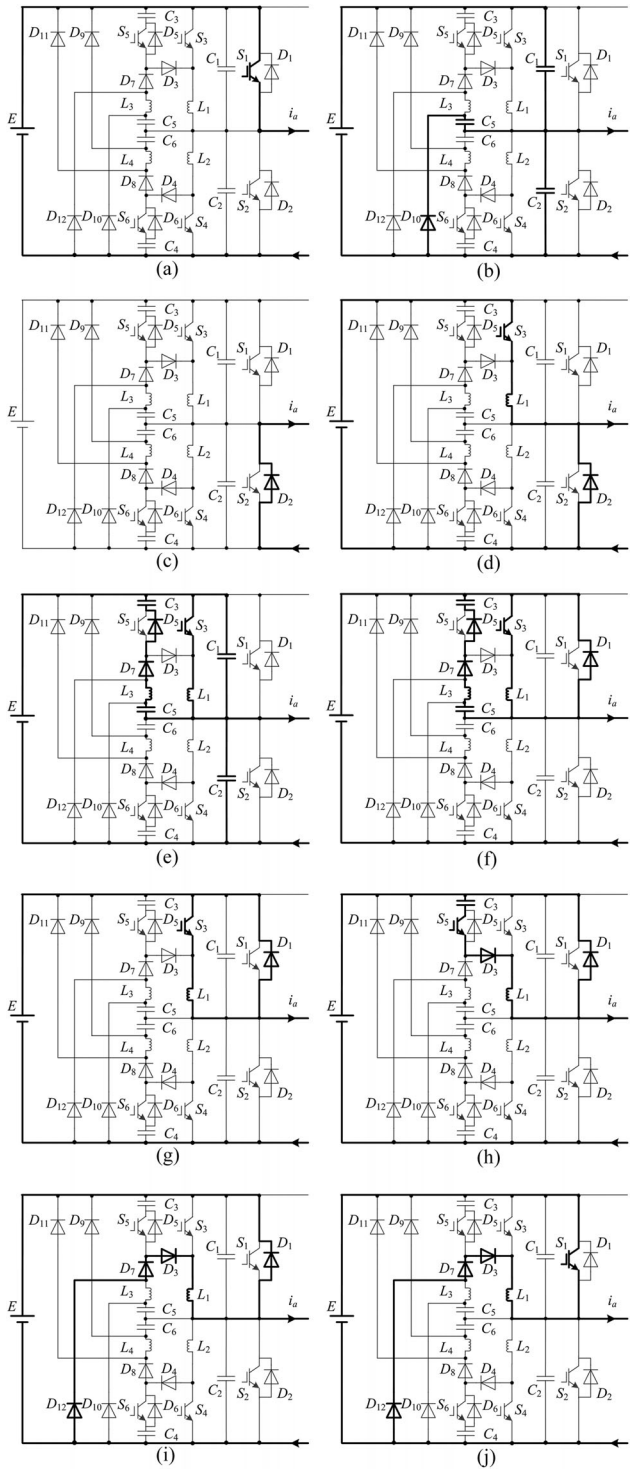

Fig. 7. Equivalent circuits of different operation modes. (a) Mode 0. (b) Mode 1. (c) Mode 2. (d) Mode 3. (e) Mode 4. (f) Mode 5. (g) Mode 6. (h) Mode 7. (i) Mode 8. (j) Mode 9.

C_1, C_2, C_3, C_5, L_1, and L_3 are, respectively

$$v_{C1}(t) = v_{L1}(t) = E\cos\omega_1 t \tag{9}$$

$$v_{C2}(t) = E - E\cos\omega_1 t \tag{10}$$

$$i_{C2}(t) = -i_{C1}(t) = \frac{1}{2}\cdot\frac{E}{\omega_1 L_a}\sin\omega_1 t \tag{11}$$

$$i_{L1}(t) = i_a + \frac{E}{\omega_1 L_a}\sin\omega_1 t \tag{12}$$

$$v_{C3}(t) = E - \frac{C_c E}{C_b + C_c}(1 - \cos\omega_2 t) \tag{13}$$

$$v_{C5}(t) = \frac{C_b E}{C_b + C_c}(1 - \cos\omega_2 t) \tag{14}$$

$$i_{L3}(t) = i_{C3}(t) = -i_{C5}(t) = \frac{-E}{\omega_2 L_b}\sin\omega_2 t. \tag{15}$$

After 1/4 of the resonant cycle $T_1(T_1 = 2\pi/\omega_1)$, the voltage across C_1 falls to zero, and mode 4 ends. The current through L_1 reaches to the maximum value $i_{L1\max}$. According to (9), the duration of mode 4 is

$$t_{3-4} = \frac{\pi}{2\omega_1} = \frac{\pi}{2}\cdot\sqrt{2L_a C_a}. \tag{16}$$

According to (12) and (16), the value of $i_{L1\max}$ is

$$i_{L1\max} = i_a + \frac{E}{\omega_1 L_a} = i_a + E\cdot\sqrt{\frac{2C_a}{L_a}} \tag{17}$$

where

$$\omega_1 = \sqrt{\frac{1}{2L_a C_a}} \tag{18}$$

$$\omega_2 = \sqrt{\frac{C_b + C_c}{L_b C_b C_c}}. \tag{19}$$

In the parameter design, the delay time δ_{t12} from S_3 turned ON to S_1 turned ON should not be less than the time ($t_{2-3} + t_{3-4}$) determined by (8) and (16), under the condition of the maximum load current $i_{a\max}$.

Mode 5 $[t_4, t_5]$: At instant t_4, the voltage across C_2 rises to E and the voltage across C_1 falls to zero. The current through L_1 reaches to the maximum value $i_{L1\max}$. D_1 starts conducting. C_3, L_3, and C_5 continue resonating. The voltage across C_3 continues falling as (13). The voltage across C_5 continues rising as (14). The energy in C_3 continues transferring to C_5. The current through L_1 keeps $i_{L1\max}$ invariably. S_1 achieves ZVS turn-on in D_1 conduction duration. The voltages and currents of C_3, C_5, and L_3 are, respectively

$$v_{C3}(t) = E - \frac{C_c E}{C_b + C_c}[1 - \cos\omega_2(t + t_{3-4})] \tag{20}$$

$$v_{C5}(t) = \frac{C_b E}{C_b + C_c}[1 - \cos\omega_2(t + t_{3-4})] \tag{21}$$

$$i_{L3}(t) = i_{C3}(t) = -i_{C5}(t) = \frac{-E}{\omega_2 L_b}\sin\omega_2(t + t_{3-4}). \tag{22}$$

When the current through L_3 falls to zero, the energy in C_3 transfers to C_5 totally, and mode 5 ends. According to (16) and (22), the duration of mode 5 is

$$t_{4-5} = \pi\sqrt{\frac{L_b C_b C_c}{C_b + C_c}} - t_{3-4} = \pi\sqrt{\frac{L_b C_b C_c}{C_b + C_c}} - \frac{\pi}{2}\sqrt{2L_a C_a}. \tag{23}$$

In the parameter design, the time $(\delta_{t12} + \delta_{t2})$ from S_3 turned ON to S_3 turned OFF should not be less than the time

$(t_{2-3} + t_{3-4} + t_{4-5})$ determined by (8), (16), and (23), under the condition of the maximum load current $i_{a\max}$.

Mode 6 $[t_5, t_6]$: At instant t_5, the current through L_3 falls to zero. At the moment, the voltage across C_3 falls to zero. D_5 and D_7 turn OFF naturally. The resonance current $i_{L1\max}$ flows through the loop circuit L_1–S_3–D_1 and this state continues until S_3 is turned OFF. When S_3 is turned OFF, mode 6 ends.

Mode 7 $[t_6, t_7]$: At instant t_6, S_3 is turned OFF. D_3 starts conducting. L_1 begins to resonate with C_3. The energy in L_1 transfers to C_3. The voltage across C_3 rises from zero. Therefore, S_3 achieves ZVS turn-off. The voltages and currents of C_3 and L_1 are, respectively

$$v_{C3}(t) = -v_{L1}(t) = \omega_3 L_a i_{L1\max} \sin \omega_3 t \tag{24}$$

$$i_{L1}(t) = i_{C3}(t) = i_{L1\max} \cos \omega_3 t \tag{25}$$

where

$$\omega_3 = \sqrt{\frac{1}{L_a C_b}}. \tag{26}$$

When the voltage across C_3 rises to E, mode 7 ends. According to (24), the duration of mode 7 is

$$t_{6-7} = \frac{1}{\omega_3} \cdot \arcsin\left(\frac{E}{\omega_3 L_a i_{L1\max}}\right). \tag{27}$$

In the parameter design, the time δ_{t3} from S_3 turned OFF to S_5 turned OFF should not be less than the time t_{6-7} determined by (27), under the condition of the maximum load current $i_{a\max}$.

Mode 8 $[t_7, t_8]$: At instant t_7, the voltage across C_3 rises to E. At this time, D_7 and D_{12} start conducting, and the residual energy in L_1 feeds back to input dc power supply through D_3, D_7, and D_{12}. The currents through L_1 and D_1 fall linearly. S_5 achieves ZVZCS turn-off during the period of this mode beginning to S_1 turned OFF. The currents of L_1 and D_1 are, respectively

$$i_{L1}(t) = i_{L1}(t_7) - \frac{E}{L_a} t \tag{28}$$

$$i_{D1}(t) = i_{L1}(t_7) - \frac{E}{L_a} t - i_a. \tag{29}$$

When the current through L_1 falls to i_a, D_1 turns OFF naturally, and mode 8 ends. According to (28), the duration of mode 8 is

$$t_{7-8} = \frac{L_a \left[i_{L1}(t_7) - i_a\right]}{E}. \tag{30}$$

Mode 9 $[t_8, t_9]$: At instant t_8, the current through L_1 falls to i_a. D_1 turns OFF. The current through L_1 continues falling linearly, and the current through S_1 rises linearly from zero. The load current is commutated from L_1 to S_1. The current of L_1 is

$$i_{L1}(t) = i_a - \frac{E}{L_a} t. \tag{31}$$

When the current through L_1 falls to zero, the load current is commutated to S_1 totally, mode 9 ends. According to (31), the duration of mode 9 is

$$t_{8-9} = \frac{L_a i_a}{E}. \tag{32}$$

At instant t_9, the current through L_1 falls to zero. The current through S_1 keeps the load current i_a invariably, and the operation mode is back to mode 0 again.

The operation modes during $i_a < 0$ are similar to the aforementioned modes $(i_a > 0)$, so the analysis to the operation modes during $i_a < 0$ is omitted.

As the analysis mentioned previously (seeing mode 4 and 5 in Figs. 6 and 7), from the moment of turning ON the first auxiliary switch $S_3(S_4)$, the energy in the first auxiliary resonant capacitor $C_3(C_4)$ begins to transfer to the second auxiliary resonant capacitor $C_5(C_6)$, the second auxiliary resonant inductor $L_3(L_4)$ and the first auxiliary resonant inductor $L_1(L_2)$. In order to achieve ZVS turn-off reliably for $S_3(S_4)$, the energy of $C_3(C_4)$ must be fully released during Mode 4 and Mode 5. This asked for the value of $C_3(C_4)$ is no more than the value of $C_5(C_6)$. Furthermore, the charging voltage across $C_5(C_6)$ is beneficial for $S_1(S_2)$ to achieve ZVS turn-off. Thus, in order to transfer to $C_5(C_6)$ as much as possible, the energy in $C_3(C_4)$ should transfer to $L_1(L_2)$ as little as possible in the duration of mode 4. This is asked for the value of $L_3(L_4)$ is much larger than the value of $L_1(L_2)$. Therefore, in the parameter design, the values of the auxiliary resonant capacitor $C_3(C_4), C_5(C_6)$ and the auxiliary resonant inductor $L_1(L_2), L_3(L_4)$ should meet $C_c \geq C_b$, $L_b \gg L_a$.

C. Separation Principle of Resonant Current and Load Current

As the analysis mentioned previously, the energy stored in $C_5(C_6)$ is completely released through load circuits during δ_{t11} (seeing mode 1 in Figs. 6 and 7). When the first auxiliary switch $S_4(S_3)$ is turned ON, there is no energy stored in the second auxiliary resonant capacitors and the DACC no longer has reactive energy to exchange. Therefore, the maximum current through the DACC in commutation processes can be calculated by (17). Because the value of C_a can be arbitrarily small, the maximum current through the DACC in commutation processes approximately equals to the load current at commutation moments.

However, the original modulation strategy has not set the shunt dead time δ_{t11}. The auxiliary switch $S_4(S_3)$ is turned ON as soon as the main switch $S_1(S_2)$ is turned OFF and the key operation modes are shown in Fig. 8. When load current i_a is commutated from main switch S_1 to freewheeling diode D_2, the initial voltage values of resonant capacitors are $v_{C1} = v_{C6} = 0$ and $v_{C2} = v_{C3} = v_{C4} = v_{C5} = E$. S_4 is turned ON as soon as S_1 is turned OFF and the circuit enters into mode 1' as shown in Fig. 8(a). C_1, C_2, and C_5 begin to resonate with L_2, and C_4, C_6, and L_4 begin to resonate with L_2, too. The current through L_2 and the voltages across C_1 and C_6 rise from zero. The voltages across C_2, C_4, and C_5 fall from E. When the voltages across C_2 and C_5 fall to zero, the resonant process is finished and mode 1' ends. During the process, a part of resonant energy transfers to the first auxiliary resonant inductor L_2.

When S_4 is turned OFF, the circuit enters into mode 2' as shown in Fig. 8(b). The energy in L_2 transfers to C_4. When the voltage across C_4 rises to E, mode 2' ends. Unlike the novel modulation strategy, the reactive energy stored in the DACC is transferred from the second auxiliary resonant capacitor C_5 to

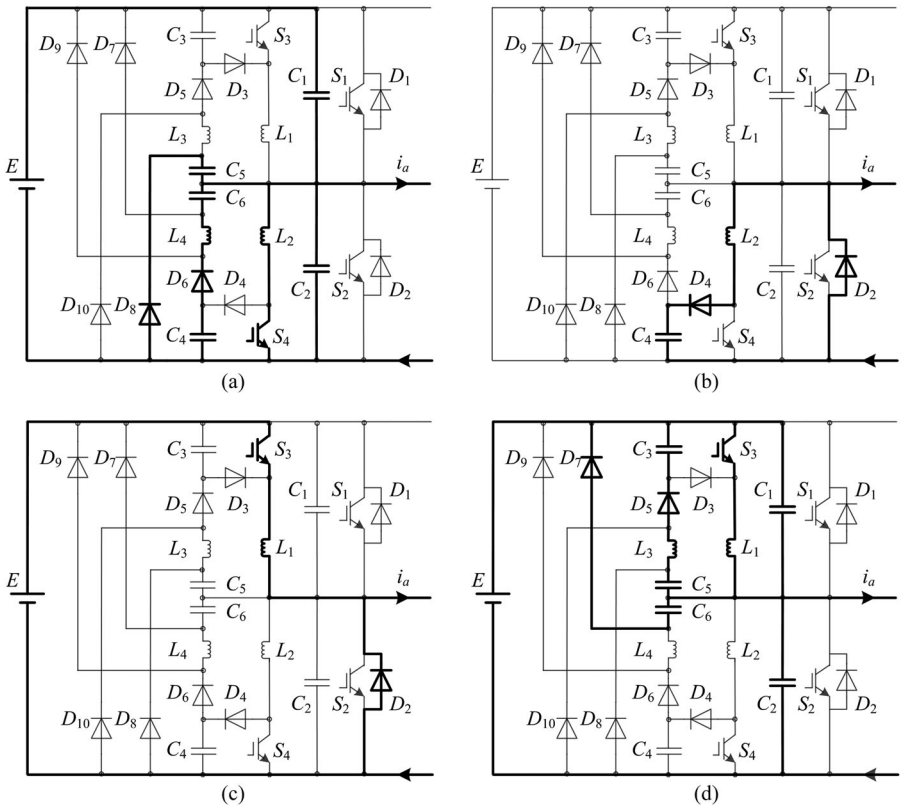

Fig. 8. Key operation modes under the original modulation strategy. (a) Mode 1'. (b) Mode 2'. (c) Mode 3'. (d) Mode 4'.

the first auxiliary resonant capacitor C_4 by the first auxiliary resonant inductor L_2. And when C_4, C_6, and L_4 resonate next time, the energy stored in the DACC will be transferred from the first auxiliary resonant capacitor C_4 to the second auxiliary resonant capacitor C_6.

When load current i_a is commutated from freewheeling diode D_2 to main switch S_1, S_3 is turned ON as soon as S_2 is turned OFF and the circuit enters into mode 3' as shown in Fig. 8(c). The current through D_2 begins to commutate to L_1 and this mode is same as mode 3 under the novel modulation strategy (seeing mode 3 in Figs. 6 and 7). When the load current i_a is completely commutated to L_1, D_2 turns OFF naturally and mode 3' ends.

Because there is energy stored in C_6, assume the voltage across C_6 is *E* (the voltage can also be smaller than *E*). When mode 3' ends, the circuit immediately enters into mode 4' as shown in Fig. 8(d). C_1, C_2, and C_6 begin to resonate with L_1, and C_3, C_5, and L_3 begin to resonate with L_1, too. The energy in C_3 begins to transfer to C_5. The voltages across C_1 and C_6 fall from *E*, and the voltage across C_2 rises from zero. The current through L_1 is the sum of resonance current and load current. After 1/4 of the resonant cycle, the voltages across C_1 and C_6 fall to zero, and mode 4' ends. The current through L_1 reaches to the maximum value $i_{L1\max}$

$$i_{L1\max} = i_a + E \cdot \sqrt{\frac{2C_a + C_c}{L_a}}. \tag{33}$$

On the basis of the key operation modes analysis under the original modulation strategy, we conclude that because the auxiliary switch $S_4(S_3)$ is turned ON as soon as the main switch $S_1(S_2)$ is turned OFF, the reactive energy stored in the DACC has no time to be released through load circuits and it is transformed into resonance current through a series of resonance. So, the peak current through the DACCs is the sum of resonance current and the load current at the moment of commutation, which increases the current stress and circulating current loss of the DACCs.

III. Steady-State Characteristics

A. Maximum Current and Voltage Stresses of Components

The voltage and current stresses of each component in the DARCP inverter under original and novel modulation strategies are shown in Table I. Under different modulation strategies, neither the voltage stresses of main switches, auxiliary switches and diodes, nor the current stress of main switches has changed. The voltage stresses of main switches, auxiliary switches, and diodes equal to input dc voltage *E*. The current stress of main switches equals to the maximum value of the load current. However, under the novel modulation strategy, the current stress of auxiliary switches is significantly lower than that under the original modulation strategy. Because the value of C_a can be set to a very small value that can be negligible, the current stress of auxiliary switches equals to the maximum value of load current under the novel modulation strategy. And the novel modulation

TABLE I
VOLTAGE AND CURRENT STRESSES OF COMPONENTS

	Original Modulation Strategy	Novel Modulation Strategy
Voltage Stress		
Main switches (S_1, S_2)	E	E
The first auxiliary switches (S_3, S_4)	E	E
The second auxiliary switches(S_5, S_6)	—	E
Diodes($D_1 - D_{12}$)	E	E
Current stress		
Main switches(S_1, S_2)	$i_{a\max}$	$i_{a\max}$
The first auxiliary switches (S_3, S_4)	$E\cdot\sqrt{\frac{2C_a+C_c}{L_a}}+i_{a\max}$	$E\cdot\sqrt{\frac{2C_a}{L_a}}+i_{a\max}$
The second auxiliary switches(S_5, S_6)	—	$E\cdot\sqrt{\frac{2C_a}{L_a}}+i_{a\max}$

strategy effectively avoids the superposition of resonance current and load current at commutation moments in DACCs.

B. dv/dt of Main Switches and di/dt of Freewheeling Diodes

Under the novel modulation strategy, according to (3) and (7), the voltage change rate of main switches during turn-off transient and the current change rate of freewheeling diodes during turn-off transient are, respectively

$$dv/dt = \frac{i_a}{2C_a + C_c} \tag{34}$$

$$di/dt = \frac{E}{L_a}. \tag{35}$$

According to (34) and (35), we know that the voltage change rate of main switches during turn-off transient and the current change rate of freewheeling diodes during turn-off transient are constants. It means that the voltage across main switches during turn-off transient and the current through freewheeling diodes during turn-off transient vary linearly and these change rates can be designed arbitrarily in the parameter design.

C. Soft-Switching Implementation Condition

According to the analysis of operation principle, the commutation time from main switches (S_1, S_2) turned OFF to freewheeling diodes (D_2, D_1) turning ON is less than the time from freewheeling diodes (D_2, D_1) turning OFF to main switches (S_1, S_2) turned ON. So, the soft-switching implementation condition depends on the time $(\delta_{t11} + \delta_{t12})$ from freewheeling diodes (D_2, D_1) turning OFF to main switches (S_1, S_2) turned ON.

1) ZVS Implementation Condition of Main Switches: According to the analysis of operation principle, the maximum commutation time $(\delta_{t11} + \delta_{t12})$ should not be larger than the dead time t_{dead} in conventional hard-switching PWM inverters, so $t_{0-1} + t_{2-3} + t_{3-4} \le \delta_{t11} + \delta_{t12} \le t_{dead}$. According to (5), (8), and (16), the relationship is

$$\frac{E(2C_a + C_c)}{i_a} + \frac{L_a}{E} i_a + \frac{\pi}{2}\cdot\sqrt{2L_aC_a} \le \delta_{t11} + \delta_{t12} \le t_{dead}. \tag{36}$$

In order to achieve ZVS turn-on for main switches (S_1, S_2), the commutation time δ_{t12} must meet the relationship $\delta_{t12} \ge t_{2-3} + t_{3-4}$. According to (8) and (16), the time δ_{t12} should meet

$$\delta_{t12} \ge \frac{L_a}{E} i_a + \frac{\pi}{2}\cdot\sqrt{2L_aC_a}. \tag{37}$$

2) ZVS Implementation Condition of the First Auxiliary Switches: In order to achieve ZVS turn-off for the first auxiliary switches (S_3, S_4), the voltage across C_3 must fall to zero within $(t_{3-4} + t_{4-5})$, so $t_{3-4} + t_{4-5} \le \delta_{t12} + \delta_{t2} - t_{2-3}$. According to (8), (16), and (23), the time δ_{t2} should meet

$$\delta_{t2} \ge \frac{L_a}{E} i_a + \pi\cdot\sqrt{\frac{L_bC_bC_c}{C_b + C_c}} - \delta_{t12}. \tag{38}$$

3) ZVZCS Implementation Condition of the Second Auxiliary Switches: On the basis of the aforementioned analysis, in order to achieve ZVZCS turn-off for the second auxiliary switches (S_5, S_6), the commutation time δ_{t3} must meet the relationship $\delta_{t3} \ge t_{6-7}$. According to (27), the time δ_{t3} should meet

$$\delta_{t3} \ge \sqrt{L_aC_b}\cdot\arcsin\left(\frac{E}{i_{L1\max}}\sqrt{\frac{C_b}{L_a}}\right). \tag{39}$$

In order to achieve ZVZCS turn-on for the second auxiliary switches (S_5, S_6), the second auxiliary switches must be turned ON in the first auxiliary switches (S_3, S_4) conduction duration.

D. Maximum Effective Duty Cycle and Minimum Duty Cycle

According to the analysis of operation principle, in order to achieve ZVS turn-on for main switch S_1, the commutation time $(\delta_{t11} + \delta_{t12})$ should meet $\delta_{t11} + \delta_{t12} \le t_{dead}$. As shown in Fig. 9, the minimum duty cycle $D_{\min}$ and the maximum effective duty cycle $D_{eff-\max}$ under the novel modulation strategy are

$$D_{\min} = D_{L1-S1} \tag{40}$$

$$D_{eff-\max} = 1 - 2D_{S1-D2} - 2D_{D2-L1} - 2D_{\mathrm{ZVS}} - D_{\min} \tag{41}$$

where $D_{S1-D2} = \frac{t_{0-1}}{T_s}$, $D_{D2-L1} = \frac{t_{2-4}}{T_s}$, $D_{\mathrm{ZVS}} = \frac{T_{ZVS}}{T_s}$, and $D_{L1-S1} = \frac{t_{8-9}}{T_s}$.

t_{0-1} is the duration of mode 1 (the commutation time when the load current is commutated from S_1 to D_2); t_{2-4} is the sum of the duration of mode 3 and mode 4 (the commutation time when the load current is commutated from D_2 to L_1); T_{ZVS} is the time for S_1 to achieve ZVS turn-on, which depends on the duration of mode 5, mode 6, mode 7, and mode 8. t_{8-9} is the duration of mode 9 (the commutation time when the load current is commutated from L_1 to S_1).

According to (40) and (41), in comparison with conventional hard-switching PWM inverters with the dead time, the minimum

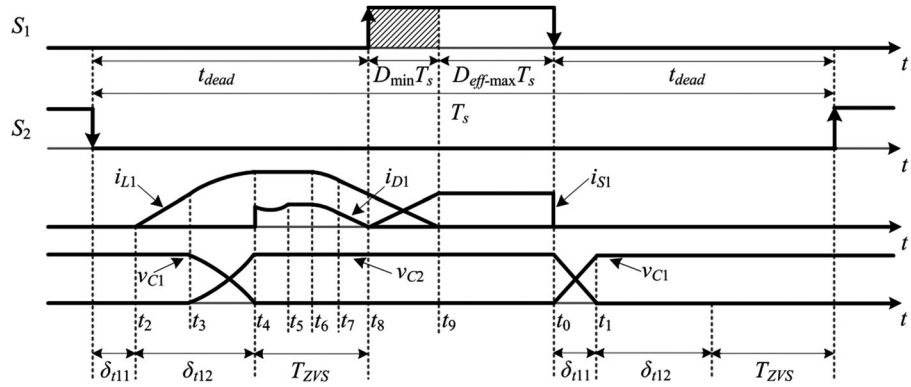

Fig. 9. Maximum effective duty cycle $D_{eff-\max}$ and minimum duty cycle $D_{\min}$.

duty cycle of this inverter increases, the maximum effective duty cycle of this inverter decreases.

IV. Optimal Parameter Design

A. Design Methodology

1) Assume the input dc voltage is *E* and the output maximum load current is $i_{a\max}$.
2) The maximum commutation time $(\delta_{t11}+\delta_{t12})$ should meet (36).
3) Design of the main resonant capacitor C_a and the second auxiliary resonant capacitor C_c.
   The optimal parameter design condition of the DACC is making the current through the DACC equal to the load current at the commutation moment when the load current reaches to the maximum value. So, in order to avoid the superposition of resonance current and load current when S_3 is turned ON, main resonant capacitor C_2 and the second auxiliary resonant capacitor C_5 should fully discharge during δ_{t11} (seeing mode 1 in Figs. 6 and 7). According to (5), δ_{t11} should meet

$$\delta_{t11} \geq \frac{E(2C_a+C_c)}{i_{a\max}}. \tag{42}$$

   If the value of C_a meets the condition of ZVS turn-off for main switches, it can be set to a very small value that can be negligible.
   According to (34) and (42), the values of C_a and C_c can be calculated.
4) Design of the first auxiliary resonant inductor L_a.

In order to meet the condition of ZVS turn-on for main switches, during δ_{t12}, the circuit should finish the commutation of load current from freewheeling diode D_2 to the first auxiliary resonant inductor L_1, and main resonant capacitor C_1 should fully discharge (seeing modes 3 and 4 in Figs. 6 and 7). According to (8) and (16), δ_{t12} should meet

$$\delta_{t12} \geq \frac{L_a}{E} i_{a\max} + \frac{\pi}{2}\cdot\sqrt{2L_aC_a}. \tag{43}$$

In order to meet the condition of ZVZCS turn-off for the second auxiliary switches, δ_{t3} should meet $\delta_{t3} \geq t_{6\text{–}7}$. According to (27), δ_{t3} should meet

$$\delta_{t3} \geq \frac{\pi}{2}\cdot\sqrt{L_aC_b}. \tag{44}$$

According to (35), (43), and (44), the value of L_a can be calculated.

During δ_{t12}, the current change rate of freewheeling diodes basically meets the condition of current change rate.

The voltage change rate of main switches during turn-off transient and the current change rate of freewheeling diodes during turn-off transient are determined by (34) and (35), respectively.

B. Design Example

In the following, a design example is explained. The input dc supply voltage *E* is 400 V and the output maximum load current $i_{a\max}$ is 50 A.

During δ_{t11}, assume the voltage change rate of main switches at turn-off transient is $dv/dt = 1000$ V/μs. According to (34) and (42), $2C_a + C_c = 50$ nF, $\delta_{t11} \geq 0.4$ μs. Take $C_a = 5$ nF, then $C_c = 40$ nF. As is known from the aforementioned analysis, $C_c \geq C_b$. Take $C_c = 2C_b$, then $C_b = 20$ nF.

During δ_{t12}, assume the current change rate of freewheeling diodes is $di/dt = 200$ A/μs. According to (35) and (43), $L_a = 2$ μH, $\delta_{t12} \geq 0.48$ μs. On the basis of analysis mentioned previously, $L_b \gg L_a$. Take $L_b = 20\ L_a$, then $L_b = 40$ μH.

During $(\delta_{t12}+\delta_{t2})$, to achieve ZVS turn-off for the first auxiliary switches (S_3, S_4), the voltage across C_3 must fall to zero, according to (38), $\delta_{t2} \geq 2.55$ μs $- \delta_{t12}$.

During δ_{t3}, to achieve ZVZCS turn-off for the second auxiliary switches (S_5, S_6), according to (44), the time δ_{t3} should meet $\delta_{t3} \geq 0.32$ μs.

According to the aforementioned analysis, δ_{t11} and δ_{t12} should meet $\delta_{t11} \geq 0.4$ μs and $\delta_{t12} \geq 0.48$ μs. So, the maximum commutation time should meet $(\delta_{t11}+\delta_{t12}) \geq 0.88$ μs.

V. Experimental Results

In order to demonstrate the validity of the aforementioned analysis, a 10-kW DARCP three-phase PWM soft-switching inverter prototype is built. The output line voltage is $200V_{\rm rms}$ and the output frequency f_o is 50 Hz. A three-phase *R–L* load is used in this prototype and $R = 4\,\Omega$, $L = 1$ mH. The parameters of the

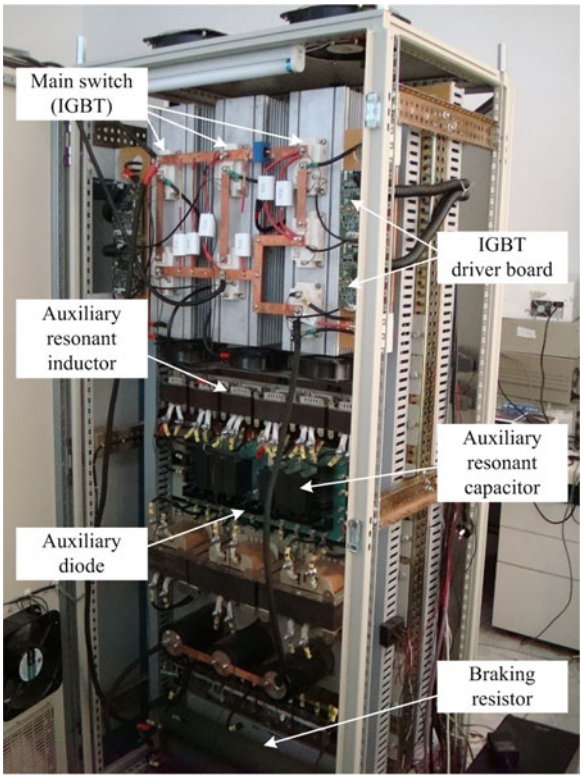

Fig. 10. Photo of the 10-kW three-phase soft-switching PWM inverter prototype.

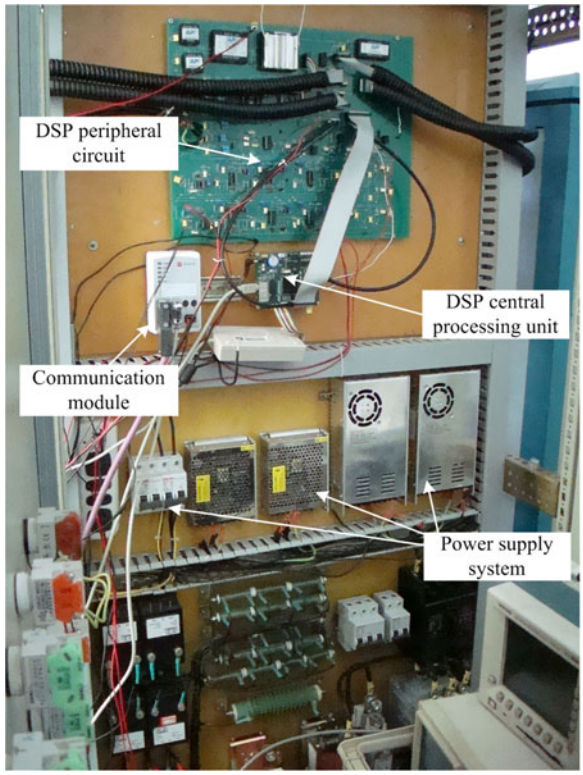

Fig. 11. Photo of the control and driver circuits.

modulation strategy are $\delta_{t11} = 1\ \mu$s, $\delta_{t12} = 2\ \mu$s, $\delta_{t2} = 1\ \mu$s, $\delta_{t3} = 0.4\ \mu$s, and $t_{dead} = 3\ \mu$s. Fig. 10 shows the photo of the three-phase soft-switching inverter prototype. Fig. 11 shows the photo of the control and drive circuits. The parameters of components in the circuit are shown in Table II.

TABLE II
COMPONENTS AND PARAMETERS OF THE INVERTER

Components	Parameters
Control board	DSP TMS320F2812
Driver board	SKHI23/17
Input DC voltage (E)	400 V
Switching frequency(f_S)	16 kHz
S_1 and S_2	SKM75GB063D(600 V,100 A)
$S_3 \sim S_6$	IRG4BC30F (600 V, 31 A)
$D_3 \sim D_{12}$	RHRG3060(600 V, 30 A)
C_1 and C_2	4.7 nF
C_3 and C_4	22 nF
C_5 and C_6	47 nF
L_1 and L_2	2 μH
L_3 and L_4	40 μH

A. Waveforms Evaluation

Fig. 12(a)–(f) shows the voltage and current waveforms of main switch S_1, the first auxiliary switch S_3, the second auxiliary switch S_5, and freewheeling diode D_2 in switching operations. Fig. 12(g) and (h) show the voltage and current waveforms of the second auxiliary resonant capacitor C_5 and the first auxiliary resonant inductor L_1. Fig. 12(a) shows the voltage and current waveforms of S_1 during turn-off transition. Fig. 12(b) shows the voltage and current waveforms of S_1 during turn-on transition. Fig. 12(c) shows the voltage and current waveforms of S_3 during switching transition. Fig. 12(d) shows the voltage and current waveforms of S_5 during switching transition. Fig. 12(e) shows the voltage and current waveforms of D_2 during turn-off transition. Fig. 12(f) shows the voltage and current waveforms of D_2 during turn-on transition. Fig. 12(g) shows the voltage and current waveforms of C_5. Fig. 12(h) shows the voltage and current waveforms of L_1. In Fig. 12, it is known that main switch S_1 achieves ZVS turn-on and ZVS turn-off, the first auxiliary switch S_3 achieves ZCS turn-on and ZVS turn-off, and the second auxiliary switch S_5 achieves ZVZCS turn-on and ZVZCS turn-off. Furthermore, it can be observed that the voltage across main switch S_1 during turn-off transient and the current through the first auxiliary switch S_3 during turn-on transient and freewheeling diode D_2 during turn-off transient vary linearly in Fig. 12(a), (c), and (e), respectively. So, the change rates can be set arbitrarily in the parameter design. In addition, according to Figs. 12 and 6, experimental waveforms in Fig. 12 are basically consistent with key theoretical waveforms in Fig. 6, which demonstrates the validity of the aforementioned theoretical analysis.

Under the original and novel modulation strategies, the waveforms of the voltage across C_5 and load current i_a (phase current) are shown in Fig. 13, and the waveforms of the current through L_1 and load current i_a are shown in Fig. 14. As shown in Figs. 13 and 14, it can be observed that the voltage across C_5 and the current through L_1 change with the load current i_a.

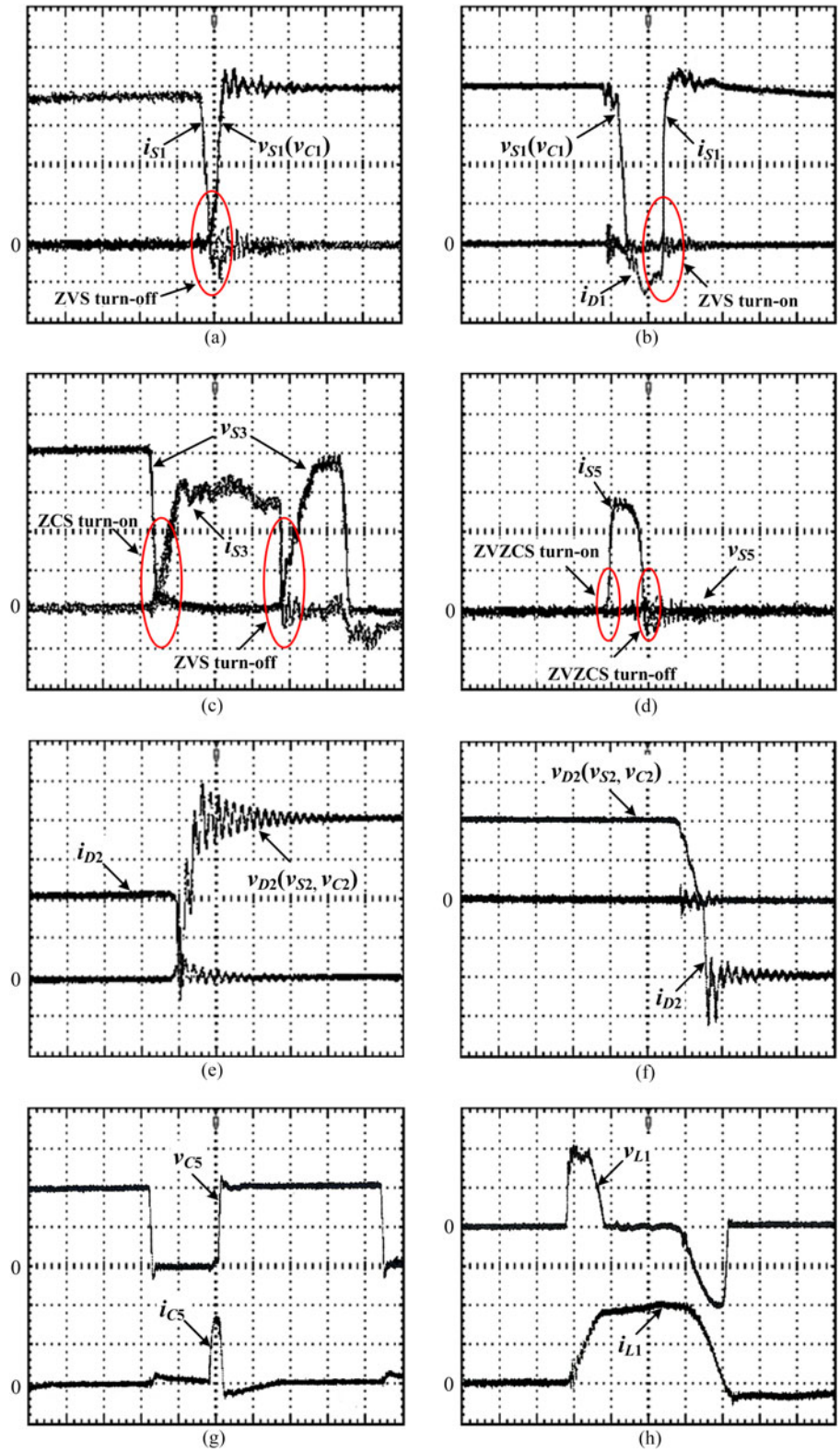

Fig. 12. Voltage and current waveforms of the proposed inverter. (a) Main switch S_1 turn-off (scales: 100 V/div, 10 A/div, 2 μs/div). (b) Main switch S_1 turn-on (scales: 100 V/div, 10 A/div, 1 μs/div). (c) First auxiliary switch S_3 turn-on and turn-off (scales: 100 V/div, 20 A/div, 1 μs/div). (d) Second auxiliary switch S_5 turn-on and turn-off (scales: 100 V/div, 20 A/div, 500 ns/div). (e) Freewheeling diode D_2 turn-off (scales: 100 V/div, 20 A/div, 1 μs/div). (f) Freewheeling diode D_2 turn-on (scales: 200 V/div, 20 A/div, 1 μs/div). (g) Second auxiliary resonant capacitor C_5 (scales: 200 V/div, 5 A/div, 10 μs/div). (h) First auxiliary resonant inductor L_1 (scales: 200 V/div, 30 A/div, 1 μs/div).

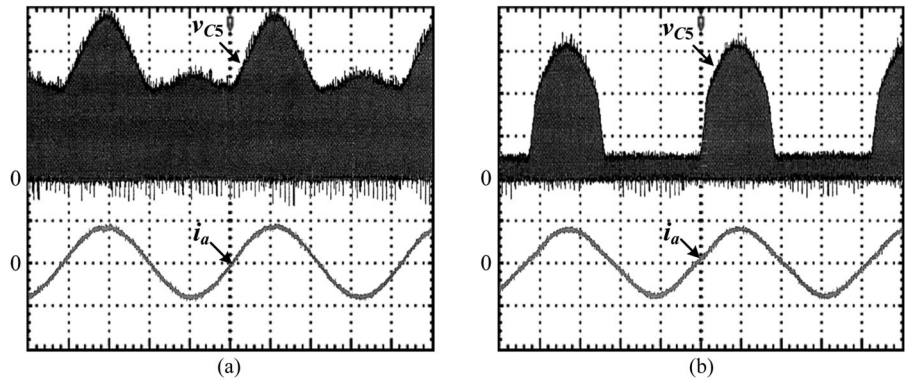

Fig. 13. Waveforms of the voltage across the second auxiliary resonant capacitor C_5 and load current i_a. (a) Waveforms under the original modulation strategy (scales: 100 V/div, 50 A/div, 5 ms/div). (b) Waveforms under the novel modulation strategy (scales: 100 V/div, 50 A/div, 5 ms/div).

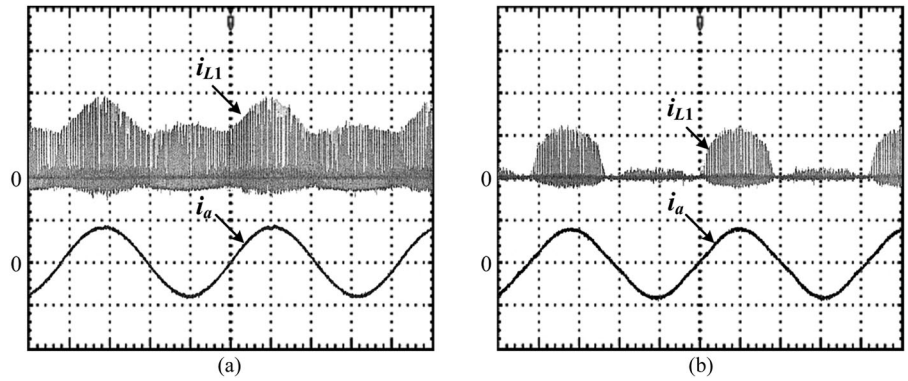

Fig. 14. Waveforms of the current through the first auxiliary resonant inductor L_1 and load current i_a. (a) Waveforms under the original modulation strategy (scales: 50 A/div, 5 ms/div). (b) Waveforms under the novel modulation strategy (scales: 50 A/div, 5 ms/div).

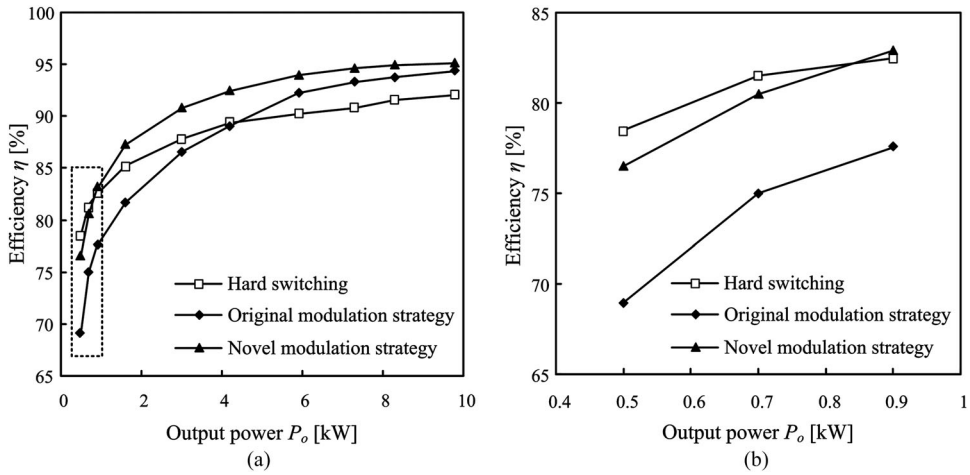

Fig. 15. Experimental efficiency curves. (a) Within whole load range. (b) Within light load range.

Under the original modulation strategy, by watching the waveforms of the voltage across C_5 and the current through L_1, it can be known that the voltage across C_5 and the current through L_1 still maintain a large value when load current i_a is in the reverse direction, which is caused by the resonance current. However, under the novel modulation strategy, the superposition voltage and current that are caused by resonance current are almost zero when the load current i_a is in the reverse direction. Because the experimental prototype installs two main resonant capacitors, there are tiny voltage and current values in C_5 and L_1 when the load current i_a is in the reverse direction.

B. Efficiency Evaluation

Fig. 15 shows the experimental efficiency curves of the DARCP inverter under the different modulation strategies and the conventional hard-switching inverter. In Fig. 15(a), we can

see that under the original modulation strategy, the efficiency of the DARCP inverter is higher than that of hard-switching inverter when the output power is larger than 50% of rated power (5 kW). When the output power is lower than 50% of rated power (5 kW), the DARCP inverter's efficiency under the original modulation strategy is unsatisfactory, even lower than the hard-switching inverter's efficiency, especially in light load range. And the lighter the load is, the more unsatisfactory the efficiency of the DARCP inverter will be [as shown in Fig. 15(b)]. However, under the novel modulation strategy, the DARCP inverter's efficiency in the whole load range is higher than that under the original modulation strategy and the hard-switching inverter's efficiency. Even in the extremely light load range, the DARCP soft-switching inverter's efficiency under the novel modulation strategy also closes to the hard-switching inverter's efficiency [as shown in Fig. 15(b)]. In comparison with the original modulation strategy, the average conversion efficiency under the novel modulation strategy is improved about 5% when the output power is lower than 50% of rated power [as shown in Fig. 15(a)]. Furthermore, the lighter the load becomes, the more the efficiency will be improved obviously [as shown in Fig. 15(b)].

VI. Conclusion

Aimed at the problem that the ACC of ARCP inverters has a high loss in commutation processes, this paper presents a novel modulation strategy based on a DARCP inverter. By theoretical analysis and experiment on the 10-kW DARCP inverter prototype, the soft-switching inverter under the novel modulation strategy has the following features.

1) Main switches achieve ZVS turn-on and ZVS turn-off. The first auxiliary switches achieve ZCS turn-on and ZVS turn-off. The second auxiliary switches achieve ZVZCS turn-on and ZVZCS turn-off. It is beneficial to reduce the switching loss and further improve the switching frequency.
2) The voltage across main switches during turn-off transient and the current through freewheeling diodes during turn-off transient vary linearly and their change rates can be set arbitrarily in the parameter design, which can restrict the production of EMI and reduce the reverse recovery loss of freewheeling diodes.
3) The novel modulation strategy can avoid the superposition of resonance current and load current at commutation moments in DACCs, and make the maximum current through the DACC approach to the load current in commutation processes. This characteristic is beneficial to reduce the loss of DACCs in commutation processes and the current stress of auxiliary switches.
4) In comparison with the original modulation strategy, the average conversion efficiency under the novel modulation strategy is improved about 5% when the output power is lower than 50% rated power. Furthermore, the lighter the load becomes, the more the efficiency will be improved obviously. So, the novel modulation strategy achieves the high conversion efficiency of the soft-switching inverter within the whole load range.

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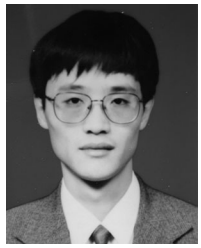

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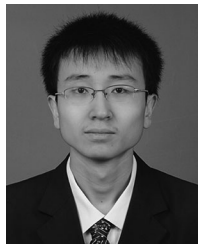

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