Optimization and Comparative Evaluation of Multiloop Control Schemes for Controllable AC Sources With Two-Stage LC Output Filters

David Olivier Boillat, *Member, IEEE*, Florian Krismer, *Member, IEEE*, and Johann Walter Kolar, *Fellow, IEEE*

***Abstract*—This study investigates the control system design and its small-signal properties for the output stage of a high-bandwidth four-quadrant three-phase switch-mode controllable AC voltage source (CVS) with an output power of 10 kW, a switching frequency of 48 kHz, and a two-stage LC output filter. Each output phase of the CVS is operated individually, i.e., the phase voltages are generated with reference to the DC input-voltage midpoint, to allow maximum flexibility in the generation of the output-voltage waveforms to supply a wide range of different load types, such as DC, single-phase, and general three-phase loads including constant-power loads leading to negative small-signal load-resistance values. Three suitable multiloop control structures with inner-current- and outer-voltage-control loops are motivated, modeled, and are optimized with respect to different control performance indicators, e.g., small-signal control bandwidth, and for common boundary conditions, e.g., maximum overshoot of the output voltage in case of a reference voltage step. All structures employ conventional P and PI controllers, due to their simplicity and widespread use. Among the three structures, the capacitor–current feedback-control structure, which controls the two filter capacitor currents and the output voltage, is identified to be most competitive. The small-signal bandwidth determined for this structure is between 7.1 kHz and 15.5 kHz, depending on the value of the load resistance. This result, in combination with an excellent matching of calculated and measured step responses of the output voltage of a 10 kW hardware prototype, point out the effectiveness of the selected control structure and the usability of control structures that are composed of conventional P and PI controllers.**

***Index Terms*—Boundary condition, large-signal, multiloop control scheme, multiobjective optimization, small-signal, three-phase controllable AC voltage source, two-stage *LC* filter.**

NOMENCLATURE

f_s	Switching frequency.
$T_s = 1/f_s$	Switching period.
T_0	Sampling period.
$v(t)$, $i(t)$, etc.	Continuous-time functions of voltages, currents, etc.
$x_k = x(kT_0)$	Discrete-time functions with sampling period T_0 and $k \in \mathbb{Z}$.
$X = X(s) = \mathcal{L}\{x(t)\}$	Laplace transform of the corresponding continuous-time function.
$X(z) = \mathcal{Z}\{x_k\}$	z-transform of the corresponding discrete-time function.
$\tilde{R}_{\mathrm{load}}$	Equivalent small-signal load resistance.

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The authors are with the Power Electronic Systems Laboratory, ETH Zürich, Zürich 8006, Switzerland (e-mail: boillat@lem.ee.ethz.ch; krismer@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

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I. INTRODUCTION

CONTROLLABLE AC voltage sources (CVSs) are in recent years emerging in the area of power-hardware-in-the-loop simulations to emulate mains connected loads/generators to analyze power grid dynamics and control strategies [1], [2], to emulate grid faults to test power electronic equipment [3]–[5], to emulate motor/generator characteristics to verify the correct operation of novel drive systems [6], [7], and to develop and conduct type tests on power electronic converters [8]–[11].

Fig. 1 depicts the output stage of the CVS considered in this study, which is a four-quadrant three-phase-plus-neutral-conductor three-level T-type voltage-source converter with a two-stage LC output filter, motivated in [12], and a balancer circuit composed of S_1, S_2, and L_{bal} that ensures in average equal DC-link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$, also in case of asymmetrical three-phase loads [13]. Table I lists the basic electrical specifications of this power converter and Table II summarizes the values of the filter components.

Since the CVS is intended to be used in a large number of different applications, it needs to be highly flexible regarding the connection of possible loads or generators. This includes linear loads, e.g., DC, single-phase AC, and three-phase AC (balanced and unbalanced) resistive and/or inductive loads [3], [8], [11], [14], [15], and nonlinear loads, e.g., constant-power loads [16], [17], diode rectifiers [3], [6], [14], and single-phase triac loads [8]. Furthermore, to test power electronic equipment in laboratory or according to international standards, the CVS may need to generate individual harmonics and/or transients in the output voltage of each phase [3]–[5], [18]. To achieve the required flexibility, the output voltages between the phases A, B, and C and the midpoint N (see Fig. 1) are controlled independently. The actual neutral is connected to the midpoint N of the DC link, i.e., serves as a reference point in case of a star connection of the load (or for connecting individual loads to the phases A, B, and C) in order to ensure maximum flexibility of the output-voltage generation; however, this requires that the output filter is realized without any inductive elements coupling the phases.

A buck-type power converter, essentially present in Fig. 1 if phase-independent control is applied, can, in principle, be controlled with solely an output-voltage controller, e.g., a

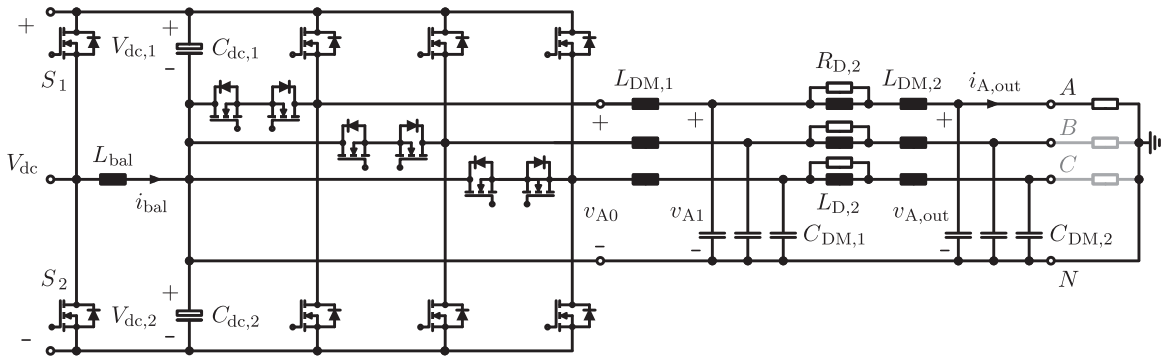

Fig. 1. Schematic drawing of the T-type three-phase-plus-neutral-conductor output stage of the CVS including a two-stage LC output filter.

TABLE I
ELECTRICAL SPECIFICATIONS OF THE POWER CONVERTER EMPLOYED FOR THE REALIZATION OF THE OUTPUT STAGE OF THE CONSIDERED CVS, CF., FIG. 1

Nominal output power, $P_{\mathrm{out,n}}$	10 kW
Nominal rms output voltage, $V_{\mathrm{A,out,n}}$ (line to neutral)	230 V
Nominal peak output voltage, $V_{\mathrm{A,out,n,pk}}$ (line to neutral)	325 V
Max. peak output voltage, $V_{\mathrm{A,out,max,pk}}$ (line to neutral)	350 V
Nominal DC-link voltage, $V_{\mathrm{dc,n}} = V_{\mathrm{dc,1,n}} + V_{\mathrm{dc,2,n}}$	700 V
Nominal rms output current, $I_{\mathrm{A,out,n}}$	14.5 A
Nominal peak output current, $I_{\mathrm{A,out,n,pk}}$	20.5 A
Output frequency, f_{out}	0–300 Hz
Switching frequency, f_s	48 kHz
Sampling frequency, f_0	96 kHz
Efficiency, η	$\geq 98.5\%$

TABLE II
COMPONENT VALUES OF THE CONVERTER'S TWO-STAGE LC OUTPUT FILTER CF., FIG. 1 (FROM [12])

$L_{\mathrm{DM,1}}$	154.2 µH
$C_{\mathrm{DM,1}}$	4.7 µF
$L_{\mathrm{DM,2}}$	11.7 µH
$C_{\mathrm{DM,2}}$	4.1 µF
$L_{\mathrm{D,2}}$	22.4 µH
$R_{\mathrm{D,2}}$	1.34 Ω

PI controller, provided that the resonances of the output filter are sufficiently attenuated. A recent publication [19] shows that a single modified PI output-voltage controller can control a buck converter single-stage LC output filter such that almost time-optimal reactions to load transients are achieved (this modified PI controller simultaneously considers the output voltage and an estimate of the filter capacitor current). In particular in the light of [19], further improvements possibly achievable with advanced – linear and nonlinear – control concepts remain unclear to a certain extent. Even though comparisons of control performances achieved with conventional PI to advanced controllers are found in the literature, e.g., [20]–[24], the selected conventional realizations are either not explained in detail, not fully optimized, or the respective discussion reveals that the conventionally controlled system does not incorporate load current and reference voltage feedforwards and/or delay compensations, which, in this study, are both found to be crucial for obtaining fast responses with little output-voltage overshoots.

For this reason and due to the P and PI controllers being well understood and accepted by design engineers, this paper details the optimizations of P and PI controllers of three control structures suitable for the considered CVS such that, in the events of voltage reference and load steps, the output voltage is stabilized within the minimum possible duration (for a given maximum transient overshoot). The investigated control structures are implemented on a digital control platform, i.e., only digital controllers are considered, which also provides the digital pulse-width modulators, operated with constant switching frequency, that generate the gate signals for the transistors. In contrast to [19], this study investigates the control of an inverter circuit with a two-stage LC filter, i.e., an LC filter, for a wide range of operating conditions and does not rely on the values of parasitic components. Since the CVS may be operated with a UPS [8], a solar inverter [9], or another CVS [1] being connected, the controller design takes different load conditions, including constant-active-power loads, into account. In this regard, the small-signal representations of constant-active-power loads are operating-point-dependent negative load resistances [17], [25]–[28], which are found to destabilize the interaction between the converter (including the output filter) and the load, and are, thus, of particular interest with respect to stable and robust converter operation.

In this paper, Section II presents the derivations of the three considered control structures, which take the possible presence of a constant-power load and the corresponding negative small-signal load-resistance values [25], [29] into consideration. The optimizations of the three control structures are detailed in Section III and verified by means of experimental results in Section IV. For the given specification and filter components, in particular for the given range of small-signal load resistances including negative values, it is shown in Section IV that the controllers stabilize the output voltage within only a few switching periods, i.e., within 97 µs [approx. 4.7 switching periods, Fig. 17(b)] in the event of a reference voltage step at rated output power and within 49 µs [approx. 2.4 switching periods, Fig. 18(b)] in case of a load step. The obtained results, thus, represent an excellent basis for industrial designs or for future comparisons to advanced, e.g., nonlinear and/or adaptive, control concepts.

II. DERIVATION OF THE INVESTIGATED CONTROL STRUCTURES

This section derives the control structures considered for each phase of the CVS with the two-stage LC filter depicted in Fig. 1. These control structures are the basis for the optimization

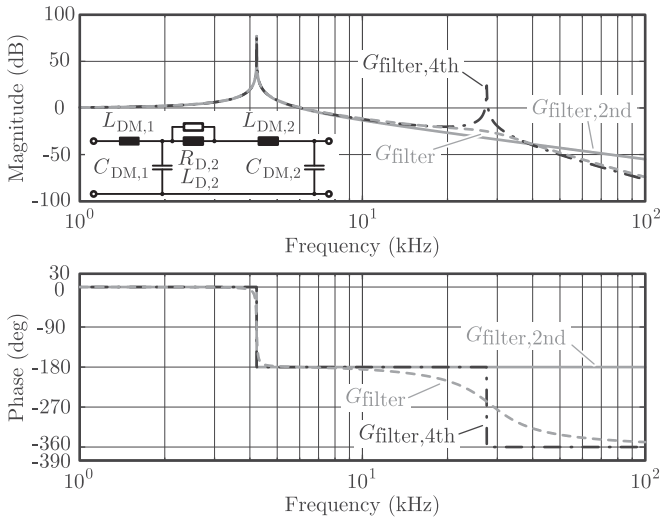

Fig. 2. Bode plots of accurate (G_{filter}) and simplified ($G_{\mathrm{filter,2nd}}$, $G_{\mathrm{filter,4th}}$) input-to-output transfer functions of the filter without load: amplitude response (top) and phase response (bottom).

detailed in Section III. *Only phase A is considered throughout this study,* since each phase is controlled independently. The obtained results are directly applicable to phases B and C.

The two-stage LC filter, optimized in [12], is essentially composed of two LC filter stages. Due to the relatively large value of $C_{\mathrm{DM,2}} \approx C_{\mathrm{DM,1}}$, cf., Table II, and the low inductances of the second filter stage, $L_{\mathrm{DM,2}} + L_{\mathrm{D,2}} \ll L_{\mathrm{DM,1}}$, the two filter stages cannot be looked at independent from each other. Fig. 2 depicts the Bode diagram of the two-stage LC filter's input-to-output-voltage transfer function, G_{filter}, with a passive series $R_{\mathrm{D,2}}L_{\mathrm{D,2}}$ damping branch, cf., Fig. 1. At no load, this transfer function has one real zero at $-59.8 \times 10^3\ \mathrm{s}^{-1}$ and five poles at

$$\begin{aligned} s_1 &= -75.8 \times 10^3\ \mathrm{s}^{-1} \\ s_{2,3} &= (-49.1 \pm \mathrm{j}\,173) \times 10^3\ \mathrm{s}^{-1} \\ s_{4,5} &= \left(-164 \pm \mathrm{j}\,26.6 \times 10^3\right)\ \mathrm{s}^{-1}. \end{aligned} \tag{1}$$

The real pole, s_1, approximately compensates the real zero and the remaining complex conjugated pole pairs correspond to resonance or crossover frequencies of $f_1 = 4.2$ kHz and $f_2 = 27.5$ kHz, respectively. With the damping network being neglected, the considered output filter can be approximated with the series connection of two reactionless second-order low-pass filters according to

$$G_{\mathrm{filter,2nd}}(s) = \frac{1}{1 + \left(\frac{s}{2\pi f_1}\right)^2} \tag{2}$$

and

$$G_{\mathrm{filter,4th}}(s) = \frac{1}{1 + \left(\frac{s}{2\pi f_1}\right)^2} \frac{1}{1 + \left(\frac{s}{2\pi f_2}\right)^2} \tag{3}$$

cf., Fig. 2.

Besides these findings, two further important properties are associated with this output filter.

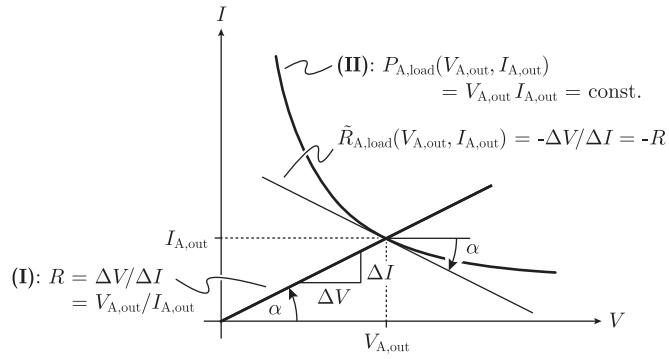

Fig. 3. Voltage–current-characteristic of **(I)** a resistor with resistance R and **(II)** a constant-active-power load with $P_{\mathrm{A,load}} = \mathrm{constant}$.

1) The first crossover frequency, $f_1 = 4.2$ kHz, is less than the achieved control bandwidths for all considered control structure, which, in anticipation of the results presented in Section III-C, are in the range between 6 kHz and 7 kHz. It is thus possible to attenuate the resonance at f_1 by means of active damping.
2) The second crossover frequency, $f_2 = 27.5$ kHz, is greater than the achieved control bandwidths and active damping cannot be applied. For this reason, passive damping is considered, which is effectively achieved with the $R_{\mathrm{D,2}}L_{\mathrm{D,2}}$ damping network depicted in Fig. 2.

According to Fig. 2, a single second-order low-pass filter with cutoff frequency f_1, e.g., achieved with $L_1 = 161\ \mu\mathrm{H} \approx L_{\mathrm{DM,1}}$ and $C_1 = 8.8\ \mu\mathrm{F}$, can be used to approximate the transfer function of the output filter for frequencies up to the maximum of the achieved control bandwidth of 7.2 kHz. For this reason, the second filter stage is first disregarded in Section II-A to allow for a simplified derivation of the considered control structures. Still, the second filter stage introduces a phase shift between its input and output voltages, v_{A1} and $v_{\mathrm{A,out}}$ in Fig. 1, also at frequencies below 7.2 kHz, which is accounted for in Section II-B and leads to a refinement of the control structures.

The CVS may be operated with passive and active loads, e.g., constant-power loads, within the limits specified in Table I. By way of example, Fig. 3 illustrates the voltage–current-characteristic of a constant-active-power dc load connected to phase A of the CVS [curve (II) in Fig. 3]. The slope of the load characteristic, $\mathrm{d}V/\mathrm{d}I$, evaluated at the operating point defined with $V_{\mathrm{A,out}}$ and $I_{\mathrm{A,out}}$, gives the small-signal load resistance [25]

$$\tilde{R}_{\mathrm{A,load}} = \frac{\mathrm{d}v_{\mathrm{A,out}}}{\mathrm{d}i_{\mathrm{A,out}}} = -\frac{V_{\mathrm{A,out}}^2}{P_{\mathrm{A,load}}}. \tag{4}$$

With $P_{\mathrm{A,load}} = V_{\mathrm{A,out}} I_{\mathrm{A,out}}$ expression (4) can be converted to $\tilde{R}_{\mathrm{A,load}} = -V_{\mathrm{A,out}}/I_{\mathrm{A,out}}$, i.e., the small-signal model of a constant-active-power load at a certain operating point, defined by $V_{\mathrm{A,out}}$ and $I_{\mathrm{A,out}}$, is a resistance and its value is equal to the negative resistance value of a load resistor, $R = +V_{\mathrm{A,out}}/I_{\mathrm{A,out}}$, at the same operating point [curve (I) in Fig. 3].

A detailed investigation of the small-signal properties of three-phase AC loads and single-phase loads (DC and AC),

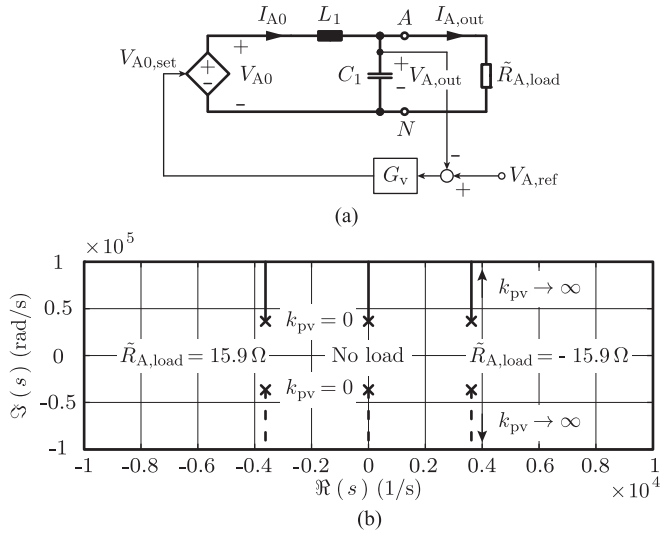

Fig. 4. (a) Output-voltage-control structure with minimum complexity applied to a single-stage LC filter. (b) Root locus calculated for the closed-loop transfer function $V_{A,out}(s)/V_{A,ref}(s)$ for $L_1 = 161$ µH, $C_1 = 8.8$ µF, a P controller, $G_v = k_{pv}$, and for different small-signal load resistances, $\tilde{R}_{A,load}$.

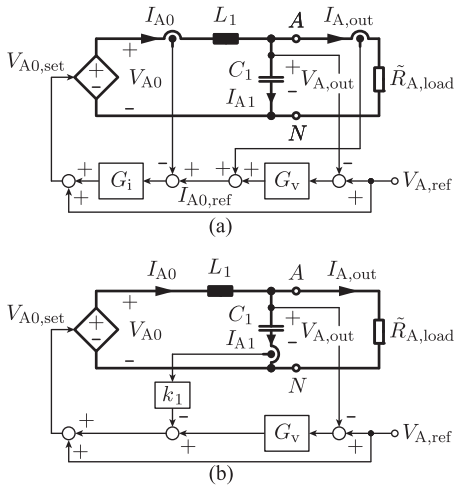

Fig. 5. (a) Commonly employed configuration with an inner-current-control loop for I_{A0} and an outer-voltage-control loop for $V_{A,out}$ to introduce active damping. (b) Alternative implementation with an inner capacitor–current feedback loop and an outer-voltage-control loop [30], [31].

reveals that the small-signal load resistance, $\tilde{R}_{A,load}$, changes within the range

$$\frac{1}{-15.9\ \Omega} \leq \frac{1}{\tilde{R}_{A,load}} \leq \frac{1}{15.9\ \Omega} \tag{5}$$

for converter operation with the following loads:

1) Three-phase resistive AC loads with $P_{load} = P_{out,n} = 10$ kW and $V_{X,out} \geq V_{X,out,n} = 230$ V ($X = A, B, C$; RMS, line to neutral),
2) Three-phase constant-active-power AC loads with $P_{load} = P_{out,n} = 10$ kW and $V_{X,out} \geq V_{X,out,n} = 230$ V ($X = A, B, C$; RMS, line to neutral),
3) Single-phase resistive loads (AC or DC) with $P_{A,load} = 3.33$ kW and $V_{A,out} \geq V_{A,out,n} = 230$ V (RMS or DC, line to neutral),
4) Single-phase constant-active-power loads (AC or DC) with $P_{A,load} = 3.33$ kW and $V_{A,out} \geq V_{A,out,n} = 230$ V (RMS or DC, line to neutral).

A. Simplified Investigation: Single-Stage LC Filter

The minimum imaginable control structure is a single-output voltage-control loop, depicted in Fig. 4(a), where the pulse width modulation (PWM) unit and the T-type bridge-leg are replaced by a controlled voltage source. The controller G_v alters the adjustable voltage source such that the output voltage follows the desired reference voltage, $V_{A,ref}(s) = \mathcal{L}\{v_{A,ref}(t)\}$. The control structures are investigated in the Laplace domain, and, therefore, the following figures with control parts use capital letters for all currents and voltages according to the Nomenclature defined at the beginning of this study.

In a first step and to obtain simple as well as comprehensive relationships between important system quantities, it is assumed that the time delay due to the digital control (cf., Section II-B) can be perfectly compensated. Conventional P and PI controllers, commonly used in power electronics, cannot stabilize this system for all regarded load conditions (and assumed lossless filter components), due to the filter being undamped and due to possible negative load resistances, cf., (5). In case of a P controller, $G_v = k_{pv}$, for example, and for $L_1 = 161$ µH and $C_1 = 8.8$ µF the root locus depicted in Fig. 4(b) is calculated for the closed-voltage-control loop: stable operation is only achievable for $\tilde{R}_{A,load} \geq 0$, since a pole-pair in the right half-plane, of which the real part is independent of k_{pv}, results for $\tilde{R}_{A,load} < 0$ (for the PI controller, a similar result is obtained). For this reason, multiloop control structures are considered in the following.

1) Two-Loop Control Structure: The commonly used configuration depicted in Fig. 5(a) can be used to introduce active damping to an undamped LC filter stage [32], [33] and represents the basis of two of the control structures evaluated in the scope of this study. This configuration is composed of an inner-current-control loop that controls the inductor current I_{A0} and a superordinate output-voltage-control loop to control $V_{A,out}$. Fig. 5(a), furthermore, includes a load current feedforward and a reference voltage feedforward. The summation of the measured output current to the voltage controller's output value establishes the load current feedforward and allows the current controller, G_i, to quickly adapt to a changing load current. The reference voltage feedforward, which adds the reference voltage $V_{A,ref}$ to the output value of the current controller, takes advantage of V_{A0} being a rather linear adjustable voltage source (in terms of an averaged model) and improves the dynamic response of the output voltage when the reference voltage changes.

In the presence of positive and negative small-signal load resistances $\tilde{R}_{A,load}$, a detailed stability analysis identifies a PI controller to be unsuitable for current control, therefore a P controller is used instead. For the voltage-control loop, a PI controller is found to be more suitable than a P controller (no steady-state error for DC reference voltages). Furthermore,

the maximum occurring negative load resistance value, here $\tilde{R}_{\mathrm{A,load}} = -15.9\ \Omega$, is identified to be a critical design parameter regarding stable converter operation.

2) Capacitor–Current Feedback-Control Structure [see Fig. 5(b)]: The capacitor current is an AC current and is equal to the inductor current minus the load current. Its dynamic (AC) component is therefore closely related to the AC components of the inductor and load currents and for this reason overall good control performances, cf., Section III-C, in case of reference and load changes are expected. Furthermore, it is shown in [31] that, for the case of no load, the capacitor–current feedback emulates a resistor, $R_1 = k_1$, connected in series to L_1, cf., Fig. 4(a) and (b) in [31]. This emulated resistor causes no losses (except negligible losses in the current sensor) but still introduces damping. For this reason, stable closed-loop output-voltage regulation is feasible with the concept shown in Fig. 5(b) even in the presence of a negative small-signal load resistance. A further advantage of the concept shown in Fig. 5(b) is the property of the capacitor current being a pure AC current, which allows for the use of an AC current sensor. The capacitor–current feedback-control structure, however, features neither inductor nor output current limitation options, since the respective DC current components are unknown.

A detailed stability analysis conducted for this control structure reveals that the maximum occurring negative small-signal load resistance value, $\tilde{R}_{\mathrm{A,load}} = -15.9\ \Omega$, is most critical with respect to stable converter operation also for this control structure.

B. Detailed Investigation: Two-Stage LC Filter

According to [12], the CVS requires a two-stage LC output filter and, hence, additional state variables are available for the control of the output voltage. Fig. 6 depicts the three control concepts considered for evaluation: Fig. 6(a) directly applies the control structure of Fig. 5(a) to the two-stage filter (in Section II-A1 a P controller has been suggested for current control); Fig. 6(b) applies the control structure of Fig. 5(b) to the two-stage filter and considers both capacitor currents, $I_{\mathrm{A1}}(s)$ and $I_{\mathrm{A2}}(s)$ to take advantage of the additionally available capacitor current[1]; and Fig. 6(c) is based on the two-loop control structure of Fig. 5(a), which employs a P controller in an inner-current-control loop and a second P controller in a superordinate loop that controls the output voltage of the first filter stage, $V_{\mathrm{A1}}(s)$. According to the initial considerations detailed in this section, $V_{\mathrm{A,out}}(s) \approx V_{\mathrm{A1}}(s)$ applies for frequencies up to the output-voltage-control bandwidth. Any remaining gain and phase errors between $V_{\mathrm{A,out}}(s)$ and $V_{\mathrm{A1}}(s)$ are eliminated with the use of a second voltage controller (PI controller) for $V_{\mathrm{A,out}}$ in Fig. 6(c). The proposed structure prefers the parallel operation of the two voltage controllers to a solution with a third control loop in order to not sacrifice the achievable closed-loop output-voltage-control bandwidth. For stabilizing $V_{\mathrm{A,out}}$, a PI controller is used

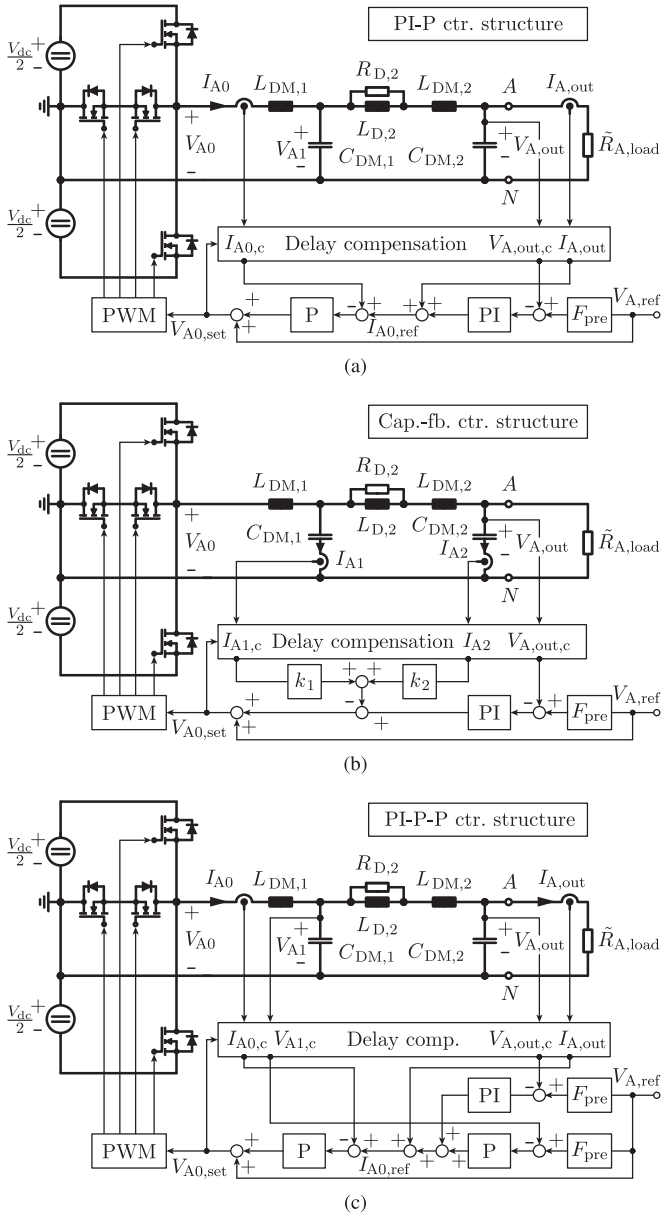

Fig. 6. Control structures suitable for the two-stage LC filter identified in this study: (a) PI-P control structure, (b) capacitor–current feedback-control structure, and (c) PI-P-P control structure.

to eliminate steady-state errors of the output voltage. Only a P controller stabilizes V_{A1} since, in a practical environment, it has been found that the control circuit does not work properly if two integrators are operated in parallel, i.e., the two integrators conflict with each other.

The final control structures shown in Fig. 6 include delay compensations according to [34] to lower the impacts of time delays, caused by the digital control system, on the achievable output-voltage-control bandwidth. Only the output current, $I_{\mathrm{A,out}}$, is excluded from this prediction, since the output current is mainly used to react on a load change, which the employed algorithm cannot predict. A derivation of the small-signal model of the delay compensations for $i_{\mathrm{A0}}(t)$ and $v_{\mathrm{A,out}}(t)$, for example,

[1]It can be considered that the capacitor current $I_{\mathrm{A1}}(s)$ more reflects the ac component of the inductor current $I_{\mathrm{A0}}(s)$ and $I_{\mathrm{A2}}(s)$ more reflects the ac component of the load current $I_{\mathrm{A,load}}(s)$ due to the separating effects of $L_{D,2}$ and $L_{\mathrm{DM},2}$.

TABLE III
FACTORS $k_{c,1} \ldots k_{c,8}$, CF., (6) AND (7), USED FOR THE DELAY COMPENSATIONS IN THE PI-P CONTROL STRUCTURE, CF., FIG. 6(A)

$k_{c,1}$	$\frac{3}{2}\frac{T_0}{L_{DM,1}}$
$k_{c,2}$	$-\frac{3}{2}\frac{T_0}{L_{DM,1}}$
$k_{c,3}$	$1-\frac{9}{16}\frac{T_0^2}{(C_{DM,1}+C_{DM,2})L_{DM,1}}$
$k_{c,4}$	$\frac{9}{16}\frac{T_0^2}{(C_{DM,1}+C_{DM,2})L_{DM,1}}$
$k_{c,5}$	$\frac{9}{16}\frac{T_0^2}{(C_{DM,1}+C_{DM,2})L_{DM,1}}$
$k_{c,6}$	$1-\frac{9}{16}\frac{T_0^2}{(C_{DM,1}+C_{DM,2})L_{DM,1}}$
$k_{c,7}$	$\frac{3}{2}\frac{T_0}{C_{DM,1}+C_{DM,2}}$
$k_{c,8}$	$-\frac{3}{2}\frac{T_0}{C_{DM,1}+C_{DM,2}}$

gives

$$i_{A0}(t_0+T_d) = k_{c,1}\, v_{A0,ref}(t_0) + k_{c,2}\, v_{A,out}(t_0) + k_{c,3}\, i_{A0}(t_0) + k_{c,4}\, i_{A,out}(t_0) \quad (6)$$

$$v_{A,out}(t_0+T_d) = k_{c,5}\, v_{A0,ref}(t_0) + k_{c,6}\, v_{A,out}(t_0) + k_{c,7}\, i_{A0}(t_0) + k_{c,8}\, i_{A,out}(t_0). \quad (7)$$

The factors $k_{c,1} \ldots k_{c,8}$ in (6) and (7) are constant factors. Table III lists the respective expressions (similar results are obtained for the remaining delay compensations). Moreover, $T_d = 1.5T_0 = 15.6\ \mu s$ and

$$T_0 = \frac{1}{2}\frac{1}{f_s} = 10.4\ \mu s \quad (8)$$

denote the time delay of the considered hardware system and the sampling time of the digital controller (double update mode PWM), respectively.

This work approximates the time delay of half a sampling period by means of a Thiran filter [35] and, thus

$$\mathcal{Z}\left\{\mathcal{L}^{-1}\left\{e^{-s\,3T_0/2}\right\}\right\} \approx \frac{1}{z}\frac{z+3}{3z+1} \quad (9)$$

approximately represents the time delay of $T_d = 1.5T_0$ in the z-domain.

All control structures of Fig. 6 employ a first-order digital prefilter

$$F_{pre}(z) = \left(1+\frac{2T_{pre}}{T_0}\frac{z-1}{z+1}\right)^{-1} \quad (10)$$

to achieve similar transient error signals at the input of the voltage controller in case of voltage reference and load steps, and hence, to realize similar responses of the output voltage in both cases [36].

This study conducts the investigations of the transfer functions in continuous-time and uses the Tustin approximation,

$$s = \frac{2}{T_0}\frac{z-1}{z+1} \quad \Leftrightarrow \quad z = \frac{2+sT_0}{2-sT_0} \quad (11)$$

to approximately convert discrete-time transfer functions, that originate from the implementation on the digital control system, to continuous-time.

A detailed inspection of the step response of the power stage reveals that a resistance of $R_{DM,1} = 192\ m\Omega$, which arises from the inductor and the output stage of the power converter [37], is considered in series to the inductor $L_{DM,1}$.

III. OPTIMIZED CONTROLLER DESIGN

This study conducts four separate optimizations for each considered control structure, with respect to the four evaluation quantities (EQs) listed below and with all conducted controller designs being subject to the boundary conditions given in Section III-A. Section III-B explains the optimization algorithm and Section III-C discusses the obtained results.

1) Reference tracking I—small-signal bandwidth, $f_{bw,ss}$: The higher the small-signal -3 dB bandwidth of the control structure the better the reference tracking capability of the CVS. The CVS shall be capable of generating sinusoidal output voltages with frequency components that are considerably greater than the mains frequency; therefore, a high small-signal bandwidth is of particular interest [38].
2) Reference tracking II—integrated squared voltage error after a reference step, $e^2_{ev,vref}$: The output voltage, $v_{A,out}$, should follow the reference with the smallest possible deviation. A measure for this can be obtained by integrating the square of the voltage error, $e^2_{ev,vref} = (v_{A,ref} - v_{A,out})^2$, until the output voltage remains within a certain tolerance band from the reference value [39]

$$e^2_{ev,vref} = \int_0^{t_{set,vref}} \times \left[\underbrace{v_{A,ref}(t)}_{\text{step change}} - \underbrace{v_{A,out}(t)}_{\text{changes due to change of } v_{A,ref}}\right]^2 dt \quad (12)$$

where $t_{set,vref}$ denotes the point in time after which the output voltage stays within a deviation band of $\pm 1\%$

$$\left|\frac{v_{A,out}(t) - v_{A,ref}(t)}{v_{A,ref}(t)}\right| \le 1\% \ \forall\ t \ge t_{set,vref}. \quad (13)$$

The optimization aims to keep $e^2_{ev,vref}$ as small as possible.
3) Disturbance rejection I—integrated voltage error squared after a step in the load current, $e^2_{ev,iload}$: A load step triggers a transient change of the output voltage. The resulting difference between reference and output voltages, $v_{A,ref} - v_{A,out}$, should be as small as possible. This can

be characterized by

$$e^2_{\mathrm{ev,iload}} = \int_0^{t_{\mathrm{set,iload}}} \times \left[\underbrace{v_{\mathrm{A,ref}}(t)}_{\text{remains unchanged}} - \underbrace{v_{\mathrm{A,out}}(t)}_{\text{changes due to load step}} \right]^2 \mathrm{d}t \tag{14}$$

where $t_{\mathrm{set,iload}}$ is the point in time after which the output voltage remains within a deviation band around the reference value of 1%, cf., (13).

4) Disturbance rejection II—output impedance, $Z_{\mathrm{A,out}}$, at $f = 3$ kHz[2]. The output impedance can be used to describe the implication of the output current, $-I_{\mathrm{A,out}}(\mathrm{j}\omega)$, on the output voltage, $V_{\mathrm{A,out}}(\mathrm{j}\omega)$, with respect to magnitude and phase; $|Z_{\mathrm{A,out}}| \ll |R_{\mathrm{A,load}}|$ is needed for the output voltage to closely follow the reference voltage. For this reason, the optimization algorithm aims for a low output impedance.

A. Considered Boundary Conditions

The controller designs are based on pole placement, since the well-known gain- and phase-margin concepts may fail in presence of a negative small-signal load resistance (unstable transfer functions of the filter with load in Fig. 6). The poles of any closed-loop transfer function of the systems depicted in Fig. 6 are located inside the area restricted by the linear boundaries depicted in Fig. 7(a) (θ denotes the angle between the imaginary axis and the pole). According to [40], $\theta_{\min} = 12\,^\circ$ is a reasonable compromise between a quick step response and adequate stability margin.

The maximum relative overshoot M_{v} of the output voltage, excited by a reference voltage step, is limited to less than 10% to only consider controller designs which achieve a tight output-voltage control. Furthermore, results that lead to settling times of the output voltage, $t_{\mathrm{set,vref}}$, greater than 1 ms are disregarded (settling times considerably less than 1 ms are expected for the given output filter [12]).

In the event of a load step, the value of M_{i}, which is related to the resulting overshoot of the output voltage and is defined in Fig. 7(b), is limited to 20% of the height of the voltage dip $\Delta V_{\mathrm{A,out}}$ to achieve a tight output-voltage control after load steps. Additionally, the settling time $t_{\mathrm{set,iload}}$ after a load step is limited to 1 ms.

The pole placements, the voltage overshoots, and $t_{\mathrm{set,vref}}$ are calculated for three different load situations, $\tilde{R}_{\mathrm{A,load}} = [-15.9\ \Omega,\ 10\ \mathrm{M}\Omega,\ 15.9\ \Omega]$ ($\tilde{R}_{\mathrm{A,load}} = 10\ \mathrm{M}\Omega$ approximates the no load situation). The amplitude of the reference voltage step is 20 V. For the load step, a current-source type of load is employed and the step amplitude is $25\% \times I_{\mathrm{A,out,n}} = 25\% \times 14.5\ \mathrm{A} = 3.6$ A. Thus, the calculated output-voltage transients due to a load step are independent of the load situation.

[2]A frequency much greater than the mains frequencies (50 or 60 Hz) is selected in order to take the technically more challenging capability of the CVS of generating the output signals with higher frequencies into consideration. Still, this frequency is selected such that $Z_{\mathrm{A,out}}(f)$ is evaluated well inside the achieved control bandwidths (between 6 kHz and 7 kHz, cf., Table IV). For this reason, $f = 3$ kHz, 60 Hz $\ll f < 6$ kHz, is found to be suitable for the purpose of a comparison.

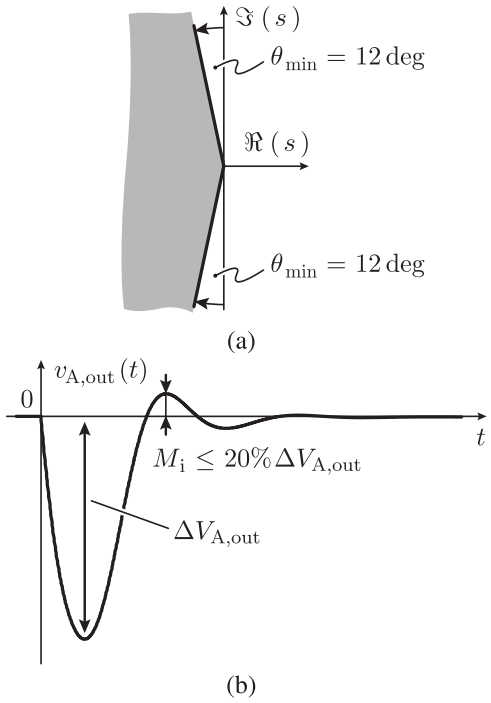

Fig. 7. (a) The gray shaded area denotes the allowed locations of the poles of the closed-current- and voltage-control loops in the Laplace domain to provide robustness to the control loops [40]. (b) Example of the response of the output voltage to a load step and related definitions of $\Delta V_{\mathrm{A,out}}$ and M_{i}.

Further constraints apply to the maximum gains of current and voltage controllers to keep random variations of the measured output voltage from the steady-state value, arising from measurement noise, smaller than ± 0.5 V. These limits have been determined by experiments carried out on the hardware prototype, cf., Section IV, and are listed below

PI-P ctr. structure:

$k_{\mathrm{pv}} k_{\mathrm{pi}} \leq 4.6\ \mathrm{V/V}$ and $k_{\mathrm{pi}} \leq 10\ \mathrm{V/A}$

Cap.-fb. curr.-ctr. structure:

$k_{\mathrm{pv}} \leq 4.6\ \mathrm{V/V}$, $k_1 \leq 10\ \mathrm{V/A}$, and $k_2 \leq 20\ \mathrm{V/A}$ (15)

PI-P-P ctr. structure:

$(k_{\mathrm{pv1}} + k_{\mathrm{pv2}}) k_{\mathrm{pi}} \leq 4.6\ \mathrm{V/V}$ and $k_{\mathrm{pi}} \leq 10\ \mathrm{V/A}$.

For the PI-P-P control structure, k_{pv1} and k_{pv2} are the gains of the voltage controllers for v_{A1} and $v_{\mathrm{A,out}}$, respectively.

B. Optimization Procedure

Fig. 8 depicts the flowchart of the algorithm used to optimize the controllers of the PI-P control structure depicted in Fig. 6(a).

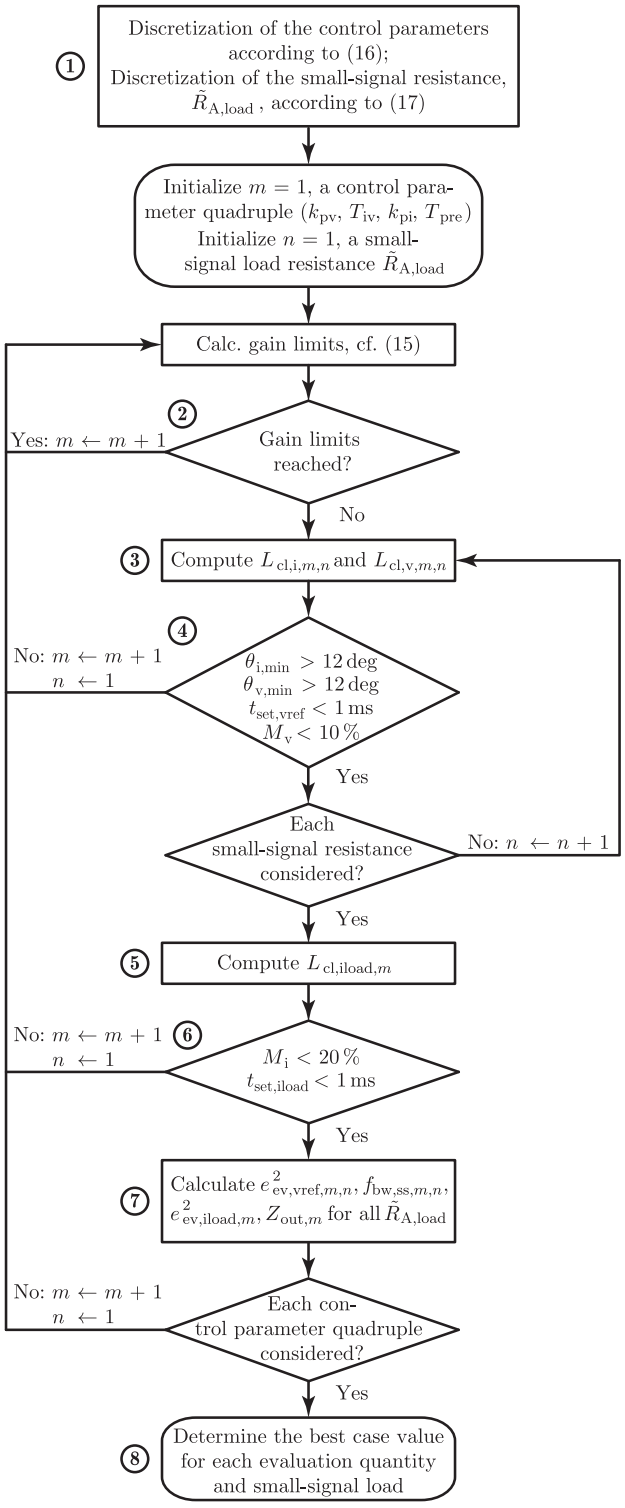

Fig. 8. Flowchart of the algorithm used to optimize the PI-P control structures with respect to the EQs and the boundary conditions defined in Section III. Similar algorithms apply to the remaining investigated control structures.

This optimization algorithm essentially remains the same for all control structures investigated in this study, only the closed-loop transfer functions change.

The algorithm first initiates a discrete search space according to geometric series, cf., ① in Fig. 8. For the PI-P control structure this is

$$\begin{aligned} k_{\mathrm{pv}} &= 10\ \mathrm{mA/V} \times 10^{\frac{i}{48}}, & 0 \le i \le 96, \quad i \in \mathbb{N}_0, \\ T_{\mathrm{iv}} &= 10\ \mu\mathrm{s} \times 10^{\frac{i}{48}}, & 0 \le i \le 144, \quad i \in \mathbb{N}_0 \\ k_{\mathrm{pi}} &= 1\ \mathrm{V/A} \times 10^{\frac{i}{48}}, & 0 \le i \le 48, \quad i \in \mathbb{N}_0, \\ T_{\mathrm{pre}} &= 10\ \mu\mathrm{s} \times 10^{\frac{i}{48}}, & 0 \le i \le 96, \quad i \in \mathbb{N}_0 \end{aligned} \tag{16}$$

for the parameters of the controllers and

$$\tilde{R}_{\mathrm{A,load}} = [-15.9\ \Omega,\ 10\ \mathrm{M}\Omega,\ 15.9\ \Omega] \tag{17}$$

for the considered load situations, which gives a total of $97 \times 145 \times 49 \times 97 \times 3 = 201 \times 10^6$ different parameter sets. In Fig. 8, the address variable m accesses the currently processed controllers' parameter set without load resistance and n accesses one of the three small-signal load resistance values.

With a given set of the controllers' parameters, the algorithm verifies in ② in Fig. 8 that the limits of the controller gains in (15) are not exceeded. Thereafter, the algorithm computes the transfer functions $L_{\mathrm{cl,i},m,n}$ and $L_{\mathrm{cl,v},m,n}$ of the closed-current- and voltage-control loops in ③ for all considered small-signal resistances and analyzes the locations of the poles of both transfer functions. The algorithm continues with the same controllers' parameter set if the above discussed boundary conditions for robustness and for reference tracking are fulfilled.

In a next step, the algorithm calculates the load current to output-voltage transfer function $L_{\mathrm{cl,iload},m}$ in ⑤ and verifies the disturbance rejection boundary conditions in ⑥. If the considered parameter set also satisfies these conditions, the algorithm calculates all EQs, $e^2_{\mathrm{ev,vref}}$, $f_{\mathrm{bw,ss}}$, $e^2_{\mathrm{ev,iload}}$, and $Z_{\mathrm{A,out}}(@\ 3\ \mathrm{kHz})$, for all small-signal resistances in ⑦, and continues with the next parameter set. The optimization procedure finally determines, which parameter sets lead to the best EQs for each considered load condition in ⑧.

C. Results of the Optimization

Table IV lists the obtained results and the parameters of the controllers for which the values are reached for each EQ (for the PI-P-P control structure, k_{pv1} and k_{pv2} are the gains of the voltage controllers for V_{A1} and $V_{\mathrm{A,out}}$, respectively). According to Fig. 6, the value of the time constant of the prefilter, T_{pre}, has no effect on the output-voltage response in the event of a load step. However, any valid parameter set must lead to a response of the system, which fulfills all boundary conditions discussed in Section III-A. Due to this requirement, the listed valid ranges of T_{pre} result for the two EQs $e^2_{\mathrm{ev,iload}}$ and Z_{out}.

The capacitor–current feedback-control structure is most competitive with respect to the minimum achievable integrated and squared deviations of the output voltage due to a reference step ($14.9\ \mathrm{mV^2s}$) and a load step ($2.0\ \mathrm{mV^2s}$) and with respect to the minimum output impedance ($1.4\ \Omega$). The PI-P-P control structure leads with respect to the maximum small-signal bandwidth ($7.2\ \mathrm{kHz}$). The PI-P control structure is found to be least competitive for all EQs. The $f_{\mathrm{bw,ss,max}}$ and the $e^2_{\mathrm{ev,vref}}$ quantities are given for $\tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$, since, for a stable system with a maximum output-voltage overshoot of 10%, this load condi-

TABLE IV
COMPARISON OF THE FOUR DIFFERENT EQS USED TO EVALUATE THE CONTROL PERFORMANCES OF THE THREE CONSIDERED CONTROL STRUCTURES

EQ	*PI-P control structure*	
	Value	*Control parameters*
$f_{\mathrm{bw,ss,max}}$	5.8 kHz	$k_{\mathrm{pv}} = 0.40\ \mathrm{A/V}, k_{\mathrm{pi}} = 8.3\ \mathrm{V/A}, T_{\mathrm{iv}} = 750\ \mu\mathrm{s}, T_{\mathrm{pre}} = 30\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,vref}}$	19.1 $\mathrm{mV^2 s}$	$k_{\mathrm{pv}} = 0.40\ \mathrm{A/V}, k_{\mathrm{pi}} = 8.3\ \mathrm{V/A}, T_{\mathrm{iv}} = 750\ \mu\mathrm{s}, T_{\mathrm{pre}} = 30\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,iload}}$	2.9 $\mathrm{mV^2 s}$	$k_{\mathrm{pv}} = 0.40\ \mathrm{A/V}, k_{\mathrm{pi}} = 8.3\ \mathrm{V/A}, T_{\mathrm{iv}} = 953\ \mu\mathrm{s}, T_{\mathrm{pre}} = 30\ \mu\mathrm{s} - 147\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$
Z_{out}@3 kHz	1.7 Ω	$k_{\mathrm{pv}} = 0.40\ \mathrm{A/V}, k_{\mathrm{pi}} = 8.3\ \mathrm{V/A}, T_{\mathrm{iv}} = 953\ \mu\mathrm{s}, T_{\mathrm{pre}} = 30\ \mu\mathrm{s} - 147\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$
EQ	*Capacitor–current feedback-control structure*	
	Value	*Control parameters*
$f_{\mathrm{bw,ss,max}}$	7.1 kHz	$k_{\mathrm{pv}} = 3.8\ \mathrm{V/V}, T_{\mathrm{iv}} = 787\ \mu\mathrm{s}, k_1 = 8.3\ \mathrm{V/A}, k_2 = 15.4\ \mathrm{V/A}, T_{\mathrm{pre}} = 14\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,vref}}$	14.9 $\mathrm{mV^2 s}$	$k_{\mathrm{pv}} = 3.0\ \mathrm{V/V}, T_{\mathrm{iv}} = 402\ \mu\mathrm{s}, k_1 = 8.3\ \mathrm{V/A}, k_2 = 18.7\ \mathrm{V/A}, T_{\mathrm{pre}} = 0, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,iload}}$	2.0 $\mathrm{mV^2 s}$	$k_{\mathrm{pv}} = 3.7\ \mathrm{V/V}, T_{\mathrm{iv}} = 715\ \mu\mathrm{s}, k_1 = 8.3\ \mathrm{V/A}, k_2 = 19.6\ \mathrm{V/A}, T_{\mathrm{pre}} = 8\ \mu\mathrm{s} - 178\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$
Z_{out}@3 kHz	1.4 Ω	$k_{\mathrm{pv}} = 3.7\ \mathrm{V/V}, T_{\mathrm{iv}} = 95\ \mu\mathrm{s}, k_1 = 8.3\ \mathrm{V/A}, k_2 = 19.6\ \mathrm{V/A}, T_{\mathrm{pre}} = 8\ \mu\mathrm{s} - 178\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$
EQ	*PI-P-P control structure*	
	Value	*Control parameters*
$f_{\mathrm{bw,ss,max}}$	7.2 kHz	$k_{\mathrm{pv2}} = 268\ \mathrm{mV/V}, T_{\mathrm{iv}} = 909\ \mu\mathrm{s}, k_{\mathrm{pv1}} = 0.37\ \mathrm{A/V}, k_{\mathrm{pi}} = 7.1\ \mathrm{V/A}, T_{\mathrm{pre}} = 17\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,vref}}$	16.3 $\mathrm{mV^2 s}$	$k_{\mathrm{pv2}} = 9\ \mathrm{mV/V}, T_{\mathrm{iv}} = 65\ \mu\mathrm{s}, k_{\mathrm{pv1}} = 0.33\ \mathrm{A/V}, k_{\mathrm{pi}} = 7.9\ \mathrm{V/A}, T_{\mathrm{pre}} = 3\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,iload}}$	2.2 $\mathrm{mV^2 s}$	$k_{\mathrm{pv2}} = 282\ \mathrm{mV/V}, T_{\mathrm{iv}} = 316\ \mu\mathrm{s}, k_{\mathrm{pv1}} = 0.37\ \mathrm{A/V}, k_{\mathrm{pi}} = 7.1\ \mathrm{V/A}, T_{\mathrm{pre}} = 19\ \mu\mathrm{s} - 170\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$
Z_{out}@3 kHz	1.4 Ω	$k_{\mathrm{pv2}} = 294\ \mathrm{mV/V}, T_{\mathrm{iv}} = 953\ \mu\mathrm{s}, k_{\mathrm{pv1}} = 0.38\ \mathrm{A/V}, k_{\mathrm{pi}} = 6.8\ \mathrm{V/A}, T_{\mathrm{pre}} = 19\ \mu\mathrm{s} - 178\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$

TABLE V
VALUES OF THE EQS OBTAINED FOR THE PI-P-P CONTROL STRUCTURE IF THE CONTROLLER GAIN LIMITATIONS DUE TO MEASUREMENT NOISE (15) WOULD NOT APPLY (THE TWO OTHER STRUCTURES DO NOT HIT THE GAIN LIMITS); k_{pv1} AND k_{pv2} DENOTE THE GAINS OF THE VOLTAGE CONTROLLERS FOR V_{A1} AND $V_{\mathrm{A,out}}$ OF THE PI-P-P CONTROL STRUCTURE, RESPECTIVELY

EQ	*PI-P control structure - without controller gain limitations*	
	Value	*Control parameters*
$f_{\mathrm{bw,ss,max}}$	8.1 kHz	$k_{\mathrm{pv2}} = 44\ \mathrm{mV/V}, T_{\mathrm{iv}} = 348\ \mu\mathrm{s}, k_{\mathrm{pv1}} = 0.51\ \mathrm{A/V}, k_{\mathrm{pi}} = 6.8\ \mathrm{V/A}, T_{\mathrm{pre}} = 0, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,vref}}$	13.9 $\mathrm{mV^2 s}$	$k_{\mathrm{pv2}} = 51\ \mathrm{mV/V}, T_{\mathrm{iv}} = 178\ \mu\mathrm{s}, k_{\mathrm{pv1}} = 0.47\ \mathrm{A/V}, k_{\mathrm{pi}} = 7.1\ \mathrm{V/A}, T_{\mathrm{pre}} = 0, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,iload}}$	2.1 $\mathrm{mV^2 s}$	$k_{\mathrm{pv2}} = 387\ \mathrm{mV/V}, T_{\mathrm{iv}} = 10\ \mathrm{ms}, k_{\mathrm{pv1}} = 0.56\ \mathrm{A/V}, k_{\mathrm{pi}} = 6.2\ \mathrm{V/A}, T_{\mathrm{pre}} = 18\ \mu\mathrm{s} - 196\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$
Z_{out}@3 kHz	1.3 Ω	$k_{\mathrm{pv2}} = 387\ \mathrm{mV/V}, T_{\mathrm{iv}} = 10\ \mathrm{ms}, k_{\mathrm{pv1}} = 0.56\ \mathrm{A/V}, k_{\mathrm{pi}} = 6.2\ \mathrm{V/A}, T_{\mathrm{pre}} = 18\ \mu\mathrm{s} - 196\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$

tion has been identified to always lead to the worst-case values for $f_{\mathrm{bw,ss,max}}$ and the $e^2_{\mathrm{ev,vref}}$. For the $e^2_{\mathrm{ev,iload}}$ and the $Z_{\mathrm{A,out}}$ quantities, a constant-current-source type of load is assumed. For the given hardware prototype, the limitations due to measurement noise, given in (15), only become active for the PI-P-P control structure. If these limitations would not apply, the PI-P-P control structure would outperform the capacitor–current feedback-control structure. For completeness, Table V lists the EQs theoretically achievable for the PI-P-P control structure if the limitations according to (15) are disregarded.

This study considers a high achievable small-signal bandwidth to be of particular interest [38], therefore, all three control structures are parameterized with respect to maximum small-signal bandwidth. With this set of the controllers' parameters, the EQs are given in Table VI for all three control structures. In comparison to the best achievable EQs, cf., Table IV, it can be seen that the EQs remain almost the same for the parameters of the controllers selected in Table VI. Furthermore, the aforementioned advantages of the capacitor–current feedback-control structure compared to the other control structures remain.

Fig. 9 presents the calculated reference voltage and load step responses of the three investigated control structures for the parameters of the controllers listed in Table VI. In accordance to the values of $e^2_{\mathrm{ev,vref}}$ and $e^2_{\mathrm{ev,iload}}$ listed in Table VI, the reference and disturbance actions of the capacitor–current feedback and the PI-P-P control structures are very similar and superior to those of the PI-P control.

Fig. 10 depicts the calculated small-signal reference tracking transfer functions of the three control structures and reveals the calculated small-signal bandwidths of 5.8 kHz, 7.1 kHz, and 7.2 kHz for the PI-P, the capacitor–current feedback, and the PI-P-P control structures, respectively.

The computed small-signal output impedances for the different control structures are shown in Fig. 11. The capacitor–current feedback-control structure features lowest impedances in the frequency range between 10 Hz and 10 kHz. For frequencies below 200 Hz, the PI-P-P control structure has the highest output impedance, while in the frequency range between 200 Hz and 10 kHz, the PI-P control structure gives the highest output impedance. The values of the output impedance at 3 kHz are given in Table IV for all control structures.

For a worst-case negative small-signal load resistance of $-15.9\ \Omega$, the calculated reference voltage responses are depicted in Fig. 12 for the parameters of the controllers given in

TABLE VI
VALUES OF THE EQS OBTAINED FOR THOSE CONTROLLERS' PARAMETER SETS (GIVEN IN PARENTHESES), WHICH LEAD TO THE MAXIMUM SMALL-SIGNAL BANDWIDTHS

Control Structure	*EQ*			
	$f_{\mathrm{bw,ss,max}}$	$e^2_{\mathrm{ev,vref}}$	$e^2_{\mathrm{ev,iload}}$	Z_{out} @3 kHz
PI-P ($k_{\mathrm{pv}} = 0.40\ \mathrm{A/V}, k_{\mathrm{pi}} = 8.3\ \mathrm{V/A}$, $T_{\mathrm{iv}} = 750\ \mu\mathrm{s}, T_{\mathrm{pre}} = 30\ \mu\mathrm{s}$)	5.8 kHz	19.1 $\mathrm{mV^2s}$	2.9 $\mathrm{mV^2s}$	1.7 Ω
Cap. fb. ($k_{\mathrm{pv}} = 3.8\ \mathrm{V/V}, T_{\mathrm{iv}} = 787\ \mu\mathrm{s}$, $k_1 = 8.3\ \mathrm{V/A}, k_2 = 15.4\ \mathrm{V/A}, T_{\mathrm{pre}} = 14\ \mu\mathrm{s}$)	7.1 kHz	16.8 $\mathrm{mV^2s}$	2.1 $\mathrm{mV^2s}$	1.4 Ω
PI-P-P ($k_{\mathrm{pv2}} = 268\ \mathrm{mV/V}, T_{\mathrm{iv}} = 909\ \mu\mathrm{s}$, $k_{\mathrm{pv1}} = 0.37\ \mathrm{A/V}, k_{\mathrm{pi}} = 7.1\ \mathrm{V/A}, T_{\mathrm{pre}} = 17\ \mu\mathrm{s}$)	7.2 kHz	16.8 $\mathrm{mV^2s}$	2.2 $\mathrm{mV^2s}$	1.5 Ω

For the PI-P-P control structure, k_{pv1} and k_{pv2} denote the gains of the voltage controllers for V_{A1} and $V_{\mathrm{A,out}}$, respectively.

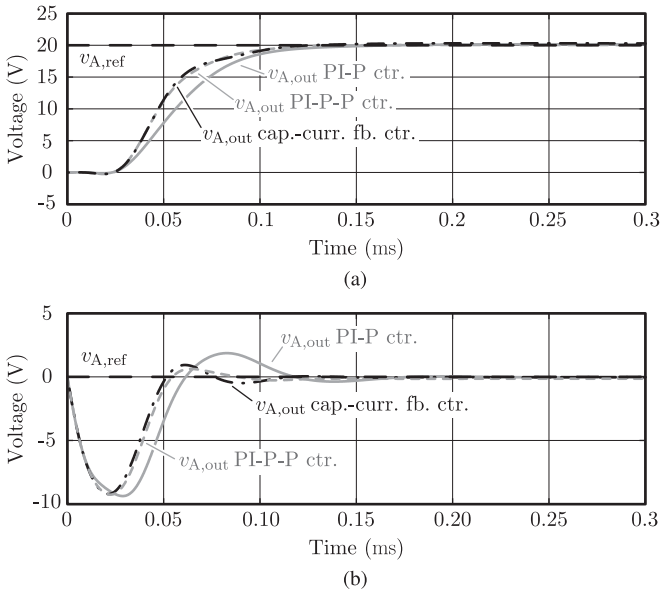

Fig. 9. (a) Calculated output-voltage step responses for a reference step of 20 V and a small-signal load resistance of 15.9 Ω for the three considered control structures, and (b) calculated output voltages due to a load step of $25\% \times I_{\mathrm{A,out,n}} = 25\% \times 14.5\ \mathrm{A} = 3.6\ \mathrm{A}$ for a current-source type of load. The parameters of the controllers are given in Table VI.

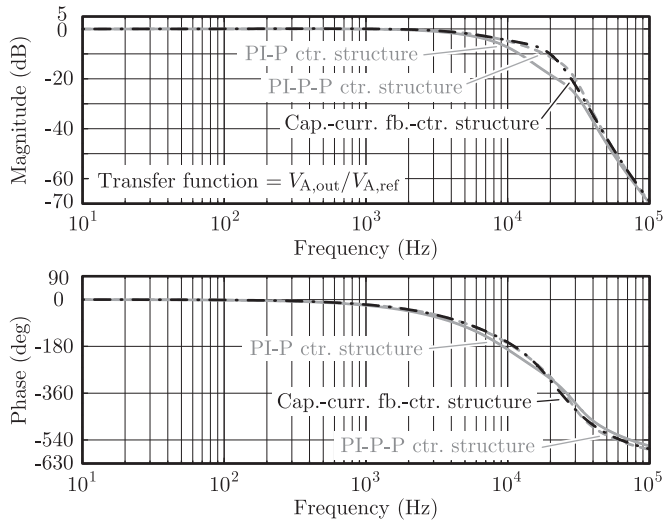

Fig. 10. Calculated small-signal reference tracking transfer functions for a load resistance of 15.9 Ω for the three considered control structures and the parameters of the controllers given in Table VI.

Table VI. As already noticed for a positive load resistance of 15.9 Ω, the capacitor–current feedback and the PI-P-P control structures achieve a faster reference tracking action than the PI-P controller. Fig. 13 depicts the small-signal frequency responses for $\tilde{R}_{\mathrm{A,load}} = -15.9\ \Omega$. For this load resistance, the control bandwidths extend to 10.6 kHz, 15.5 kHz, and 13.9 kHz for the PI-P, the capacitor–current feedback, and the PI-P-P control structures, respectively.

So far only the small-signal capabilities of the CVS are discussed. To allow for a more complete picture, Fig. 14 shows the large-signal capability of the CVS for the most suitable control structure (the capacitor–current feedback structure), nominal load ($R_{\mathrm{A,load}} = 15.9\ \Omega$), and for a hardware limited bridge-leg output current ($\max|i_{\mathrm{A0}}(t)| = \sqrt{2} \times 17\ \mathrm{A} = 24\ \mathrm{A}$ [12]). Fig. 14(a) depicts the magnitude of the fundamental component of the output voltage $v_{\mathrm{A,out}}$ for different modulation indexes, $m = V_{\mathrm{A,ref,pk}}/(V_{\mathrm{dc}}/2)$ where $V_{\mathrm{A,ref,pk}}$ is the peak value of the

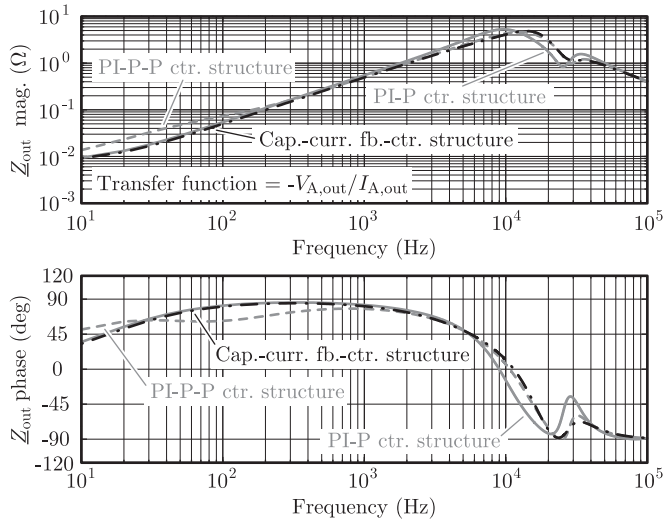

Fig. 11. Calculated small-signal output impedances for the three considered control structures and the parameters of the controllers given in Table VI.

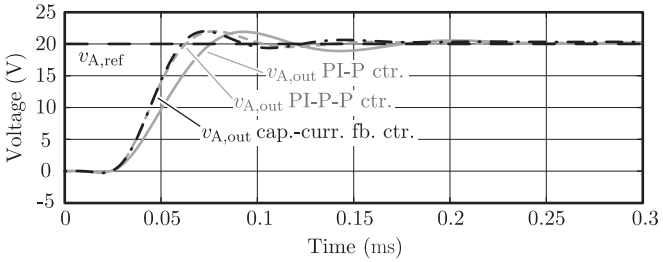

Fig. 12. Calculated output-voltage step responses for a reference step of 20 V, $\tilde{R}_{\mathrm{A,out}} = -15.9\ \Omega$, the three considered control structures, and the parameters of the controllers given in Table VI.

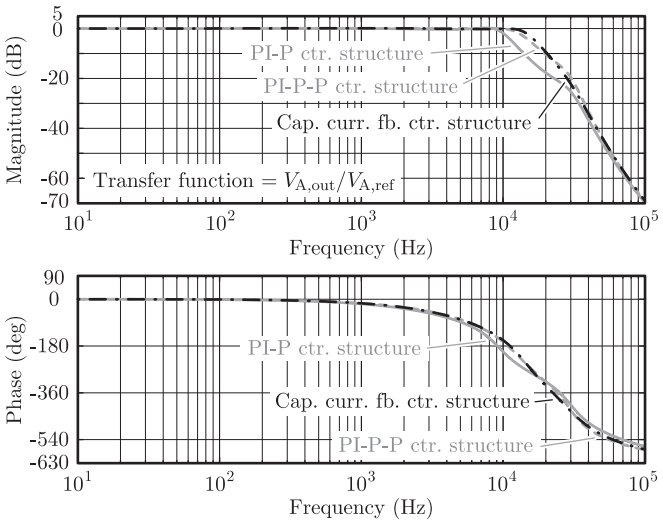

Fig. 13. Calculated small-signal reference tracking transfer functions for $\tilde{R}_{\mathrm{A,out}} = -15.9\ \Omega$, the three considered control structures, and the parameters of the controllers listed in Table VI.

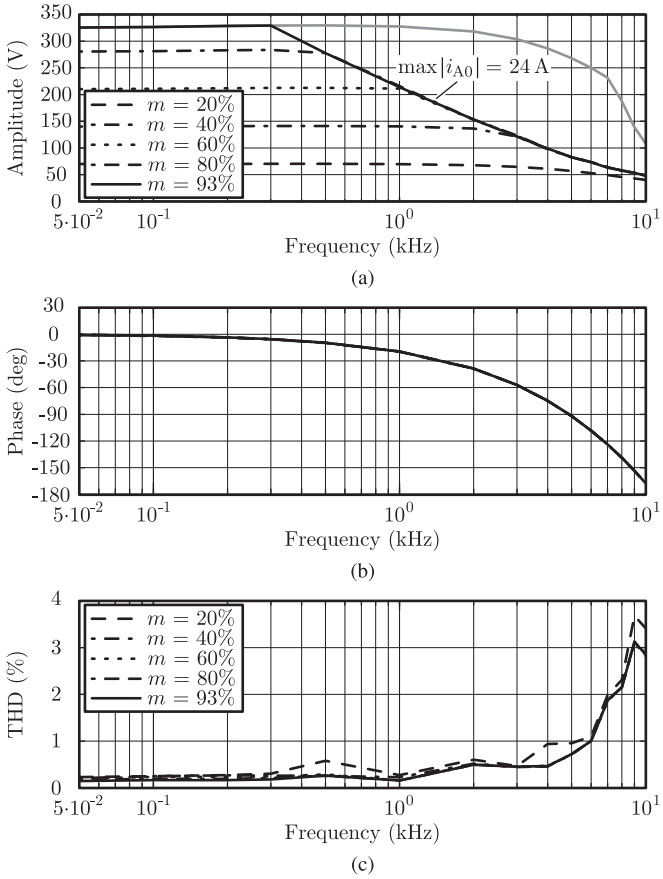

Fig. 14. Results of large-signal calculations elaborated for the capacitor–current feedback-control structure, $R_{\mathrm{A,load}} = 15.9\ \Omega$, and a hardware limited bridge-leg output current i_{A0} of 24 A, cf. [12]: (a) the magnitude of the fundamental component of the output voltage $v_{\mathrm{A,out}}$ for sinusoidal reference voltages with peak values $V_{\mathrm{A,ref,pk}}$ and different modulation indexes, $m = V_{\mathrm{A,ref,pk}}/(V_{\mathrm{dc}}/2)$ [the gray curve is computed for no limitation of $|i_{\mathrm{A0}}|$ and $m = 93\%$], (b) phase shift between the fundamental component of $v_{\mathrm{A,out}}$ and the reference voltage, and (c) THD (including interharmonics) calculated for $v_{\mathrm{A,out}}(t)$.

sinusoidal reference voltage, and Fig. 14(b) shows the phase shift between the fundamental component of $v_{\mathrm{A,out}}$ and the reference voltage. With the maximum selected modulation index of $m = 93\%$ the nominal RMS output voltage of 230 V results.

Full and half nominal active power, i.e., $10\ \mathrm{kW}/3 = 3.33\ \mathrm{kW}$ and $1.67\ \mathrm{kW}$, respectively, can be provided for frequencies up to 300 Hz (voltage amplitude of 325 V) and 840 Hz (voltage amplitude of 230 V), respectively, which has been verified by experiments. Without the limitation of $|i_{\mathrm{A0}}|$ and $m = 93\%$ [gray curve in Fig. 14(a)], full nominal power is feasible up to a frequency of 1.2 kHz and at the small-signal bandwidth of 7.1 kHz, still, half nominal power can be provided. The calculated results further reveal identical large-signal phase responses for different m, which are comparable to the small-signal phase response given in Fig. 10. Fig. 14(c) gives the calculated THD (considering harmonics with ordinal numbers ≤ 40 as proposed in IEC 61000-3-2 [41] and including interharmonics), which is less than 1% or 4% for frequencies less than 5 kHz or 10 kHz for all modulation indexes, respectively. It is remarked that the shown large-signal properties have been found to be characteristic for the inverter and the output filter with load and nearly independent of the selected control structure.

IV. Experimental Verification

The hardware setup used to verify the theoretical results, depicted in Fig. 15, is a realization of the output stage shown in Fig. 1 and uses the filter component values listed in Table II and SiC MOSFETs (Cree's C2M0025120D). This hardware setup features the specifications given in Table I. The fast switching SiC MOSFETs enable the use of a relatively short interlocking time of 180 ns. In addition, no compensation methods are implemented for reducing eventually present output voltage distortions that stem from the interlocking-time interval.

Fig. 16 depicts the measured waveforms of unfiltered and filtered output voltages and output currents, v_{A0}, $v_{\mathrm{A,out}}$, i_{A0}, and $i_{\mathrm{A,out}}$, for the capacitive-current feedback-control structure in the event of a reference voltage step of $10\% \times v_{\mathrm{A,out}}(t = 0) = 10\% \times 200\ \mathrm{V} = 20\ \mathrm{V}$ and for the operating conditions given Table VII [$\langle i_{\mathrm{A0}}(t)\rangle_{T_{\mathrm{s}}}$ denotes the average of i_{A0} over one switching period]. Fig. 16(b) reveals that the output filter modifies the dynamic properties of the bridge-leg output current of the CVS, $\langle i_{\mathrm{A0}}(t)\rangle_{T_{\mathrm{s}}}$, e.g., with respect to overshoot and time delay.

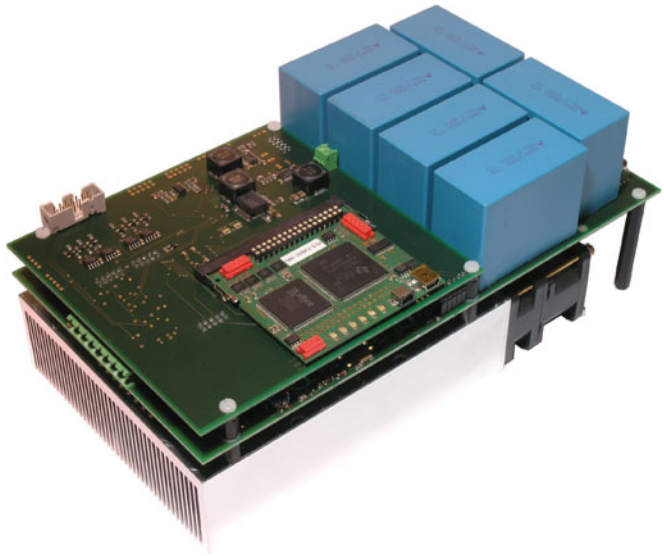

Fig. 15. Three-phase three-level T-type inverter prototype with SiC MOSFETs C2M0025120D and a floating-point DSP TMS320F28335 as well as an FPGA LFXP2-5E-5TN144C featuring the specifications listed in Table I.

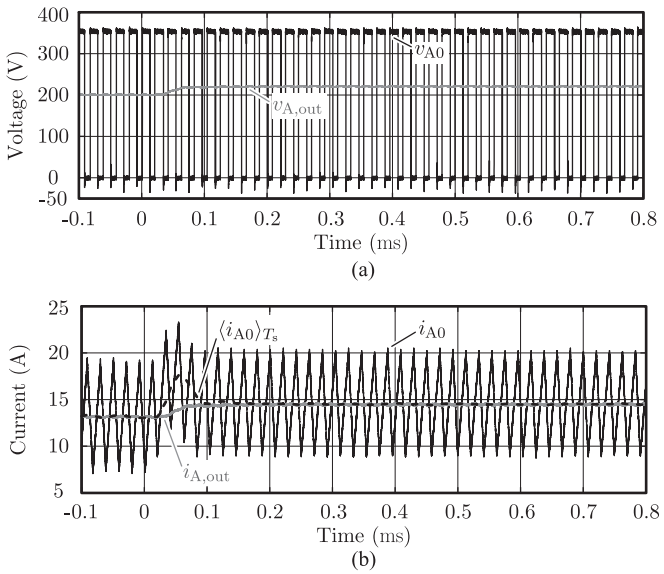

Fig. 16. (a) and (b) Measured waveforms of unfiltered and filtered output voltages and output currents, v_{A0}, $v_{A,out}$, i_{A0}, and $i_{A,out}$, for the capacitive–current feedback-control structure, a reference voltage step of 20 V, and the operating conditions given in Table VII. Table VI lists the controller settings.

TABLE VII
OPERATING CONDITIONS FOR WHICH THE REFERENCE VOLTAGE AND LOAD STEPS SHOWN IN FIGS. 17 AND 18 WERE MEASURED (APPLIES TO ALL THREE CONTROL STRUCTURES)

DC-link voltage V_{dc}	700 V
Switching frequency f_s	48 kHz
Sampling frequency f_0	96 kHz
Output voltage before the step $v_{A,out}(t=0)$	200 V
Output load $R_{A,load}$ (reference step)	15.9 Ω
Output load $R_{A,load}$ (load step)	22.2 Ω → 15.9 Ω

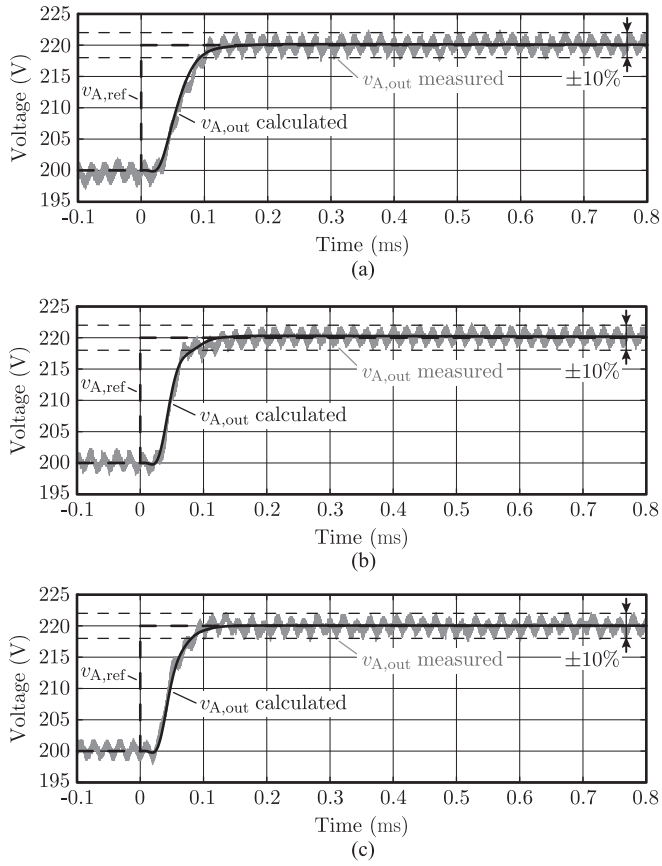

Fig. 17. Measured and calculated step responses of the output voltages of (a) the PI-P control structure, (b) the capacitor–current feedback-control structure, and (c) the PI-P-P control structure. The reference voltage step is 20 V, Table VII summarizes the operating conditions, and Table VI lists the controller settings.

Fig. 17 compares calculated to measured output voltages due to a reference voltage step from 200 to 220 V for all three control structures and for the operating conditions listed in Table VII. Small random variations of the measured output voltages from the steady-state values of at most ±0.5 V can be seen (especially in the measurements for the PI-P-P control structure) because of measurement noise. Apart from these minor errors, the calculated and measured waveforms of $v_{A,out}(t)$ fit nicely.

Fig. 18 compares simulated and measured transient changes of the output voltage of the CVS if the connected load, $R_{A,load}$, changes from 22.2 Ω to 15.9 Ω (resulting in a current step of 3.6 A), for all three control structures, and for the operating conditions given in Table VII. In accordance with the corresponding calculated load steps, discussed in Section III-C and depicted in Fig. 9(b), the momentary decreases of the output voltage, approximately 8 V, are the same for all three control structures. However, with the capacitor-current feedback and the PI-P-P control structures, the output voltages recover more quickly than with the PI-P control structure.

With the achieved high control bandwidth and the low input impedance, the presented control structures feature the generation of high-quality output voltages. Fig. 19, for example,

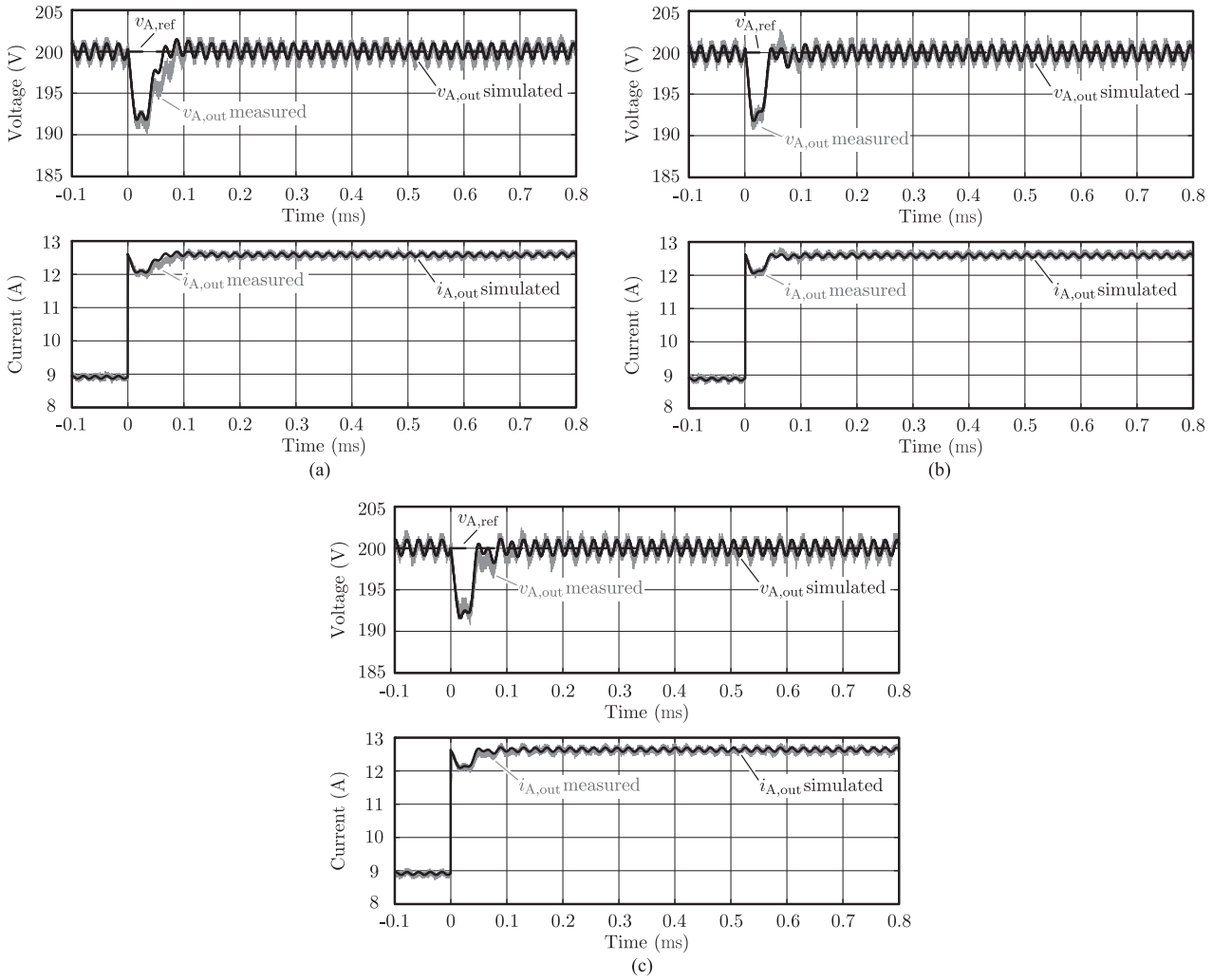

Fig. 18. Measured and simulated output voltages for a load step from 22.2 Ω to 15.9 Ω (leading to a load current step of 3.6 A) and the operating condition given in Table VII: (a) PI-P control structure, (b) capacitor–current feedback-control structure, and (c) PI-P-P control structure. The parameters of the controllers are listed in Table VI.

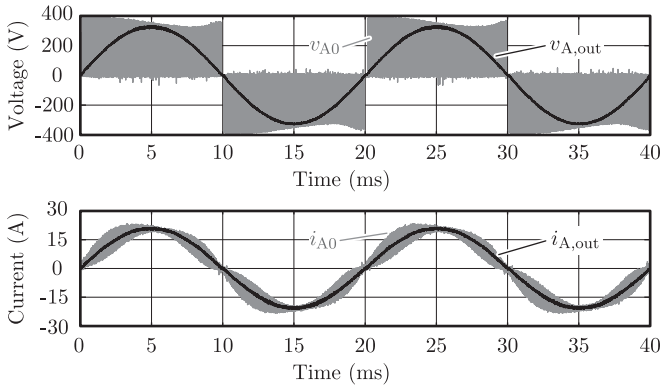

Fig. 19. Measured waveforms of v_{A0}, $v_{A,out}$, i_{A0}, and $i_{A,out}$ for a sinusoidal output voltage $v_{A,out}$ (amplitude is 328 V, frequency is 50 Hz, output power is 3.3 kW); the measured THD for $v_{A,out}$ is 0.67%.

depicts the measured waveform of a sinusoidal voltage with an amplitude of 328 V and a frequency of 50 Hz, generated with the considered inverter prototype and capacitor–current feedback control and for a resistive load; the output power is 3.3 kW and the measured THD is 0.67%.

Even in presence of nonlinear loads, output voltages with low THD values are feasible. This is demonstrated for the capacitor–current feedback-control structure and a diode rectifier type of load, depicted in Fig. 20(a), which comprises of $L_{rec} = 3.4$ mH, $C_{rec} = 3.8$ mF, and $R_{rec} = 88\ \Omega$, provides an output power of 1 kW, and a power factor of $\lambda = 0.7$ for $v_{A,out}$ being sinusoidal with a frequency of 50 Hz and an RMS value of 230 V. L_{rec} is designed such that, at the output frequency of 50 Hz, $Z_{L,rec} = 2\% \times Z_{rec0}$ applies, with $Z_{L,rec} = 2\pi \times 50\ \text{Hz} \times L_{rec}$ and $Z_{rec0} = (230\ \text{V})^2/1\ \text{kW}$. The selected values of L_{rec} and C_{rec} lead to a relative voltage ripple of 2% at the rectifier's DC port. Due to the good matching of calculated, simulated, and measured results found in Figs. 17 and 18, the results obtained for the nonlinear load, depicted in Fig. 20(b), are obtained by way of accurate circuit simulation that includes a model of the switching stage and correctly reproduces the turn-on and turn-off delays of the switches.

The output current of the output filter of the CVS, $i_{A,out}$ in Fig. 20(b), is clearly nonlinear; its RMS and peak values are 6.2 A and 14.9 A, respectively. Still, $v_{A,out}$ is close to a sinusoidal waveform, with a THD of 0.31% (obtained from the

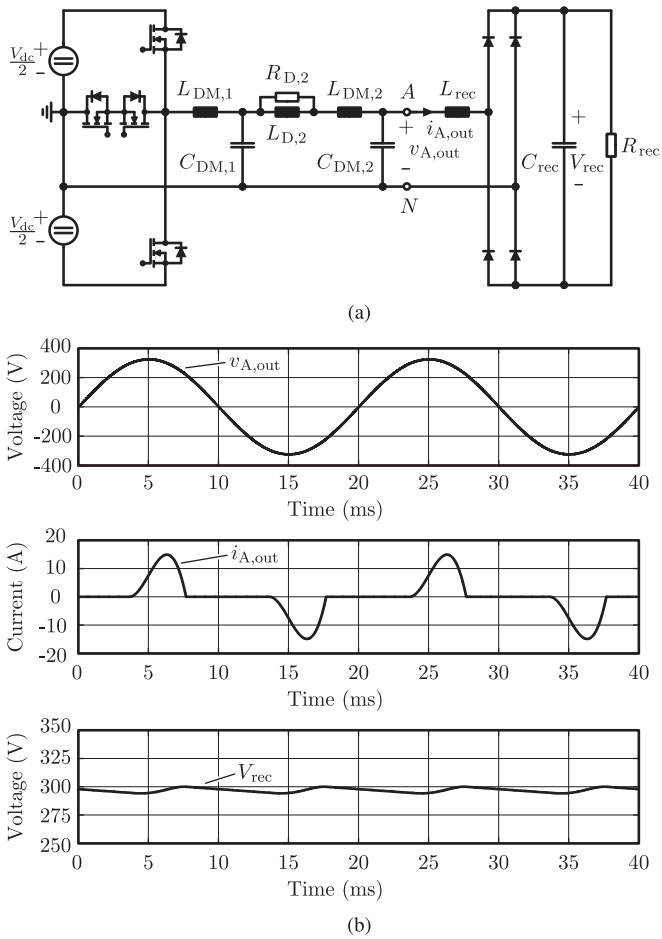

Fig. 20. Nonlinear load connected to the CVS: (a) connection of the CVS to a single-phase diode-rectifier load with $L_{\rm rec} = 3.4$ mH, $C_{\rm rec} = 3.8$ mF, and $R_{\rm rec} = 88\ \Omega$; (b) simulated waveforms of $v_{\rm A,out}$, $i_{\rm A,out}$, and $V_{\rm rec}$. The capacitor–current feedback-control structure is used to control the CVS.

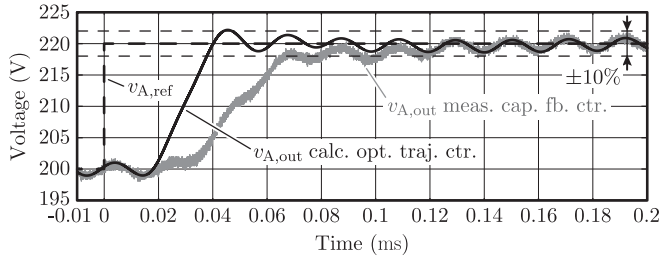

Fig. 21. Output voltage due to a reference step of 20 V obtained for an optimal trajectory-based controller (black curve) and for the capacitor–current feedback-control structure (gray curve) employing PI-controllers, identified to be the most suitable structure for the CVS.

circuit simulator, i.e., this value does not consider the implication of slight distortions due to minor measurement errors in the voltage and current sensing circuits used on the hardware prototype; for comparison, at no load and for a single-phase resistive load with $P_{\rm A,out} = 1$ kW, THD values of 0.24% and 0.21%, respectively, are obtained from the simulator). Further investigations also reveal a negligible impact of the output impedance of the CVS on the obtained results: in this regard, the peak value of the current in $L_{\rm rec}$ only increases from 14.9 A to 15.0 A if the CVS with output filter is replaced by an ideal AC voltage source.

V. Conclusion

This paper motivates, models, and optimizes three different control structures, composed of conventional P and PI controllers and suitable for the output stage of a 10 kW, four-quadrant three-phase switch-mode CVS with $f_s = 48$ kHz and a two-stage LC output filter, with respect to reference tracking and disturbance rejection, which are characterized by means of four defined EQs, and for common boundary conditions, e.g., for a maximum overshoot of the output voltage of 10% in case of a reference voltage step. Each output phase of the CVS is operated individually to allow for maximum flexibility in the generation of the output phase voltages to supply a wide range of different types of load, such as DC, single-phase and three-phase AC loads including loads with constant-power characteristics featuring negative small-signal load resistance values.

It is emphasized that the use of accurate small-signal models features an excellent matching between the presented control structure models and the measurements. Further it has been found that the achievable control performance, i.e., with respect to the values of the EQs defined in Section III, strongly depends on the two aspects listed below.

1) *Delay Compensation:* To achieve a high control bandwidth and tight output-voltage control, it is found to be crucial to minimize the deteriorating impact of the system time delay $T_{\rm d}$. For this reason, all three control structures incorporate delay compensation algorithms, which estimate the expected values of the controlled variables at $t = t_0 + T_{\rm d}$ based on previous measurements.
2) *Feedforwards and Prefilter:* The prefilter for the voltage reference and the feedforwards of the reference voltage and the load current are found to allow for a considerable improvement of the investigated EQs.

For the given hardware setup and among the three structures depicted in Fig. 6, the capacitor–current feedback-control structure is identified to be most competitive considering the four EQs. This control structure realizes an output impedance of less than $500\ {\rm m}\Omega$ for output frequencies below 1 kHz, a small-signal bandwidth between 7.1 kHz (for nominal load, $\tilde{R}_{\rm load} = 15.9\ \Omega$) and 15.5 kHz (for $\tilde{R}_{\rm load} = -15.9\ \Omega$, e.g., occurring for constant-active-power load). At $\tilde{R}_{\rm load} = -15.9\ \Omega$, the CVS completes a small-signal reference voltage step within five switching cycles (approximately $100\ \mu$s).

Fig. 21 compares the output-voltage step response obtained with the capacitor–current feedback-control structure to the response obtained for an optimal trajectory control. The PWM pattern for tracking the optimal trajectory has been calculated offline and minimizes the integrated squared output-voltage error (including the boundary condition of a maximum overshoot of 10%). The resulting step response, thus, reveals that optimal trajectory control can decrease the response time by two to three switching cycles. Optimal trajectory control, however, requires an accurate model of the complete system inclusive load, which may, for example, be achieved with the use of a load estimator

according to [42]. The fast step responses achieved with P and PI controllers and the low complexities of the proposed control structures clearly support the use of well-known linear controllers, e.g., in an environment that is highly sensitive to other aspects like development time and cost. Still, the widespread use of digital control platforms and increasing computing capacity enable realizations of advanced control concepts that are expected to fill the gap between the two step responses depicted in Fig. 21.

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David Olivier Boillat (S'11–M'15) received the bachelor's and master's degrees in electrical power systems and mechatronics from the Department of Electrical Engineering and Information Technology, Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland, in October 2007 and October 2010, respectively. He started his Ph.D. studies at the Power Electronic Systems Laboratory, ETH Zürich, Zürich, Switzerland, in January 2011 focusing on the design and realization of a high-bandwidth switch-mode controllable AC voltage source.

Florian Krismer (S'05–M'12) received the M.Sc. degree from the University of Technology Vienna, Vienna, Austria, in 2004, and the Ph.D. degree from the Power Electronic Systems Laboratory (PES), Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland, in 2011.

He is currently a Postdoctoral Fellow at PES, ETH Zürich. His research interests include the analysis, design, and optimization of high-current and high-frequency power converters.

Johann Walter Kolar (F'10) received the M.Sc. degree and Ph.D. degree *(summa cum laude)* from the University of Technology Vienna, Vienna, Austria.

He is currently a Full Professor and the Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland. He has proposed numerous novel PWM converter topologies, and modulation and control concepts, e.g., the Vienna rectifier, the Swiss rectifier, and the three-phase ac–ac sparse matrix converter and has published more than 600 scientific papers in international journals and conference proceedings and has filed more than 100 patents. His current research include the ultracompact and ultraefficient converter topologies employing latest power semiconductor technology (SiC and GaN), solid-state transformers, power supplies on chip, and ultrahigh speed and bearingless motors.

Dr. Kolar received ten IEEE Transactions Prize Paper Awards, ten IEEE Conference Prize Paper Awards, the SEMIKRON Innovation Award 2014, the Middlebrook Achievement Award 2014 of the IEEE Power Electronics Society, and the ETH Zürich Golden Owl Award 2011 for Excellence in Teaching.