# Open-Circuit Fault Diagnosis and Fault-Tolerant Control for a Grid-Connected NPC Inverter

Ui-Min Choi, *Student Member, IEEE*, June-Seok Lee, *Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, and Kyo-Beum Lee, *Senior Member, IEEE*

***Abstract*—This paper presents an open-circuit fault detection method for a grid-connected neutral-point clamped (NPC) inverter system. Further, a fault-tolerant control method under an open-circuit fault in clamping diodes is proposed. Under the grid-connected condition, it is impossible to identify the location of a faulty switch by the conventional methods which usually use the distortion of outputs because the distortion of the outputs is the same in some fault cases. The proposed fault detection method identifies the location of the faulty switch and the faulty clamping diode of the NPC inverter without any additional hardware or complex calculations. In the case of the clamping diode faults, the NPC inverter can transfer full rated power with sinusoidal currents by the proposed fault-tolerant control. The feasibility of the proposed fault detection and the fault-tolerant control methods for the grid-connected NPC inverter are verified by simulation and experimental results.**

***Index Terms*—Fault detection, fault-tolerant control, grid-connected inverter, neutral-point clamped (NPC) inverter, open-circuit fault, reliability.**

## I. Introduction

THE power electronic converters which convert electrical power efficiently from one stage to another stage play an important role in various applications to achieve high efficiency and also achieve high performance of the systems [1]. As the power electronics has progressively gained an important status in power generation, distribution, and consumption, recent research endeavor to improve the reliability of the power electronic systems to comply with more stringent constraints on cost, safety, and availability in various applications [2], [3].

The power electronic systems consist of various components. Among them, the power devices are one of the most fragile components and, thus, play a key role in the robustness and reliability of the overall power electronics systems. The semiconductor device failure accounts for total 21% of converter system's failures [4]. According to the survey based on more than 200 products from 80 companies, semiconductor power devices have been selected by 34% of responders as the most fragile components [5]. Insulated gate bipolar transistor (IGBT) power module are the most widely used of their kind, and the temperature swing has the most significant impact on the wear-out failures of the power IGBT modules [6]–[9].

Manuscript received July 3, 2015; revised November 3, 2015; accepted December 9, 2015. Date of publication December 17, 2015; date of current version May 20, 2016. Recommended for publication by Associate Editor H. Wang.

U.-M. Choi and F. Blaabjerg are with the Center of Reliable Power Electronics, Department of Energy Technology, Aalborg University, Aalborg DK-9220, Denmark (e-mail: uch@et.aau.dk; fbl@et.aau.dk).

J.-S. Lee and K.-B. Lee are with the Department of Electrical and Computer Engineering, Ajou University, Suwon 443-749, Korea (e-mail: junpb@ajou.ac.kr; kyl@ajou.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2510224

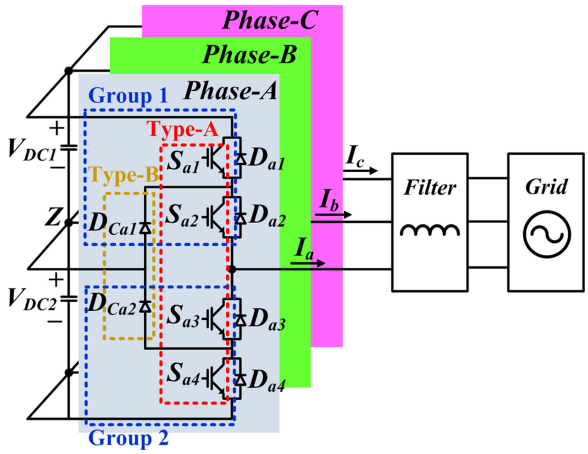


Fig. 1. Grid-connected NPC inverter system.

The open-circuit fault occurs mainly due to the lifting and crack of the bond wires in the module [9]. The bond wires which are normally aluminum (Al) and power device which is silicon (Si) materials have the different coefficient of thermal expansion (CTE). Generally, CTE of Al is $23.5 \times 10^{-6}$/K and CTE of Si is $2.6 \times 10^{-6}$/K [8]. The thermal cycling causes repeated cooling and heating; thus, allowing the joint materials to expand and shrink at different rates and it applies the stress at the point of contact. This CTE mismatch with the temperature swing causes the failures of bond wires in the power module. Further, the bond-wire lift-off and rupture may be able to occur due to one single overstress event such as short-circuit current. A gate driver fault is also one of the common causes of the open-circuit fault [3].

A neutral-point clamped (NPC) inverter shown in Fig. 1 is widely used because of their advantages over conventional two-level converter. For example, their output ac voltage provides lower *dv/dt* values and reduced total harmonic distortion (THD). Therefore, the output filter size can be reduced. In addition, power devices are operated at low-voltage stress and, thus, smaller capacity switches can be used. Finally, it can improve the efficiency compared with the conventional two-level converter in certain switching frequency ranges [10]–[12].

The open-circuit fault does not cause a serious damage, compared to a short-circuit fault, but reduces the system performance considerably. It leads to current distortion of the output-phase currents, increase of the currents in the other normal phases, and unbalance of the neutral-point voltage. Further, it may cause

secondary problems in other components or loads like transformer and motors by applying the distorted currents. If the open-circuit fault occurs, fault-tolerant control needs to be applied to maintain the converter system performance. The fault detection is performed before the fault-tolerant control, because the fault-tolerant strategies are typically different according to the specific faulty switch. Further, identifying the faulty switch can give the advantage to know where the converter needs to be repaired.

A lot of fault diagnosis methods for the two-level converter have been proposed. Most of previous methods can detect the open-circuit fault by analyzing the distortion of the output currents [13]–[16]. According to the faulty switch, the distortion of the output currents is different and the difference can be detected by slope method, current vector method using Park's transformation, normalized average current method, etc.

In [17], the current vector method is applied to the NPC inverter for the ac motor driver. This approach is only able to identify the faulty switch pair which is two upper switches or two lower switches in the leg. To identify the faulty switch between a pair of switches, the average values of the normalized currents during each positive and negative half fundamental period are used with current vector method in [18]. Under ac motor drive condition, the distortion of the currents is different according to the faulty switch. However, under the grid-connected condition, the distortion of the currents under the open-circuit fault in one of the two upper switches in a leg is the same with the distortion of the currents in the other one of the two upper switches. In the case of faults in two lower switches, the distortions of the currents are also the same. Therefore, it is impossible to identify the faulty switches between a pair of switches.

In [19], the slope method is applied for back-to-back NPC converter for wind turbine system. For the generator side converter, the faulty switch can be identified using slope method because the current distortion is different according to the faulty switch. However, in the case of the grid side inverter, the faulty switch cannot be detected clearly because the same current distortion occurs between two upper switch faults or between two lower switch faults.

The methods using additional circuits or components are proposed in [20] and [21]. In [20], the pole voltage is measured by the additional hardware circuit. The open-circuit fault is detected when the abnormal pole voltage is measured. This method can detect the fault in a short time. However, it is only possible to identify the faulty leg and it is not cost-effective.

In [21], the current through the clamping diodes are measured by the additional current sensors. By comparing the switching state and the polarities of the output and clamping diodes currents, the faulty switch can be detected. However, this approach also only considers not the gird-connected condition but the *R–L* loads condition. Under the grid-connected condition, it is impossible to identify the faulty switch by this approach.

Besides aforementioned methods, there are many methods to detect the faulty switch in the NPC converter based on the distortions of the outputs like current, voltage, etc., [22], [23]. Most of methods are considering the rectifier operations because, under this condition, the NPC converter has the different distortion characteristics in all cases. However, unfortunately, these methods cannot identify the faulty switch under grid-connected NPC inverter operation due to the same distortion characteristics in some cases.

In this paper, a new open-circuit fault detection method for the grid-connected NPC inverter system is proposed. Further, the fault-tolerant control method for the open-circuit fault in clamping diodes is also suggested. Two different types of open-circuit faults are first defined. The analysis of the inverter operation under each fault condition is presented. Then, the proposed fault detection method is explained. Finally, the fault-tolerant control method under the clamping diode faults is presented. The presented method can identify the faulty switches and the faulty clamping diodes without any additional hardware and complex calculations. Further, the proposed fault-tolerant control allows the NPC inverter to operate with acceptable output performance under the open-circuit fault in clamping diodes. The simulation and experimental results confirm the feasibility and reliability of the proposed methods.

## II. Operation of the Grid-Connected NPC Inverter Under Open-Circuit Fault Condition

In this section, the operation of the grid-connected NPC inverter under the open-circuit faults is analyzed considering the open-circuit faults in phase-A. Two different kinds of open-circuit faults within the NPC inverter are considered; one is when the open-circuit fault occurs in one of the switches (Type-A fault), and the other one is when the open-circuit fault occurs in one of the clamping diodes (Type-B fault). The current from inverter to grid is considered being the positive direction.

### A. Type-A Fault

*1) Open-Circuit Fault in $S_{a1}$:* Fig. 2(a) shows a current path under the normal condition. The current path is formed through $S_{a1}$ and $S_{a2}$ when the switching state is [P] with the positive current. If the open-circuit fault occurs in $S_{a1}$, the switching state [P] is impossible but the switching state [O] is possible functionally. If the open-circuit fault occurs while the positive current flows, the current flows through $D_{\mathrm{Ca1}}$ and $S_{a2}$ while the positive current decreases to zero and then, if the current is reached to zero, $D_{\mathrm{Ca1}}$ is reverse biased due to the positive grid voltage. Consequently, there are no current paths and the positive current of the faulty phase does not flow as shown in Fig. 3(a). The upper capacitor voltage $V_{\mathrm{DC1}}$ becomes larger than the lower capacitor voltage $V_{\mathrm{DC2}}$, because of the distortion in the positive current.

*2) Open-Circuit Fault in $S_{a2}$:* Under the normal condition, the current path is formed through $D_{\mathrm{Ca1}}$ and $S_{a2}$ when the switching state is [O] with the positive current as shown in Fig. 2(b). However, if the open-circuit fault occurs in $S_{a2}$, the switching states [P] and [O] are impossible. The possible current path is only through $D_{a3}$ and $D_{a4}$. If the open-circuit fault occurs in $S_{a2}$ while the positive current flows, the current flows through $D_{a3}$ and $D_{a4}$ until it decreases to zero and then, $D_{a3}$ and $D_{a4}$ are reverse-biased due to the positive grid voltage. It means that there are no current paths and the positive current

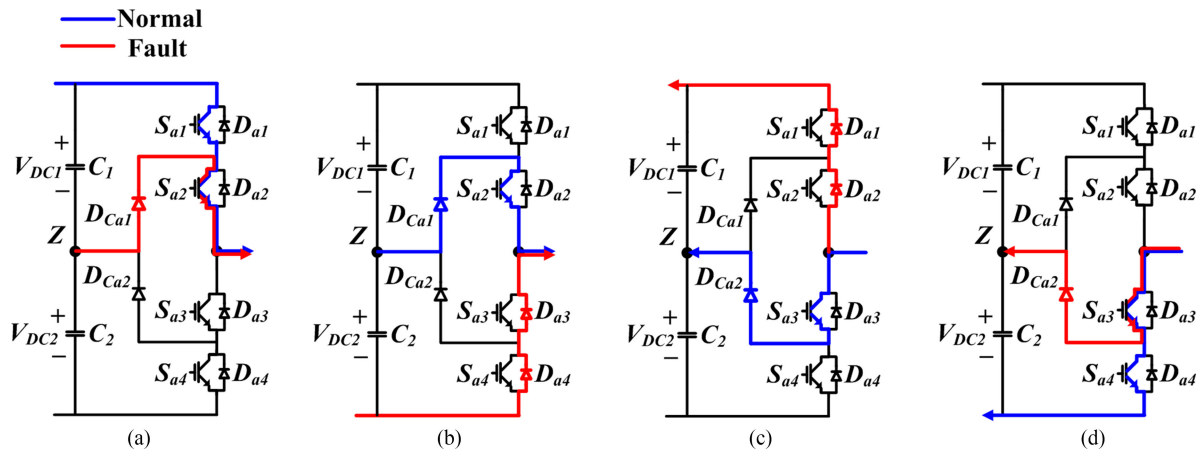


Fig. 2. Current paths under the normal condition (a) switching state [P], $I_a > 0$ (b) switching state [O], $I_a > 0$ (c) switching state [O], $I_a < 0$ (d) switching state [N], $I_a < 0$.

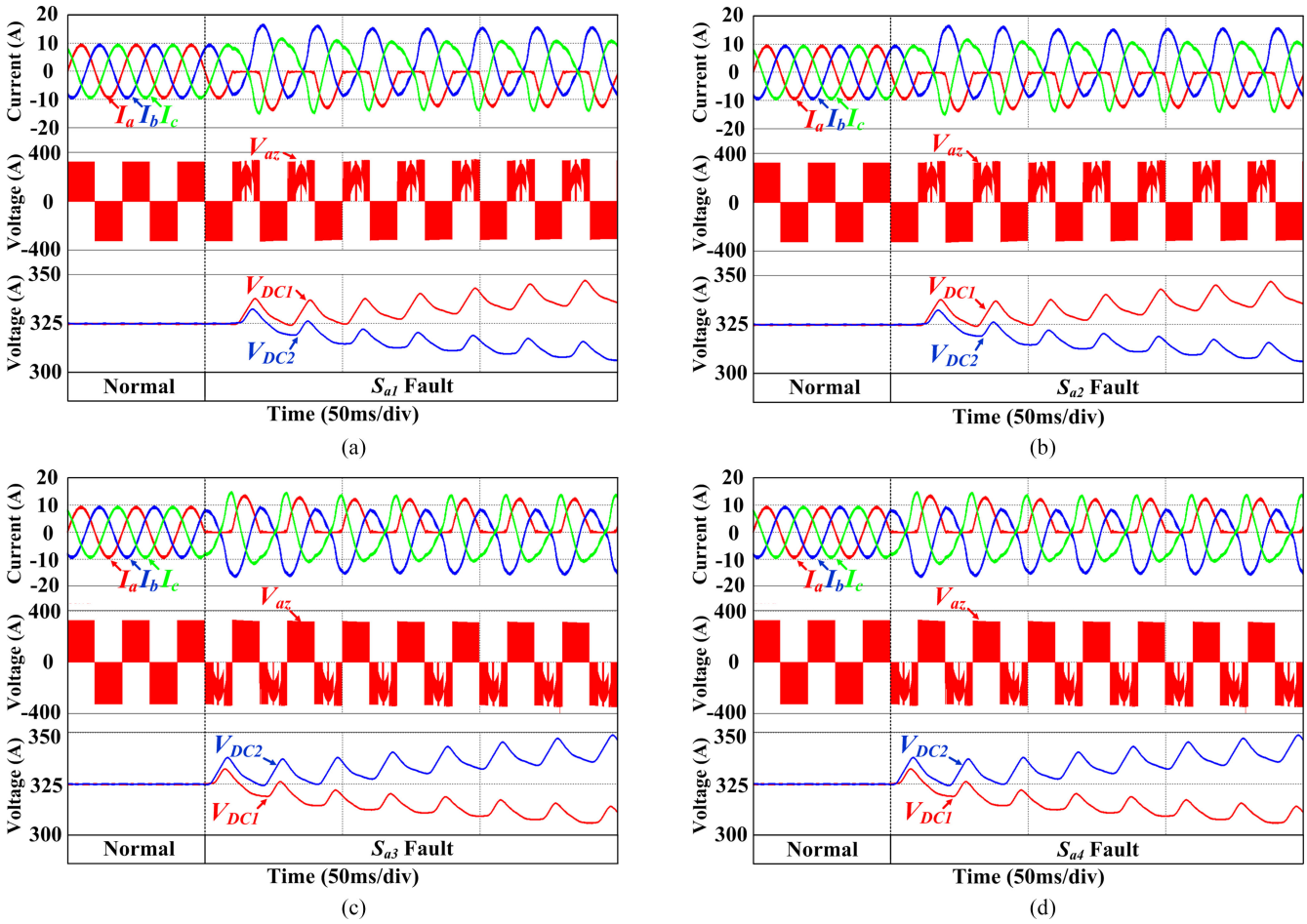


Fig. 3. Currents, pole voltage, and capacitor voltages under the open-circuit fault in switches (a) $S_{a1}$ fault, (b) $S_{a2}$ fault, (c) $S_{a3}$ fault, (d) $S_{a4}$ fault.

of the faulty phase does not flow as shown in Fig. 3(b). In this case, the distorted outputs are the same with the outputs under the $S_{a1}$ fault condition.

*3) Open-Circuit Fault in $S_{a3}$:* The overall analysis is almost the same with the previous case except for the current direction. Under the normal condition, the current path is formed through $S_{a3}$ and $D_{\mathrm{Ca2}}$ while the switching state [O] with the negative current. In the case of the switching state [N], the current path is formed through the switches $S_{a3}$ and $S_{a4}$ as shown in Fig. 2(d). If the open-circuit fault occurs in $S_{a3}$ while the negative current flows, the current path is formed through the $D_{a1}$ and $D_{a2}$ until the current decreases to zero as shown in Fig. 2(c). If it

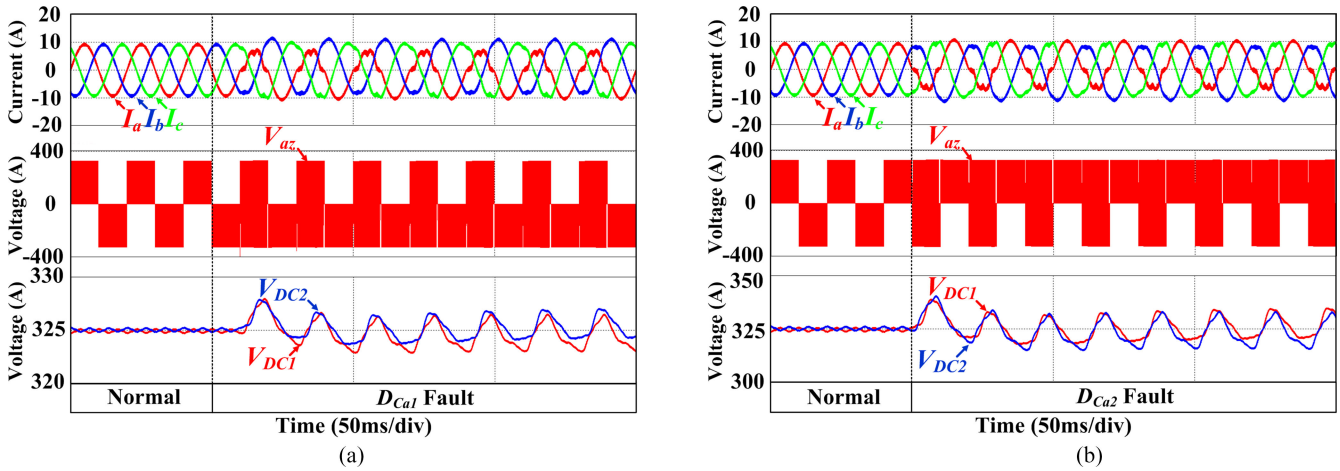


Fig. 4. Currents, pole voltage, and capacitor voltages under the open-circuit fault in clamping diodes (a) $D_{\mathrm{Ca1}}$ fault, (b) $D_{\mathrm{Ca2}}$ fault.

decreases to zero, $D_{a1}$ and $D_{a2}$ are reverse biased due to the negative grid voltage. Therefore, the negative current does not flow because both switching state [O] and [N] are impossible, and $V_{\mathrm{DC2}}$ becomes larger than $V_{\mathrm{DC1}}$ as shown in Fig. 3(c).

*4) Open-Circuit Fault in $S_{a4}$:* Under the $S_{a4}$ open-circuit fault condition, the switching state [N] is impossible but the switching state [O] is possible. If the open-circuit fault occurs in $S_{a4}$ when the negative current flows, the current flow through $D_{a1}$ and $D_{a2}$ until it decreases to zero. After the current is reached to zero, however, the current path is not made in this case also because the diode $D_{\mathrm{Ca2}}$ is reverse-biased and the diodes $D_{a1}$ and $D_{a2}$ are also reverse-biased due to the negative grid voltage. Therefore, the negative phase current of the faulty phase does not flow and $V_{\mathrm{DC2}}$ becomes larger than $V_{\mathrm{DC1}}$ as shown in Fig. 3(d). The distortion of the outputs under the $S_{a4}$ fault is the same as the outputs under the $S_{a3}$ fault condition.

### B. Type-B Fault

*1) Open-Circuit Fault in $D_{\mathrm{Ca1}}$:* If the open-circuit fault occurs in the clamping diode $D_{\mathrm{Ca1}}$, the switching state [P] is possible but the switching state [O] is impossible. Under the normal condition, the current path is formed through $D_{\mathrm{Ca1}}$ and $S_{a2}$ when the switching state is [O] with the positive current. However, under the $D_{\mathrm{Ca1}}$ fault condition, the output is connected to the negative DC-link through $D_{a3}$ and $D_{a4}$ instead of $D_{\mathrm{Ca1}}$ and $S_{a2}$ as shown in Fig. 2(b) even though the negative voltages are applied across $D_{a3}$ and $D_{a4}$ by the negative grid voltage. This is because there is a positive current which is generated by the switching state [P]. Therefore, the output pole voltage becomes $-V_{\mathrm{DC}}/2$ and this wrong output voltage causes the distortion of the positive phase current as shown in Fig. 4(a). In this case, the current distortion is smaller than under Type-A fault because the output voltage is distorted only when the switching state is [O]. Therefore, the neutral-point voltage unbalance is also smaller than that of the Type-A fault case.

*2) Open-Circuit Fault in $D_{\mathrm{Ca2}}$:* In the case of $D_{\mathrm{Ca2}}$ fault, the current path is formed through $D_{a1}$ and $D_{a2}$, instead of the $S_{a3}$ and $D_{\mathrm{Ca2}}$ when the switching state is [O] with negative current as shown in Fig. 2(c). Therefore, the output pole voltage becomes $V_{\mathrm{DC}}/2$ instead of 0. This undesirable current path and pole voltage make the negative phase current to be distorted as shown in Fig. 4(b).

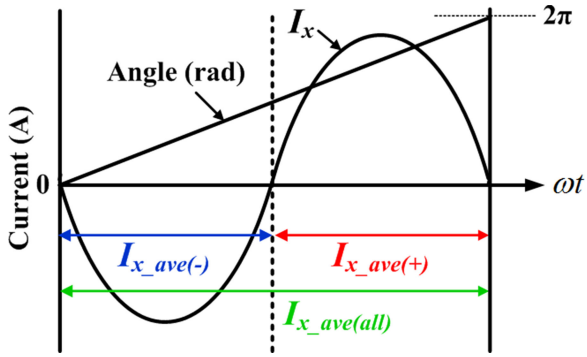


Fig. 5. Definition of variables for the fault detection.

Several methods to detect the open-circuit fault have been proposed such as the current pattern method, slope method, and dc current method [13], [14]. However, it is impossible to identify the faulty switch by the existing methods because the output distortions between the $S_{x1(x=a,b,c)}$ fault and the $S_{x2}$ fault or between the $S_{x3}$ fault and the $S_{x4}$ fault are the same as illustrated in Fig. 3.

## III. Open-Circuit Fault Detection Method

### A. Identification of Faulty Leg and Group

The proposed fault detection method is explained considering the open-circuit faults in phase-A. The faulty phase and group can be identified based on the characteristic of the distorted currents. The average value of the positive current of each phase is defined by $I_{x\_\mathrm{ave}(+)}$, and the average value of the negative current is defined by $I_{x\_\mathrm{ave}(-)}$. The average value during one fundamental period of the phase current is defined by $I_{x\_\mathrm{ave(all)}}$ as shown in Fig. 5.

Each phase can be divided into two groups. For example, phase-A, a group 1 consists of the two upper switches ($S_{a1}$ and $S_{a2}$) and the diode $D_{\mathrm{Ca1}}$. A group 2 is composed of the two

lower switches ($S_{a3}$ and $S_{a4}$) and the diode $D_{\mathrm{Ca2}}$. Under the normal condition, the average of the phase current is zero. It means that the summation of $I_{x\_\mathrm{ave}(+)}$ and $I_{x\_\mathrm{ave}(-)}$ which is $I_{x\_\mathrm{ave(all)}}$ is also zero. However, if the open-circuit fault occurs among the upper components ($S_{a1}$ or $S_{a2}$ or $D_{\mathrm{Ca1}}$), $I_{a\_\mathrm{ave(all)}}$ has a negative value because the positive current of the phase-A is distorted. The average values of the other phases have the positive values and the total amount of increasing average values is the same with the $I_{a\_\mathrm{ave(all)}}$ if it is a three-phase balanced system. Thus, $I_{a\_\mathrm{ave(all)}} = -(I_{b\_\mathrm{ave(all)}} + I_{c\_\mathrm{ave(all)}})$. On the contrary, if the open-circuit fault occurs in the lower component ($S_{a3}$ or $S_{a4}$ or $D_{\mathrm{Ca2}}$) of the phase-A, $I_{a\_\mathrm{ave(all)}}$ has a positive value and the other phases have negative values. Therefore, the faulty phase and group can be identified using the polarities of $I_{a\_\mathrm{ave(all)}}$, and the summation of $I_{b\_\mathrm{ave(all)}}$ and $I_{c\_\mathrm{ave(all)}}$. However, this direct average current method tends to be highly unreliable, and it is difficult to set the threshold value to a constant because it depends on the variations of the output currents. Therefore, the normalized phase currents are also used for fault diagnosis. The phase currents can be normalized as given by (1) and (2) [24]

$$|I_s| = \sqrt{(I_{\mathrm{ds}})^2 + (I_{\mathrm{qs}})^2} \tag{1}$$

$$I_{x\_\mathrm{normal}} = \frac{I_{x(x=a,b,c)}}{|I_s|} \times |I_{\mathrm{rated}}| \tag{2}$$

where $I_{\mathrm{ds}}$ and $I_{\mathrm{qs}}$ are $d$- and $q$-axis currents in a stationary reference frame, respectively, and $I_{\mathrm{rated}}$ is the rated current of the inverter.

### B. Classification of the Fault Type

The fault type can be classified after the faulty phase and group are detected. The large difference between the Type-A fault, which is the open-circuit fault in the switches, and the Type-B fault, which is the open-circuit fault in the clamping diodes is whether the current flows or not during the half cycle of the faulty phase current as illustrated in Figs. 3 and 4. For example, if the open-circuit fault occurs in $D_{\mathrm{Ca1}}$, the positive phase current of the faulty phase is distorted, but it flows as shown in Fig. 4(a). Thus, $I_{a\_\mathrm{ave}(+)}$ has a positive value and $I_{a\_\mathrm{ave(all)}}$ has a negative value. However, in the case of the Type-A fault ($S_{a1}$ or $S_{a2}$ fault), the positive phase current does not flow as shown in Fig. 3(a). $I_{a\_\mathrm{ave(all)}}$ has also a negative value but $I_{a\_\mathrm{ave}(+)}$ has a zero value. Therefore, the Type-A and Type-B faults can be classified using the different distortion characteristic of the output current. The identification of the group and fault type in the faulty phase-A is described in Table I. The threshold value $I_{\mathrm{thr1}}$ is used to protect against a false alarm in the fault detection when the polarity of the average current value is determined.

### C. Diagnosis of the Faulty Switch Under the Type-A Fault

The remarkable difference between the open-circuit faults in the upper switches ($S_{x1(x=a,b,c)}$ and $S_{x2}$) or between the open-circuit faults in the lower switches ($S_{x3}$ and $S_{x4}$) is the possibility of the switching state [O]. For instant phase-A, under

TABLE I
IDENTIFICATION OF FAULTY GROUP AND OPEN-CIRCUIT FAULT TYPE IN PHASE-A

| $I_{a\_\mathrm{ave}(+)}$ | $I_{a\_\mathrm{ave}(-)}$ | $I_{a\_\mathrm{ave(all)}}$ | $I_{b\_\mathrm{ave(all)}} + I_{c\_\mathrm{ave(all)}}$ | Fault (Fault Type) |
|---|---|---|---|---|
| $> I_{\mathrm{thr1}}$ | $< -I_{\mathrm{thr1}}$ | $< -I_{\mathrm{thr1}}$ | $> I_{\mathrm{thr1}}$ | $D_{\mathrm{Ca1}}$ *(B)* |
| $-I_{\mathrm{thr1}} <, < I_{\mathrm{thr1}}$ | $< -I_{\mathrm{thr1}}$ | $< -I_{\mathrm{thr1}}$ | $> I_{\mathrm{thr1}}$ | $S_{a1}$ or $S_{a2}$ *(A)* |
| $> I_{\mathrm{thr1}}$ | $< -I_{\mathrm{thr1}}$ | $> I_{\mathrm{thr1}}$ | $< -I_{\mathrm{thr1}}$ | $D_{\mathrm{Ca2}}$ *(B)* |
| $> I_{\mathrm{thr1}}$ | $-I_{\mathrm{thr1}} <, < I_{\mathrm{thr1}}$ | $> I_{\mathrm{thr1}}$ | $< -I_{\mathrm{thr1}}$ | $S_{a3}$ *or* $S_{a4}$ *(A)* |

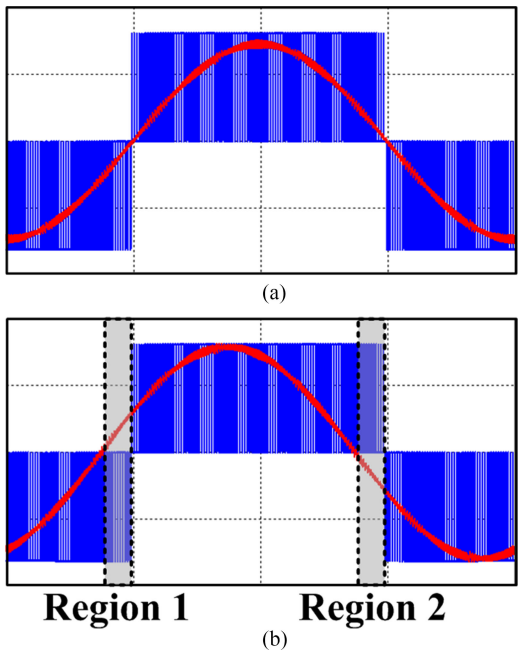


Fig. 6. Phase currents $I_a$ (7.5 A/div) and pole voltage $V_{az}$ (200 V / div) (a) before, (b) after underexcited reactive current is injected.

the $S_{a1}$ open-circuit fault, the switching state [P] is only impossible when the current is positive. In the case of $S_{a2}$ open-circuit fault, both switching states [P] and [O] are impossible. However, it is impossible to determine the possibility of the switching state [O] under the faulty condition due to the same distortion characteristic of the phase currents as shown in Fig. 3. To determine the possibility of the switching state [O], an underexcited reactive power may be injected.

Usually, the grid-connected inverter transfer electric power to the grid with a unity power factor (PF). Therefore, the polarities of the output phase current and the output voltage are almost the same as shown in Fig. 6(a). If an underexcited reactive power is injected, the phase current leads the output pole voltage and the grid voltage and, thus, the regions which have the different polarities between the phase current and the output voltage occurs as shown in Fig. 6(b). In this section, region 1 means that the phase current is positive and the output pole voltage is negative and region 2 means that the phase current is negative and the output voltage is positive. By making the regions 1 and 2 through the underexcited reactive power injection, the

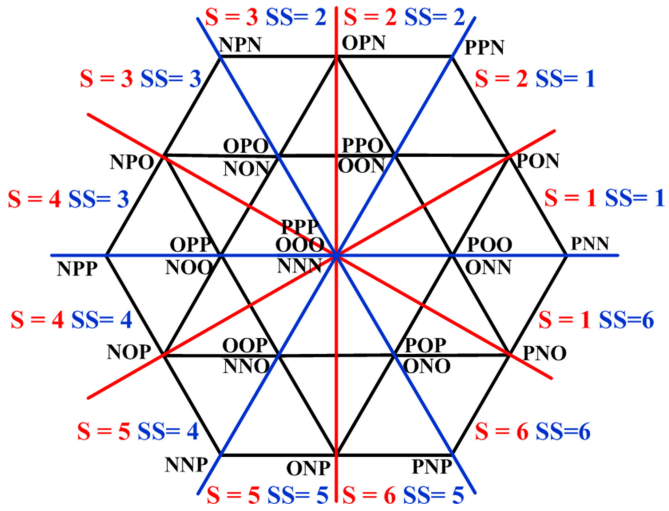


Fig. 7. Sectors of the space vector diagram for faulty switch detection.

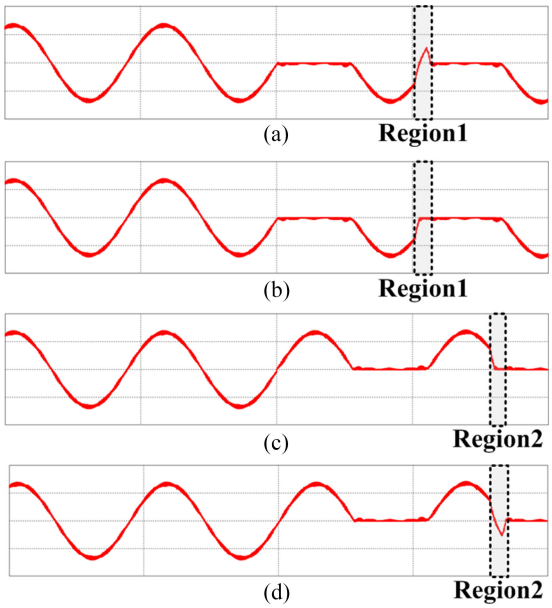


Fig. 8. Current of faulty phase with the proposed fault detection method for the faulty switch identification under the Type-A fault (a) $S_{a1}$, (b) $S_{a2}$, (c) $S_{a3}$, (d) $S_{a4}$ open-circuit fault.

possibility of the switching state [O] can be determined and the faulty switch also can be identified. Depending on the faulty switch, the current in the region 1 or 2 flows or not.

The voltage space vector diagram of the NPC inverter can be divided into sectors as shown in Fig. 7 to decide the region where the underexcited reactive power is injected for the identification of the faulty switch.

To identify the faulty switch between $S_{a1}$ and $S_{a2}$, the underexcited power is injected when $S = 5$ and $SS = 5$ so that the region 1 is made. In the region 1, the reference voltage is negative and, thus, it is made by the switching states [O] and [N]. All current paths by these switching states [O] and [N] are possible regardless of the open-circuit fault in $S_{a1}$. Therefore, the positive phase current flows in the region 1 as shown in Fig. 8(a). However, in the case of the open-circuit fault in $S_{a2}$, the positive phase current does not flow in the region 1 as shown in Fig. 8(b) because the switching state [O] is impossible. From this characteristic, the possibility of the switching state [O] is checked, and the faulty switch between the upper switches ($S_{a1}$ and $S_{a2}$) can be identified.

TABLE II
SECTORS OF UNDEREXCITED CURRENT INJECTION FOR FAULTY SWITCH IDENTIFICATION

| Faulty switch | Sector |
|---|---|
| $S_{a1}$ or $S_{a2}$ | $S = 5, SS = 5$ |
| $S_{a3}$ or $S_{a4}$ | $S = 2, SS = 2$ |
| $S_{b1}$ or $S_{b2}$ | $S = 1, SS = 1$ |
| $S_{b3}$ or $S_{b4}$ | $S = 4, SS = 4$ |
| $S_{c1}$ or $S_{c2}$ | $S = 3, SS = 3$ |
| $S_{c3}$ or $S_{c4}$ | $S = 6, SS = 6$ |

In the case of the Type-A fault in the group 2, the underexcited reactive power is injected, when $S = 2$ and $SS = 2$ in order to make the region 2. In this region, the positive reference voltage is made by the switching states [P] and [O], and all current paths by the switching states [P] and [O] are possible because the grid voltage is negative. Therefore, the negative phase current flows in the region 2 as shown in Fig. 8(d), regardless of the open-circuit fault in $S_{a4}$. On the contrary, if the open-circuit fault occurs in $S_{a3}$, the current path when the switching state [O] is impossible. Therefore, the negative current does not flow in the region 2 as shown in Fig. 8(c). From this characteristic, the faulty switch between $S_{a3}$ and $S_{a4}$ can be determined.

The magnitude of the injected underexcited reactive current can be determined according to the magnitude of the output currents and the threshold value ($I_{\mathrm{thr2}}$) of the current for the faulty switch identification.

To make the positive current flow above the threshold value in the region 1 ($S = 5$ and $SS = 5$) or the negative current flow above the threshold value in the region 2 ($S = 2$ and $S = 2$) sufficiently, the PF should be changed properly by injecting the underexcited reactive current. Further, underexcited reactive current to be injected should be larger than $I_{\mathrm{thr2}}$. In this paper, the PF is changed to 0.9 (leading) to make the regions 1 and 2 in sectors that are described in Table II, and to make the current flow.

Table II shows the sectors where the underexcited reactive current is injected for the faulty switch identification. The minimum reactive current is set to $2 \cdot I_{\mathrm{thr2}}$ by considering a margin. The underexcited reactive current is injected under the open-circuit fault condition, which is an abnormal condition. It means that the produced current by the reference of the reactive current may not be guaranteed because the unbalanced capacitor voltages make a much smaller output pole voltage than that of under the normal condition. Therefore, the larger reference of the underexcited reactive current than the threshold value ($I_{\mathrm{thr2}}$) should be set. The demanded underexcited reactive current can be defined as

$$I_{\mathrm{de\_ref(-)}} = -I_{\mathrm{qe}} \cdot \tan(\cos^{-1}(0.9)) \quad (\text{if } I_{\mathrm{de\_ref(-)}} < -2 \cdot I_{\mathrm{thr2}})$$
$$I_{\mathrm{de\_ref(-)}} = -2 \cdot I_{\mathrm{thr2}} \quad (\text{if } I_{\mathrm{de\_ref(-)}} \geq -2 \cdot I_{\mathrm{thr2}}). \tag{3}$$

Fig. 9 shows the flowchart of the proposed fault detection method considering the faults in the phase A.

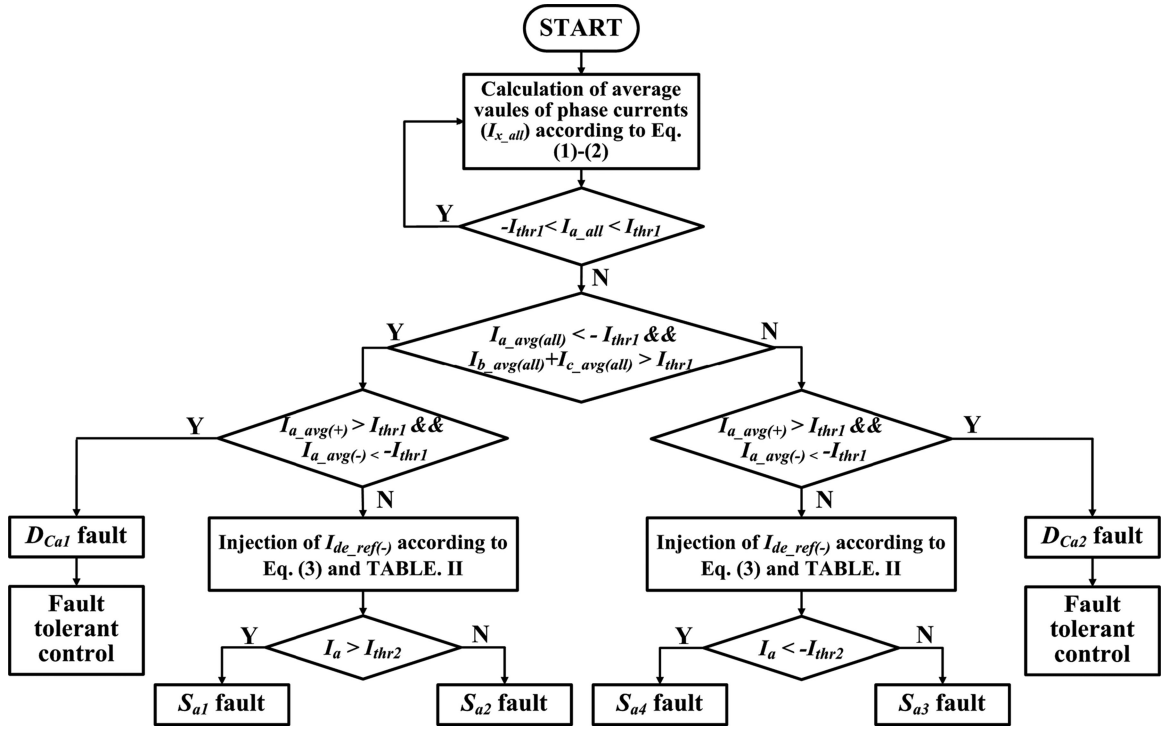


Fig. 9. Flow chart of the proposed fault detection method considering the faults in the phase-A.

## IV. Fault-Tolerant Control Under the Open-Circuit Fault in the Clamping Diodes

### A. Operation of a Fault-Tolerant Control Method

If the open-circuit fault happens in $D_{\mathrm{Ca1}}$, it is impossible to generate the switching states of the small voltage vectors [OON], [ONN], [ONO], and the switching states of the medium voltage vectors [OPN] and [ONP] when $I_a$ is positive. The impossible switching states should be replaced with other switching states to generate the outputs without distortion. The impossible N-type switching states [OON], [ONN], and [ONO] can simply be replaced with the P-type switching states [PPO], [POO], and [POP] by subtracting the shortest turn-on time ($T_{\mathrm{short}}$) from the turn-on times of three phases ($T_a, T_b, T_c$). The turn-on time is a time that the switching state of each phase is changed from the current state to another state, and $T_{\mathrm{short}}$ is the shortest turn-on time among $T_a, T_b$ and $T_c$. If the reference voltage is in the region 1 of sector I (see Fig. 10), the switching sequence is developed as [ONN]-[PNN]-[PON]-[POO]-[PON]-[PPN]-[ONN] as shown in Fig. 11(a).

Fig. 11(b) shows the switching sequence after $T_{\mathrm{short}}$ is subtracted from the three-phase turn-on times. The switching sequence is formed as [PNN]-[PON]-[POO]-[PON]-[PNN]. The switching state [ONN] is replaced with [POO], and the dwell time of [POO] becomes double.

The turn-on times for the fault-tolerant control is simply redefined as

$$\begin{aligned} T_a' &= T_a - T_{\mathrm{short}} \\ T_b' &= T_b - T_{\mathrm{short}} \\ T_c' &= T_c - T_{\mathrm{short}} \end{aligned} \tag{4}$$

where $T_{\mathrm{short}} = T_a$.

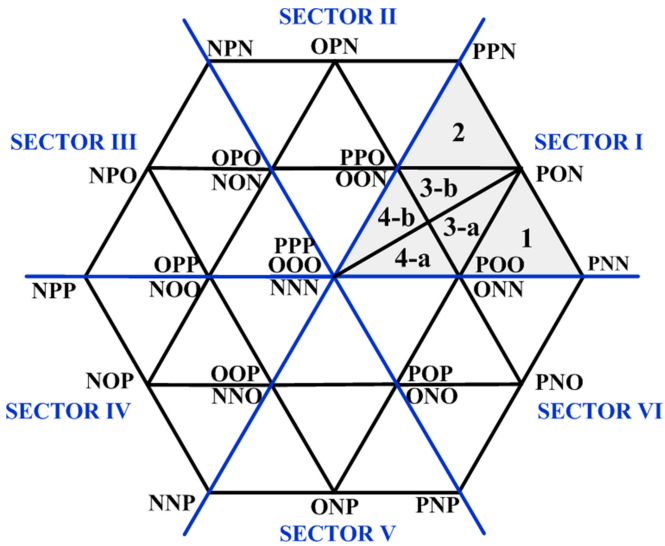


Fig. 10. Space vector diagram of the NPC inverter for the fault-tolerant control.

If there is only one N-type switching state in the switching sequence, the impossible N-type switching state can be replaced by subtracting $T_{\mathrm{short}}$. However, if there are two impossible N-type switching states in the switching sequence, it is impossible to get the switching sequence for the fault-tolerant control by only subtracting $T_{\mathrm{short}}$. If the reference voltage is in the region 3-a of sector I, the switching sequence is formed as [ONN]-[OON]-[PON]-[POO]-[PON]-[OON]-[ONN] as shown in Fig. 12(a). Fig. 12(b) shows the switching sequence after $T_{\mathrm{short}}$ is subtracted to replace the N-type switching state [ONN] with [POO]. There is still the impossible N-type switching state

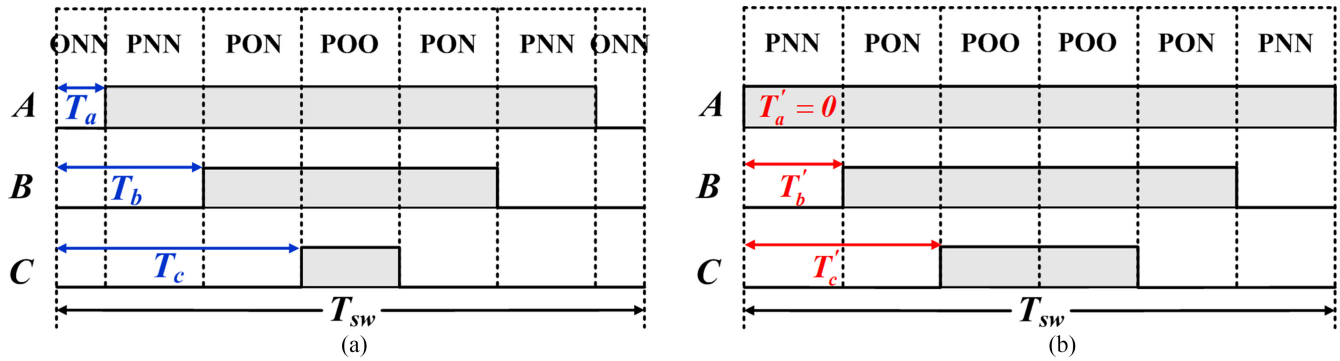


Fig. 11. Switching sequence in region 1 of sector I (a) under the normal condition, (b) for the fault-tolerant control.

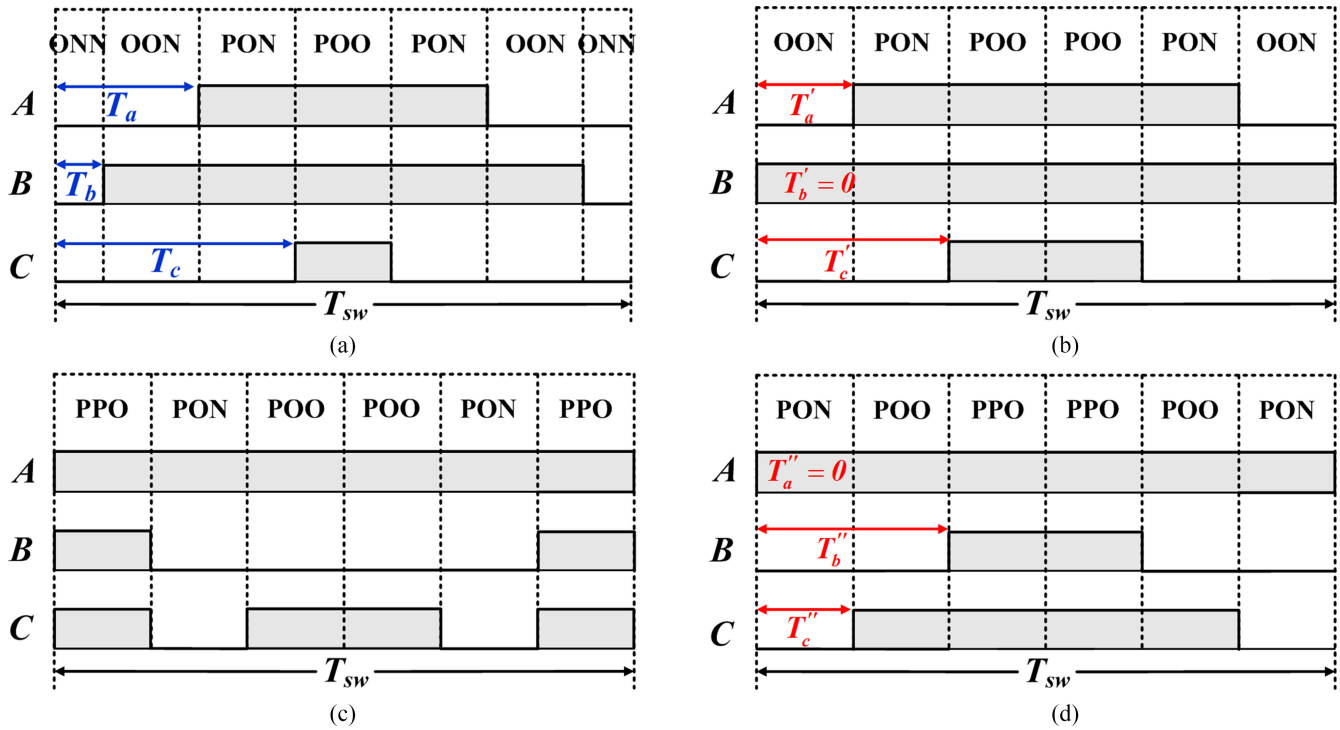


Fig. 12. Switching sequence in region 3-a of sector I for fault-tolerant control (a) under the normal condition, (b) after $T_{\text{short}}$ is subtracted, (c) before rearrangement, (d) after rearrangement.

[OON], and it also should be substituted to the P-type switching state [PPO] as shown in Fig. 12(c). In this switching sequence, the phase-C changes its switching state twice. To reduce the number of switching, the switching sequence should be rearranged as [PON]-[POO]-[PPO]-[POO]-[PON] as shown in Fig. 12(d). In order to rearrange the switching sequence, the dwell time of each switching state should be obtained. The dwell time ($T_d$) can be expressed by the turn-on times as

$$\begin{aligned} T_{d[\text{OON}]} &= 2\,(T_a - T_b) \\ T_{d[\text{PON}]} &= 2\,(T_c - T_a) \\ T_{d[\text{POO}]} &= 2\,(T_{\text{sw}}/2 - T_c + T_b) = 4T_b. \end{aligned} \tag{5}$$

From the dwell time of each switching state, the redefined turn-on times ($T_a'', T_b'', T_c''$ ) for the switching sequence rearrangement are obtained as

$$\begin{aligned} T_a'' &= 0 \\ T_b'' &= \frac{1}{2}(T_{d[\text{PON}]} + T_{d[\text{POO}]}) = 2T_b + T_c - T_a \\ T_c'' &= \frac{1}{2}T_{d[\text{PON}]} = T_c - T_a. \end{aligned} \tag{6}$$

All impossible N-type switching states in the sectors I and IV should be substituted to P-type switching states for the fault-tolerant control. However, it means that the dwell times between N-type switching states and P-type switching states are not equal during the fundamental period. It makes the average of a neutral current nonzero. Consequently, it causes the unbalance of two DC-link capacitor voltages. The P-type switching states increase the lower capacitor voltages and decrease the upper capacitor voltage. On the contrary, the N-type switching states decrease

the lower capacitor voltage and increase the upper capacitor voltage. Therefore, the total dwell times of the P-type and N-type switching states during the fundamental period should be equal so that the average of the neutral current is zero resulting in balance of the two capacitor voltages. To make the average of the neutral current zero, the P-type switching states in sectors III and IV should be replaced with N-type switching states in their switching sequences. It can be achieved by adding $T_{\rm short}$ to the turn-on times. In the regions that have two P-type switching states, all P-type switching states should be replaced to N-type switching states and the switching sequence should also be rearranged as explained above.

The impossible switching states of the small voltage vectors can be replaced with the other type of the switching states. However, in the case of medium voltage vectors, there are no possibilities to replace the switching state with another one which indicate the same voltage vector. Therefore, a new switching sequence should be applied in the regions that have the impossible medium voltage vectors. In the case of the open-circuit fault in $D_{\rm Ca1}$, the medium switching states [OPN] in the sectors II and [ONP] in the sector V are impossible. The new switching sequence without these switching states can be achieved by applying the two-level switching method. If the reference voltage of the phase-A is made by the switching states [P] and [N], the switching sequence can be obtained without impossible medium switching state [OPN] and [ONP] in the sectors II and V, respectively. The two-level switching method can be implemented by adding an offset time ($T_{\rm offset}$) to the turn-on time of the faulty phase as below [25]

$$\begin{aligned} T_{\rm offset} &= -\frac{1}{2}T_x \qquad\quad \text{if } (V_x > 0) \\ T_{\rm offset} &= -\frac{1}{2}T_x + \frac{1}{4}T_{\rm sw} \quad \text{if } (V_x < 0) \end{aligned} \tag{7}$$

where $T_x$ is the turn-on time, $V_x$ is the reference voltage of the faulty phase, and $T_{\rm sw}$ is the switching period. For example, phase-A, the turn-on time is redefined as

$$\begin{aligned} T_a' &= \frac{1}{2}T_a \qquad\quad \text{if } (V_a > 0) \\ T_a' &= \frac{1}{2}(T_a + \frac{1}{2}T_{\rm sw}) \quad \text{if } (V_a < 0). \end{aligned} \tag{8}$$

$S_{a1}$ and $S_{a2}$ are turned ON by the redefined turn-on time $T_a^{'}$ at the same time, and $S_{a3}$ and $S_{a4}$ are operated complementarily with $S_{a1}$ and $S_{a2}$. The proposed fault-tolerant control for the clamping diodes is arranged as shown in Table III.

### B. Effect of a Fault-Tolerant Control on Junction Temperature

The junction temperature ($T_j$) of power devices is an important factor to be considered when the inverter is designed, because it is closely related to the failure of the power devices. It means that $T_j$ should be in a safety range when the fault-tolerant control is applied. To investigate the effect of the proposed fault-tolerant control on junction temperatures of power devices, thermal simulations are carried out. A 10-kW NPC inverter with F3L30R06W1E3_B11 module which is manufactured by the Infineon is considered for a case study. The parameters of a 10-kW NPC inverter are summarized in Table IV.

TABLE III
FAULT-TOLERANT CONTROL FOR THE OPEN-CIRCUIT FAULT IN THE CLAMPING DIODES

| | Faulty position of the clamping diode | | |
|---|---|---|---|
| SECTOR | Phase-A | Phase-B | Phase-C |
| I | Changing N-type to P-type switching state | Two-level switching method | Changing P-type to N-type switching state |
| II | Two-level switching method | Changing N-type to P-type switching state | Changing P-type to N-type switching state |
| III | Changing P-type to N-type switching state | Changing N-type to P-type switching state | Two-level switching method |
| IV | Changing P-type to N-type switching state | Two-level switching method | Changing N-type to P-type switching state |
| V | Two-level switching method | Changing P-type to N-type switching state | Changing N-type to P-type switching state |
| VI | Changing N-type to P-type switching state | Changing P-type to N-type switching state | Two-level switching method |

TABLE IV
PARAMETERS OF A 10-KW NPC INVERTER FOR A CASE STUDY

| | |
|---|---|
| Rated Power | 10 kW |
| DC-link voltage ($V_{\rm DC}$) | 600 V |
| Rated current ($I_{\rm rated}$) | $15.2A_{\rm rms}$ |
| Switching frequency ($f_{\rm sw}$) | 10 kHz |
| Grid voltage ($E_{x(x=a,b,c)}$) | $220V_{\rm rms}$ |
| Output frequency ($f_{\rm out}$) | 50 Hz |

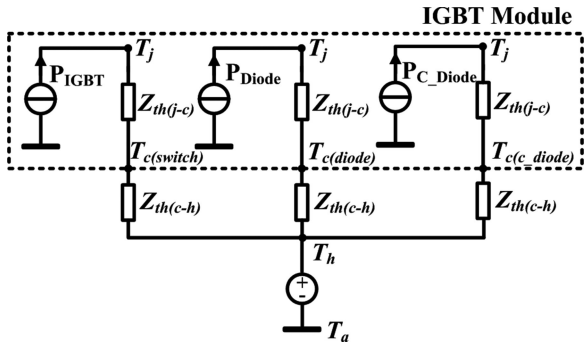


Fig. 13. Thermal equivalent block diagram of a part of a NPC IGBT module.

The phase-A is considered for comparison of the junction temperatures between normal condition and fault-tolerant control condition.

Fig. 13 shows the thermal equivalent block diagram of a part of an NPC IGBT module.

Thermal characteristic of power devices from junction to case $Z_{{\rm th}(j-c)}$ or junction to heat-sink $Z_{{\rm th}(j-h)}$ can be represented by a Foster model as shown in Fig. 14 and can be expressed by

$$Z_{{\rm th}(j-h)}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i}) \tag{9}$$

where $\tau_i = R_i^* C_i$.

Table V shows the thermal parameters of the IGBT module for the Foster model which can be obtained from datasheet.

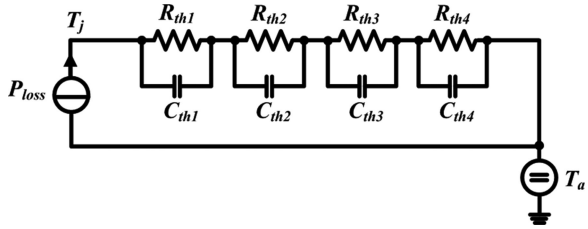


Fig. 14. Foster thermal model for an IGBT module.

TABLE V
PARAMETERS FOR THERMAL MODEL OF IGBT MODULE

| Thermal Impedance | $i$ | | | |
|---|---|---|---|---|
| | 1 | 2 | 3 | 4 |
| $R_{(j-h)\mathrm{IGBT}}$ (K/W) | 0.142 | 0.309 | 0.719 | 0.58 |
| $\tau_{\mathrm{IGBT}}$ (s) | 0.0005 | 0.005 | 0.05 | 0.2 |
| $R_{(j-h)\mathrm{Diode}}$ (K/W) | 0.29 | 0.495 | 0.894 | 0.622 |
| $\tau_{\mathrm{Diode}}$ (s) | 0.0005 | 0.005 | 0.05 | 0.2 |
| $R_{(j-h)\mathrm{Claming\_Diode}}$ (K/W) | 0.215 | 0.396 | 0.752 | 0.537 |
| $\tau_{\mathrm{Claming\_Diode}}$ (s) | 0.0005 | 0.005 | 0.05 | 0.2 |

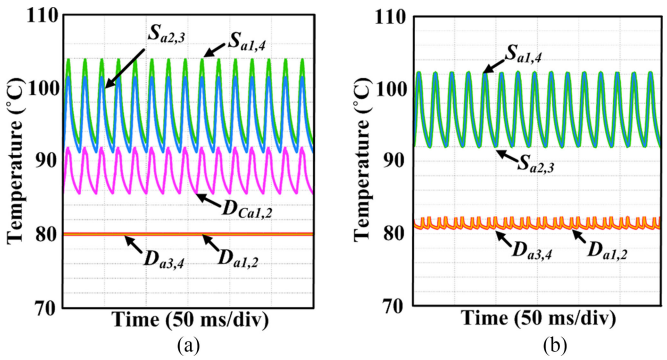


Fig. 15. Junction temperatures of power devices under full load operation (10 kW) (a) normal condition, (b) fault-tolerant control when the open-circuit fault occurs in the clamping diodes.

Considering the reliability of the power device modules, the rating of the power device module is chosen so that the junction temperature under the rated power of the inverter is 70%–80% of the maximum junction temperature [26]. The capacity of a heat-sink is also chosen considering safety ranges of the case and junction temperatures. In this simulation, the heat-sink temperature is set by 80 °C, and considered as a constant under assumption that the heat-sink is designed properly considering the junction temperature and the case temperature. The losses in the power devices are calculated based on datasheet values.

Fig. 15(a) shows the junction temperatures of the power devices, when the NPC inverter is operated with rated power under the normal condition. The hottest parts are the outer switches $S_{a1}$ and $S_{a4}$ in this case study and the maximum junction temperature is about 104 °C. Fig. 15(b) shows the junction temperatures of the power devices, when the proposed fault-tolerant control is applied. The hottest parts are both inner and outer switches because these switches are operated at the same time. The maximum junction temperature is about 102 °C. From the simulation

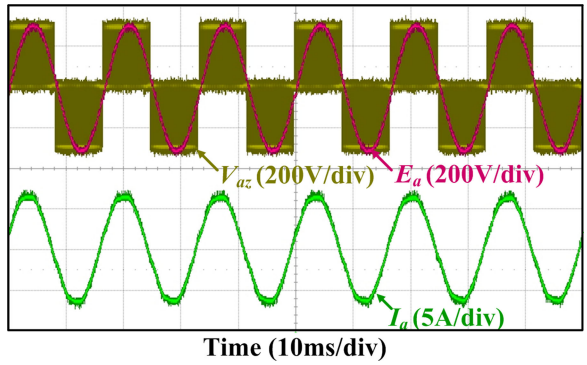


Fig. 16. Outputs of the grid-connected NPC inverter under the normal operation; pole voltage ($V_{az}$), grid voltage ($E_a$), and phase current ($I_a$).

results, it can be seen that all power devices are under the safety temperature regions when the proposed fault-tolerant control is applied. Consequently, the proposed fault-tolerant control can be applied without any modifications such as heat-sink and water cooling ability from its initial system condition.

## V. EXPERIMENTAL RESULTS

Experiments have been carried out to verify the validity and effectiveness of the proposed fault detection and fault-tolerant control methods. A 10-kW small-scaled prototype has been built and used for the experiments. The design specifications and parameters used for the experiments are listed as given below: DC-Link voltage ($V_{\mathrm{DC}}$): 600 V, DC-link capacitors ($C_{\mathrm{DC}}$): 2200 $\mu$F, grid voltage ($E_a$): 300 $V_{\mathrm{peak}}$, output frequency ($f_{\mathrm{out}}$): 60 Hz, switching frequency ($f_{\mathrm{sw}}$): 10 kHz, threshold value of average current ($I_{\mathrm{thr1}}$): 1.5 A, and threshold value of current for faulty switch identification ($I_{\mathrm{thr2}}$): 2 A.

Fig. 16 shows the outputs of the grid-connected NPC inverter under the normal condition. The phases of the output pole voltage, the output current, and the grid voltage are almost same when it is operated with unity PF.

Fig. 17 shows the experimental waveforms, when the open-circuit fault has occurred in each switch of phase-A (Type-A fault), respectively. If the open-circuit fault occurs, the positive or negative currents of the faulty phase do not flow. Further, the distortion of the output currents between $S_{a1}$ and $S_{a2}$ open-circuit faults or between $S_{a3}$ and $S_{a4}$ open-circuit faults are the same as analyzed in Section II.

Fig. 18 shows the output phase currents when the Type-B open-circuit fault has occurred in phase A. The output currents are distorted but both positive and negative currents of the faulty phase flow on the contrary to the Type-A open-circuit fault.

Fig. 19 shows the experimental result of the fault-type classification when the Type-A and Type-B open-circuit faults have occurred in $S_{a1}$ and $D_{\mathrm{Ca1}}$, respectively. $I_{a\_\mathrm{ave(all)}}$ and $I_{a\_\mathrm{ave}(-)}$ have negative values in both cases and these are smaller than the negative threshold value due to the distortion on the positive phase current. However, $I_{a\_\mathrm{ave}(+)}$ and $I_{b\_\mathrm{ave(all)}} + I_{c\_\mathrm{ave(all)}}$ have positive values and these are larger than the positive threshold value when the Type-B open-circuit fault has occurred.

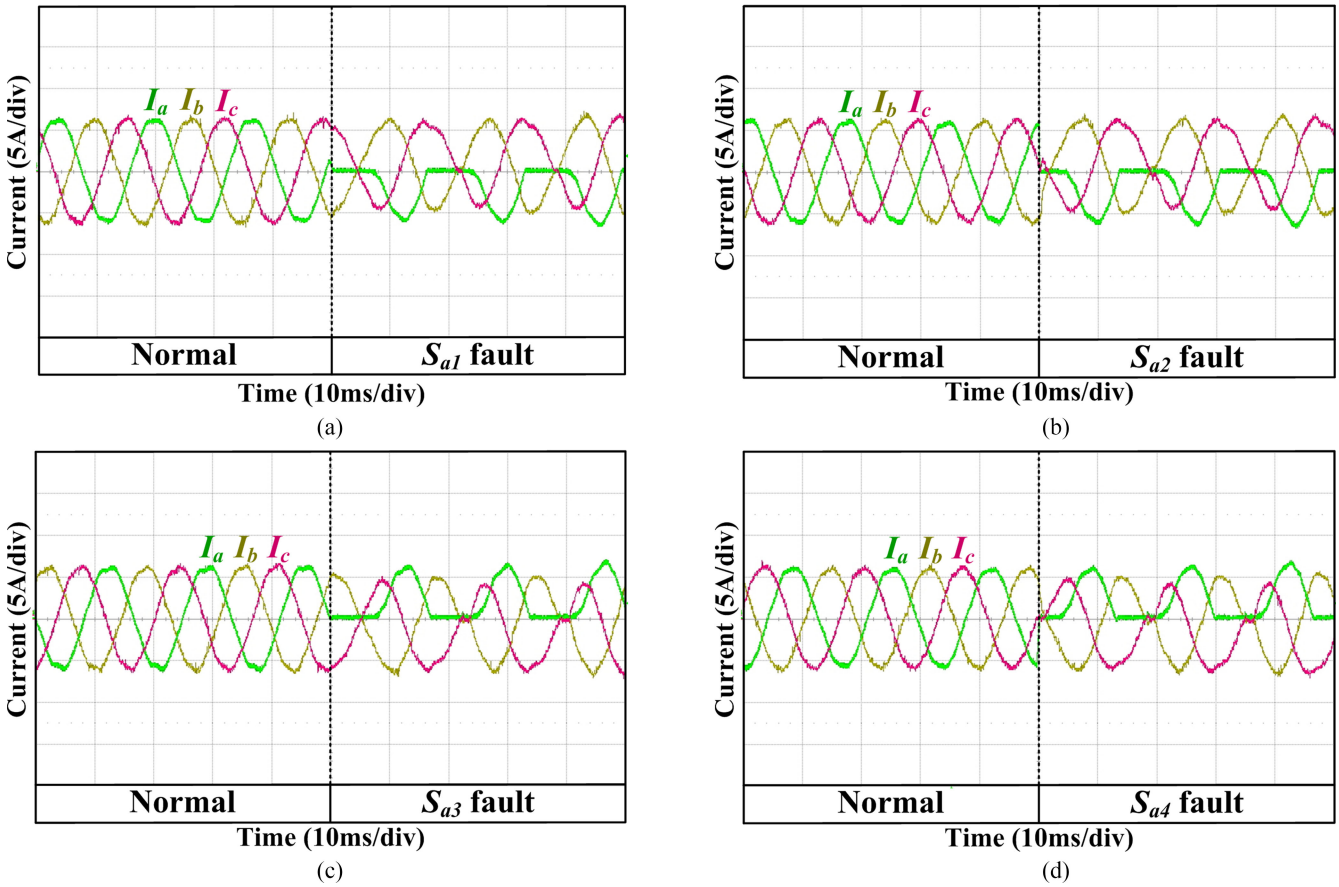


Fig. 17. Phase currents under the Type-A open-circuit fault in (a) $S_{a1}$, (b) $S_{a2}$, (c) $S_{a3}$, (d) $S_{a4}$.

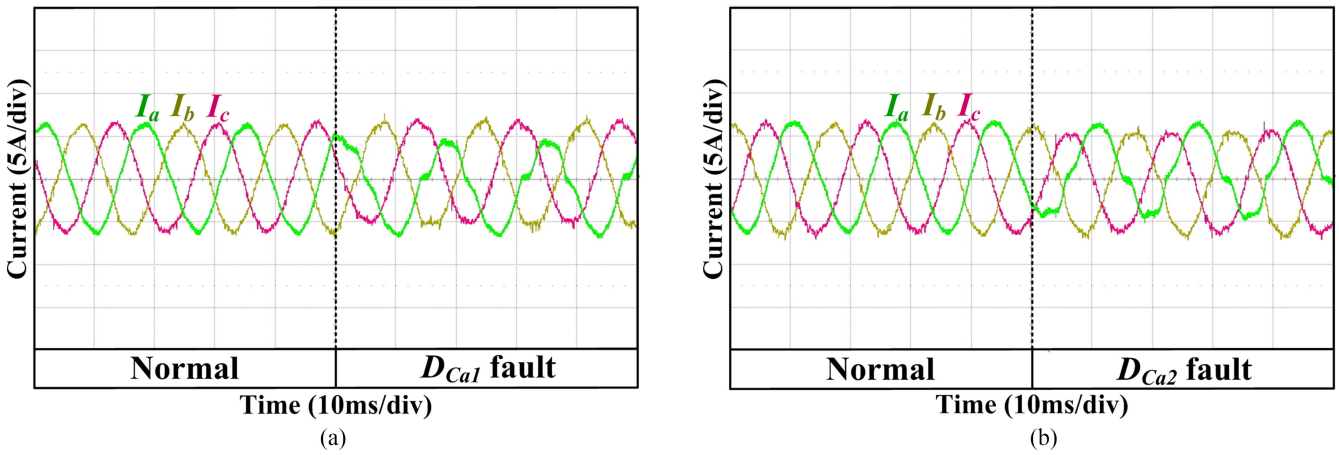


Fig. 18. Phase currents under the Type-B open-circuit fault in (a) $D_{\mathrm{Ca1}}$, (b) $D_{\mathrm{Ca2}}$.

In the case of the Type-A open-circuit fault, $I_{a\_\mathrm{ave}(+)}$ is in the range of the threshold value, which is $\pm 1.5$ A. As it can be seen in Fig. 19, the Type-A and Type-B faults can be identified precisely using the characteristics of the distorted output currents. After the fault type is determined, the faulty switch can be detected by the proposed method under the Type-A fault.

Fig. 20(a) and (b) shows the experimental results of the proposed fault detection method, when the Type-A open-circuit fault has occurred in $S_{a1}$ and $S_{a2}$, respectively. The Type-A fault detection signal indicates the occurrence of the open-circuit fault, and whether the open-circuit-fault occurs in upper switches or in lower switches. The fault detection signal "1" means that the open-circuit fault occurs in one of two upper switches and "2" means that the open-circuit fault occurs in one of two lower switches. The fault switch identification signal denotes the location of a faulty switch in the faulty phase.

After the fault type and group are detected by the detection signal as 1, the underexcited reactive current has been injected

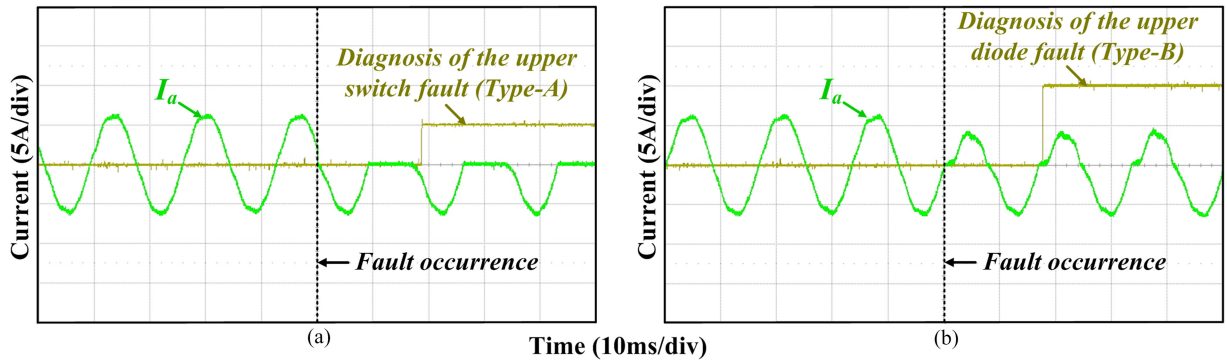


Fig. 19. Identification of fault type when (a) Type-A open-circuit fault has occurred in $S_{a1}$, (b) Type-B open-circuit fault has occurred in $D_{\mathrm{Ca1}}$.

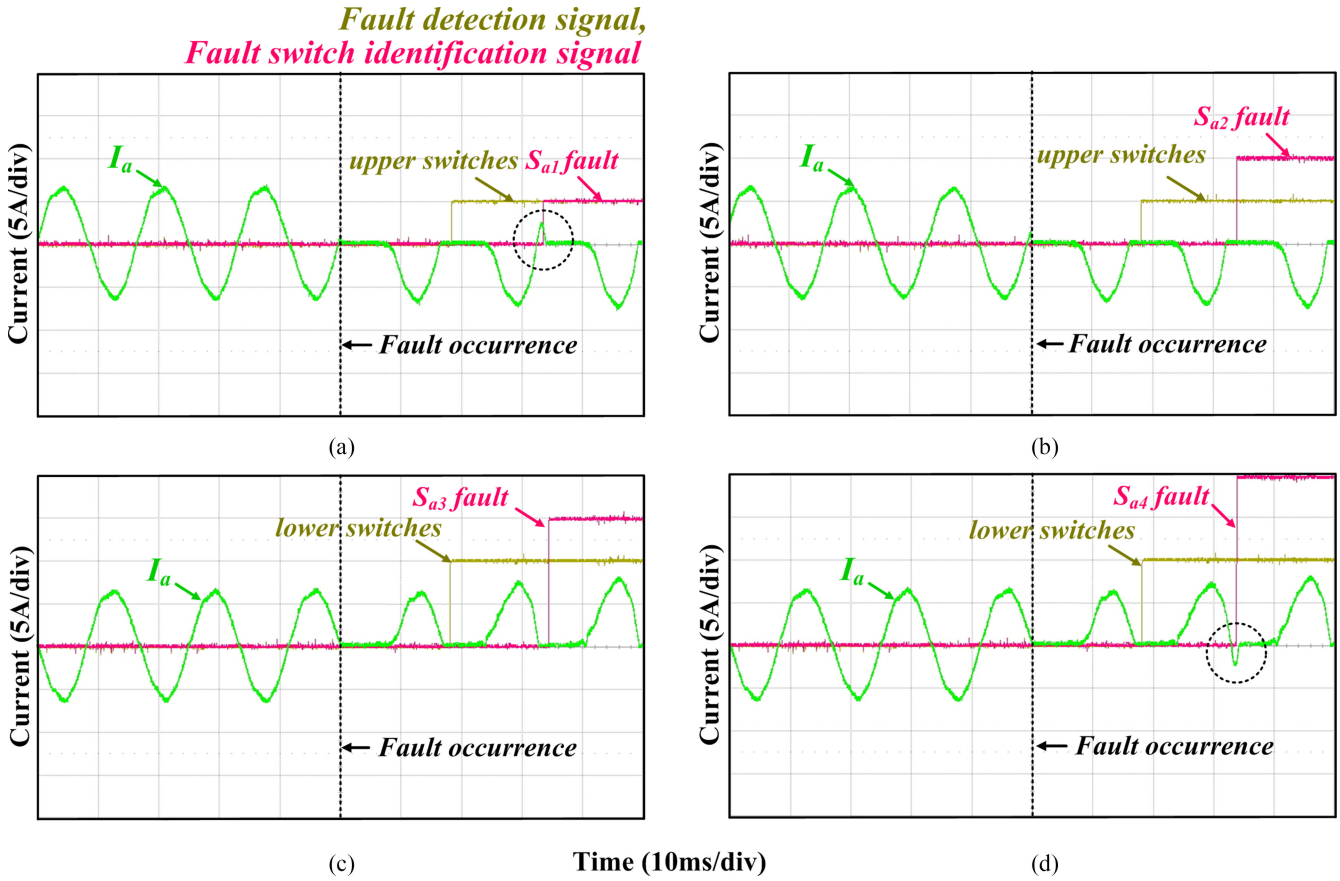


Fig. 20. Diagnosis of the faulty switch under the Type-A open-circuit fault in (a) $S_{a1}$, (b) $S_{a2}$, (c) $S_{a3}$, (d) $S_{a4}$ by underexcited reactive current injection.

when $S = 5$ and $SS = 5$ to identify the faulty switch between $S_{a1}$ and $S_{a2}$.

In the case of the $S_{a1}$ fault, the positive phase current flows in the region where the underexcited current is injected as shown in Fig. 20(a). However, if the open-circuit fault occurs in $S_{a2}$, the positive current does not flow as shown in Fig. 20(b). From this result, the faulty switch between upper two switches can be identified correctly.

Fig. 20(c) and (d) shows the experimental results of the proposed fault detection method when the Type-A open-circuit fault has occurred in $S_{a3}$ and $S_{a4}$, respectively. To separate the fault location between the two lower switches ($S_{a3}$ and $S_{a4}$), the underexcited reactive current has been injected when $S = 2$ and $SS = 2$. The negative current does not flow under the open-circuit fault in $S_{a3}$, but the negative current flows in the case of the open-circuit fault in $S_{a4}$. The location of the faulty switch is identified precisely by the proposed method.

Fig. 21 shows the results of the proposed fault-tolerant control method under the open-circuit fault in $D_{\mathrm{Ca1}}$ (Type-B fault). THD of the output currents increase compared with the currents under the normal condition, since the two-level switching method is applied in some regions. Under the normal condition, the THDs of line-to-line voltages are 33.9%. If the proposed fault-tolerant control is applied, the line-to-line voltages ($V_{\mathrm{ab}}$

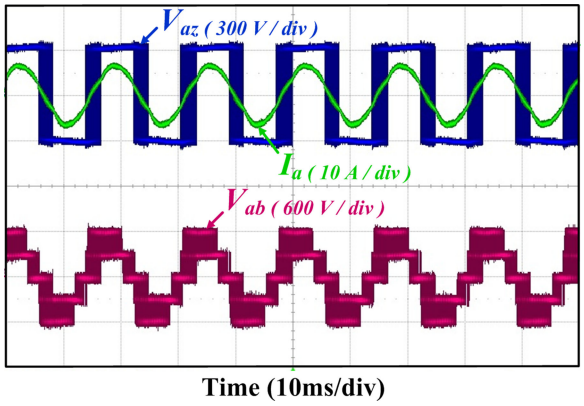


Fig. 21. Experimental result of the proposed fault-tolerant control under the open-circuit fault in $D_{\mathrm{Ca1}}$.

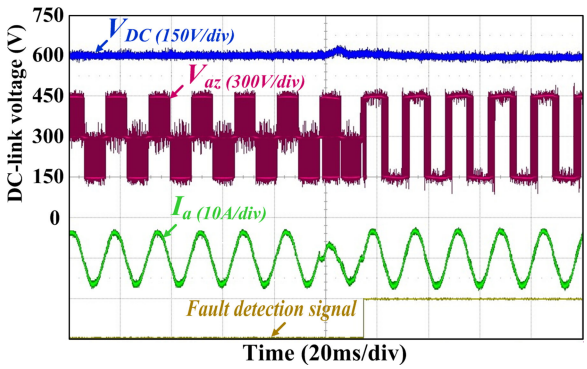


Fig. 22. Experimental result of the proposed method from fault detection to fault-tolerant control under the open-circuit fault in $D_{\mathrm{Ca1}}$.

and $V_{\mathrm{ac}}$) which contain the faulty leg increase by 44.3%. The other line-to-line voltage ($V_{\mathrm{bc}}$) keeps the same THD with normal condition.

The most of world leading companies have designed their inverters with a margin of the THD of current to be less than 2–3% at the nominal power [27], [28]. Therefore, even though the THD of the line-to-line voltages are increased, the inverter can be complied with standards for the grid-connection. Further, manufacturers can consider the fault-tolerant control mode when the output filter is designed to improve the reliability and availability under the open-circuit fault conditions.

Fig. 22 shows the experimental results of the overall procedure from fault detection to fault-tolerant control when the open-circuit fault occurs in the clamping diode $D_{\mathrm{Ca1}}$. Due to the distortion of the positive current in phase A, the DC-link voltage increases about 25 V when the open-circuit fault occurs in $D_{\mathrm{Ca1}}$. The fault-tolerant control is applied after the fault is detected. The distortion of the output currents is eliminated and the DC-link voltage becomes stable. The experimental results demonstrate that the grid-connected NPC inverter is operated with well-maintained performance by the proposed fault-tolerant control method when the open-circuit fault occurs in the clamping diodes.

## VI. Conclusion

Open-circuit fault-detection and fault-tolerant control methods for the NPC inverter under the grid-connection have been proposed.

In the beginning of this paper, the operation of the grid-connected NPC inverter under the open-circuit fault conditions has been studied. Then, the open-circuit fault detection and fault-tolerant control methods for the grid-connected NPC inverter system have been presented. Under the grid-connected condition, it is impossible to identify the fault switch by existing methods, which have been developed based on the outputs distortions for the conventional two-level inverter system. The fault between switches and clamping diodes can be identified by checking whether the current flows or not during the half period of the output current of the faulty phase. The faulty switch between the upper two switches or between the lower two switches is classified by injecting an underexcited reactive current during a short period. In the case of the open-circuit fault in the clamping diode, the fault-tolerant control method can be applied. Even though the THD of the output currents increase, the NPC inverter can be operated with acceptable output performance and without derating of the output power.

The feasibility and effectiveness of the proposed open-circuit fault detection and fault-tolerant control methods have been verified by simulation and experimental results.

## References

[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "Review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[2] H. Wang, M. Liserre, F. Blaabjerg P. De Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 1, pp. 97–114, Mar. 2014.

[3] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 17–26, Jun. 2013.

[4] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.

[5] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.

[6] *Handbook Robustness Validation Automotive Electrical/Electronic Modules*. Frankfurt am Main, Germany: ZVEI, Jun. 2008.

[7] H. Wang, K. Ma, and F. Blaabjerg, "Design for reliability of power electronic systems," in *Proc. IEEE 38th Annu. Conf. Ind. Electron. Soc.*, 2012, pp. 33–44.

[8] J. Lutz, H. Schlangenotto, U. Scheuermann, R. D. Doncker, *Semiconductor Power Device*. New York, NY, USA: Springer-Verlag, 2011, ch. 11.

[9] M. Ciappa, "Selected failure mechanism of modern power modules," *Microelectron. Rel.*, vol. 42, nos. 4/5, pp. 653–667, Apr./May 2002.

[10] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[11] L. G. Franquelo, J. Rodríguez, J. I. León, S. Kouro, R. Portillo, and M. M. Prats, "The age of multilevel converters arrives," *IEEE Trans. Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[12] B. Wu, *High-Power Converters AC Drives*. Hoboken, NJ, USA: Wiley, 2006.

[13] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517–2533, May 2015.

[14] B. Lu and S. Sharma, "A literature review of IGBT fault diagnostic and protection methods for power inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1770–1777, Sep./Oct. 2009.
[15] J. O. Estima and A. J. Marques Cardoso, "A new approach for real-time multiple open-circuit fault diagnosis in voltage-source inverters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2487–2494, Nov./Dec. 2011.
[16] J. O. Estima and A. J. Marques Cardoso, "A new algorithm for real-time multiple open-circuit fault diagnosis in voltage-fed PWM motor drives by the reference current errors," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3496–3505, Aug. 2013.
[17] M. B. Abadi, A. M. S. Mendes, and S. M. A. Cruz, "Three-level NPC inverter fault diagnosis by the average current Park's vector approach," in *Proc. Int. Conf. Electr. Mach.*, 2012, pp. 1893–1898.
[18] A. M. S. Mendes, M. B. Abadi, and S. M. A. Cruz, "Fault diagnostic algorithm for three-level neutral point clamped AC motor drives based on average current Park's vector," *IET Power Electron.*, vol. 7, no. 5, pp. 1127–1137, May 2014.
[19] J. S. Lee, K. B. Lee, and F. Blaabjerg, "Open-switch fault detection method of a back-to-back converter using NPC topology for wind turbine systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 325–335, Jan./Feb. 2015.
[20] T. J. Kim, W. C. Lee, and D. S. Hyun, "Detection method for open-circuit fault in neutral-point-clamped inverter systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2754–2763, Jul. 2009.
[21] P. Fazio, G. Maragliano, M. Marchesoni, and G. Parodi, "A new fault detection method for NPC converter," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.
[22] L. M. A. Caseiro and A. M. S. Mendes, "Real-time IGBT open-circuit fault diagnosis in three-level neutral-point-clamped voltage-source rectifiers based on instant voltage error," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1669–1678, Mar. 2015.
[23] H. K. Ku and J. M. Kim, "Multiple open-switch faults detection and faults tolerant method for three-level three-phase NPC active rectifier," in *Proc. IEEE Ind. Electron. Soc. Conf.*, 2013, pp. 1062–1067.
[24] U. M. Choi, K. B. Lee, and F. Blaabjerg, "Diagnosis and tolerant strategy of an open-switch fault for T-type three-level inverter systems," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 495–508, Jan./Feb. 2014.
[25] U. M. Choi, J. S. Lee, and K. B. Lee, "New modulation strategy to balance the neutral-point voltage for three-level neutral-clamped inverter systems," *IEEE Trans. Energy Convers.*, vol. 29, no. 1, pp. 91–100, Mar. 2014.
[26] Mitsubishi Elect. Power Module Rel. [Online]. Available: www.mitsubishi electric.com/semiconductors/products/pdf/reliability/0512_e.pdf)
[27] ABB, Datasheet of string inverters: PVI-10.0-TL-OUTD and PVI-12.5-TL-OUTD, 2015.
[28] SMA, Datasheet of SUNNY CENTRAL 1000CP XT.

**Ui-Min Choi** (S'11) received the B.S. and M.S. degrees in electrical and computer engineering from Ajou University, Suwon, Korea, in 2011 and 2013, respectively. He is currently working toward the Ph.D. degree at Aalborg University, Aalborg, Denmark.

His research interests include reliability of power device and converter, renewable power generation, and multilevel converter.

**June-Seok Lee** (S'11–M'15) received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from Ajou University, Suwon, Korea, in 2011, 2013, and 2015, respectively.

Since 2015, he has been with the Korea Railroad Research Institute, Uiwang, South Korea. His research interests include grid-connected systems, multilevel inverter and reliability.

**Frede Blaabjerg** (S'86–M'88–SM'97–F'03) received the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 1992.

He was with ABB-Scandia, Randers, from 1987–1988. He was an Assistant Profes-sor in 1992, an Associate Professor in 1996, and a Full Professor in power electronics and drives in 1998. He has been a part-time Research Leader at the Research Center Risoe, Denmark. From 2006 to 2010, he was the Dean of the Faculty of Engineering, Science and Medicine and was a Visiting Professor at Zhejiang University, China, in 2009. He was a Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for IEEE Industry Applications Society from 2010 to 2011. Since 2007, he has been the Chairman of EPE and Performance Environment Design Group, Aalborg, in 2012. His research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives.

Dr. Blaabjerg was an Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006–2012. He received the 1995 Angelos Award for his contribution in modulation technique and the Annual Teacher prize at Aalborg University. In 1998, he received the Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society. He has received 15 IEEE prize paper awards and another prize paper award at PELINCEC Poland 2005. He received the IEEE PELS Distinguished Service Award in 2009 and the EPE-PEMC 2010 Council Award and the IEEE William E. Newell Power Electronics Award 2014. He has received a number of major research awards in Denmark.

**Kyo-Beum Lee** (S'02–M'04–SM'10) received the B.S. and M.S. degrees in electrical and electronic engineering from the Ajou University, Suwon, Korea, in 1997 and 1999, respectively. He received the Ph.D. degree in electrical engineering from the Korea University, Seoul, Korea, in 2003.

From 2003 to 2006, he was with the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. From 2006 to 2007, he was with the Division of Electronics and Information Engineering, Chonbuk National University, Jeonju, Korea. In 2007, he was with the School of Electrical and Computer Engineering, Ajou University, Suwon, Suwon.

Dr. Lee is an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, the *Journal of Power Electronics*, and the *Journal of Electrical Engineering*.